Designing of TSPC D-Flip Flop Using 28nm CMOS Technology

True Single-Phase Clock (TSPC) D flip flop is designed using 28nm CMOS technology by using Synopsys Custom Design Platform.

Table of Content

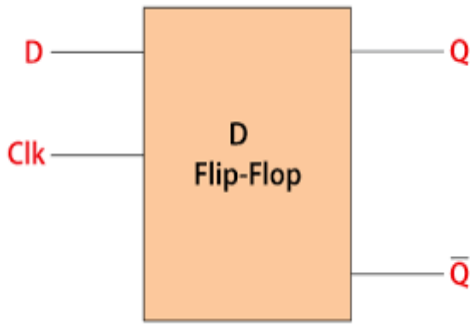
ABSTRACT

This paper is about a low power, high speed design of D flip-flop having less number of transistors. In flip-flop design only one transistor is being clocked by short pulse train which is known as True Single-Phase Clocking (TSPC) flip-flop. The true single-phase clock (TSPC) is common dynamic flip-flop which performs the flip-flop operation with little power and at high speeds.

Introduction

D Flip Flop (also known as a D Latch or a 'data' or 'delay' flip-flop) is a type of flip flop that tracks the input, making transitions with match those of the input D. The D stands for 'data'; this flip-flop stores the value that is on the data line.). In recent years, however, this has begun to change rapidly and power is being given equal importance in comparison to area and speed. There is always a trade- off between power and performance. Reference circuit figure shows the positive edge triggered 11 transistors

TSPC (True Single-Phase Clocking) flipflop. During the ON period whatever is the value of input it becomes output. TSPC flip-flop consists of 3 stages which corresponds to three cascaded inverters (and a 4th stage of static inverter). Setup characterization is done for the circuit.



Clock	D	Q	Q′	Description
↓ » 0	X	Q	Q′	Memory no change
↑ » 1	0	0	1	Reset Q » 0
↑ » 1	1	1	0	Set Q » 1

For positive edge triggered D flip-flop, when clock signal transits from 0 to 1 then only input data (D) is passed to the output line of flip-flop. Above table shows truth table for positive edge triggered D flip-flop

TOOL USED

- Synopsys Custom Compiler: The Synopsys Custom Compiler™ design environment is a modern solution for full-custom analog, custom digital, and mixed-signal IC design. As the heart of the Synopsys Custom Design Platform, Custom Compiler provides design entry, simulation management and analysis, and custom layout editing features. This tool was used to design the circuit on a transistor level.

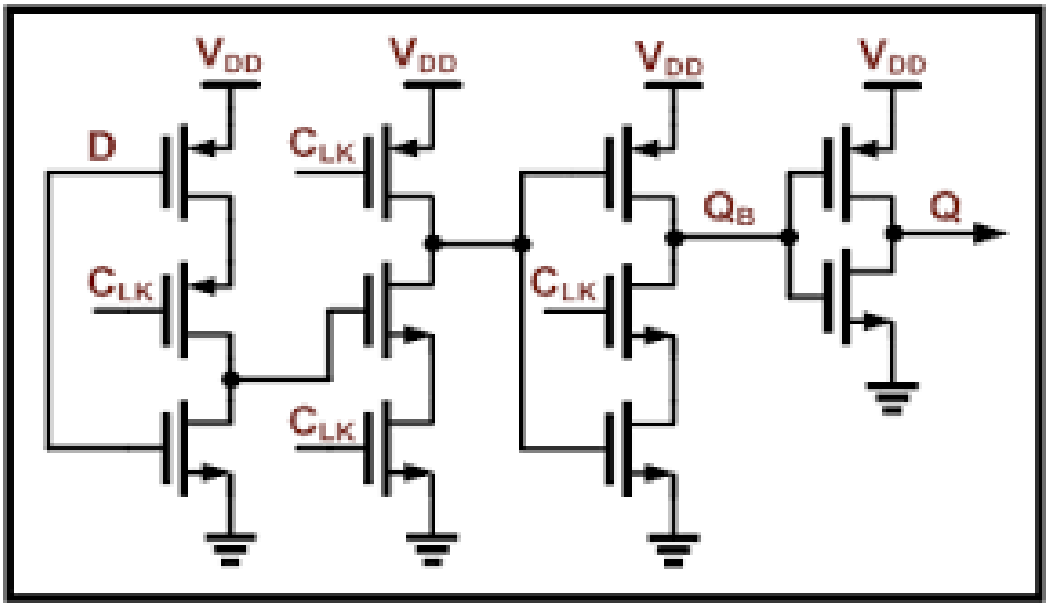
- Synopsys Primewave: PrimeWave™ Design Environment is a comprehensive and flexible environment for simulation setup and analysis of analog, RF, mixed-signal design, custom-digital and memory designs within the Synopsys Custom Design Platform. This tool helped in various types of simulations of the above designed circuit.

- Synopsys 28nm PDK: The Synopsys 28nm Process Design Kit(PDK) was used in creation and simulation of the above designed circuit.

TSPC D FLIP FLOP CIRCUIT DESIGN

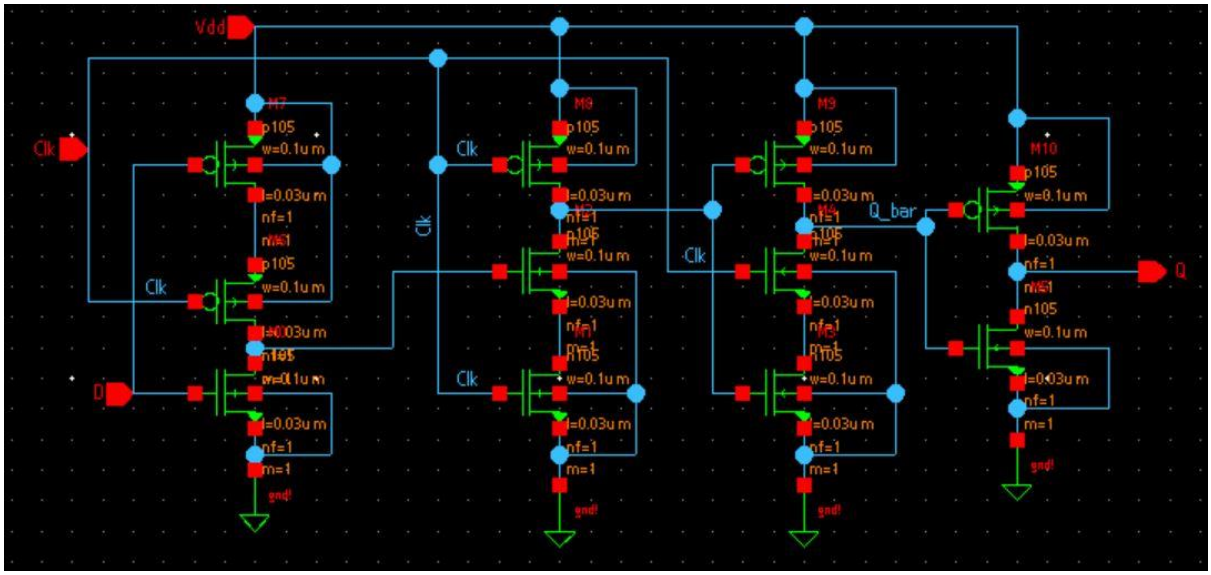
Below figure shows the positive edge triggered 11 transistors TSPC (True Single-Phase Clocking) D flipflop. During the ON period whatever is the value of input it becomes output. TSPC flip-flop consists of 3 stages which corresponds to three cascaded inverters (and a 4th stage of static inverter). Setup and Hold time characterization is

done for the circuit. In the design of TSPC flip-flop edge triggered (positive or negative) D flip-flop is used. The Design is implemented using Synopsys Custom Compiler in 28 nm CMOS technology.

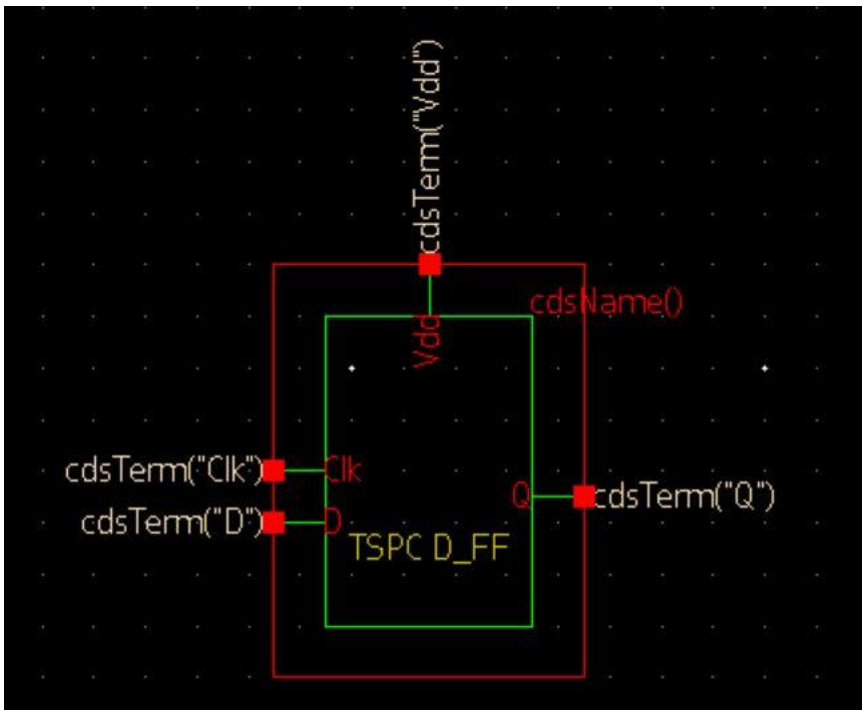


CMOS D FLIP FLOP (TSPC)

- SCHEMATIC

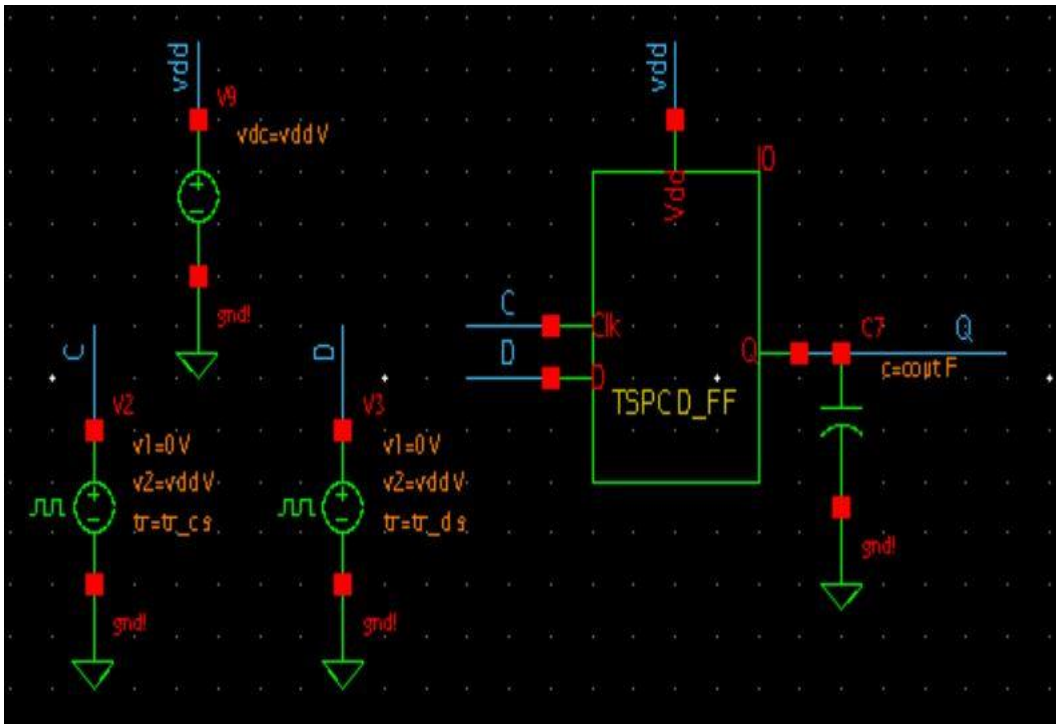


- SYMBOL

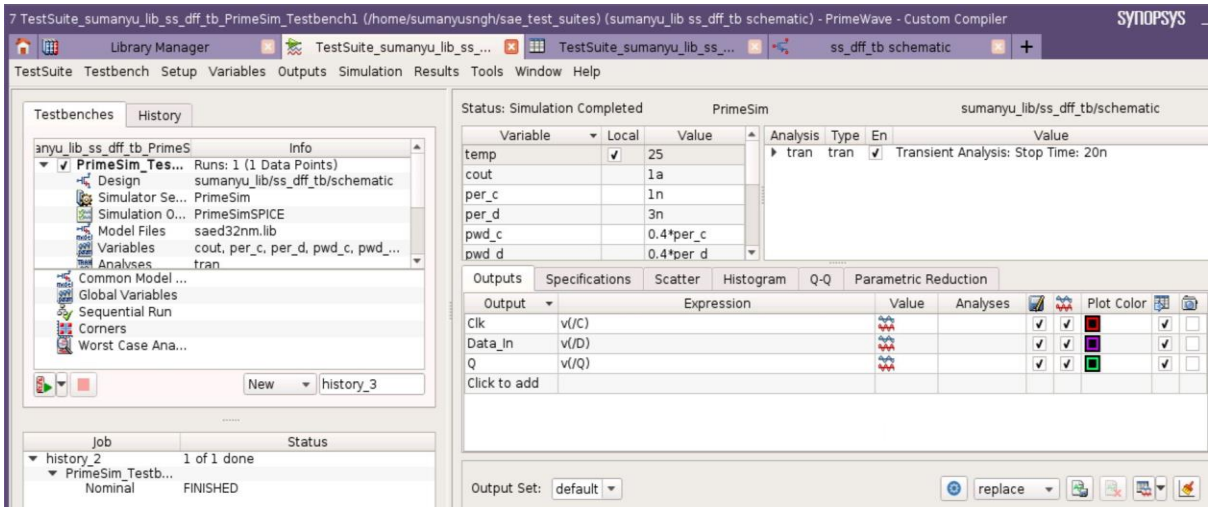


1. INPUT = VPULSE WAVE

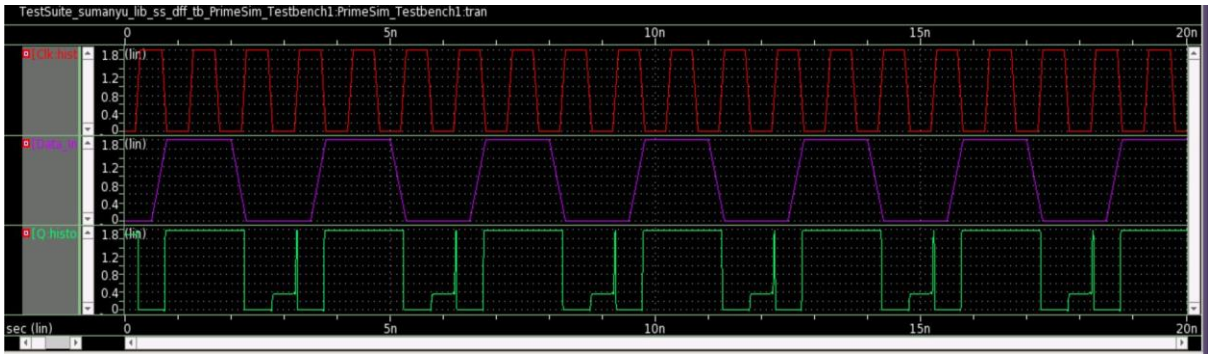
- TESTBENCH SYMBOL



- PRIMEWAVE WINDOW

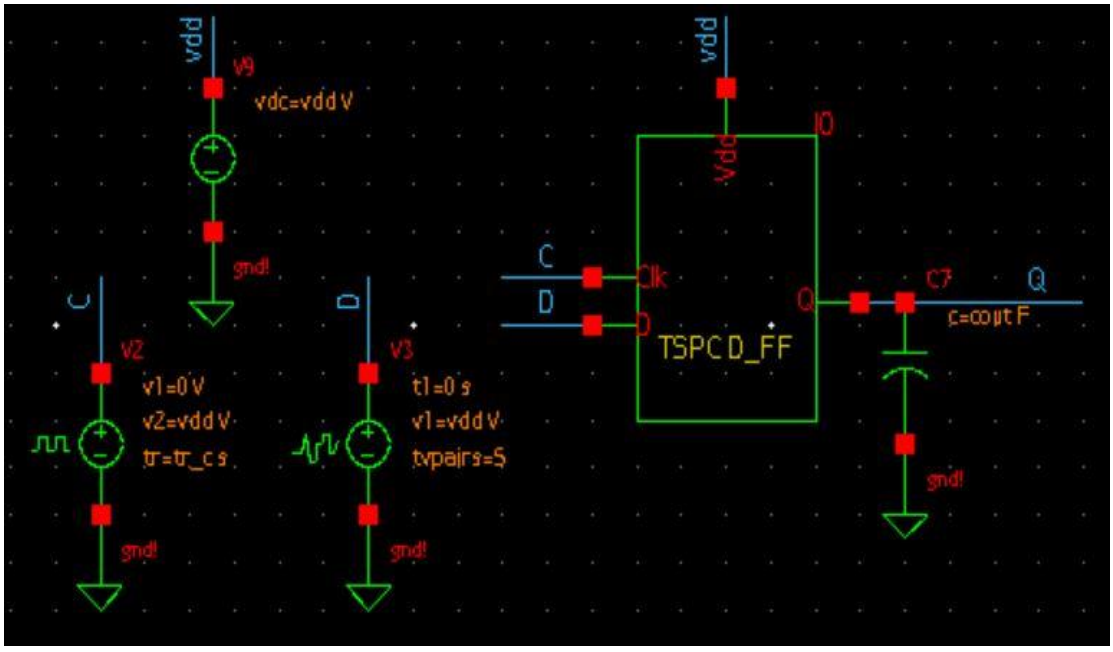


- TESTBENCH WAVEFORM

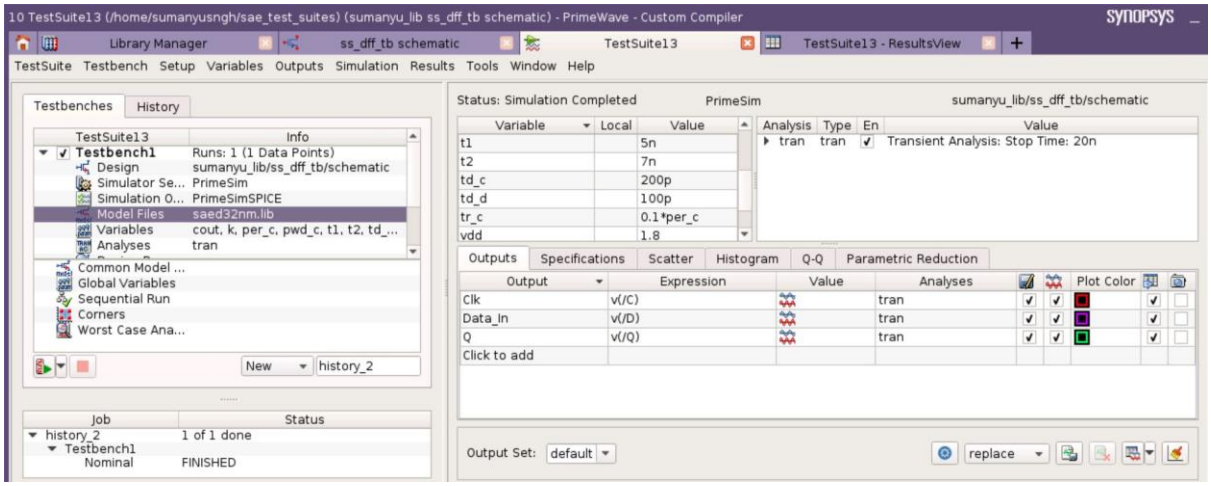


2. INPUT = VPWL WAVE

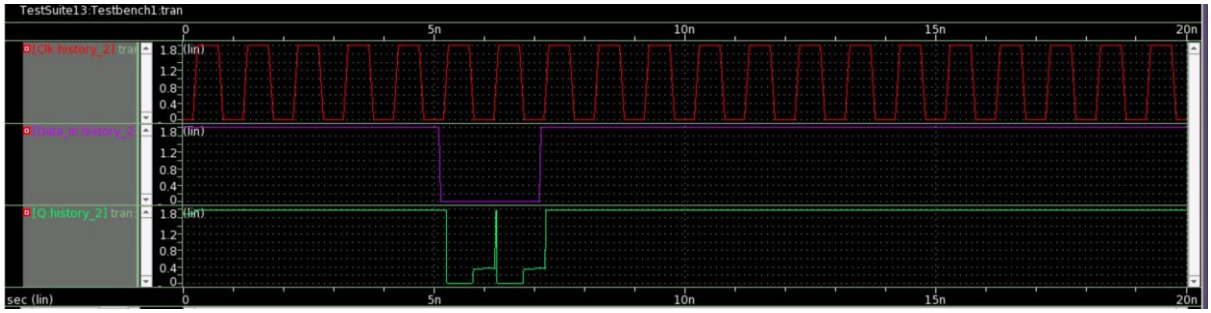
- TESTBENCH SYMBOL



- PRIMEWAVE WINDOW



- TESTBENCH WAVEFORM



SETUP TIME

- Setup time

Minimum time requires for which the data should be stable before the active edge of the clock. Tcq is clock to output delay. Tdc is data to active edge difference.

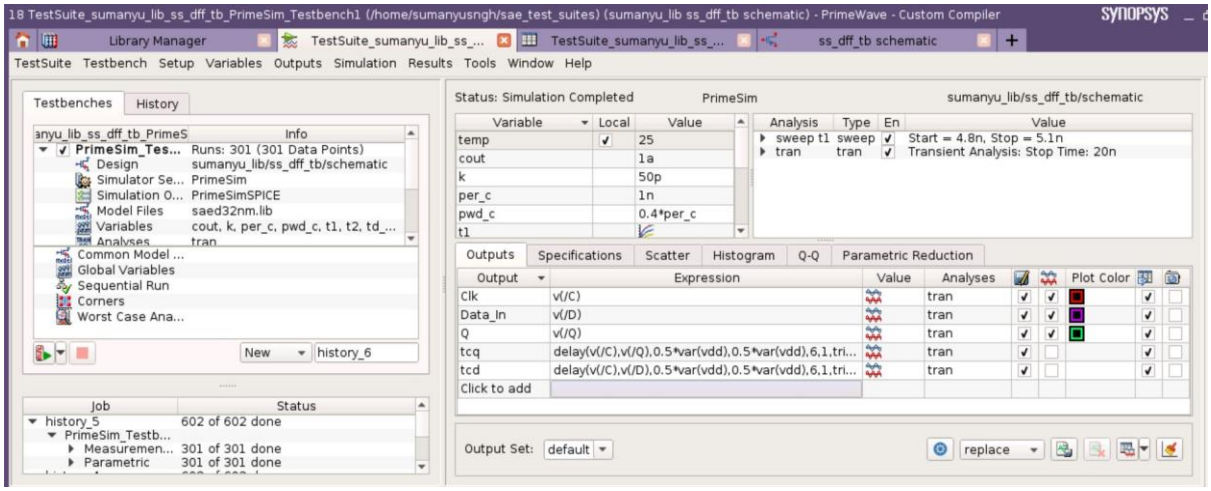
- Setup Rise time

To calculate the setup rise time the output should be logic 0. So when the active edge comes the output becomes logic 1, for given high input. When we shift the data from left to right across the active edge of the clock, if data is far from the active edge Tcq(Clock to output delay) is stable. When data comes near to the active edge

of the clock, the Tcq will start increasing after some time it fails. When data is far from the active edge the Tcq is said to be base delay. So when Tcq = 110% of base delay, At that time the value of Tdc is called setup rise time.

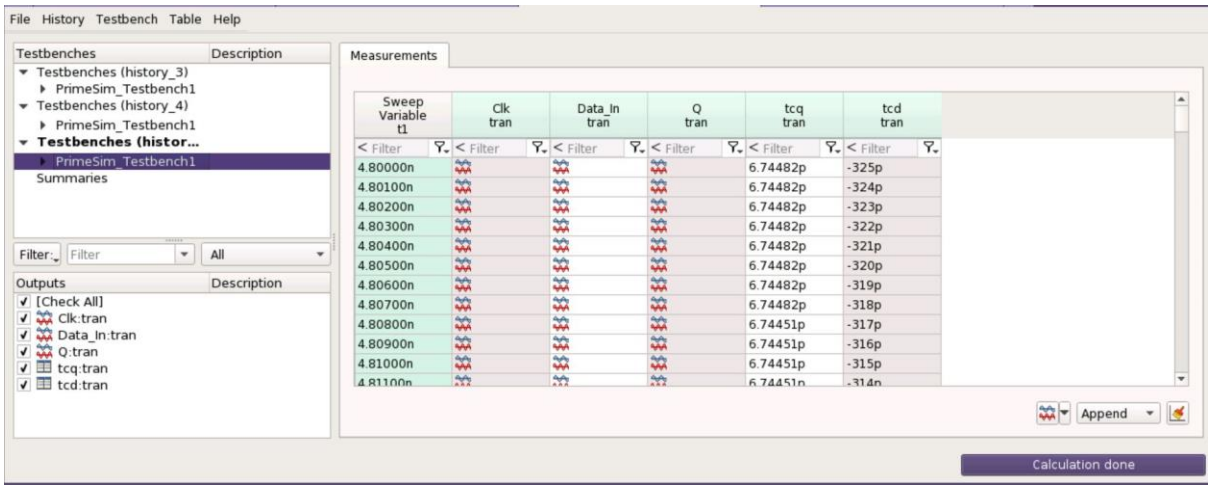
- PRIMEWAVE PARAMETERS

Here we have varied the input voltage coordinate t1 from 4.8n to 5.1n sec.

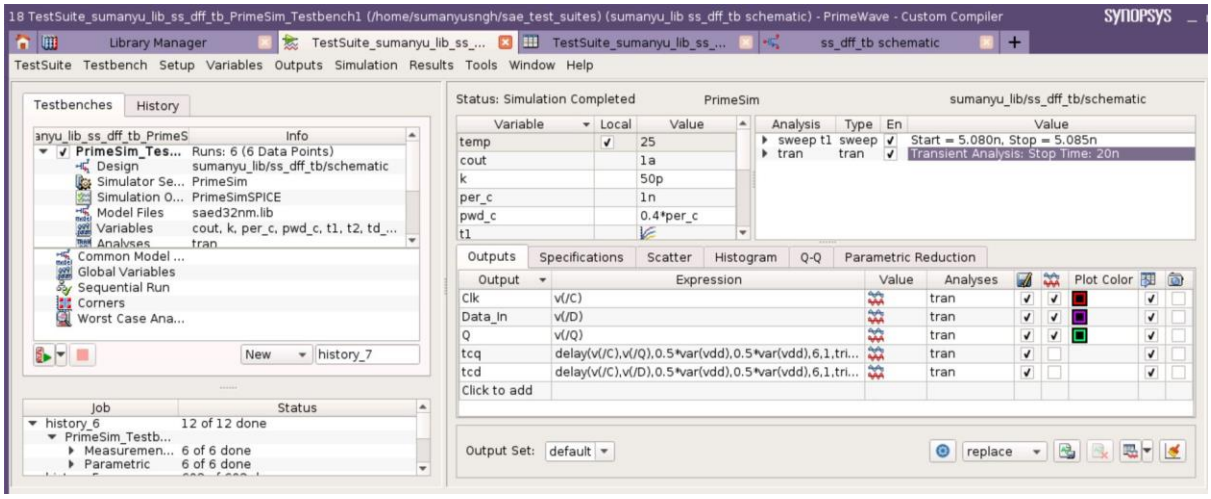


- TESTBENCH RESULTS

From the results we have observed the tcq is 6.744p sec. Then for 110% of tcq is 7.4184p sec.

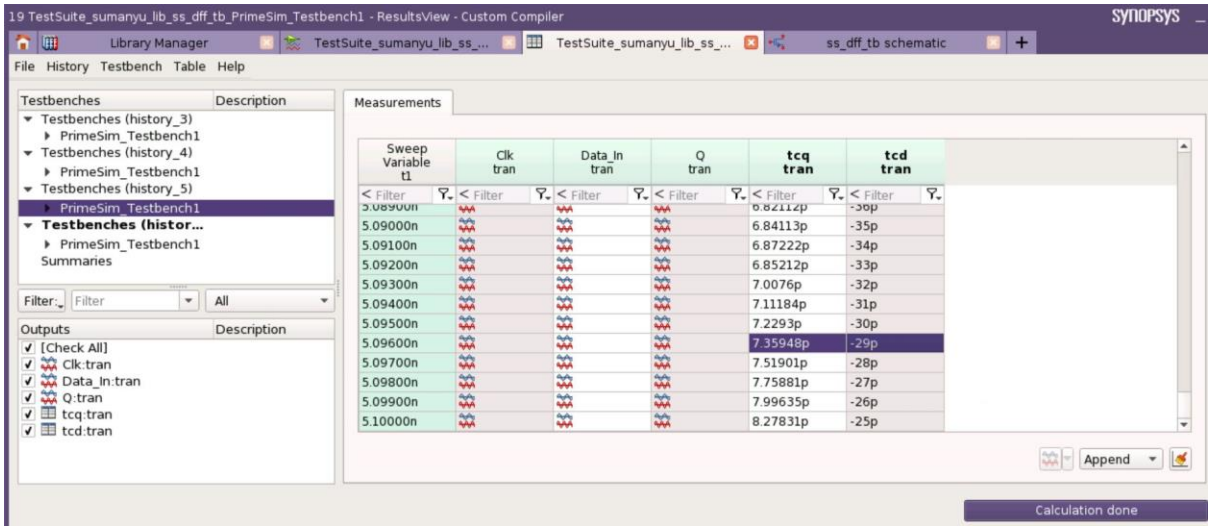


- PRIMEWAVE PARAMETERS Here we have varried the input voltage coordinate t1 from 5.080n to 5.085nsec.



- TESTBENCH RESULTS

From the testbench result we can observe that for tcq =7.359p sec the calculated tcd= -29p sec Calculated Set up time = -29p sec

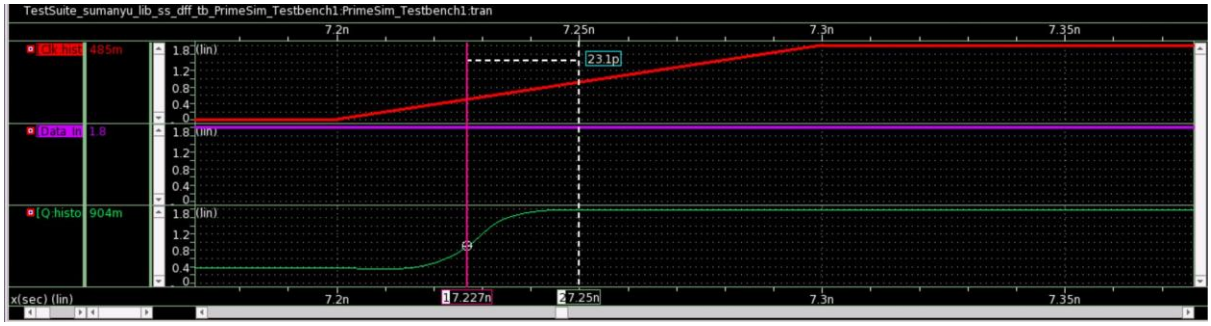


- TESTBENCH WAVEFORM

PROPAGATION DELAY

Finally, for the propagation delay, the inputs transition at least one set-up time before the rising edge of the clock and the delay is measured from the 50% point of the CLK edge to the 50% point of the Q output. From this simulation Tc-q (low to high) was 23.1 psec and Tc-q (high to low) was 6.97 psec.

Tc-q (Low to High)



Tc-q (High to Low)

POWER CALCULATION

- Steps to calculate the Avg Current

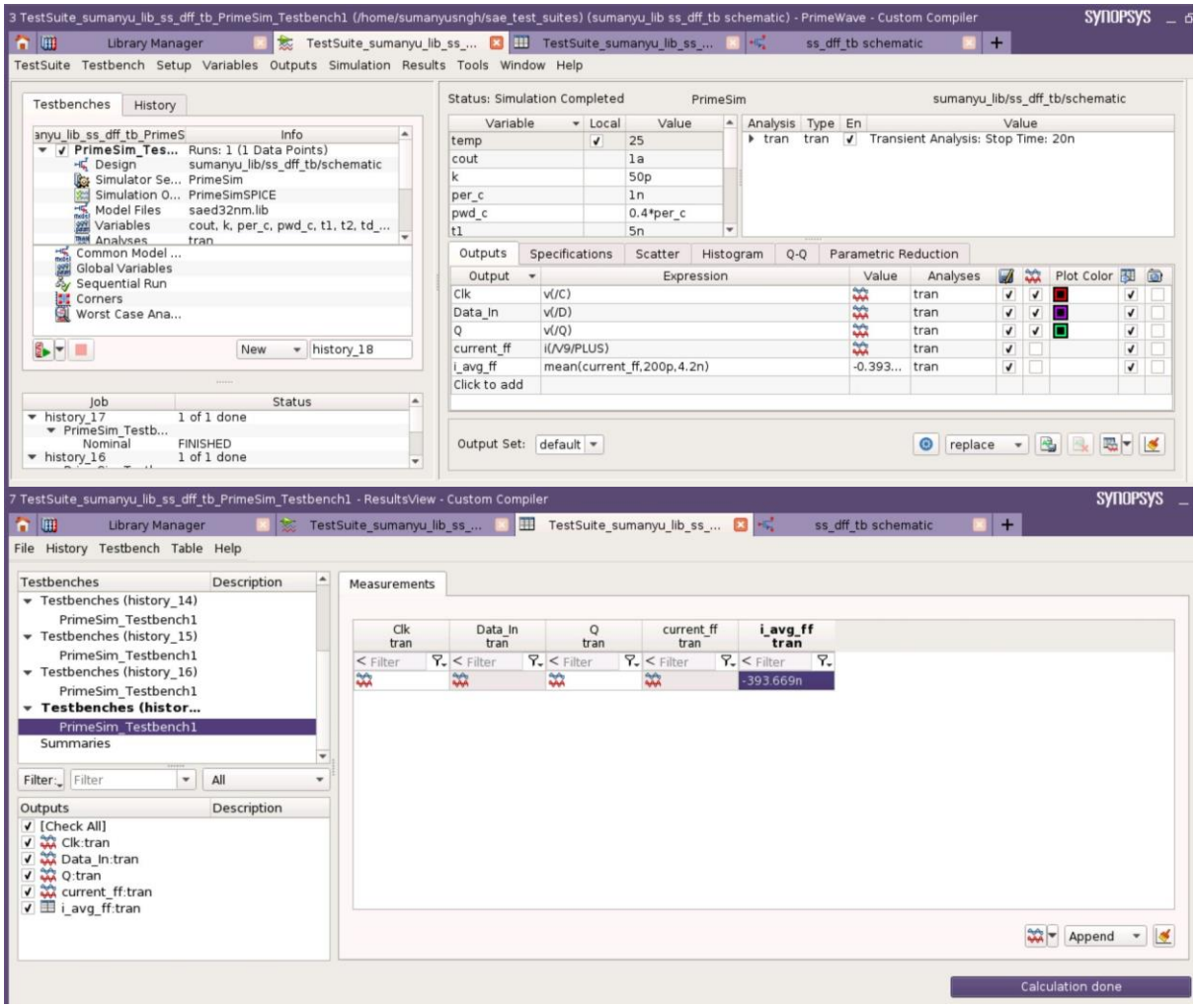
1. Take Vdd node Current from the output option (Select from the Design). I have named it as current_ff.
2. Open the calculator from output option and select mean filter.
3. Give Required values (current_ff, 200ps, 4.2n). We need to give the 3rd value as integer multiple of time period thats why I took it for 4 cycles (you can take any number of cycles).
4. Now netlist and run the simulation.
5. Open viewer from the results option.
6. We can see the Avg Current value is 393.669n amp.

- PRIMEWAVE PARAMETERS

The value of average current at Node vdd is calucalted for 1 GHZ clock frequency.

- TESTBENCH RESULTS

The value of average current is 393.669 nano amp.



SIMULATION RESULT

- Set up time = -29p sec
- Tc-q (Low to High) =23.1p sec
- Tc-q (High to Low) =6.97p sec
- Average Current = 393.669 nano amp
- Power = 393.669n Amp. *Vdd(=1.8V) = 708.60 nano Watt.

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REFERENCES

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