SAMEER AYACHIT

ayachitsameer@gmail.com   9008550561

Electronics and Communication Engineering student in the 6th semester under VTU, with a strong foundation in digital systems, VLSI design, and circuit simulation. Experienced in Verilog and Python, with hands-on projects involving logic design and fault detection in circuits. Passionate about applying technical skills to real-world problems and continuously learning to grow in the field of electronics and embedded systems.

Education

ENGINEERING   Aug 2022 - Present
J.S.S. ACADEMY OF TECHNICAL EDUCATION BANGALORE

Overall Grade: 7.38

10TH   96, 5th Main Rd, BEML Layout, 5th
Swargarani School & PU College   Stage, Rajarajeshwari Nagar, Ben-
                                                                                         galuru, Karnataka, 560098
                                                                                         Jun 2015 - Jul 2020

Overall Grade: 87.00

12TH/PUC   1/1A, 1st Main Rd, Brindavan Layout,
Sri Kumaran Children's Home Composite Junior College   Padmanabhanagar, Bengaluru, Kar-
                                                                                         nataka 560061
                                                                                         Jun 2020 - Jun 2022

Overall Grade: 74.50

Projects

Carry skip adder   Jan 2025 - Jan 2025
JSSATEB

The implementation of a Carry Skip Adder using Verilog involves designing a fast adder that reduces propagation delay by skipping over carry generation blocks when possible. This project includes modeling, simulation, and verification of the adder's functionality and performance using Verilog HDL, enhancing understanding of efficient arithmetic circuit design

Fault detection in vlsi circuits using artificial intelligence and ma-   Sep 2024 - Dec 2024
chine learning
JSSATEB

This project is a machine learning based project, where we found the faults, specifically syntax and logical faults such as stuck at faults in vlsi circuits using different models of machine learning like logistic regression, support vector machine, etc.

Deep Learning   NumPy   Scikit-learn   Python   Machine Learning   Pandas

CMOS Inverter   Dec 2024 - Jan 2025
JSSATEB

The implementation of a CMOS inverter using the Cadence tool involves designing and simulating a basic digital logic gate using complementary MOSFETs. This process includes schematic design, layout creation, DRC/LVS checks, and transient analysis to verify performance.

Skills

Python   Machine Learning   Deep Learning   MATLAB   C++   C   Java   Scikit-learn

NumPy   Object-Oriented Programming

Certifications

Internship   Dec 2024 - Dec 2024
Corizo edutech Private LTD.

Python essentials 1   Aug 2023 - Aug 2023
Cisco networking Academy

Python

Training certificate   Nov 2024 - Dec 2024
Corizo edutech Private LTD.