Parineeta S

+91 7019489085 parineetapari15@gmail.com www.linkedin.com/in/parineeta-s-419443313

Summary

Motivated and detail-oriented Bachelor of Engineering student with hands-on experience in both software development and hardware systems. Skilled in programming languages such as C++, Python, and Java, with a solid foundation in embedded systems, circuit design, and hardware testing. Experience in developing and automating test frameworks, executing system integration tests, and collaborating on multidisciplinary engineering projects. Interested in applying a hybrid skill set to innovate and optimize solutions in dynamic engineering environments.

Education

JSS Academy of Technical Education **August 2022 – August 2026**
Bachelor's in Electronics and Communication Engineering - ***CGPA 8.1*** *Bangalore, India*

Vidyaniketan PU college **August 2020 – May 2022**
PUC Percentage - 86.6 *Bangalore, India*

Aryan Presidency School **June 2019 – March 2020**
10th Std Percentage - 89 *Bangalore, India*

Internship

AICTE and VOIS | *Data Analytics* **October 2024**

- Analyzed large datasets and applied Artificial Intelligence (AI) techniques to extract actionable insights for business decision-making, improving data-driven strategies.
- Utilized Large Language Models (LLM) to enhance data processing, text analysis, and natural language understanding for automating tasks and improving data accuracy.
- Developed and deployed AI models, integrating them with data pipelines to deliver real-time analytics and streamline reporting workflows.

Projects

Smart Road Sign Recognition | *Ardiuno* **October 2024**

- Developed an Arduino-based smart road sign recognition system integrating camera modules and proximity sensors for real-time environment awareness.
- Integrated ultrasonic sensors and IR sensors to enhance system safety and automate vehicle responses based on recognized signs.
- Programmed Arduino using python to control decision-making logic based on detected road signs and sensor inputs.

Odd parity Check | *Verilog HDL* **March 2024**

- Designed and implemented a digital circuit to perform odd parity checking on input binary data using Verilog HDL.
- Developed behavioral and structural models to validate the parity bit for 4-bit/8-bit input sequences and Optimized design for minimal gate usage and verified timing performance through synthesis.
- Simulated and verified functionality using testbenches in ModelSim

Training/Workshops

- Completed a comprehensive Udemy course on Data Structures and Algorithms, covering arrays, linked lists, stacks, queues, trees, graphs, sorting, and searching techniques.
- Completed a certification course in Internet of Things (IoT) from Simplilearn, covering IoT architecture, sensors, communication protocols, and application development.
- Participated in a PCB Design Workshop, gaining hands-on experience in schematic design, layout techniques, and using PCB design software such as Eagle/Altium.
- Attended a Full Stack Web Development Workshop at Prinston Smart Engineers, gaining hands-on experience in both front-end and back-end.

Technical Skills

Languages: C++, Java, C, Python, SQL, VHDL, MATLAB, SIMULINK.
Simulation and Design: Digital Circuit Simulation, Schematic Design, PCB Design, VHDL/Verilog Simulation.
Platforms: Linux, AWS, Microsoft, Windows,Arduino IDE, Raspberry Pi
Soft Skills: Team-player, Leadership, Problem solving, Communication.