MAHALAKSHMI J







ABOUT

I am a passionate Electronics and Communication Engineering student at JSS Academy of Technical Education, Bangalore, with a deep interest in VLSI, embedded systems, and the semiconductor domain. I have honed my skills in Verilog, C++, Python, C, and Embedded C through academic projects and hands-on experiences, including the "Design and Implementation of a Single Cycle Core RISC-V Processor".

TECHNICAL SKILLS

SOFT SKILLS

Python (basics)C language	Verilog HDLEmbedded C	Communication Leadership quality Active listener
EDUCATION		Problem solving

YEAR	INSTITUTE	SGPA/Percentage				
2022- PRESENT	Bachelor of Engineering , Electronics and Communication JSS Academy of Technical Education, Bangalore	8.2	II 9.40	III 8.15	IV 8.40	V 8.82
2020-2022	ASC PU College ,Bangalore	87%				
2020	KLE Society's School ,Bangalore	85%				

PROJECT WORK

PROJECT TITLE

• Design and Implementation of RISC-V Single cycle core Processor

HIGHLIGHTS

- Design and implement Single cycle core of RISC-V processor using Verilog ,which can perform Arithmetic and Logical operations to handle wide range of operations
- Verify funcionality of RISC-V processor using testbench and simulate the same

LANGUAGES KNOWN

- English
- Kannada
- Hindi

CERTIFICATIONS

Machine Learning with Python: Foundations

Entry -Level Python Programming