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# 深圳市灵星芯微电子科技有限公司

Shenzhen Lingxing Microelectronics Technology Co., Ltd.

编号: CD4017-LX-A17

# **CD4017 (LX) 5-stage Johnson Decade Counter**

# **Specification Product**

### **Specification Revision History:**

Version	Date	Description
2021-12-A1	2021-12	New

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# 1. General Description

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The CD4017 is a 5-stage Johnson decade counter with ten spike-free decoded active HIGH outputs (Q0 to Q9), an active LOW carry output from the most significant flip-flop (Q5-9), active HIGH and active LOW clock inputs (CP0, CP1) and an overriding asynchronous master reset input (MR).

The counter is advanced by either a LOW-to-HIGH transition at CP0 while  $\overline{\text{CP1}}$  is LOW or a HIGH-to-LOW transition at  $\overline{\text{CP1}}$  while  $\overline{\text{CP0}}$  is HIGH.

When cascading counters, the Q5-9 output, which is LOW while the counter is in states 5, 6, 7, 8, and 9, can be used to drive the CP0 input of the next counter. A HIGH on MR resets the counter to zero (Q0=Q 5-9=HIGH; Q1 to Q9=LOW) independent of the clock inputs (CP0, CP1).

Automatic counter code correction is provided by an internal circuit: following any illegal code the counter returns to a proper counting mode within 11 clock pulses.

It operates over a recommended  $V_{DD}$  power supply range of 3V to 15V referenced to  $V_{SS}$  (usually ground). Unused inputs must be connected to  $V_{DD}$ ,  $V_{SS}$ , or another input.

#### **Features:**

- Wide supply voltage range from 3V to 15V
- Automatic counter correction
- Tolerant of slow clock rise and fall times
- 5V, 10V, and 15V parametric ratings
- Standardized symmetrical output characteristics
- Specified from -40°C to +125°C
- Packaging information: DIP16/SOP16/TSSOP16

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### **Ordering Information:**

# **Tube packing specifications:**

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Type number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Packing box number	Packing quantity	Notes
CD4017BE(LX)	DIP16	CD4017BE	25 PCS/tube	40 tube/box	1000 PCS/box	10 box/pack	10000 PCS/pack	Dimensions of plastic enclosure: 19.0mm×6.4mm Pin spacing: 2.54mm

### **Reel packing specifications:**

Type number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Packing quantity	Notes
CD4017BM(LX)	SOP16	CD4017BM	4000 PCS/reel	8000 PCS/box	64000 PCS/pack	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing:1.27mm
CD4017BPW(LX)	TSSOP16	CD4017	5000 PCS/reel	10000 PCS/box	80000 PCS/pack	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing:0.65mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

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# 2. Block Diagram And Pin Description

### 2.1 、 Block Diagram

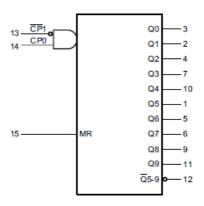


Figure 1. Logic symbol

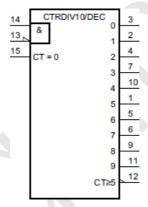


Figure 2. IEE logic symbol

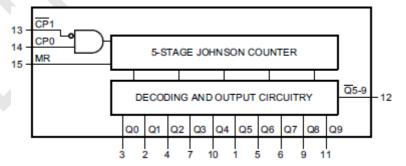


Figure 3. Functional diagram

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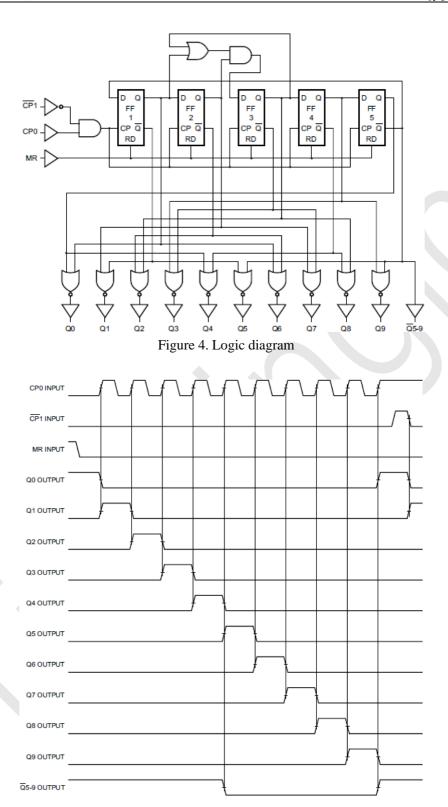


Figure 5. Timing diagram

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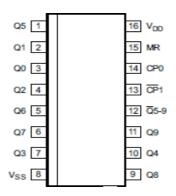


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#### 2.2 \ Pin Configurations

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### 2.3 , Pin Description

Pin No.	Pin Name	Description		
1	Q5	decoded output		
2	Q1	decoded output		
3	Q0	decoded output		
4	Q2	decoded output		
5	Q6	decoded output		
6	Q7	decoded output		
7	Q3	decoded output		
8	$V_{SS}$	ground (0V)		
9	Q8	decoded output		
10	Q4	decoded output		
11	Q9	decoded output		
12	Q5-9	carry output (active LOW)		
13	CP1	clock input (HIGH-to-LOW edge-triggered)		
14	CP0	clock input (LOW-to-HIGH edge-triggered)		
15	MR	master reset input		
16	$V_{DD}$	supply voltage		

# 2.4 . Function Table

	Input		Onevetion	
MR	CP0	CP1	Operation	
Н	X	X	Q0=Q5-9=H; Q1 to Q9=L	
L	Н	$\downarrow$	counter advances	
L	1	L	counter advances	
L	L	X	no change	
L	X	Н	no change	
L	Н	1	no change	
L	<u> </u>	L	no change	

Note: H=HIGH voltage level; L=LOW voltage level; X=don't care;

 $\uparrow$ =positive-going transition;  $\downarrow$ =negative-going transition.

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#### 3. Electrical Parameter

#### 3.1 Absolute Maximum Ratings

(Voltages are referenced to V<sub>SS</sub> (ground=0V), unless otherwise specified.)

Parameter	Symbol	Cond	Conditions Min		Max.	Unit	
supply voltage	$V_{\mathrm{DD}}$	-		-0.5	+18	V	
DC input current	$I_{IK}$	any one input		-	±10	mA	
input voltage	$V_{I}$	all in	-0.5	V <sub>DD</sub> +0.5	V		
storage temperature	$T_{stg}$	-	-65	+150	°C		
total power dissipation	$P_{tot}$	-		-	500	mW	
device dissipation	P	per output transistor		-	100	mW	
Soldering	$T_{ m L}$	10s	DIP	2	45	°C	
temperature	ıΓ	108	SOP	2.	50	C	

#### Note:

- [1] For DIP16 packages: above  $70^{\circ}$ C the value of  $P_{tot}$  derates linearly with 12mW/K.
- [2] For SOP16 packages: above 70°C the value of Ptot derates linearly with 8mW/K.
- [3] For (T)SSOP16 packages: above 60°C the value of Ptot derates linearly with 5.5mW/K.

### 3.2 Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Тур.	Max.	Unit
supply voltage	$V_{DD}$	-	3	1	15	V
ambient temperature	$T_{amb}$	in free air	-40	1	+85	°C
-11-:		$V_{DD}=5V$	1	1	2.5	MHz
clock input frequency	$f_{CL}$	$V_{DD}=10V$	ı	ı	5	MHz
nequency		$V_{DD}=15V$	-	-	5.5	MHz
		$V_{DD}=5V$	200	-	-	ns
clock pulse width	$t_{\mathrm{w}}$	$V_{DD}=10V$	90	1	-	ns
		$V_{DD}=15V$	60	1	-	ns
1 1 1		$V_{DD}=5V$				-
clock rise and fall time	$t_{rCL}, t_{fCL}$	$V_{DD}=10V$	unlimited			-
Tan time		V <sub>DD</sub> =15V				-
-1111-1-1-1-		$V_{DD}=5V$	230	-	-	ns
clock inhibit setup time	$t_{\rm s}$	$V_{DD}=10V$	100	-	-	ns
setup time		$V_{DD}=15V$	70	-	-	ns
		$V_{DD}=5V$	260	1	-	ns
reset pulse width	$t_{RW}$	$V_{DD}=10V$	110	-	-	ns
		$V_{DD}=15V$	60	1	-	ns
		V <sub>DD</sub> =5V		1	-	ns
reset removal time	$t_{rec}$	$V_{DD}=10V$	280	1	-	ns
time		$V_{DD}=15V$	150	-	-	ns

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#### 3.3 Lectrical Characteristics

#### 3.3.1, DC Characteristics 1

(T<sub>amb</sub>=25°C, voltages are referenced to V<sub>SS</sub> (ground=0V), unless otherwise specified.)

Danier Arm	Symbol		onditions (		1	TT4		
Parameter	Symbol	Vo	$V_{IN}$	$V_{DD}$	Min.	Тур.	Max.	Unit
		-	0, 5	5	-	0.04	5	uA
supply current	$I_{DD}$	-	0, 10	10	-	0.04	10	uA
		-	0, 15	15	-	0.04	20	uA
LOWI		0.4	0, 5	5	0.51	1	-	mA
LOW-level output current	$I_{OL}$	0.5	0, 10	10	1.3	2.6	-	mA
output current		1.5	0, 15	15	3.4	6.8	-	mA
		4.6	0, 5	5	-0.51	-1	-	mA
HIGH-level	T	2.5	0, 5	5	-1.6	-3.2	-	mA
output current	$I_{OH}$	9.5	0, 10	10	-1.3	-2.6	-	mA
		13.5	0, 15	15	-3.4	-6.8	-	mA
LOWI		-	0, 5	5	-	0	0.05	V
LOW-level output voltage	$V_{OL}$	_	0, 10	10	-	0	0.05	V
output voltage		-	0, 15	15	-	0	0.05	V
HIGH-level		-	0, 5	5	4.95	5	-	V
output voltage	$V_{OH}$	-	0, 10	10	9.95	10	-	V
output voltage		-	0, 15	15	14.95	15	-	V
LOW local		0.5, 4.5	-	5	-	-	1.5	V
LOW-level input voltage	$V_{IL}$	1, 9	-	10	-	-	3	V
input voitage		1.5, 13.5		15	-	-	4	V
IIICII I	V	0.5, 4.5	-	5	3.5	-	-	V
HIGH-level input voltage		1, 9	-	10	7	-	-	V
input voitage		1.5, 13.5	-	15	11	-	-	V
input leakage current	II	-	0, 15	15	-	±10 <sup>-5</sup>	±0.1	uA

### 3.3.2 DC Characteristics 2

 $(T_{amb}$ =-40°C to +85°C, voltages are referenced to  $V_{SS}$  (ground=0V), unless otherwise specified.)

Parameter	Cymbol	C	onditions (	V)	T <sub>amb</sub> =	-40°C	T <sub>amb</sub> =	+85°C	Unit
rarameter	Symbol	$\mathbf{v_o}$	$V_{IN}$	$V_{DD}$	Min.	Max.	Min.	Max.	Omt
		1	0, 5	5	-	5	-	150	uA
supply current	$I_{DD}$	-	0, 10	10	-	10	-	300	uA
		1	0, 15	15	-	20	-	600	uA
LOWI		0.4	0, 5	5	0.61	-	0.42	-	mA
LOW-level output current	$I_{OL}$	0.5	0, 10	10	1.5	-	1.1	-	mA
output current		1.5	0, 15	15	4	-	2.8	-	mA
		4.6	0, 5	5	-0.61	-	-0.42	-	mA
HIGH-level	T	2.5	0, 5	5	-1.8	-	-1.3	-	mA
output current	$I_{OH}$	9.5	0, 10	10	-1.5	-	-1.1	-	mA
	13.5	0, 15	15	-4	-	-2.8	-	mA	
LOW-level	$V_{\mathrm{OL}}$	1	0, 5	5	-	0.05	-	0.05	V
output voltage	V OL	-	0, 10	10	-	0.05	-	0.05	V

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		-	0, 15	15	-	0.05	-	0.05	V
IIIGII 1		-	0, 5	5	4.95	-	4.95	-	V
HIGH-level output voltage	$V_{OH}$	-	0, 10	10	9.95	1	9.95	1	V
output voltage		-	0, 15	15	14.95	1	14.95	1	V
LOWI		0.5, 4.5	-	5	-	1.5	-	1.5	V
LOW-level input voltage	$V_{IL}$	1, 9	-	10	-	3	-	3	V
input voitage		1.5, 13.5	-	15	-	4	-	4	V
IIIGII 1		0.5, 4.5	-	5	3.5	-	3.5	-	V
HIGH-level input voltage	$V_{IH}$	1, 9	-	10	7	-	7	-	V
input voitage		1.5, 13.5	1	15	11	1	11	-	V
input leakage	$I_{I}$	-	0, 15	15	-	±0.1	-	±1	uA

### 3.3.3 、 AC Characteristics

 $(T_{amb}=25^{\circ}C, V_{SS}=0V, t_r, t_f=20ns, C_L=50pF, R_L=200k\Omega, unless otherwise specified.)$ 

Parameter	Symbol	Conditie	ons	Min.	Тур.	Max.	Unit
		CP0, CP1 to Q0 to	V <sub>DD</sub> =5V	-	325	650	ns
		Q9;	V <sub>DD</sub> =10V	-	135	270	ns
		see Figure 7	V <sub>DD</sub> =15V	-	85	170	ns
		CP0, CP1 to Q5-9; see Figure 7	V <sub>DD</sub> =5V	-	300	600	ns
propagation delay time	$t_{PHL}$ , $t_{PLH}$		$V_{DD}=10V$	-	125	250	ns
delay time			V <sub>DD</sub> =15V	-	80	160	ns
		ND - 00 - 00	V <sub>DD</sub> =5V	-	265	530	ns
		MR to Q0 to Q9; see Figure 7	V <sub>DD</sub> =10V	-	115	230	ns
		see Figure 7	V <sub>DD</sub> =15V	-	85	170	ns
			V <sub>DD</sub> =5V	-	100	200	ns
transition time	t <sub>t</sub>	see Figure 7	V <sub>DD</sub> =10V	-	50	100	ns
			V <sub>DD</sub> =15V	-	40	80	ns
			V <sub>DD</sub> =5V	-	100	200	ns
pulse width	tw	see Figure 8	V <sub>DD</sub> =10V	-	45	90	ns
			V <sub>DD</sub> =15V	-	30	60	ns
1 1 1 1			V <sub>DD</sub> =5V				
clock rise and fall time	$t_{rCL}, t_{fCL}$	-	$V_{DD}=10V$	unlimited			-
Tan time			$V_{DD}=15V$				-
maximum			$V_{DD}=5V$	2.5	5	-	MHz
clock	$f_{CL}$	see Figure 8	$V_{DD}=10V$	5	10	-	MHz
frequency			V <sub>DD</sub> =15V	5.5	11	-	MHz
		_	$V_{DD}=5V$	-	115	230	ns
setup time	$t_{\rm s}$	CP0 to CP1;	$V_{DD}=10V$	-	50	100	ns
		see Figure 9	$V_{DD}=15V$	-	35	70	ns
	t t	MD:	V <sub>DD</sub> =5V	-	200	400	ns
reset removal time		MR input; see Figure 8	V <sub>DD</sub> =10V	-	140	280	ns
time		see Figure 6	V <sub>DD</sub> =15V	-	75	150	ns
input capacitance	C <sub>I</sub>	any inp	out	-	5	-	pF

Note:  $t_t$  is the same as  $t_{TLH}$  and  $t_{THL}$ .

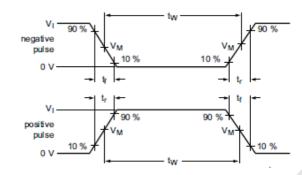
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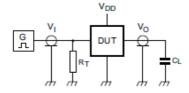
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# **4.** Testing Circuit

### 4.1 、 AC Testing Circuit



#### a. Input waveforms



#### b. Test circuit

Figure 6. Test circuit for switching times

Definitions for test circuit:

**DUT=Device Under Test.** 

C<sub>L</sub>=Load capacitance including jig and probe capacitance.

 $R_T$ =Termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator.

#### 4.2 , AC Testing Waveforms

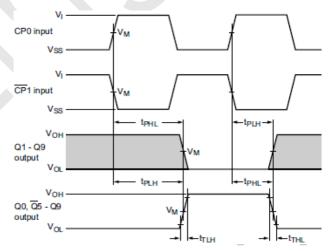


Figure 7. Waveforms showing the propagation delays for CP0, CP1 to Qn, Q5-9 outputs and the output transition times

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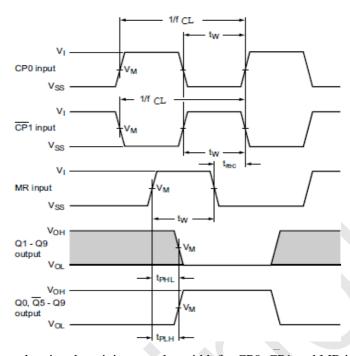


Figure 8. Waveforms showing the minimum pulse width for CP0, CP1 and MR input; the maximum frequency for CP0 and CP1 input; the recovery time for MR and the MR input to Qn and Q5-9 output propagation dela

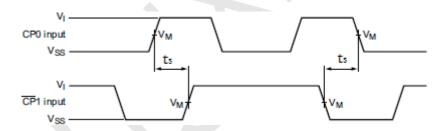


Figure 9. Waveforms showing hold times for CP0 to CP1 and CP1 to CP0

#### 4.3 Measurement Points

Supply voltage	Input	Output
$ m V_{DD}$	$\mathbf{V}_{\mathbf{M}}$	$\mathbf{V}_{\mathbf{M}}$
5V to 15V	$0.5 \times V_{DD}$	$0.5 \times V_{DD}$

#### 4.4 \ Test Data

Supply voltage	In	Load		
$ m V_{DD}$	$V_{I}$	$t_{ m r}$ , $t_{ m f}$	$C_{L}$	
5V to 15V	V <sub>SS</sub> or V <sub>DD</sub>	≤ 20ns	50pF	

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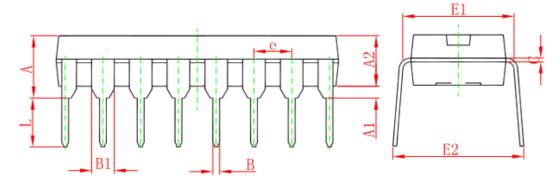


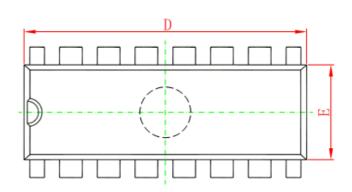
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# **5. Package Information**

# 5.1 、 **DIP16**





Symbol	Dimensions In	n Millimeters	Dimensions In Inches		
	Min	Max	Min	Max	
Α	3. 710	4. 310	0.146	0. 170	
A1	0. 510		0.020		
A2	3. 200	3.600	0.126	0. 142	
В	0. 380	0.570	0.015	0. 022	
B1	1. 524	(BSC)	0.060 (BSC)		
С	0. 204	0.360	0.008	0.014	
D	18. 800	19. 200	0.740	0.756	
E	6. 200	6.600	0. 244	0. 260	
E1	7. 320	7.920	0.288	0.312	
е	2. 540	(BSC)	0. 100 (BSC)		
L	3. 000	3.600	0. 118	0.142	
E2	8, 400	9.000	0.331	0.354	

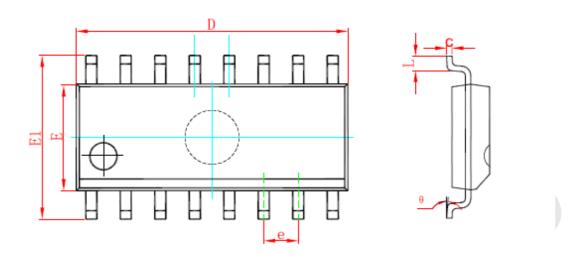
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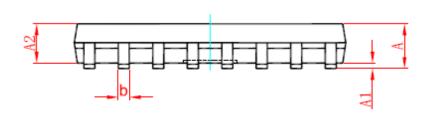
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### 5.2 SOP16

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Symbol	Dimensions In	n Millimeters	Dimensions In Inches			
	Min	Max	Min	Max		
Α	1. 350	1. 750	0. 053	0. 069		
A1	0. 100	0. 250	0.004	0. 010		
A2	1. 350	1. 550	0. 053	0. 061		
b	0. 330	0. 510	0. 013	0. 020		
С	0. 170	0. 250	0.007	0. 010		
D	9. 800	10. 200	0. 386	0. 402		
E	3. 800	4. 000	0. 150	0. 157		
E1	5. 800	6. 200	0. 228	0. 244		
е	1. 270	(BSC)	0. 050 (BSC)			
L	0. 400	1. 270	0. 016	0. 050		
θ	0°	8°	0°	8°		

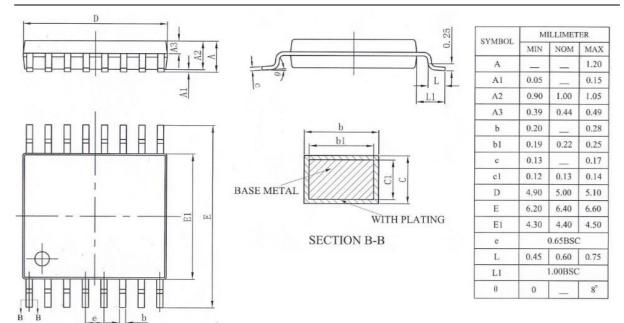
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#### 5.3 、TSSOP16



### 6. Statements And Notes

#### 6.1. The name and content of Hazardous substances or Elements in the product

	Hazardous substances or Elements									
Part name	Lead and lead compo unds	Mercur y and mercur y compo unds	Cadm ium and cadmi um comp ounds	Hexaval ent chromiu m compoun ds	Polybro minated biphenyl s	Polybro minate d biphen yl ethers	Dibutyl phthala te	Butylbe nzyl phthala te	Di-2-et hylhex yl phthala te	Diisobu tyl phthala te
Lead frame	0	0	0	0	O	0	0	0	0	0
Plastic resin	0	0	0	0	0	0	0	0	0	0
Chip	0	0	0	0	O	0	0	0	0	0
The lead	0	0	0	0	0	0	0	0	0	0
Plastic sheet installed	0	0	0	0	0	0	0	0	0	0
explanation	o: Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard.  ×: Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

#### 6.2 Notion

Recommended carefully reading this information before the use of this product;

The information in this document are subject to change without notice;

This information is using to the reference only, the company is not responsible for any loss;

The company is not responsible for the any infringement of the third party patents or other rights of the responsibility.

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