# CSA - Computer systems architecture

1. **Match the computer systems generations:**

| | |
|---|---|
| First generation | 1945-1958 |
| Second generation | 1958-1964 |
| Third generation | 1964-1974 |
| Fourth generation | 1974 – present |

2. **Controls the operation of the computer and performs its data processing functions:**

- Main memory
- I/O
- CPU
- System interconnection

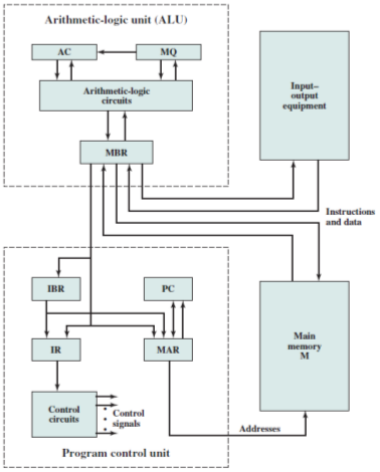
3. **What provides storage internal to the CPU?**

- Registers
- Arithmetic and logic unit
- CPU interconnection
- Control unit

4. **ENIAC stands for:**

- Electronical Numerical Integrator And Computer
- Electronic Numerical Integration Analogue Computer
- Electronic Numerical Integrator And Computer
- Electronic Numerical Interaction And Calcuation

5. **The figure reveals that both the control unit and the ALU contain storage, called registers, match the definitions:**




| |
|---|
| Contains a word to be stored in memory or sent to the I/O unit, or is used to receive a word from memory or from the I/O unit. |

Memory buffer register (MBR)

Specifies the address in memory of the word to be written from or read into the MBR.

Memory address register (MAR)

Contains the 8-bit opcode instruction being executed.

Instruction register (IR)

Employed to hold temporarily the right-hand instruction from a word in memory.

Instruction buffer register (IBR)

Contains the address of the next instruction pair to be fetched from memory.

Program counter (PC)

Employed to hold temporarily operands and results of ALU operations.

Accumulator (AC) and multiplier quotient (MQ)

6. **How the central termination point for data channels, the CPU, and memory is called. It schedules access to the memory from the CPU and data channels, allowing these devices to act independently.**

- ○ Transistor
- ● Multiplexor
- ○ Integrated circuit
- ○ Resistors
- ○ Capacitors

7. **Expand the abbreviation VLSI**

- ● Very-large-scale integration
- ○ Very-little-scale integration
- ○ Very-large-scale interactions
- ○ Very-large-scale integrator

8. **Which technique allows to processor simultaneously work on multiple instructions?**

- ○ Branch prediction
- ○ Data flow analysis
- ● Pipelining
- ○ Speculative execution

9. **Using this technique processor looks ahead in the instruction code fetched from memory and predicts which groups of instructions are likely to be processed next.**

- ● Branch prediction
- ○ Data flow analysis
- ○ Pipelining
- ○ Speculative execution

10. **Which technique helps to processor investigates which instructions are dependent on each other's results, or data, to create an optimized schedule of instructions**

- ○ Branch prediction
- ● Data flow analysis
- ○ Pipelining

- Speculative execution

**11. This technique enables the processor to keep its execution engines as busy as possible by executing instructions that are likely to be needed.**

- Branch prediction
- Data flow analysis
- Pipelining
- Speculative execution

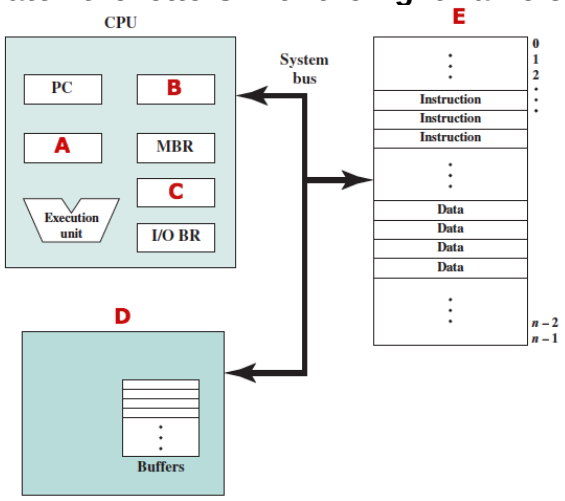
**12. The world's first general-purpose microprocessor. It was used in the first personal computer, the Altair.**

- 8070
- 8080
- 8086
- 8090

**13. Which of the following laws deals with the potential speedup of a program using multiple processors compared to a single processor.**

- Moor's Law
- Little's Law
- Murphy's law
- Amdahl's law

**14. Match the letters with the right name of the Computer Components: Top-Level View:**




A
IR -Instruction register

B
MAR-Memory address registers

C
I/O Input/output address register

D
I/O Module

E
Main memory

15. **The processor responds by suspending operation of the current program, branching off to a program to service that particular I/O device, known as _____, and resuming the original execution after the device is serviced. Which of the following will be the missing word:**

- interrupt handler
- interrupt cycle
- disabled interrupt
- interrupt request

16. **What is the data line?**

- provide a path for moving data among system modules
- is used to designate the source or destination of the data on the data bus
- is used to control the access to and the use of the data and address lines
- indicates that a module needs to gain control of the bus

17. **What is used to manage the access to and the use of the data and address lines?**

- address bus
- control lines
- memory write
- bus grant
- address lines

18. **Bus lines can be separated into two generic types:**

- Dedicated
- Centralized
- Distributed
- Multiplexed
- Synchronous
- Asynchronous

19. **PCI stands for:**

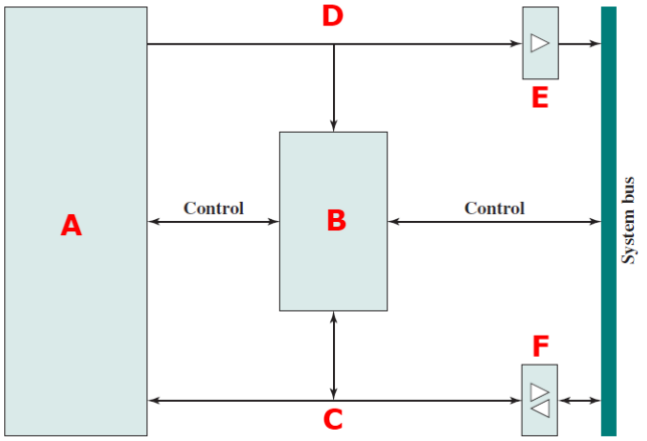
- Power Control Interface
- Peripheral component interconnect
- Property Casualty Insurers
- Programmable Communications Interface

20. **The methods of accessing units of data:**

- Sequential access
- Pseudo access
- Direct access
- Indirect access
- Single access
- Random access

- Associative access

**21. Match the letters on the picture with right name of the cash memory component's names:**




| | |
|---|---|
| A | Processor |
| B | Cache |
| C | Data |
| D | Address |
| E | Address buffer |
| F | Data buffer |

**22. What kind of memory type stores data using virtual addresses:**

- Logical
- Virtual
- Peripheral
- Main
- Buffer

**23. Amdahl's law:**

- Speed up= 1/(1 + f ) * f/N
- Speed up= 1/(1 - f ) * f/N
- Speed up= 1/(1 - f ) - f/N
- Speed up= 1/(1 - f ) + f/N
- Speed up= 1/(1 + f ) + f/N

**24. AMAT stands for:**

- Average memory access time
- Automatic Message Accounting Transmitter
- Asymptotic Mean Acquisition Time

- Absolute memory access time

**25. _____ is a special purpose system that is used to perform one or few dedicated functions.**

- Distributed systems
- Embedded systems
- Ultra-Large-Scale Systems
- Centralized systems
- Ubiquitous systems

**26. Microprocessor can't do all the functions of a computer system on its own**

**27. Match the statements with the right architecture**

| | |
|---|---|
| Von Neumann | One memory for data and program, with one bus for both |
| Von Neumann | CPU provides address to get data or instructions |
| Von Neumann | Data and instructions must have the same width |
| Harvard | Separate program and data memories and separate busses, can be accessed simultaneously |
| Harvard | Separated buses allow one instruction to execute while the next instruction is fetched |
| Harvard | Data and instructions mustn't have the same width |

**28. How many generations semiconductor memory has been through, since 1970? (please write number)**

- 13

**29. MIC stands for:**

- mini integrated core
- many integrated core
- main integrated core
- many interaction core
- main interaction core

**30. Clock Frequency of SDRAM is equal to:**

- 200
- 600
- 300
- 166
- 156

**31. An instruction pipeline increases the performance of a processor by overlapping the processing of several different instructions. How many stages it is consist of:**

- 6

- 3
- 5
- 7
- 4

**32. There are three types of hazards that can happen while pipelined execution. Match the hazards with their definitions:**

Structural hazards
different instructions in different stages (or the same stage) conflicting for the same resource

Data hazards
an instruction cannot continue because it needs a value that has not yet been generated by an earlier instruction

Control hazards
fetch cannot continue because it does not know the outcome of an earlier branch – special case of a data hazard

**33. _____ is the amount of time it takes the program to perform in seconds**

- Elapsed time
- Overall time
- Estimate time
- Execution time
- Process time

**34. How many number systems are exist?**

- 4
- 3
- 2
- 1
- 5

**35. Basic memory elements hold only two states: Zero / One**

- True
- False

**36. Which of the following is the right result for this operation: 11001+110001=**

- 10101010
- 10101110
- 01001010
- 01100110
- 10001010

**37. Convert decimal 230 to the binary:**

- 011000110
- 011100110
- 101100110
- 011100110

38. **Convert binary 1100111 to decimal:**

- [x] 103
- [ ] 100
- [ ] 95
- [ ] 130
- [ ] 110

39. **A single, self-contained transistor is called _____.**

- [ ] integrated circuit
- [ ] microchip
- [x] discrete component
- [ ] single transistor
- [ ] small-scale integration

40. **GPU stands for:**

- [ ] graphical processing unit
- [ ] graphical performing units
- [x] graphics processing units
- [ ] graphics processing utility

41. **What measures the ability of a computer to complete a single task?**

- [ ] Clock rate
- [x] Speed metric
- [ ] Clock speed
- [ ] Clock cycle
- [ ] Execution speed

42. **Convert hexadecimal value: DAD to decimal:**

- [ ] 3500
- [x] 3501
- [ ] 4501
- [ ] 4500
- [ ] 3503

43. **Convert decimal value: 877 to hexadecimal:**

- [x] 36D
- [ ] 38A
- [ ] 36B
- [ ] 38C
- [ ] 36A

44. **How we call the thing that is connects major computer components (processor, memory, I/O)?**

- [ ] System connector

- System controllers
- System bus
- System interconnector

**45. Match the three performance parameters with their definitions**

Access time (latency)
This is the time it takes to perform a read or write operation, that is, the time from the instant that an address is presented to the memory to the instant that data have been stored or made available for use

Memory cycle time
This concept is primarily applied to random-access memory and consists of the access time plus any additional time required before a second access can commence.

Transfer rate
This is the measurement at which data can be transferred into or out of a memory unit

**46. Which of the following is the result of the binary multiplication: 100010*100101=**

- 11011101010
- 10111101010
- 10010001010
- 10010101010
- 10011101010

**47. Convert the binary value: 111011 to decimal**

- 59
- 58
- 56
- 60
- 69

**48. DRAM stands for:**

- Direct random access memory
- Dynamic random accessible memory
- Dynamical random access memory
- Dynamic random access memory
- Discrete random access memory

**49. How is called the permanent physical defect when the memory cell or cells affected cannot reliably store data but become stuck at 0 or 1 or switch erratically between 0 and 1?**

- Soft error
- Hard error
- Hard failure
- Soft failure
- Epic failure

**50. How is called a random, nondestructive event that alters the contents of one or more memory cells without damaging the memory?**

- Soft error
- Hard error
- Hard failure
- Soft failure
- Epic failure

**51. Choose the feature(s) of first generation computer architecture**

- Magnetic core memory
- Semiconductor memory
- Machine code
- Vacuum tubes
- Assembly language

**52. Choose the feature(s) of third generation computer architecture**

- Object-Oriented programming
- Floating point arithmetic
- Graphics
- Timesharing
- Use of cache memory

**53. Choose the feature(s) of second generation computer architecture**

- High level languages
- Transistors
- 2 Kb memory, 10 KIPS
- 2 Mb memory, 5 MIPS
- Different types of supported instructions

**54. Choose the feature(s) of fourth generation computer architecture**

- Object-Oriented programming
- Wide spread use of data communications
- Smallest in size
- Use of cache memory
- Use of drum memory or magnetic core memory

**55. How many generations of computer architecture are there?**

- 4
- 3
- 2
- 1
- 5

**56. Choose the years of the first generation computer architecture**

- 1958-1964
- 1964-1974
- 1974-present
- 1945-1964
- 1945-1958

**57. Choose the years of the second generation computer architecture**

- 1945-1958
- 1964-1974
- 1974-present
- 1945-1964
- 1958-1964

**58. In 1976 Apple II computer model was released**

- True
- False

**59. IBM System/360 Model 91 was introduced in 1966**

- True
- False

**60. Choose two types of models for a computing machine**

- Harvard architecture
- Von Neumann architecture
- Oxford architecture
- Stanford architecture

**61. How many number systems are there?**

- 1
- 2
- 3
- 4

**62. How a binary digit is called?**

- byte
- digit
- kilobyte
- bit

**63. Four bits make octal digit**

- True
- False

**64. Three bits make hexadecimal digit**

- True
- False

**65. Octal and hexadecimal numbers are hard on use and conversion**

- True
- False

**66. Which digits are used in octal number system?**

- 0-7
- 0 and 1
- 0-9
- All digits

**67. What does CPI stand for?**

- Cycles Per Instruction
- Clocks Per Instruction
- Cycles Per Interface
- Clocks Per Interface

**68. What is time elapsed to program execution?**

- CPU Time
- User time + OS Time
- I/O waiting & Other programs
- CPU Time + I/O waiting & Other programs

**69. The execution time of a program clearly depends on the number of instructions**

- True
- False

**70. The more clock rate of processor, the faster is processor**

- True
- False

**71. CPU Time = I * CPI / R. Which parameter requires special profiling software?**

- Cycles Per instruction
- Clock Rate
- Numbers of instructions
- Execution time

**72. Select the correct interpretation(s) of Amdahl's Law**

- is used to compare computers' performance
- is used calculate the execution time of a program
- is used to find the maximum expected improvement
- it means that it is the algorithm that decides the speedup not the number of processors

73. **Into how many parts a program (or algorithm) which can be parallelized can be split up?**
    - 3
    - 4
    - 5
    - 2

74. **The time interval is called a clock rate**
    - True
    - False

75. **What does LRU stand for?**
    - Least Right Used
    - Last Recently User
    - Last Recently Used
    - Least Recently Used

76. **Static RAM has a reduced power consumption, and a large storage capacity**
    - True
    - False

77. **How a memory unit accessed by contents is called?**
    - Associative Memory
    - Content Addressable Memory
    - Auxiliary Memory
    - Cache Memory
    - Virtual Memory

78. **Choose the access method(s)**
    - Parallel Access
    - Indirect Access
    - Random Access
    - Direct Access
    - Sequential Access

79. **ROM is the place in a computer where the operating system, application programs, and data in current use are kept.**
    - True
    - False

80. **In which cache memory mapping technique any block from main memory can be placed anywhere in the cache?**
    - Associative Mapping
    - Set Associative Mapping

- Direct Mapping

**81. In LRU replacement algorithm, the block that is in the cache longest is replaced**

- True
- False

**82. In which cache memory mapping technique any memory block is mapped to exactly one block in the cache?**

- Direct Mapping
- Set Associative Mapping
- Associative Mapping

**83. In which cache memory mapping technique any memory block mapped to subset of cache locations?**

- Set Associative Mapping
- Direct Mapping
- Associative Mapping

**84. Which type of memory accessed via the input/output channels?**

- Main Memory
- Cache Memory
- Virtual Memory
- Auxiliary Memory
- Secondary Memory

**85. Which type of memory stores frequently used data?**

- Main Memory
- Virtual Memory
- Auxiliary Memory
- Secondary Memory
- Cache Memory

**86. Choose the right formula for AMAT**

- AMAT = Hit time + Miss rate + Miss penalty
- AMAT = Hit time * Miss rate + Miss penalty
- AMAT = Hit time * Miss rate * Miss penalty
- AMAT = Hit time + Miss rate * Miss penalty

**87. Choose the definition for compulsory misses**

- Occurs if the cache cannot contain all the blocks needed during execution of a program
- Occurs if the block placement strategy is not fully associative
- The very first access to a block cannot be in the cache

**88. Choose the definition for capacity misses**

- Occurs if the cache cannot contain all the blocks needed during execution of a program

- The very first access to a block cannot be in the cache
- Occurs if the block placement strategy is not fully associative

**89. Choose the definition for conflict misses**

- Occurs if the block placement strategy is not fully associative
- Occurs if the cache cannot contain all the blocks needed during execution of a program
- The very first access to a block cannot be in the cache

**90. Select cache optimizations to reduce miss penalty**

- Multilevel Caches
- Giving Reads Priority over Writes
- Way Prediction
- Higher associativity

**91. Select cache optimizations to increase the Cache Bandwidth**

- Nonblocking Caches
- Multibanked Caches
- Pipelined Cache Access
- Multilevel Caches
- Small and Simple First-Level Caches

**92. In virtual memory, memory can be used efficiently because a section of program always loaded**

- True
- False

**93. The advantage of virtual memory is that it takes less time to switch between applications because of additional memory**

- True
- False

**94. Choose basic cache optimizations**

- Compiler-Controlled Prefetching
- Nonblocking Caches
- Small and Simple First-Level Caches
- Multilevel Caches
- Avoiding Address Translation during Cache Indexing

**95. Choose advanced cache optimizations**

- Giving Reads Priority over Writes
- Larger Cache Size
- Hardware Prefetching of Instructions and Data
- Merging Write Buffer

- Critical Word First and Early Restart

**96. Select cache optimizations to reduce hit time (both basic and advanced)**

- Avoiding Address Translation during Cache Indexing
- Small and Simple First-Level Caches
- Way Prediction
  - Compiler Optimizations
  - Compiler-Controlled Prefetching

**97. Physical address used by program, and which OS must translate into virtual address**

  - True
- False

**98. Process of instruction execution is divided into two or more steps, called**

  - pipelining
- pipe stages
- pipe segments
  - instruction execution
  - pipeline hazard

**99. Pipelining can only be implemented on hardware**

  - True
- False

**100. Choose hazard for the following definition: different instructions in different stages (or the same stage) conflicting for the same resource**

- Structural
  - Data
  - Control

**101. Choose hazard for the following definition: an instruction cannot continue because it needs a value that has not yet been generated by an earlier instruction**

- Data
  - Structural
  - Control

**102. Choose hazard for the following definition: fetch cannot continue because it does not know the outcome of an earlier branch – special case of a data hazard**

- Control
  - Structural
  - Data

**103. A technique used in advanced microprocessors where the microprocessor begins executing a first instruction before the second has been completed is called pipelining**

- True
- False

**104. Stage in which the instruction is fetched from memory and placed in the instruction register called**

- Memory read/write
- Instruction Decode
- Execution
- Write Back
- Instruction Fetch

**105. Which stage is responsible for storing and loading values to and from memory?**

- Instruction Fetch
- Memory read/write
- Instruction Decode
- Execution
- Write Back

**106. How the stage in which the results of the operation are written to the destination register is called?**

- Instruction Fetch
- Write Back
- Instruction Decode
- Execution
- Memory read/write

**107. In execution stage identification of the operation is performed**

- True
- False

**108. Choose data dependences**

- Read-After-Read
- Read-After-Write
- Write-After-Write
- Write-After-Read

**109. Halting the flow of instructions until the required result is ready to be used is called**

- waiting
- delaying
- halting
- stalling

**110. A common measure of performance for a processor is the rate at which instructions are executed, called**

- CPI
- Clock Rate
- MFLOPS

- MIPS

**111. Floating point performance is expressed as**

- CPI
- FLOPS
- MIPS

- MFLOPS

**112. Choose the key characteristics of computer memory systems**

- Location
- Unit of Transfer
- Access Method
  - Stalling
  - Hazards

**113. Choose the key characteristics of computer memory systems**

- Capacity
- Performance
- Organization
  - Instruction Fetch
  - Instruction Decode

**114. Choose the key characteristics of computer memory systems**

- Physical Type
- Physical Characteristics
- Access Method
- Unit of Transfer
- Performance

**115. Word is the “natural” unit of organization of memory**

- True
  - False

**116. The “natural” unit of organization of memory is called block**

- True

- False

**117. After implementing embedded systems, you can easily use them for another purposes**

- True
- False

**118. Digital circuits are inflexible and slower, because they are technology dependent**

- True
- False

**119. When using microprocessor based systems, it is enough to update the software**

- True
- False

**120. For random-access memory, the time it takes to perform a read or write operation is called**

- Clock Rate
- CPI
- Access Time
- Latency

**121. The rate at which data can be transferred into or out of a memory unit is called**

- Transfer time
- Transfer Rate
- MIPS
- FLOPS
- MFLOPS

**122. The particular block is currently being stored is called tag**

- True
- False

**123. How many elements of cache design are there?**

- 2
- 5
- 4
- 6
- 7

**124. Choose the element(s) of cache design**

- Tag
- Latency
- AMAT
- Mapping Function
- Replacement Algorithm
- Number of Caches

**125. Choose the element(s) of cache design**

- Tag
- Latency
- AMAT
- Cache Size
- Line Size
- Number of Caches

**126. There are three types of cache addresses**

- True
- False

**127. There are two types of mapping functions**

- True
- False

**128. We can find needed block in associatively mapped cache by its block address**

- True
- False

**129. How many access methods are there?**

- 3
- 2
- 4
- 5
- 6

**130. Choose the type(s) of auxiliary memory**

- Flash Memory
- Optical Disk
- Hard Drive
- SSD
- RAM

**131. How many performance factors are there**

- 5
- 4
- 3
- 2
- 6

**132. Choose the performance factor(s)**

- Cache Size

- Line Size
- Instruction Count
- Number of Processor Cycles
- Mapping function
- Latency

**133. Choose the performance factor(s)**

- Cache Size
- Line Size
- Instruction Count
- Number of Processor Cycles
- Number of memory references

**134. Choose the system attribute(s) by which the performance factors are influenced**

- Cache size
- Unit of Transfer
- Compiler Technology
- Processor Implementation
- Cache and memory hierarchy

**135. How many physical characteristics of disk systems are there?**

- 4
- 5
- 2
- 3
- 6

**136. Choose the physical characteristic(s) of disk systems**

- Disk system implementstion
- Disk Size
- Head Mechanism
- Platters
- Sides

**137. Choose the physical characteristic(s) of disk systems**

- Disk system implementstion
- Disk Size
- Head Mechanism
- Head Motion
- Disk Portability

**138. What does RAID stand for?**

- Random Array of Independent Disks
- Redundant Array of Independent Disks
- Redundant Array of Interoperable Disks
- Random Access to Independent Disks

**139. The RAID scheme consists of 7 levels**

- True
- False

**140. Choose the components of SSD**

- Controller
- Addressing
- Data buffer/cache
- Data size
- Memory hierarchy

**141. SSD is over 10 times faster than the spinning disks in HDD**

- True
- False

**142. SSDs are susceptible to mechanical wear**

- True
- False

**143. SSDs are more susceptible to physical shock and vibration**

- True
- False

**144. SSD stands for**

- Solid State Drive
- Solid State Driver
- Speed State Drive
- Speed State Driver

**145. Choose the component of SSD for the following definition: provides SSD device level interfacing and firmware execution**

- Controller
- Addressing
- Data buffer/cache
- Error correction
- Flash memory components

**146. Choose the component of SSD for the following definition: Logic for error detection and correction**

- Error Correction
- Addressing
- Data buffer/cache
- Controller
- Flash memory components

**147. Choose the component of SSD for the following definition: Individual NAND flash chips**

- Flash Memory Components
- Addressing
- Data buffer/cache
- Controller
- Error Correction

**148. Choose the component of SSD for the following definition: Logic that performs the selection function across the flash memory components**

- Addressing
- Flash Memory Components
- Data buffer/cache
- Controller
- Error Correction

**149. Choose the component of SSD for the following definition: High speed RAM memory components used for speed matching and to increased data throughput**

- Data buffer/cache
- Flash Memory Components
- Addressing
- Controller
- Error Correction

**150. The basic element of a semiconductor memory is the memory cell**

- True
- False

**151. How external nonvolatile memory is called?**

- Secondary memory
- Main memory
- Cache memory
- Virtual memory

**152. What is included into physical type characteristic of computer memory systems?**

- Semiconductor
- Magnetic
- Word

- Access Time
- Number of bytes

**153. What is included into performance characteristic of computer memory systems?**

- Access time
- Cycle Time
- Transfer Rate
- Word
- Number of bytes
- Number of words

**154. What does IDE stand for?**

- Integrated Development Environment

**155. Choose the characteristics of CISC processors**

- large number of instructions
- support many addressing modes
- more elaborate way of accessing data
- less number of instructions
- instructions are of fixed length
- few addressing modes

**156. Choose the characteristics of RISC processors**

- less number of instructions
- instructions are of fixed length
- few addressing modes
- large number of instructions
- support many addressing modes
- more elaborate way of accessing data

**157. Choose the characteristics of Von Neumann architecture**

- one memory for data and program
- CPU provides address to get data or instructions
- data and instructions must have the same width
- separate busses, can be accessed simultaneously
- separated buses allow one instruction to execute while the next instruction is fetched
- data and instructions mustn’t have the same width

**158. Choose the characteristics of Harvard architecture**

- separate program and data memories
- separated buses allow one instruction to execute while the next instruction is fetched

- data and instructions mustn’t have the same width
- one memory for data and program
- CPU provides address to get data or instruction
- data and instructions must have the same width

**159. Which of the following architectures differs by memory accessing?**

- Von Neumann
- Harvard
- Complex Instruction Set Computers
- Reduced Instruction Set Computers

**160. Choose the correct answer for the following characteristics: 1. Depend mainly on its peripherals 2. Used for a few dedicated functions 3. Usually used as a part of a larger system**

- Microcontroller
- General purpose microprocessor

**161. Choose the correct syntax of assembly statements**

- name operation operand(s) comments
- operation name operand(s) comments
- operation operand(s) name comments
- comments name operation operand(s)

**162. The assembler translates names into memory addresses**

- True
- False

**163. Name field of assembly statement is not case sensitive**

- True
- False

**164. Choose the legal name(s) in assembly**

- @variable_name
- variable?
- variable&name
- variable name
- 1variable

**165. In two-operand instruction, the first operand is source and the second operand is destination**

- True
- False

**166. An instruction may have one or more operands**

- True

- False

**167. In assembly language you can express data only in binary and decimal**

- True
- False

**168. You should use a radix symbol in order to differentiate between binary, octal or hexadecimal**

- True
- False

**169. Which symbol you should use to leave the variable uninitialized**

- ?
- !
- @
- $

**170. In assembly language, you can skip the name of variable**

- True
- False

**171. Choose the correct syntax of variable declaration in assembly**

- variable_name type initial_value
- type variable_name initial_vaule
- variable_name type initial_value
- type initial_value variable_name

**172. Match the memory models in assembly**

| | |
|---|---|
| Small | code in one segment, data in one segment |
| Medium | code in more than one segment, data in one segment |
| Compact | code in one segment, data in more than one segment |
| Large | both code and data in more than one segments, no array larger than 64kb |
| Huge | both code and data in more than one segments, array may be larger than 64kb |

**173. Choose the definition of code segment in assembly**

- Contains a program's instructions
- A block of memory to store a stack
- All variable definitions

**174. Choose the definition of data segment in assembly**

- All variable definitions

- A block of memory to store a stack
- Contains a program’s instructions

**175. Choose the definition of stack segment in assembly**

- A block of memory to store a stack
- All variable definitions
- Contains a program’s instructions

**176. There is no memory allocated for constants in assembly language**

- True
- False

**177. Which keyword you should use in order to define a constant in assembly language**

- EQU
- DD
- CONST
- EQ
- DW

**178. In assembly statement name and comment are mandatory**

- True
- False

**179. How many deadlock recovery algorithms are there?**

- 4
- 3
- 2
- 5
- 1

**180. There are 3 approaches of deadlock avoidance**

- True
- False

**181. There are 2 policies of deadlock prevention**

- True
- False

**182. Choose the correct approach for the following definition "involves recognizing when deadlock has occurred, and trying to recover"**

- Deadlock detection and recovery
- Deadlock avoidance
- Deadlock prevention

**183. Choose the correct approach for the following definition "involves making dynamic choices that guarantee prevention"**

- Deadlock avoidance
- Deadlock prevention
- Deadlock detection and recovery

**184. Choose the correct approach for the following definition "adopting a static policy that disallows one of the four conditions above"**

- Deadlock prevention
- Deadlock detection and recovery
- Deadlock avoidance

**185. There are 4 approaches of dealing with deadlock**

- True
- False

**186. Choose the correct answer for the following definition "A closed chain of processes exists, such that each process is blocked waiting for a resource held by another process in the set"**

- Circular wait
- Mutual exclusion
- No preemption
- Hold and wait

**187. Choose the correct answer for the following definition: "No process can be forced to release a resource"**

- No preemption
- Mutual exclusion
- Hold and wait
- Circular wait

**188. Choose the correct answer for the following definition "A process may hold some resources while waiting for others"**

- Hold and wait
- Mutual exclusion
- Circular wait
- No pre-emption

**189. Choose the correct answer for the following definition "Only one process may use a resource at one time"**

- Mutual exclusion
- Circular wait
- No preemption
- Hold and wait

**190. How many policy conditions for deadlock to be possible are there?**

- 3
- 4
- 2
- 5
- 1

**191. What is the deadlock?**

- Permanent blocking of a set of processes that either compete for global resources or communicate with each other
- Interleaving of processes in time to give the appearance of simultaneous execution
- When one process is inside a critical section of code, other processes must be prevented from entering that section
- Processes “communicate” via global counters that are initialized to a positive integer and that can be accessed only through two atomic operations

**192. Deadlock occurs when each process in the set is blocked awaiting an event that can be triggered only by another blocked process in the set**

- True
- False

**193. In which of the following approaches there is no shared data?**

- Message passing
- Mutual exclusion
- Monitors
- Semaphores

**194. Choose the correct answer for the following definition "Synchronization between processes is defined by the blocking policy attached to the sending and receiving of messages"**

- Message passing
- Mutual exclusion
- Monitors
- Semaphores

**195. Monitors are similar to classes in java and has methods and fields**

- True
- False

**196. In atomic operations semSignal(x) and semWait(x), what is the 'x'?**

- The number of processes that can execute critical section
- The number of processes
- The number of monitors
- No correct answer

**197. When using semaphores, processes communicate using messages**

- True

- False

**198. We can implement mutex through the OS or using programming languages**

- True
- False

**199. How many approaches of mutex implementation are there?**

- 3
- 4
- 2
- 5
- 1

**200. Choose the correct answer for the following definition "When one process is inside a critical section of code, other processes must be prevented from entering that section"**

- Mutual exclusion
- Semaphores
- Monitors
- Message passing
- Critical section

**201. In concurrency optimal allocation of resources is difficult**

- True
- False

**202. In concurrency, locating programming errors can't be difficult, because the contexts in which errors occur cannot always be reproduced easily**

- True
- False

**203. In concurrency, sharing global resources safely is difficult**

- True
- False

**204. Concurrency offers genuine simultaneous execution**

- True
- False

**205. Parallelism is interleaving of processes in time to give the appearance of simultaneous execution**

- True
- False

**206. Choose the correct answer for the following definition "multiple processes on multiple systems"**

- Distributed processing
- Multiprogramming
- Multiprocessing

**207. Choose the correct answer for the following definition "multiple processes on a system with multiple processors"**

- Multiprocessing
- Multiprogramming
- Distributed processing

**208. Choose the correct answer for the following definition "multiple processes on a system with a single processor"**

- Multiprogramming
- Multiprocessing
- Distributed processing

**209. How many categories of process management are there?**

- 3
- 2
- 4
- 5
- 1

**210. Operations performed by a processor, such as fetching an instruction, decoding the instruction, performing an arithmetic operation, and so on, are governed by:**

- a system clock
- a system processor
- a clock processor
- a processor
- a clock

**211. Typically all operations performed by a processor begin with the:**

- pulse of the clock
- pulse of the processor
- it begins by itself
- both of clock and processor pulse
- none of the above

**212. The time between pulses called?**

- Cycle time
- Clock speed
- Clock rate
- Clock cycle

**213. A processor is driven by a clock with a constant frequency f or, equivalently, a constant cycle time t, where t = 1/f:**

- Instruction execution rate
- Instruction execution cycle
- Instruction execution time
- Instruction execution period
- None of the above

**214. Measures such as MIPS and MFLOPS have proven adequate to evaluating the performance of processors.**

- False
- True

**215. ENIAC stands for:**

- Electronic Numerical Integrator and Computer
- Electronic Nuclear Integrator and Computer
- Encapsulation Numerical Integrator and Commerce
- Encapsulation Numerical Integrator and Computer
- Electronic Numerical Integer and Computer

**216. Contains a word to be stored in memory or sent to the I/O unit, or is used to receive a word from memory or from the I/O unit**

- Memory buffer register (MBR)
- Memory address register (MAR)
- Instruction register (IR)
- Instruction buffer register (IBR)
- Program counter (PC)

**217. Specifies the address in memory of the word to be written from or read into the MBR**

- Memory address register (MAR)
- Memory buffer register (MBR)
- Instruction register (IR)
- Instruction buffer register (IBR)
- Program counter (PC)

**218. Contains the 8-bit opcode instruction being executed**

- Instruction register (IR)
- Memory buffer register (MBR)
- Memory address register (MAR)
- Instruction buffer register (IBR)
- Program counter (PC)

**219. Employed to hold temporarily the right-hand instruction from a word in memory**

- Instruction buffer register (IBR)

- Memory buffer register (MBR)
- Memory address register (MAR)
- Instruction register (IR)
- Program counter (PC)

**220. Contains the address of the next instruction pair to be fetched from memory**

- Program counter (PC)
- Memory buffer register (MBR)
- Memory address register (MAR)
- Instruction register (IR)
- Instruction buffer register (IBR)

**221. The use of the _____ defines the second generation of computers.**

- Transistor
- Vacuum tube
- Small and medium-scale integration
- Large-scale integration
- Very-large-scale integration

**222. The use of the _____ defines the first generation of computers.**

- Vacuum tube
- Transistor
- Small and medium-scale integration
- Large-scale integration
- Very-large-scale integration

**223. The use of the _____ defines the third generation of computers.**

- Small and medium-scale integration
- Transistor
- Vacuum tube
- Large-scale integration
- Very-large-scale integration

**224. RAID stands for**

- Redundant Array Independent Disk
- Random Access Integral Disk
- Redundant Access Integral Disk
- Random Array Independent Disk
- Redundant Access Independent Disk

**225. The basic element of a semiconductor memory is:**

- Memory cell
- Cache memory
- RAM

- DRAM
- None of the above

**226. A state in which data requested for processing by a component or application is found in the cache memory**

- Cache hit
- Cache miss
- Cache set
- Cache overwrites
- Cache access time

**227. For random-access memory, this is the time it takes to perform a read or write operation**

- Access time
- Memory cycle time
- Transfer rate
- Performance
- All of the above

**228. Memory is organized into units of data, called records; access must be made in a specific linear sequence**

- Sequential access
- Word
- Addressable units
- Unit of transfer
- Direct access

**229. The "natural" unit of organization of memory**

- Word
- Sequential access
- Addressable units
- Unit of transfer
- Direct access

**230. Moore's law: "The cost of a chip has remained virtually unchanged during this period of rapid growth in density. This means that the cost of computer logic and memory circuitry has increasing at a dramatic rate"**

- False
- True

**231. Moore's law: "Because logic and memory elements are placed closer together on more densely packed chips, the electrical path length is shortened, decreasing operating speed"**

- False
- True

**232. Moore's law: "The computer becomes smaller, making it more convenient to place in a variety of environments"**

- True
- False

**233. Moore's law: "There is a reduction in power and cooling requirements"**

- True
- False

**234. Moore's law: "The interconnections on the integrated circuit are much more reliable than solder connections. With less circuitry on each chip, there are fewer interchip connections"**

- True
- False

**235. Processor can simultaneously work on multiple instructions. How this technique called?**

- Pipelining
- Branch prediction
- Data flow analysis
- Speculative execution
- None of the above

**236. The L2 cache is slower and typically larger than the L1 cache, and the L3 cache is slower and typically larger than the L2 cache**

- True
- False

**237. The L2 cache is faster and typically larger than the L1 cache, and the L3 cache is slower and typically larger than the L2 cache**

- False
- True