UNIVERSITY OF MORATUWA
Faculty of Engineering
Department of Electronic and Telecommunication Engineering
B.Sc. Engineering
Semester 3 (2018 Batch) Examination

EN2022 DIGITAL ELECTRONICS

Time allowed: *Two (2)* hours August 2021

INSTRUCTIONS TO CANDIDATES:

- This paper contains 4 questions on 6 pages.
- Answer **all** questions.
- All questions carry **equal** marks.
- This examination accounts for **70**% of the module assessment. The total maximum mark attainable is **100**. The marks assigned for each question & sections thereof are indicated in square brackets.
- The symbols and abbreviations used in this paper have their usual meanings.
- This is an **open-book** and **open-internet** examination.
- Derivations are not required if they are not explicitly requested in the question.
- Assume reasonable values for any data not given in or with the examination paper. Clearly state such assumptions.
- If you have any doubt as to the interpretation of the wording of a question, make your own decision, and clearly state it.

ADDITIONAL MATERIAL:

- No additional material is provided.

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Question 1.

(a) Consider the simplification of Boolean functions using K-maps. A simplified expression corresponding to a 5-variable Boolean function $f(a, b, c, d, e)$ is given by

$$f(a, b, c, d, e) = \bar{a}\bar{b}e + \bar{b}\bar{c}e + bcd + \bar{c}d\bar{e}. \quad (1)$$

The don't care minterms of $f(a, b, c, d, e)$ are $2, 14, 15, 18, 25$ and 28.

i. Draw the corresponding 4-variable K-maps for the two cases: $a = 0$ and $a = 1$. [4 marks]

ii. The simplified expression given in eq. (1) contains four prime implicants. Determine the *essential* prime implicant/implicants out of these four prime implicants. [4 marks]

iii. Determine the minterm/minterms that make each prime implicant mentioned in the answer of **Q1(a)ii** is an essential prime implicant. [5 marks]

iv. Briefly explain whether the simplified expression given in eq. (1) is the only solution for the simplification of $f(a, b, c, d, e)$. [3 marks]

(b) Consider the Boolean function f defined as

$$f(a, b, c, d) = \sum(1, 2, 5, 8, 10, 11, 14, 15).$$

The Boolean function f is required to be implemented using *only two* 4×1 multiplexers with *active-high* enable inputs, *one* 1×2 decoder, *one* two-input OR gate and *one* NOT gate.

i. Construct the truth table by selecting the binary variable d as the input to the multiplexers. [4 marks]

ii. Draw the realization of the digital circuit corresponding to f. Clearly indicate all the inputs and the outputs of the multiplexers and the decoder. [5 marks]

Question 2.

(a) Consider the simplification of the Boolean function f using the Quine-McCluskey method;

$$f(a, b, c, d) = \sum(1, 2, 5, 7, 11) + d(0, 8, 10),$$

where $d(\cdot)$ denotes don't care minterms.

i. Group the relevant minterms based on the number of 1's in their binary representations. [2 marks]

ii. Obtain all possible prime implicants. [5 marks]

iii. Obtain a simplified expression for the Boolean function f using a prime implicant chart and a reduced prime implicant chart (if necessary) in the sum-of-products form (with a minimal number of literals). [5 marks]

(b) An n-bit binary number $B_{n-1}B_{n-2}\ldots B_1B_0$ can be converted to the corresponding n-bit Gray code $G_{n-1}G_{n-2}\ldots G_1G_0$ using the following algorithm:

- Start at B_0
- For each $i = 0, 1, \ldots, n-1$:
  - If $B_{i+1} = 1$, then $G_i = 1 - B_i$
  - Else $G_i = B_i$
- Assume $B_n = 0$

i. Using the above algorithm or otherwise, state the truth table for a 4-bit binary to Gray code converter. Here, the input is a 4-bit binary number and the output is the corresponding 4-bit Gray code. [5 marks]

ii. Draw the implementation of the above truth table using a 16×3 ROM. [6 marks]

iii. In the above 16×3 ROM, what are the words stored in the memory addresses 1 and 4? [2 marks]

Question 3.

(a) Draw the logic circuit of a NAND SR latch with an enable input and state its characteristic table (function table). [3 marks]

(b) Consider the state diagram of a Moore machine shown in Figure Q3.

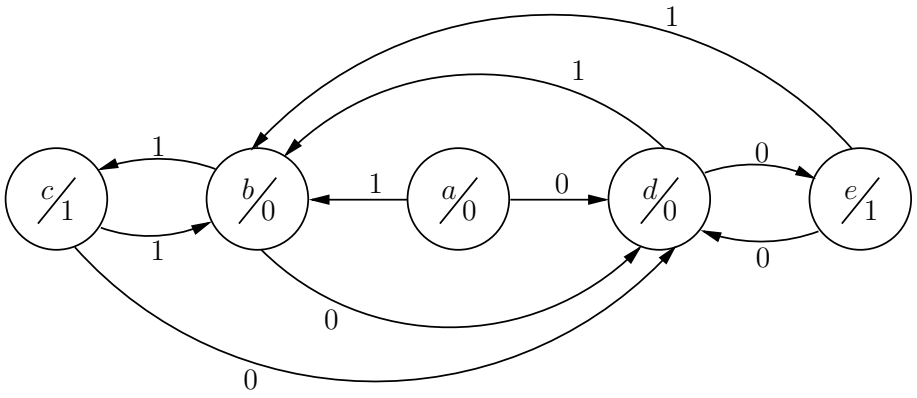

Figure Q3: State diagram.

i. Briefly describe the functionality of the state machine, considering the state transitions. [3 marks]

ii. A sequential logic circuit is required to be designed to realize the state machine using the least number of JK filp-flops. Derive the state table for this purpose. Use the binary number order for state assignment. [14 marks]

iii. Derive the necessary flip-flop input equations and the output equation. [5 marks]

Question 4.

(a) Figure Q4 shows a circuit of a logic gate. Assume that all the transistors and diodes are made of Silicon (Si), and let $\beta = 30$ for all the transistors. Here, A and B are the inputs and Y is the output of the logic gate.

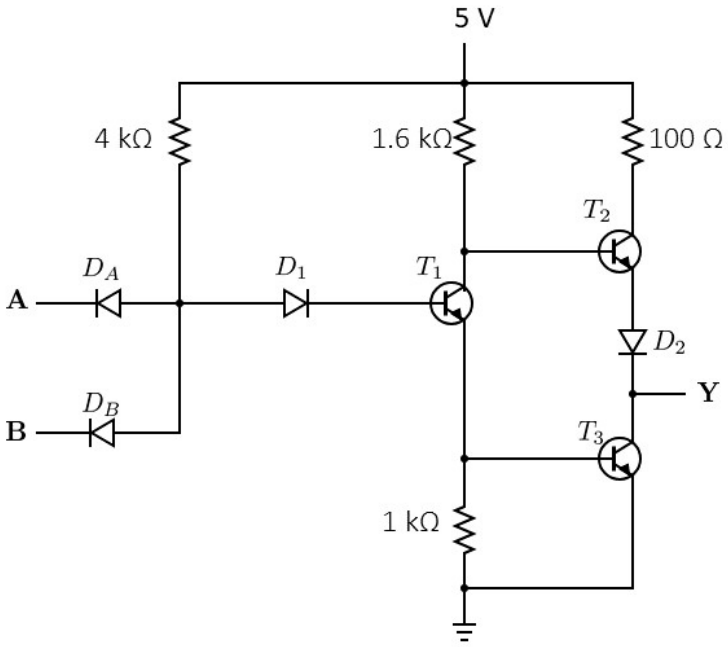

Figure Q4: Circuit of a Logic gate.

i. Identify the logic gate shown in Figure Q4. [4 marks]

ii. What is the importance of diode D2? [5 marks]

iii. Calculate the noise margin of the logic gate. [5 marks]

iv. Draw the circuit of a tristate inverter by appropriately modifying the above circuit. [3 marks]

(b) Draw the circuit of the complex logic gate using CMOS logic for the function $f = \overline{(A + B) \cdot (C + D)}$. [8 marks]

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