UNIVERSITY OF MORATUWA
Faculty of Engineering
Department of Electronic and Telecommunication Engineering
B.Sc. Engineering
Semester 3 (2019 Batch) Examination

EN2022 DIGITAL ELECTRONICS

Time allowed: *Two (2)* hours January 2022

INSTRUCTIONS TO CANDIDATES:

- This paper contains 4 questions on 6 pages.
- Answer **all** questions.
- All questions carry **equal** marks.
- This examination accounts for **70**% of the module assessment. The total maximum mark attainable is **100**. The marks assigned for each question & sections thereof are indicated in square brackets.
- The symbols and abbreviations used in this paper have their usual meanings.
- This is an **open-book** and **open-internet** examination.
- Derivations are not required if they are not explicitly requested in the question.
- Assume reasonable values for any data not given in or with the examination paper. Clearly state such assumptions.
- If you have any doubt as to the interpretation of the wording of a question, make your own decision, and clearly state it.

ADDITIONAL MATERIAL:

- No additional material is provided.

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Question 1.

(a) Consider the simplification of the Boolean function f using the Quine-McCluskey method;

$$f(a,b,c,d) = \sum(1,2,5,8,11) + d(0,9,10),$$

where $d(\cdot)$ denotes don't care minterms.

i. Group the relevant minterms based on the number of 1's in their binary representations. [3 marks]

ii. Obtain all possible prime implicants. [6 marks]

iii. Obtain a simplified expression for the Boolean function f using a prime implicant chart and a reduced prime implicant chart (if necessary) in the sum-of-products form (with a minimal number of literals). [6 marks]

(b) Consider the Boolean function f defined as

$$f(a,b,c,d) = \prod(0,2,4,6,7,12) \cdot D(9,11),$$

where $D(\cdot)$ denotes don't care maxterms. The Boolean function f is required to be implemented using *only two* 4×1 multiplexers with *active-high* enable inputs, *one* 1×2 decoder, and *one* two-input OR gate.

i. Construct the truth table by selecting the binary variable d as the input to the multiplexers. [4 marks]

ii. Draw the realization of the digital circuit corresponding to f. Clearly indicate all the inputs and the outputs of the multiplexers and the decoder. [6 marks]

Question 2.

(a) Draw the logic circuit of a D latch with an enable input, and state its characteristic table (function table). [3 marks]

(b) Briefly explain the difference between a Mealy machine and a Moore machine. [3 marks]

(c) Consider a digital circuit that can detect the 0110 bit stream without overlaps.

i. Define states. [2 marks]

ii. Draw the state diagram to design the digital circuit as a Moore machine. [5 marks]

iii. Using the least number of JK filp-flops, derive the state table. Use the binary number order for state assignment. [5 marks]

iv. Derive the flip-flop input equations and the output equation. [7 marks]

Question 3.

(a) Consider a combinational logic circuit that accepts a 3-bit number x and output an n-bit number y equal to the following equation,

$$`y = x^3 + x.$$

This combinational logic circuit is implemented using a ROM.

i. Find the range of the output y. [1 mark]

ii. Find the number of bits n required for the output to represent the range of y. [1 mark]

iii. What is the size of the ROM require to implement this combinational logic circuit? [1 mark]

iv. State the truth table that shows the word content of each address for the implementation considering all bits are stored in the ROM (i.e., without reduction). [8 marks]

v. Draw the implementation of the above truth table (part iv) using the standard symbols and notations (without reduction). [5 marks]

vi. State the truth table for the minimum size ROM that can be used to implement this combinational logic circuit? (with possible reduction). [5 marks]

vii. Draw the implementation of the above truth table (part vi) corresponding to the minimum size ROM using the standard symbols and notations. [4 marks]

Question 4.

(a) The specifications for the Schottky transistor-transistor logic (TTL) 74S00 quadruple 2-input NAND gates are presented in Table Q4.

Table Q4

Parameter	Description	Value
V_{CC}	Supply voltage	5 V
I_{CCH}	High-level supply current	10 mA
I_{CCL}	Low-level supply current	20 mA
V_{OH}	High-level output voltage (min)	2.7 V
V_{OL}	Low-level output voltage (max)	0.5 V
V_{IH}	High-level input voltage (min)	2 V
V_{IL}	Low-level input voltage (max)	0.8 V
I_{OH}	High-level output current (max)	1 mA
I_{OL}	Low-level output current (max)	20 mA
I_{IH}	High-level input current (max)	0.05 mA
I_{IL}	Low-level input current (max)	2 mA
t_{PLH}	Low-to-high delay	3 ns
t_{PHL}	High-to-low delay	3 ns

Calculate

i. Fan-out, [2 marks]

ii. Propagation delay, [2 marks]

iii. Power dissipation, [2 marks]

iv. Noise margin, [2 marks]

of the Schottky TTL NAND gate.

(b) The fact that a diode can act as a switch is used in diode logic (DL) gates.

i. Express two limitations related to DL. [2 marks]

ii. Figure Q4a shows cascaded DL gates where the outputs of two AND gates are connected to the inputs of an OR gate. Analyze the operation of the circuit under the following two cases.

α) Case 1: all the inputs are at logic 0 (0 V) [1 mark]

β) Case 2: both inputs of either AND gate are at logic 1 (+5 V) [4 marks]

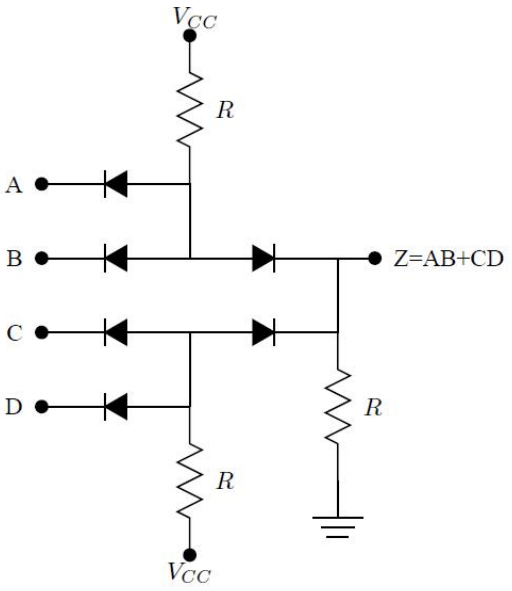

Figure Q4a: Cascaded DL gates.

(c) Resistor-transistor logic (RTL) uses transistors to combine multiple input signals, which also amplify and invert the resulting combined signal.

i. Explain what is meant by current hogging in RTL gates. [3 marks]

ii. Explain how this is avoided using a series resistor at the base of each transistor. [3 marks]

iii. Analyze and identify the RTL gate shown in Figure Q4b. [4 marks]

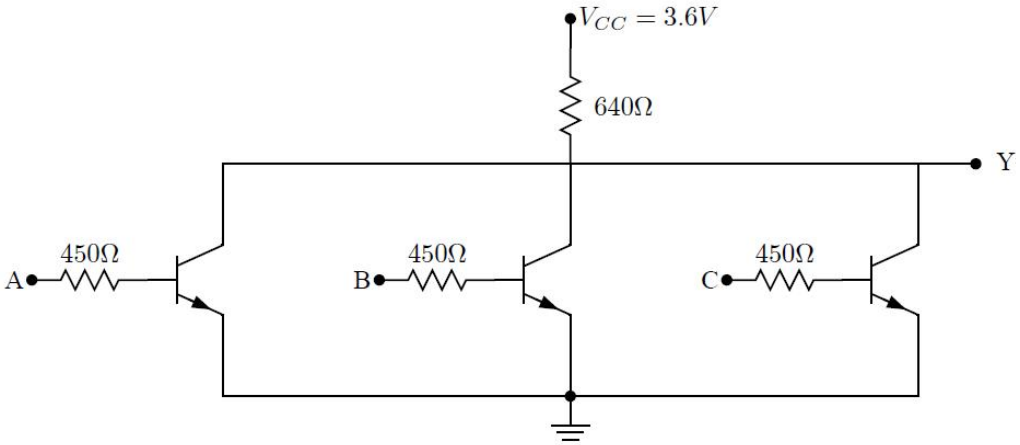

Figure Q4b: RTL logic gate.

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