Laptop CPU Complexity and its Influence on Vulnerability to Ionizing Radiation in Near-Earth Orbit

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I. Abstract

It's been known for some time that ionizing radiation frequent in space has detrimental effects on the performance and lifetime of electronics in the space environment [1]. Current understanding of electronic theory suggests that the trend of rising computer complexity of the commercial market will lead to greater vulnerability to Single Event Effects (SEE's) in spaceflight [1],[2]. Thus, if a consumer market trends persist, Commercial Off the Shelf (COTS) Computers will no longer be viable for use on future missions like the ISS or Artemis. However, this meta-analysis of testing previously done on the HP Zbook 15 G2 [3], Surface Pro 5 [4] and the Lenovo ThinkPad T61P [5] has shown that there is moderate positive linear correlation between CPU clock speed and stability under SEE's. However, a Pearson Coefficient of 0.629 was determined to not be statistically significant. Additionally, there was a moderate negative correlation between lithography processes and stability under SEE's. Although, again, a Pearson Coefficient of -0.578 was determined to not be statistically significant. These results demonstrate that newer more complex commercial CPU's may in fact be more stable under SEE's compared to older models. However, this trend is more likely a result of changes in the topology of transistors in the sub-22nm node, and other material, architectural, and manufacturing differences.

II. Introduction

The space environment is extremely hostile, and is known to have several effects on a spacecraft and its electronics. It's been known for some time that ionizing radiation frequent in space has detrimental effects on the performance and lifetime of electronics in the space environment [1]**.** It is therefore imperative that electronics be tested under the influence of ionizing radiation before being sent into space. Current practice entails the use of electronics which were previously used on spaceflight missions and our known to work in space [6]**.** This practice is generally fairly effective with satellites, as the number of past satellite missions means that there is a fairly large variety of electronics to choose from.

However, this has not been very effective for human spaceflight missions. While a satellite or probe can have all systems connected electronically, human spaceflight missions require buttons, screens and other interfaces for astronauts to operate. Laptops have often filled this gap by acting as a portable terminal for several systems [7]. They have also filled other general-purpose roles, allowing astronauts to send emails, write reports, and video chat.

IBM Thinkpads have been used on every Space Shuttle flight since 1995, on the International Space Station since 1998, and are one of the only laptops certified for use on the ISS [8]**.** Only in 2016, NASA began phasing in the use of the HP Zbook a process which is still continuing [7],[9].

A primary reason for the lack of new technologies in this field is the high cost of attaining particle accelerator time in order to test these electronics [2]. This is especially true as variations in the consumer manufacturing process a great enough for previous radiation testing to be considered invalid, and every lot of commercial parts for a given mission with radiation requirements must be tested again [1]. Further, the highly specific purpose of rad-hardened electronics makes them expensive to develop, as they are not profitably produced in volume.

As a result, Commercial Off The Shelf (COTS) computers are widely preferable to custom designed laptops. And the range of electronics tested under these conditions are limited to specific electronics desired for use such as the aforementioned HP Zbook and ThinkPad [3],[5], [9].

Further, this method of testing selection has resulted in very little testing on how specific computer characteristics influence stability under cosmic radiation. One notable characteristic is computer complexity, which has steadily grown in the commercial space as noted by A. Bauman [10]. This trend has been observed for some time, most notably by Moore's law which states that the number of transistors that can be fit on a processor die will double every two years. While Moore's Law has certainly slowed, transistor density and other measures of computer complexity continue to rise [10].

Current understanding of electronic and radiation theory suggests that the shrinkage and higher density of MOSFET transistors required for the consumer market's demand for increased computer complexity will raise the probability of Single Event Effects (SEE's) and therefore make the component or system more vulnerable to SEE's caused by cosmic radiation (see Section III A). It is therefore a possibility that, should this trend hold true, COTS laptops developed and produced in the near future will not be suitable for use on near Earth Missions like the International Space Station, or for use on cis-lunar flights, such as the Artemis program, whose first mission is planned for 2021, and aims to return to the moon by 2024 [11].

It is therefore imperative to investigate the relationship between computer complexity and stability so to as predict the viability of near-future laptops in the space environment.

A study which proved or disproved this relationship might be able to predict which laptops could be fit for testing beforehand, saving huge costs in allocating particle accelerator time. Further such a study would be able to determine whether COTS laptops produced in the near future might be fit for use, and determine whether investing in custom designed laptops for use in space is a necessary measure.

This study investigates the possibility of a correlation between computer complexity and stability under SEE's through a meta-analysis of the aforementioned HP Zbook, Lenovo T61P, and Surface Pro 5. In an attempt to predict the vulnerability of future laptops under spaceflight testing and cis-lunar spaceflight.

The remainder of the paper is organized as follows. Section II presents related work. In Section III, the adopted approach for selecting, isolating, and combining studies. Section IV presents the results. Section V concludes the paper and presents directions for future study.

III. Related Work

A. Sources of Radiation

J.W. Howard and D. M. Hardage [1] presents that the near-Earth radiation environment is composed of both a trapped radiation environment and transient radiation environment. The trapped radiation environment is caused by the Earth's magnetic field confining charged particles to specific regions of space called Van Allen Belts. The transient radiation environment is induced by solar events (solar winds and flares) and galactic cosmic radiation (GCR) [1].

Trapped radiation belts can extend from about 500 km to roughly 76,000 km which include two electron bands and one proton band [1].

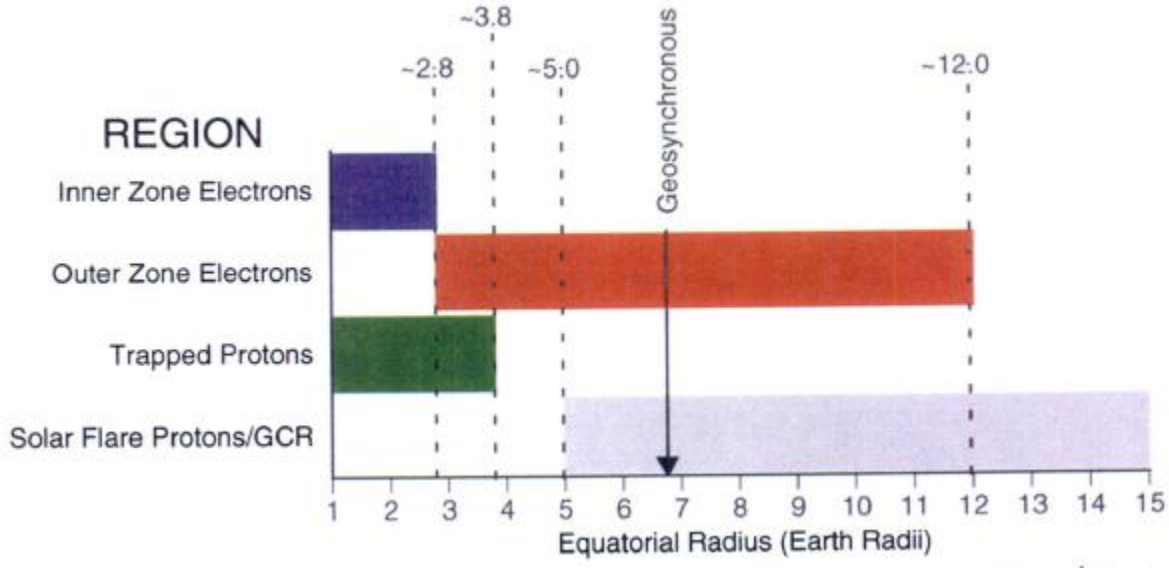

Fig. 1. From J.W. Howard and D.M. Hardage [1], "Pictogram showing regions of space where radiation types are significant. Regions are plotted as a function of the equatorial radius, in Earth radii (~6370 km), because the belts vary with magnetic field that changes with increase inclination off the equator" "Note that boundaries are approximate and bands are not sharp transitions".

Note that the ISS, has an altitude between 415 and 423 km [12], so both the outer zone electron bands and trapped protons are relevant to this study. Additionally, the South Atlantic Anomaly, where a deformation of Earth's magnetic field, allows for harsher influence from the radiation belts at low altitudes, such as the orbit of the ISS [1].

The gray bar representing "Solar Flare Protons/GCR" gives the approximate boundaries for the transient radiation environment. The lower end depicts "where geomagnetic effects are beginning to remove some of the environment" [1]. Generally speaking very little radiation from this source makes it to lower altitudes, but detailed computer models are required to accurately predict how much radiation is removed.

B. Electronic Effects

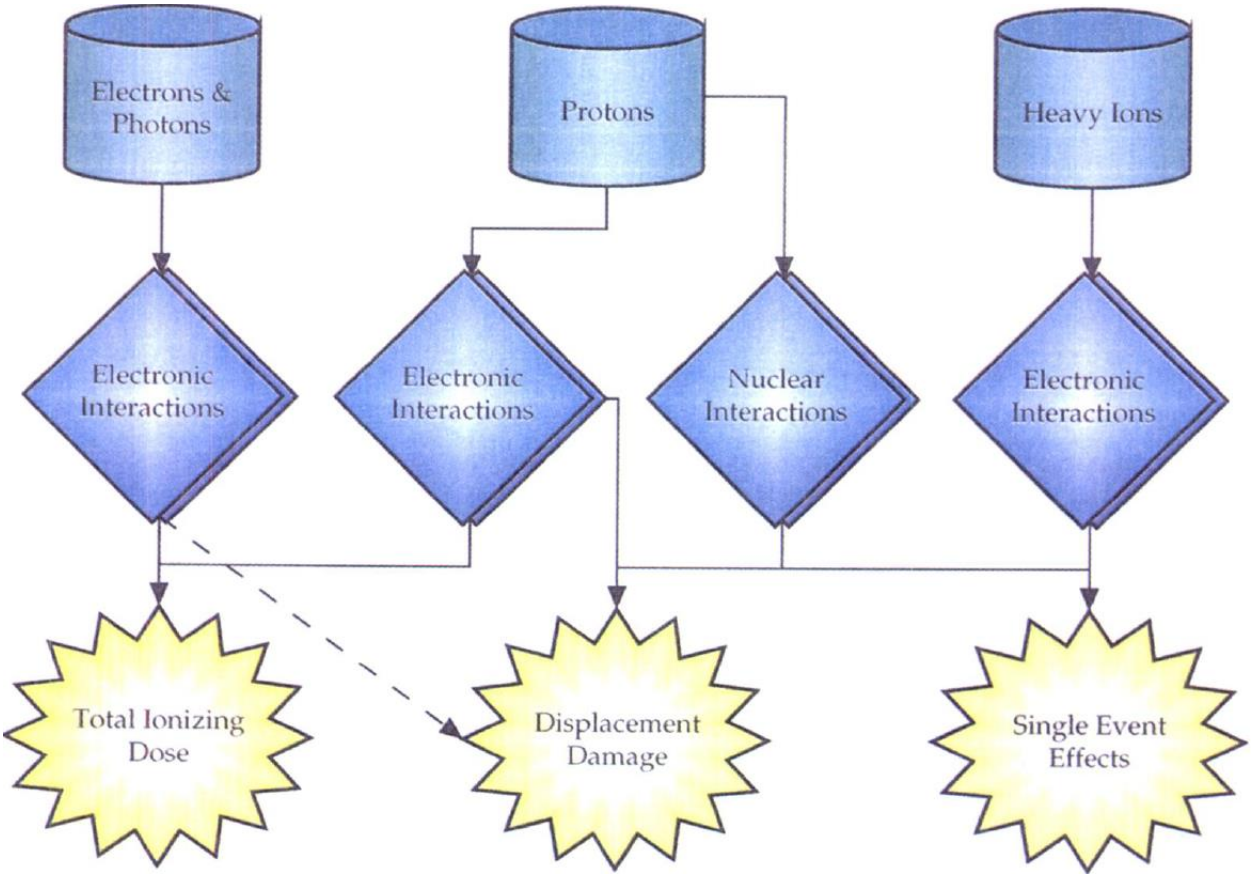

Fig. 2. From J.W. Howard and D. M. Hardage [1], "Diagram of radiation effects on electronic systems"

Radiation effects can vary depending on the ion that interacts with the electronic. Comprehensive testing will test for as many of these ions as feasible. Variability between manufacturing samples is to be expected, but large variability can exist for components produced, even more so for electronics produced for the general market such as the laptop CPU's this paper is concerned with. Additionally, while Total Ionizing Dose (TID) is an essential factor in determining how long a component may last in space, this paper will focus specifically on SEE's.

To understand how these effects occur, one must understand how the MOS-FET or field effect transistor works. The MOS-FET is at the building block of ever computer and allows the system to send signals in binary (a language of 1's and 0's) by conducting and blocking the flow of electricity. In order to do this, the transistor relies on the existence of a depletion zone, a barrier which blocks of the flow of electricity if the voltage is too low (see Fig.3.).

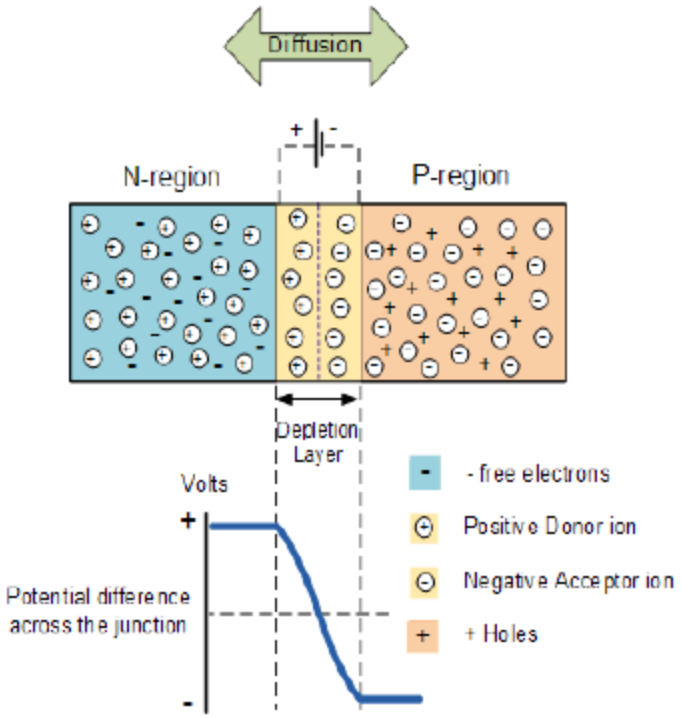

Fig. 3. From S. Koontz [2], a depiction of the MOS-FET depletion layer

If a heavy ion or Proton were to pass through this depletion layer, the ion could lower the barrier and switch the transistor to a conducting state to a non-conducting state or vice versa. On a low level this is okay, but can cause a chain reaction of effects on system wide scale. For example, the CMOS, inverter structure, relies on a series of MOS-FETs working in tandem (see Fig. 4. and Fig. 5.). Note that the "SEE change of output is possible only if the latch characteristics response time is small enough to respond to the transient currant [sic] / voltage pulse" [2].

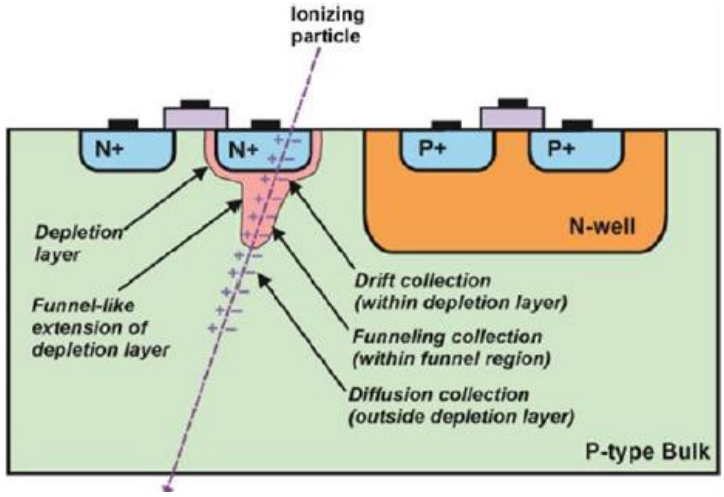

Fig. 4. From S. Koontz [2], depiction of a cosmic ray strike on a sensitive location on a CMOS inverter structure causing the output to change

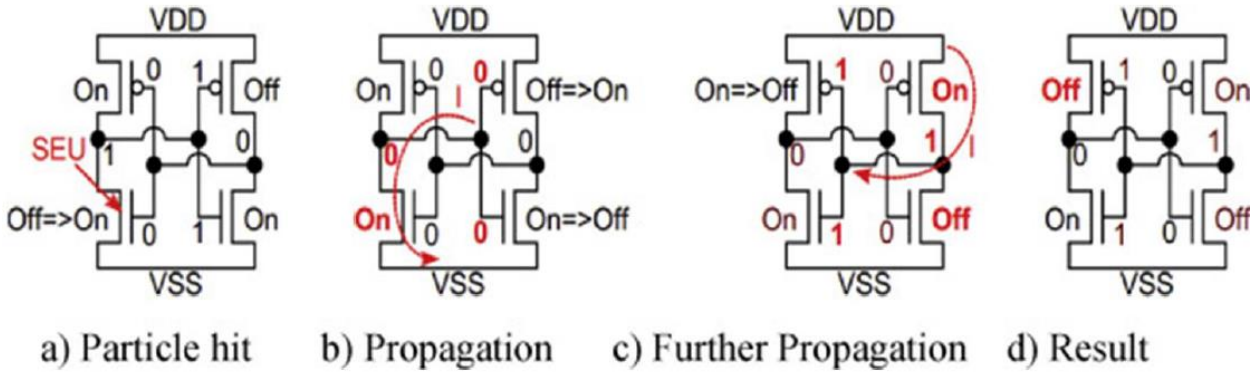

Fig. 5. From S. Koontz [2], depiction of a CMOS latch switching states due to a particle hit.

There are several destructive effects on electronic systems which can occur as a result of ionizing radiation, The Single Event Transient (SET), Single Event Upset (SEU), Single Event Functional Interrupt (SEFI), Single Event Latch-up (SEL), Single Event Burnout (SEB), Single Event Gate Rupture (SEGR), Single event Hard Effects (SHE), and Micro Latch-ups, which are generalized as Single Event Effects (SEE) [2].

This paper will be primarily focused on the SHE and micro latch-up, which are caused by stuck-bits and cause a permanent change of state of a memory/register [2]. While these two both cause higher level issues in the device, the micro latch-up is generally correctable by a power cycle if done quickly enough, but the SHE will cause the entire memory block to fail permanently, possibly causing the entire device to fail.

C. Empirical Testing

As mentioned above there have been few laptops tested under spaceflight conditions, almost all of which have been tested by the Johnson Space Center [3], [4], [5]. This lack of data is a result of the high cost of testing, something that would be unfeasibly expensive for the scope of this paper to expand upon. However, the tested laptops, Lenovo T61P, Surface Pro 5, and HP Zbook cover a wide range of processors produced over the years, and could show a trend of where the market is heading.

While each study was conducted at different laboratories, each made similar assumptions about the space environment which would be typical of the environment experienced on the International Space Station [3],[4],[5].

D. Simulated Testing

Warren et al. [13] proposes the feasibility of simulation-based testing on lower level electrical components, and demonstrates the viability of the Monte-Carlo Energy Deposition Simulation in testing SRAM components. A method which could be applied to Laptop CPU's to determine LET. However this method requires the access to "mixed-mode TCAD modeling" [13]. These TCAD models are complex and are not widely available to the public.

Similarly, Ramos et al. [14] proves the feasibility of the SEE evaluation of COTS many-core/multicore processors through simulation-based testing in memory applications by means of

fault injection. With access to many varied processors, this approach could be effective, however it remains outside the scope of this project as it would require access to a large number of systems with several different processors.

IV. Approach

While a true, industry wide survey would certainly be more conclusive, this study opts to do a meta-analysis based on currently existing data primarily to avoid the exorbitant costs of testing. On its own, testing of single devices require large amounts of money, so a comprehensive survey would have greatly inflated costs. Further, this approach avoids the safety issues that arise with using particle accelerators, and avoids the training time required to test these electronics.

A. Selection of Studies

The Johnson Space Center (JSC-NASA) and its associates in the industry have already done testing on several laptops including the IBM Thinkpad, Lenovo Thinkpad T61P (T61P), Lenovo Thinkpad T61 (T61), Surface Pro 5, and HP Zbook. These laptops were chosen primarily because of the availability of their data, and because of the wide range of computer complexity and production years, these computers represent. The T61P has been used on the ISS for years with strong results [8]; The HP Zbook was recently cleared and flown in space [9]; and the Surface Pro 5 is planned to be flown on the upcoming Orion missions [15].

Each of these electronics were used in studies which analyzed each section of the computer would react to proton or other ion based cosmic radiation passing through. As a result, this study used the data which pertained to the Central Processing Unit (CPU) and the storage device, usually a hard disk drive (HDD) or solid-state drive (SSD).

These studies primarily reported data in the form of Mean Time Between Failure (MTBF). In each of the studies, MTBF was calculated according to the following formula [16]:

$$MTBF = \frac{fluence}{SEE's}$$

The public resource, Intel Ark [18], further completes these technical specifications by providing manufacturing specifications on each CPU, all of which are produced by the Intel Corporation (Intel).

B. Adapting studies and controlling variables.

Each of the studies focuses on errors and device failures which cannot be fixed by rebooting the system, a normal part of operation on the ISS. These, reboots generally clear any bitflip or corrupted memory errors [3], [4], [5]. That being said, it is possible that the SEU's on these devices are similar, as such the design of the CPU may be vulnerable component.

Current testing methodology requires the simulation of radiation to be done by ionizing beams at large labs [2], which allows for certain portions of the device to be examined under radiation while others are untouched [3], [4], [5]. However, this method also means multiple components must be tested at a single time, and getting performance measurements of specific components

can be difficult depending on the architecture of the device. Because each laptop has widely different architectures, each sectional testing could have vastly different components in addition to the primary components of interest (see Fig. 6 and Fig. 7.).

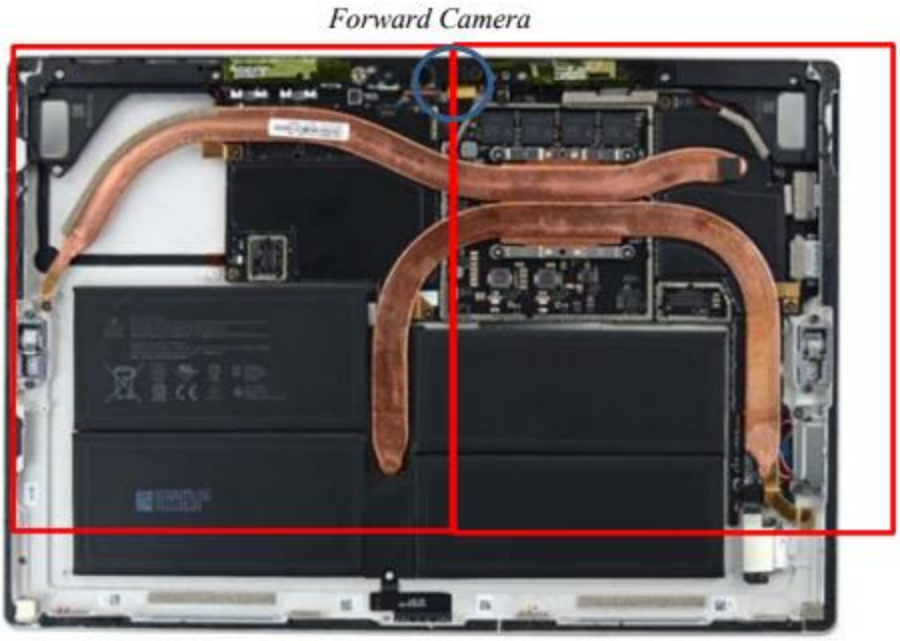

Fig. 6. From K.V. Nguyen [4], depiction of beam position placement on the Surface Pro 5.

Fig. 7. From K.V. Nguyen [3], Beam placement diagram for the HP Zbook.

This issue is most obvious in the testing of the Surface Pro 5, which required the entire right side and entire left side be tested in the same trial (see Fig. 6.). As a result of this, the number of SEE's and calculated MTBF may be skewed by the reliability of the other components.

Each of the tested laptops either have publicly available technical specifications, or those specifications can be found directly in the report. It should be noted when referencing the Surface Pro 5 testing report, that the paper lists both the Intel i5-7300U and m3-7Y30 as the CPU inside the model tested [4]. Correspondence with the testing team has confirmed that the i5-7300U is the CPU inside the model tested [17].

C. Measurement of CPU complexity

Because the properties of the MOS-FET are directly linked to the vulnerability of the electronic component to SEE's, transistor count is the most obvious measurement to use as a predictor of SEE vulnerability. And as Moore's law predicts, the number of transistors housed in a single die has grown steadily over the last few decades, and will likely continue into the future. However, Intel stopped publishing specification on transistor count soon after releasing their 4th Generation Core I processor [18]. As a result of this, the Surface Pro 5, cannot be evaluated by any model using transistor count as a basis.

However, lithography process can be used as a proxy for Transistor Count and a measure for transistor density as lithography process indicates the precision of the manufacturing processes can loosely be interpreted as how close one transistor is to another.

The second measurement of CPU complexity used is clock speed. A CPU's clock speed indicates how many cycles a CPU makes in a given time frame. And with most CPU Instruction Per Clock (IPC) counts increasing [10], CPU clock speed can be used as a measurement for how quickly MOS-FET states will change and how quickly the CPU makes calculations, a factor linked to vulnerability to SEE's.

D. Combining studies

Each report lists a variety of testing conditions, and a variety of errors. Some of the laptops were tested under both Proton and Neutron Beam testing. While it would be more accurate to analyze the effects under both Neutron and Proton Beam testing, especially acknowledging the influence of the transient and trapped radiation environments which the ISS regularly passes through [1], this study is focused on the SEE's caused in the CPU under Proton Beam testing. This is primarily due to the lack of Neutron testing data for the T61P.

A Pearson Correlation Coefficient could then by calculated to determine the relationship between MTBF and the selected transistor geometry to analyze the possible correlation. Should a correlation be determined, a projection of future laptop CPU performance under these conditions could also be made.

V. Evaluation of Studies

Table I

Lenovo ThinkPad CPU Complexity and SEE's Stability

Laptop	*CPU*	*Transistor Count (Millions)*	*Lithography (nm)*	*Clock Speed (GHz)*	*MTBF (Days)*
A53_1	T7500	291	65	2.2	25.5
A53_2	T7500	291	65	2.2	19.6
A52_1	T7700	291	65	2.4	28.5
A52_1	T7700	291	65	2.4	27
A52_1	T7800	291	65	2.6	35.6
AV3_1	T7700	291	65	2.4	14.2
AV3_2	T7300	291	65	2	38
AV3_2	T7800	291	65	2.6	26.9

Table II

HP Zbook Complexity and SEE's Stability

Laptop	*CPU*	*Transistor Count (Millions)*	*Lithography (nm)*	*Clock Speed (GHz)*	*MTBF (Days)*
Zbook	I7-4810mq	1400	22	2.8	421
Zbook	I7-4810mq	1400	22	2.8	421
Zbook	I7-4810mq	1400	22	2.8	142

Table III

Surface Pro 5 Complexity and SEE's Stability

Laptop	*CPU*	*Transistor Count (Millions)*	*Lithography (nm)*	*Clock Speed (GHz)*	*MTBF (Days)*
SP5-1	i5-7300U	Unreported	14	2.6	74
SP5-2	i5-7300U	Unreported	14	2.6	15

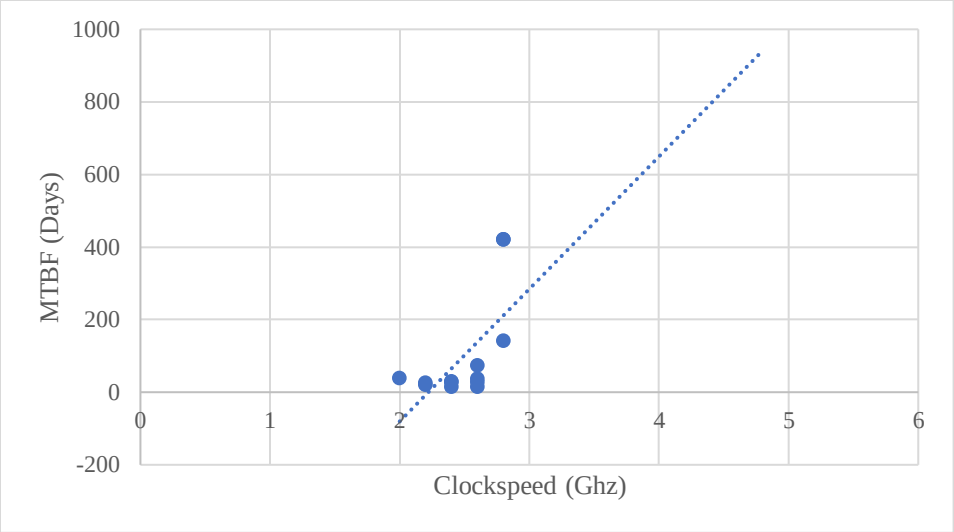

Fig. 8. MTBF of tested CPU's by CPU clock speed

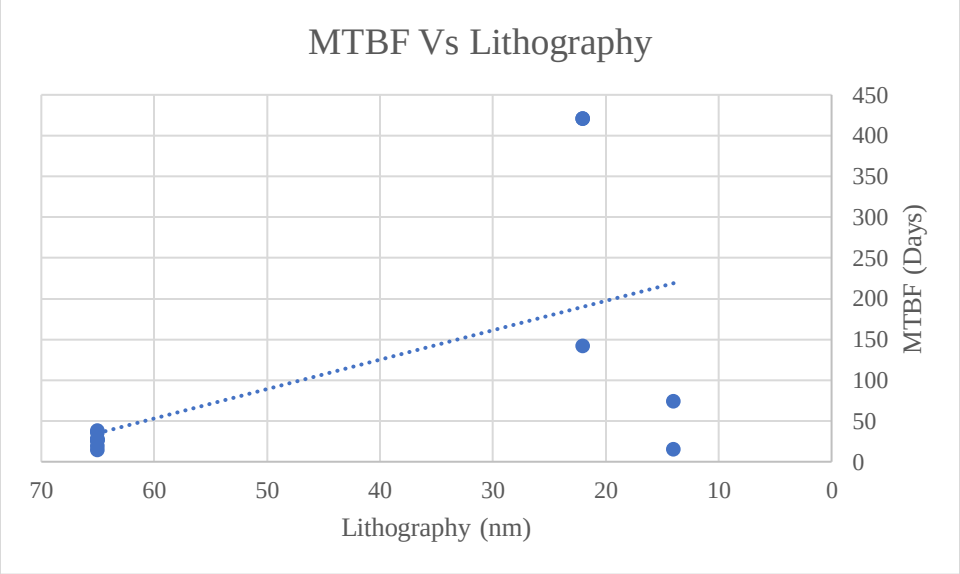

Fig. 9. MTBF of CPU's tested by CPU Lithography process.

Because of the lack of data points, the general trend and relationship between each point is difficult to interpret. That being said, the trend line does indicate that increased clock speed has actually increased resilience to SEE's (see Fig. 8). A Pearson Correlation Coefficient of 0.629 shows that there is a strong positive linear correlation between CPU Clock speed and stability under SEE's, however the Pearson Correlation Coefficient was not determined to be statistically significant. It's likely that the high Pearson Correlation Coefficient only exists because of the outliers created by the two Zbook tests. This trend may disappear or strengthen in the presence of more data, as the linear model only accounted for about 39.5% of the variation in the vulnerability to SEE's.

Likewise, the trend indicates that smaller and higher precision lithography process increased resilience to SEE's (see Fig. 9). A Pearson Correlation Coefficient of -0.578 shows there is a

moderate negative linear correlation between CPU lithography process and stability under SEE'S, but the correlation was not deemed to be statistically significant. Again, this may have been influenced by the two Zbook outlier, as the linear model only accounted for about 33.4% of the variation in the vulnerability to SEE's.

It seems the stronger trend is that the newer CPU's, which have smaller lithography processes and higher clock speeds, are more resilient to SEE's. This may be a result of changes in CPU architecture, manufacturing process or materials each are more likely to be responsible for the increased stability rather than the Clock speed or lithography process alone.

VI. Conclusion

While it's possible that the cycle time and density of the MOS-FET in the CPU correlates with increasing resilience of CPU's to SEE's, more data will need to be provided to order to make a scientifically rigorous conclusion. The inclusion of more data may strengthen or weaken the existing trend shown in Fig. 8 and Fig. 9.

As mentioned in section V, it's possible that several confounding variables, notably changes in CPU architecture, manufacturing process, or materials may be responsible for the rise in stability of newer CPU's. These changes could be responsible for the resulting contradiction of the theories put forth by J.W. Howard [1] and S. Koontz [2].

While this studies results have proven inconclusive, the results suggest that while transistor geometry may play a role in CPU vulnerability to SEE's, this vulnerability likely is negligible when compared to other sources of vulnerability.

Further Research

A more comprehensive survey on CPU's under Proton and Neutron beams is needed to understand how the properties of the CPU influences vulnerability to SEE's. Further each of the CPUs considered in this study was produced by Intel, a study of systems based around CPUs produced by Advanced Micro Devices (AMD) may also be beneficial, as the altered architecture may prove to be more resilient to SEE's in Spaceflight. Further experimentation is needed especially in the way of isolated CPU testing.

Further studies may also want to consider the influence of the DRAM and Storage devices in each system as those changes may prove to be more influential to a system's performance and resilience to SEE's.

Acknowledgement

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Appendix A, Glossary of Relevant Terms

Selected definitions from the Glossary of J.W. Howard and D. M. Hardage [1], and from "MOSFET" [19]

Burnout	"A catastrophic failure of a high power transistor caused by transient radiation. In the space environment a single ion can induce a degenerative feedback current in the transistor that will lead to its failure due to excessive current." [1]
Dose	"The Energy absorbed per unit mass from any radiation in any material. This indicates the amount of energy transferred to the material through which the radiation" [1]
Electron	"The fundamental atomic building block particle with a net charge of negative one."[1]
Electron Volt	"The kinetic energy an electron gains by its acceleration though a potential difference of one volt." [1]
Fluence	"The number of particles passing through a given area. The fluence is the time integrated flux. Typical unit is cm^{-2}" [1]
Flux	"The number of particles passing through a given area per unit time. Typical units are $cm^{-2}sec^{-1}$" [1]
Gate Rupture	"A catastrophic failure of a high power transistor caused by transient radiation. In the space environment a single ion can induce sufficient buildup and discharge occurs across the gate of the transistor. A short circuit develops and the transistor fails." [1]
Heavy Ion	"The atomic nucleus of an element great than hydrogen with a number of electrons less than the electrically neutral atom. The difference between the number of electrons present and the number in the neutral state is called the charge state of the heavy ion." [1]

Latchup	"A destructive, high current mode of operation that CMOS structures can transfer into if the parasitic structures exist and the radiation induced transient currents are sufficiently high. If not current limited, due to the current feedback and temperature effects, the currents will continue to increase until the part fails from overcurrent" [1]
LET	"The linear energy transfer is that amount of energy an incident particle will transfer, locally, to a given material per unit distance. Typical units are $MeV \cdot cm^2 \cdot mg^{-1}$" [1]
Lithography	Refers to the process by which Central Processing Units and other IC's are produced. Lithography process nodes are generally named by their size [19]. For this reason one can loosely associate lithography with transistor density. For example, one may say that CPU produced on the 14nm node has a higher transistor density than that of a CPU produced on the 22nm node.
MOS-FET	Metal-Oxide-semiconductor field-effect transistor "is a type of insulated-gate field-effect transistor" with "the ability to change conductivity with the amount of applied voltage" and "can be used for amplifying or switching electronic signals" [19]
Photons	"A radiation type that is electromagnetic energy that quantum mechanically interacts as both a wave packet and particle." [1]
Proton	"The fundamental nuclear building block particle with a net charge of positive one. A proton is also the nucleus of a hydrogen atom." [1]
Rad-hard	"Terminology that indicates the electronic component design was modified to ensure radiation reliability and survivability. This category is sometimes divided into military and space qualifications, where the military qualification also indicates a nuclear weapon survivability specification." [1]
Rad-tolerant	"Terminology that indicates the electronic component design was not modified to ensure radiation reliability and survivability but has a significant level of tolerance to radiation inherently in its design." [1]
SEE	"A single event effect is an effect in an electronic device that is induced by the passage of a single ionizing particle through its structure. The effects can vary from simple bit flips to catastrophic failures." [1]
TID	"The total ionizing dose is the cumulative buildup of dose that produces effects in electronics by ionization of the materials in the device." [1]
Upset	"The most common form of single event effect. In digital microelectronics, information is stored as a zero or one. An upset is the transition from one to the other." [1]

Van Allen Belt	“The region of space where Earth’s magnetic field has “trapped radiation. Due to the dipole nature of the Earth’s magnetic field and intensity variation with altitude, any charged particle that enters this region will continually travel along lines of force effectively “trapping” the particle” [1]

Appendix B, A Note on Copyright

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