Switching Theory & Logic Design Laboratory
CSE Department, IIT Kharagpur
Spring Semester 2023-24

Module 3 : SEQUENTIAL CIRCUITS AND FSM

Assignment 7 :

1. Design a synchronous sequential circuit that will take a serial bit stream as input in synchronism with a clock, and will output a 1 whenever the pattern (possibly overlapping) 01111 is encountered.

2. Design a modulo-9 synchronous binary counter using T flip-flops.

3. Design an asynchronous 4-bit up/down counter using T flip-flops.

(1 day)