Switching Theory & Logic Design Laboratory
CSE Department, IIT Kharagpur
Spring Semester 2023-24

Module 1 : Combinational Logic Circuits

Assignment 5:

Design and test a Full Adder / Subtractor using 4:1 Multiplexer (IC) and minimum number of logic gates, as per the given specifications :

- If S = 1 : Full Adder or If S = 0 : Full Subtractor

(1 day)