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Sem- 3rd

Subject - DCLD (ACEC-16302)

Assignment - 3rd

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Section-A

Q1. Difference between Asynchronous and synchronous Counter.

Ans:- There are many difference between Asynchronous and synchronous Counter.

Asynchronous Counter	synchronous Counter
In asychronous Counter, different flip flops are triggered with different clock not simultaneously.	In synchronous Counter, all flip flops are triggered with same clock simultaneously.
Asynchronous Counter will operate only in fixed count sequence (UP/DOWN).	Synchronous Counter will operate in any desired Count sequence.
In asynchronous Counter, there is high propagation delay.	In synchronous Counter, propagation delay is less.

Q2. Performance Comparison of TTL, CMOS, ECL?

Ans:- TTL :→

→ It stands for transistor-transistor logic
→ This logic family, basic TTL gate has improvence over Standard DTL gate.
→ TTL gate has 3 different types of output Configurations.

(1) Open collector output.
(2) Tri term pole output.
(3) Three state output.
→ Standard TTL Series of logic family starts with 7504, 74586, 74 AL, S161.

ECL :-
→ It standards for Emitter Coupled logic.
→ ECL is based on use of Current Steering switch. realised using differential transistor pair.
→ Co
(i) ~~Prog~~ propagation rate is about 1 to 2 ml.
(2) Noise immunity and power dissipation is worst of all logic families.
(3) High level is 0.8V and low level is 1.8V
→ ECL gate Provides both true as well as Complemented output.

CMOS :-
→ It stands for Complementary metal oxide semi-Conductor.
→ CMOS logic Families has more delay as Compared to transister logic families.

Specification	TTL	ECL	CMOS
Basic gate	NAND	OR, NOR	NAND, NOR
Fanout	10	25	>50
power/gate (m watt)	1-22	4-55	101 MHz
noise immunity	very good	good	Excellent
LPD (ns)	1.5-33	1-4	1-200

Q4. What are the application of Flip flop?

Ans:- There are many applications of flip flop.

(i) Counter.
(ii) Frequence dividers.
(iii) shift Registers.
(iv) storage Registers.
(v) Bounce elimination switch.
(vi) Data transfer.
(vii) Latch
(viii) Registers.
(ix) Memory.

Q4. Define the T Flip flop.

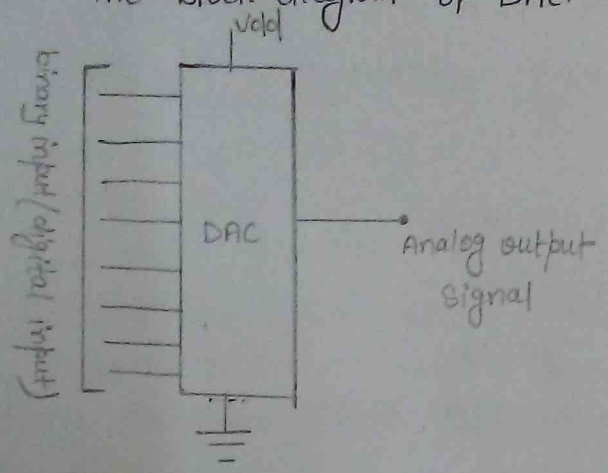
Ans:- A T Flip flop is known as a toggle flip flop because of its toggling operation. It is a modified form of the JK Flip flop. T flip flop is a single input flip flop. Along with this input, we need to give a clock signal to the flip flop.

Q5. Draw the excitation table of SR Flip Flop.

Ans:-

Q_n	Q_{n+1}	S	R
0	0	0	x
0	1	1	0
1	0	0	1
1	1	x	0

Q6. Draw the block diagram of DAC.



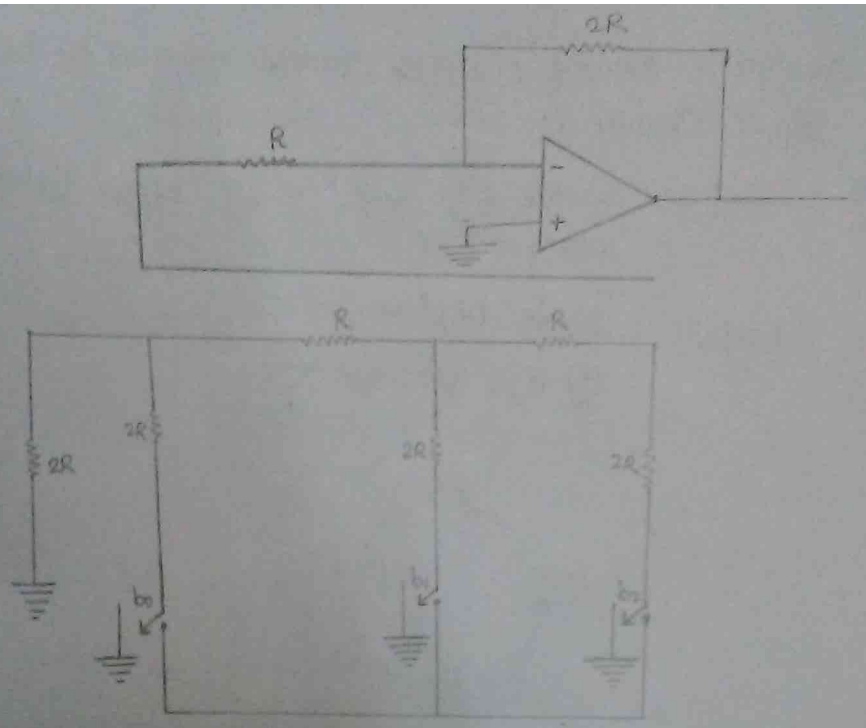
Basic Digital to Analog Converter.

Section-B

Q7. Draw and explain the R-2R ladder type DAC.

Ans:- The R-2R ladder DAC overcomes the disadvantages a binary weighted register DAC. As the name suggests R-2R ladder DAC produces an analog output which is almost equal to the digital (binary) Input by using a R-2R ladder network in the inverting adder circuit the circuit diagram of 3 bit R-2R ladder network in the inverting adder circuit.

Recall that the bits of a binary number can have only one of the two value ie either 0 or 1. Let the 3 bit binary input is b_2, b_1, b_0 Here the bits b_2 and b_0 denote the most significant Bit (MSB) and least significant Bit (LSB) respectively.

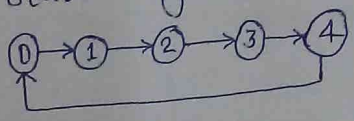


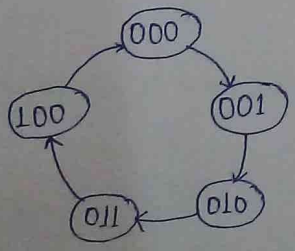
The digital switches shown in the above fig. will be connected to ground. when the corresponding input bits are equal to '0' similarly the digital switches shown in above figure will be connected to the +ve reference voltage -ve. when the crossponding input bits are equal to 1. It is different to get the generated output voltage equation of R-2R ladder DAC. But we can find the analog output voltage of a R-2R ladder DAC for individual binary input combinations only.

Q8. Design a moudle-5 ripple Counter using a 3-bit ripple Counter.

Ans:- Step 1: Decide flip-flop 3-bit ripple Counter
meang : 3FF

Step 2: State diagram





Step 3: Excitation table

Qn	Qn+1	T
0	0	0
0	1	1
1	0	1
1	1	0

Step 4:

A	B	C	A*	B*	C*	T_A	T_B	T_C
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1

a 3- bit

Counter

Step 5: K map for T_A T_B T_C

A \ BC	00	01	11	10
0	0	0	1	0
1	0	0	1	0

$T_A = BC$

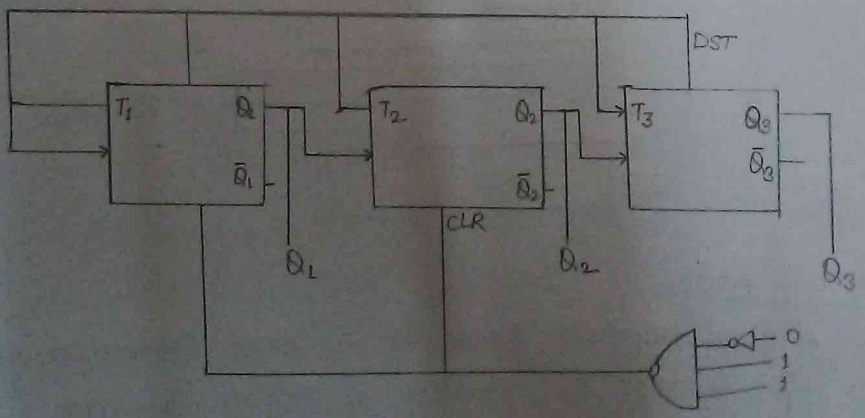
A \ BC	00	01	11	10
0	0	1	1	0
1	0	1	1	0

$T_B = C$

A \ BC	00	01	11	10
0	1	1	1	1
1	1	1	1	1

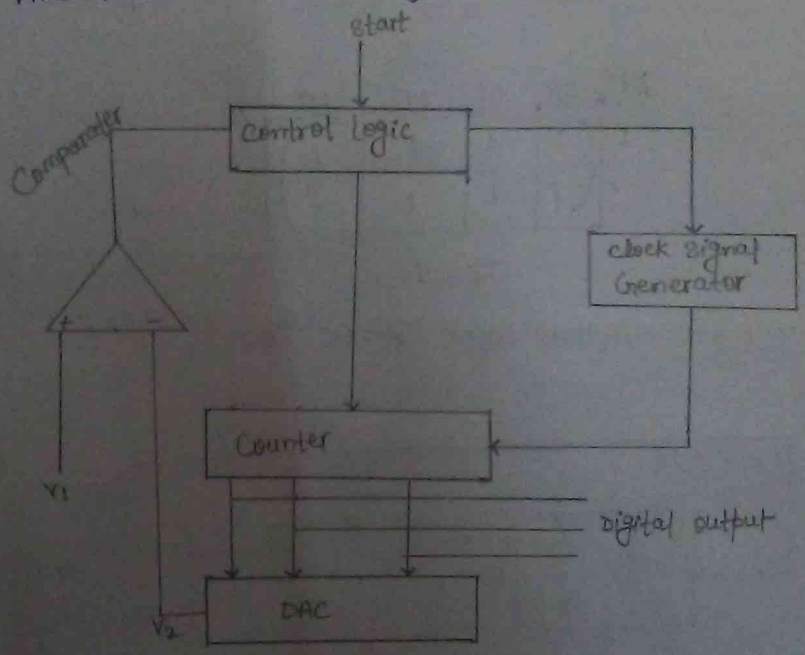
$T_C = 1$

Step 6: Diagram logic $T_A = BC$, $T_B = C$, $T_C = 1$



Q9. Describe the Counter type ADC and Flash ADC in det

Ans:- A Counter type ADC produces a digital output which is approximately equal to the analoy input by using Counter operation internally.
The Counter type ADC mainly consists of 5 blocks. clock signal Generator Counter DAC. Comparator & Control Logic. The block diagram of a Counter type ADC is snow below in fig.



Flash ADC:-
A Flash ADC (also know as a direct Conversion ADC) is a type of Analog of digital Convertor that uses a linear voltage ladder with a Comparator each "rung" of the ladder to Compare the

input voltage to successive reference voltage often these reference ladders are constructed of many resistors, however modern implementations show that capacitive voltage division is also possible.

The output of these comparators is generally fed into a digital encoder. which converts the inputs into a binary value.