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Section-A

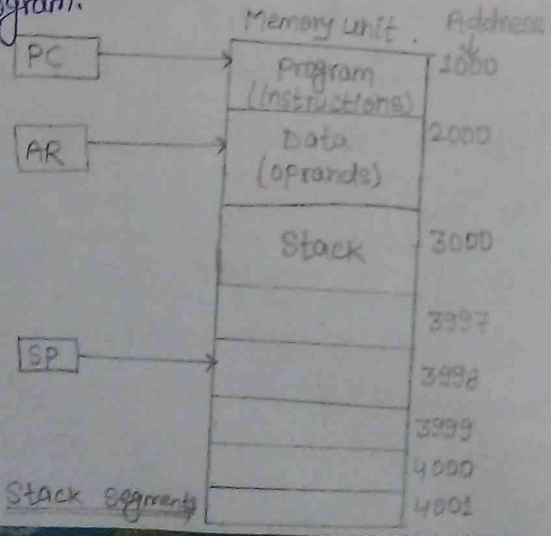
Q1.

(a) what do you mean by Addressing mode?

Ans:- Addressing mode operation field of an instruction specifies the operation to be performed. This operation must be excuted on some data stored in Computer registers or memory words. The addressing mode specifies a rule for interpreting or modifying the address field of the instruction before the operand is actually referenced.

(b) what do you mean by memory stack?

Ans:- A stack can exist as a stand-alone unit as or Can be implemented in a random-access memory attached to a CPU. The implementation of a stack in the CPU is done by assigning a portion of memory to a stack operation. The program Counter PC points at the address of the next instruction in the program.



(c) Define IOP.

Ans:- An input-output processor may be classified as a processor with direct memory Access capability that communication with input/output devices in this configration Computer system can be divided into memory units and member of processor Composed of CPU and one or more IOPs. Each IOP takes care of inputs and outputs takes relieving the CPU. IOP always use data transfer by interrupts by DMA.

(d) Define programmed I/O data transfer technique.

Ans:- programmed inputs and outputs are the result I/O instructions written in the Computers program. Each data item transfer is initited by an instruction in the program. usually the transfer is to and from of CPU register and peripheral transferring data under program control required Constant monitoring of the peripheral by the CPU. once the data transfer is initiated the CPU is required to monitor the interface to see when a transfer can again be made.

(e) Give the major characteristics of RISC and CISC architecture.

Ans:- There are many major characteristics of RISC and CISC architecture.

RISCS	CISC
Emphasis of software.	Emphasis on hardware.
instruction of same set with few formates.	multiply instruction sizes an formates.
more register	less Register
fewer addressing mode	more addressing mode.
Pipeling is easy	Pipling is diffcult

(f) what do you mean by asynchronous data transfer?

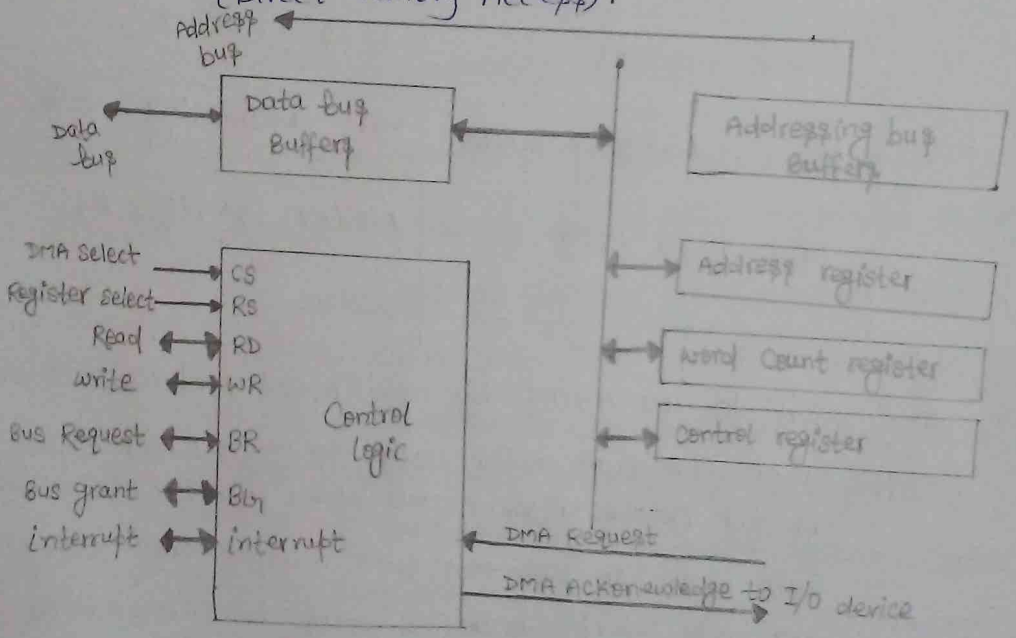
Ans:- when the two units uses its own clock that transfer is the asynchronous data transfer Asynchronous data transfer between two independent units requires that control signals be transmitted between communicating units to indicate the time at which data is being transmitted.

It one way of achieving this is by means of a store be pulse supplied by one of the units to indicate to the other units when the transfer has to accure.

Section-B

Q2. what do you mean by DMA? Explain DMA Controller with Diagram.

Ans:- DMA Controller is a hardware device that allows I/O devices to directly access memory with less participation of the Processor. Direct memory Access Removing the CPU from the path and peripherial device manage Buses directly whould improved the speed transfer, this transfer is Called DMA (Direct memory Access).



Q3. Explain various addressing modes with examples.

Ans:- (i) Immediate Addressing mode.

Ex:- MOV R0, 300, $R_0 \leftarrow 300$

(ii) Implied Addressing mode.

Ex:- CMA (Complement AC)

(iii) Direct addressing mode.

Ex:- LDAM[X], $AC \leftarrow M[X]$

(iv) indirect Addressing mode.

Ex:- load R_1, M[M[200]] (LD) Add 08.

(v) Register Addressing mode.

Ex:- Add R_1, R_2, $R_1 \leftarrow R_1 + R_2$

(vi) Register indirect Addressing mode.

Ex:- Load.

(vii) Auto increament or Auto decrement Add. mode

Ex:- LDA X B

(viii) Relative Addressing mode.

Ex:- Jump +8(PC), EA = PC + 8 = PC = 300 ∴ EA = 308

(ix) Index Addressing mode.

Ex:- EA = Address + Contents field of index Reg.

(x) Base Register Addressing mode.

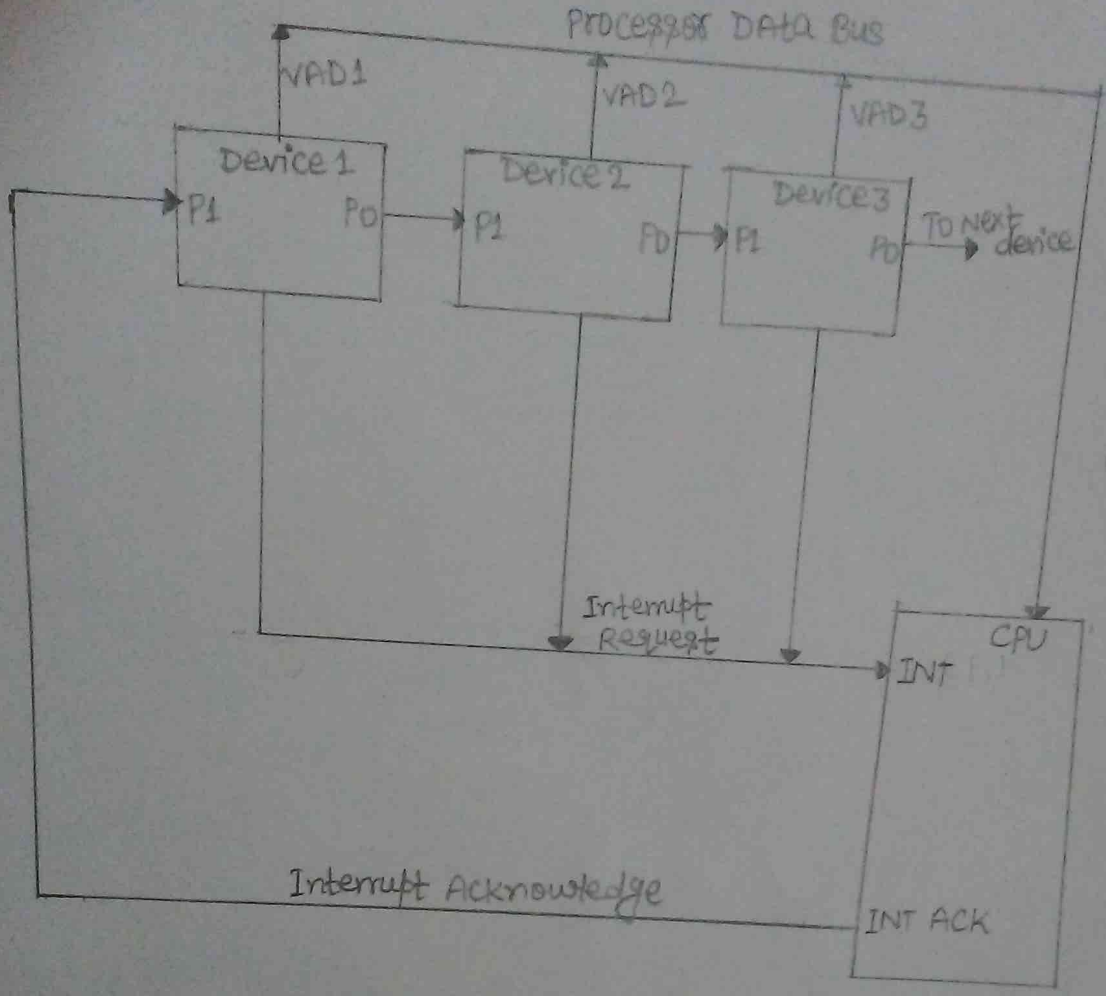
Ex:- EA = Address field + Contents of Base Reg.

Addressing modes:- The term addressing modes refers to the way in which the operand of an instruction is specified. The addressing mode specifies a rule for interpreting or modifying the address field of the instruction before the operand is actually executed.

Q4. Explain daisy changing interrupt example.

Ans:- The device with the highest priority is placed in the first position followed by lower-priority device upto this device with the lowest priority which is placed last in the chain. The CPU responds to an interrupt request by enabling the interrupt the signal passes on the next device. A device with a_0 = 0 in its PI inputs generates a_0 = 0 in its P_0 output to inform the next lower priority device that the acknowledge signal has been placed. A device that is requesting an interrupts and has a device that is input which interrupts the acknowledge signals by placing a_0 in its P_0 output. In the device does not have pending interrupts. It transmits the signal to the next device by placing a_i in its P_0 output.

The device with PI = 1 and PO = 0 is the one with highest priority that is requesting an interrupts and this devices place its VAD on the data bus. The daisy-chaining method involves connecting all the devices that can request an interrupt in a serial manner.



DAISY CHAINING.