Name- Sumit Kumar Giri
Course- B.Tech (CSE)
Uni. Roll No. - 2000213
Sem. - 3rd
Sub- DCLD.

Section-A

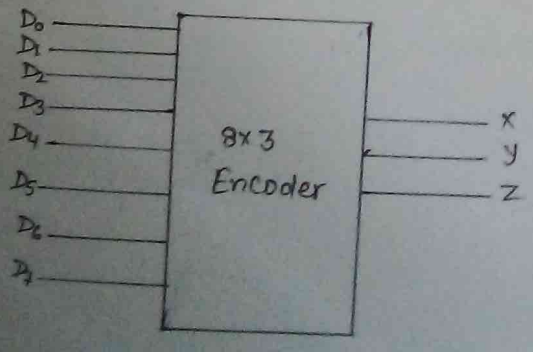
Q1. Difference between mux and Demux.

Ans:- There are difference between mux and demux.

mux.	Demux.
multiplexer processes the digital information from various sources into a single source.	Demultiplexer receives digital information from a single source and converts it into several sources.
It is known as Data selector multiplexer is a digital switch	It is known as Data Distributor Demultiplexer is a digital circuit.
It follows Combinational logic type and It has n data Input.	It also follows Combinational logic type and It has single data input.

Q2. what is Encoder?

Ans:- An Encoder is a Combinational circuit that converts binary information in the from of a 2^N input lines into N output lines, which represent N bit Code for the input.



Q3. What are the application of multiplexer?

Ans:- It is some application of multiplexer.

(i) Communication system.

(ii) Computer Memory.

(iii) Computer system of a stateline Transmission.

(iv) Telephone Network.

Q4. Define the Sequential Circuits.

Ans:- A Sequential Circuits is a Combinational logic circuit that it produces an output based on current input and previous input variable. A Sequential Circuits include memory elements that are capable of storing binary information.

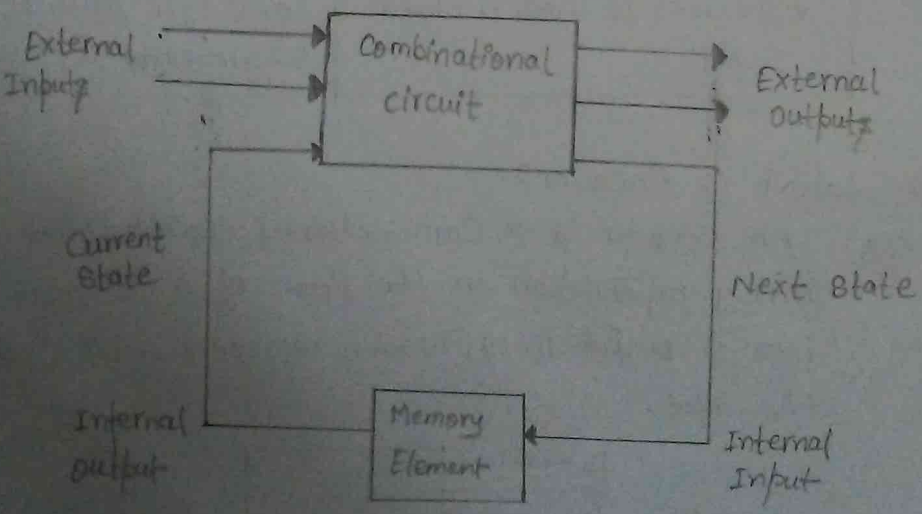


fig:- Sequential circuit

Q5. Draw the excitation table of JK flip flop.

Ans:- The excitation table of JK flip flop.

Q	Q(next)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

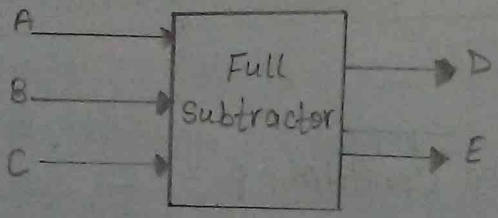
Q6. What is race condition ?

Ans:- Race Condition occur in RS flip-flop when the S and R inputs of an SR flip flop is at logical 1 and then the input is changed to any other condition, the the output becomes unpredictable and this is called the race around condition

Section-B

Q7. Draw and explain the Full Subtractor with logical diagram.

Ans:- A **Full Subtractor**:- A full subtractor is a Combinational Circuit that performs subtractor of two bits, one is minuend and other is subtrahend. This circuit has three inputs and two outputs.

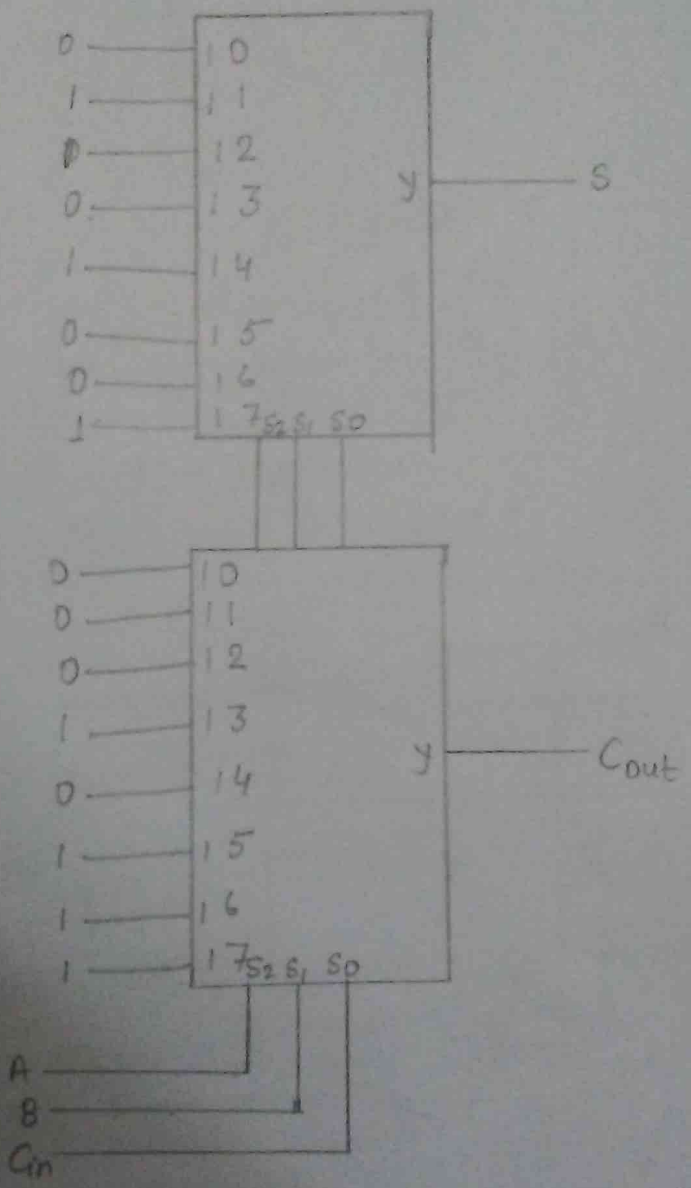


Truth table:-

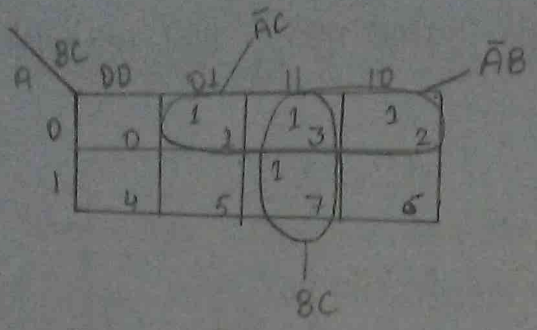
INPUT			OUTPUT	
A	B	C	D	E
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Q. Implement the full adder using 8:1 multiplexer.

Ans:-



LOGIC DIAGRAM of full-ADDER using 8:1 multiplexer



$X = \bar{A}C + BC + \bar{A}B$

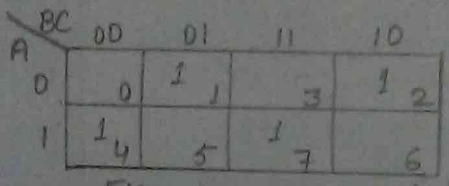
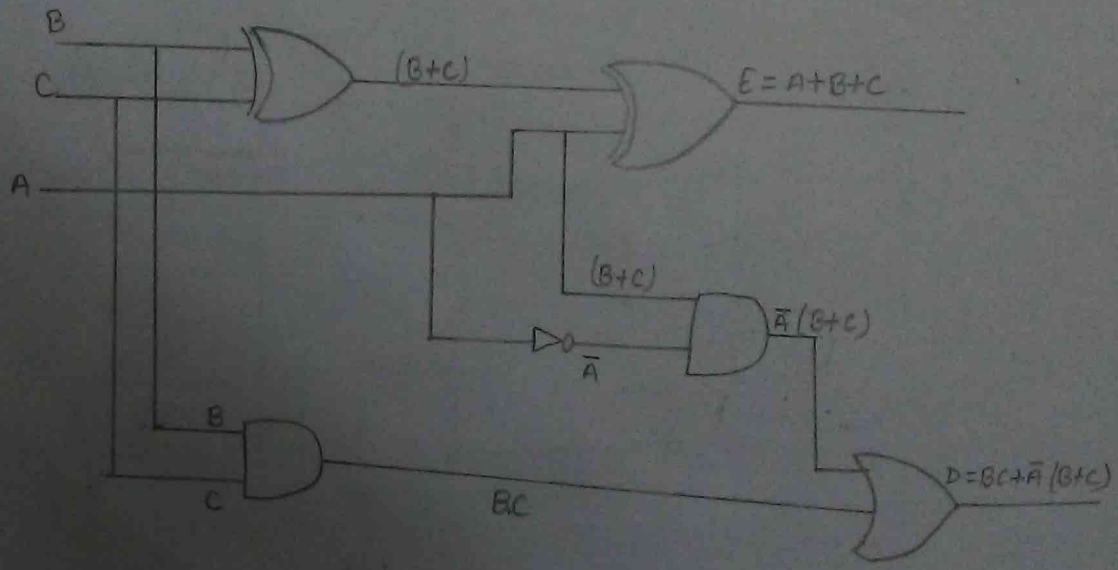


Fig:- Karnaugh map for full adder.

$y = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$



Circuit diagram for Full Subtractors.

TRUTH TABLE :-

A	B	Cout	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Truth Table of 8:1 multiplexer.

Q9. Describe the working of JK flip flop.

Ans:- The JK flip-flop also works likes SR flip flop but only difference is that in JK flip-flop. there is no invalid state in JK flip-flop.

The JK flip-flop and other from $\bar{Q}$ and similarly and from K and other from $\bar{Q}$ and in two difference NAND Gate.

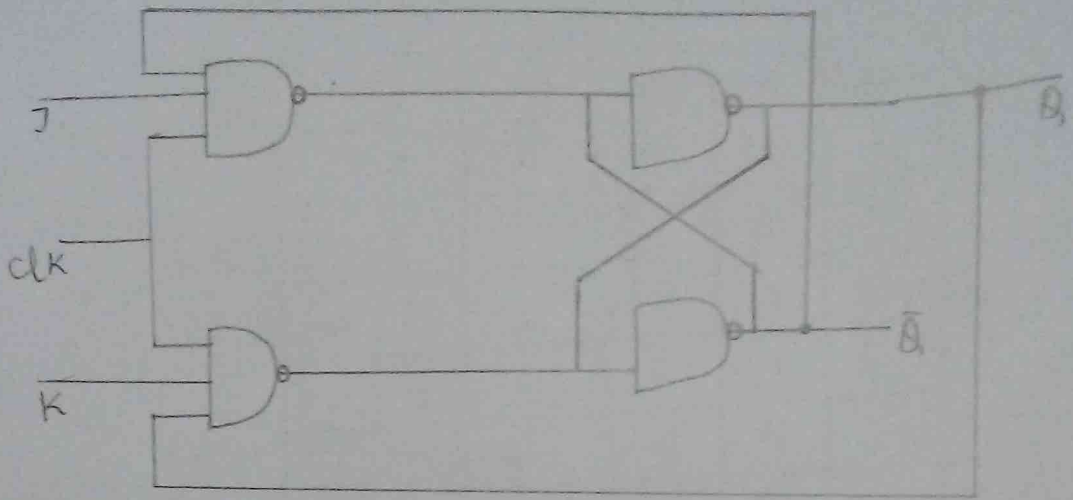
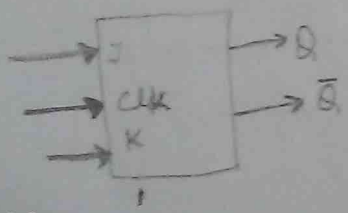


Diagram: JK flip flop



Truth Table :-

clk	J	K	Q_n	Q_{n+1}	Comment
0	X	X	Q_n	Q_n	NC
1	0	0	Q_n	Q_n	NC
1	0	1	0	1	Reset
1	1	0	1	0	Set
1	1	1	$\bar{Q}_n$	Q_n	Toggle

Working :-

(i) when J=0, K=0

→ No change o cells even if clock.

(ii) when J=0, K=1

→ flip-flop reset.

(iii) when J=1, K=0

→ flip-flop set.

(iv) when J=1, K=1

→ the flip flop toggle.