Ch - 8

CPU

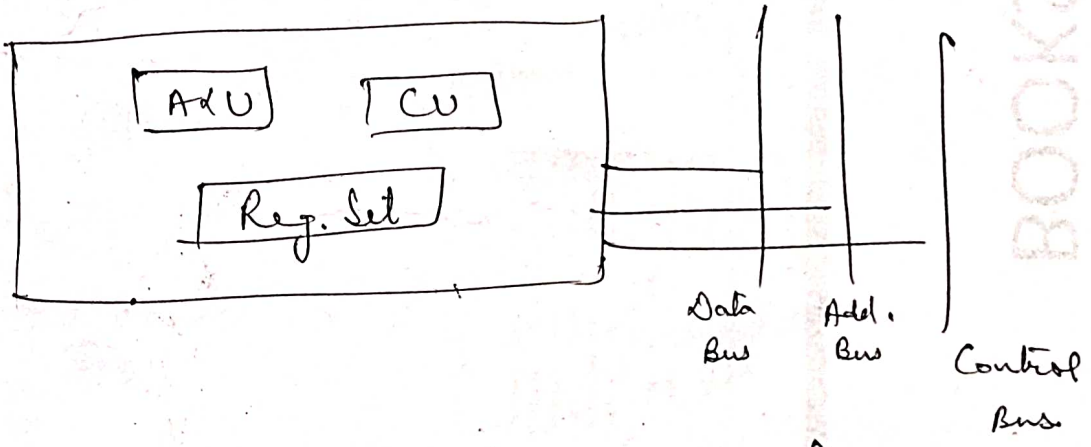
The part of the Comp that performs the bulk of Data processing op^n is called CPU. Termed as brain of computer.

Major Components.

(i) ALU → arithmetic & Logical Cal.

(ii) CU → issue control signal to ALU to perform specific opn.

(iii) Register Set
↳ store intermediate data during the exc. of inst



Data Access in Register faster Compare to Memory.

CPU is governed by its org., inst format, addressing modes & inst set. The main fx of CPU is to fetch the inst from mem. & execute it.

CPU is divided into 3 types of org:-

(i) Sngle AC org

(ii) Gen. Reg Org

(iii) Stack Org.

Central Processing Unit

CPU performs a variety of functions dictated by the type of instructions that are incorporated in the Computer.

* In programming, memory locations are needed for storing pointers, counters, return addresses, temp result etc.
Memory access is most time consuming op^n in a Computer.

* It is then more convenient & more efficient to store these intermediate values in processor registers.
∴ Data Access in Registers is much faster than the memory Access.

CPU is governed by its organization, instruction format, addressing modes and instruction set. The designer of CPU designs the instruction set by using software and hardware to perform computer operations effectively. These instructions are used by computer programmer for arithmetic and logical calculations. CPU more rapidly accesses its registers than that of memory. Because register can provide data to CPU at faster speed.

The main function of CPU is to fetch the instruction from memory and execute it. Program counter (PC) is used to store the address of current instruction under execution. Traditionally CPU is divided into three types of organization.

1. Single Accumulator Organization
2. General Register Organization
3. Stack Organization

10.1.1 Single Accumulator Organization

5 5 5 6

Figure 10.6 Control Word

10.1.3 STACK ORGANIZATION

Stack is a storage mechanism such that data items are stored in consecutive locations. Their data items are accessed by mechanism last in first out (LIFO). Stack is the concept as the number of plates placed one over the other. Any new plate is to be added at the

FILO

top of plates. Any plates have to removed should also be from the top. This concept is termed as LIFO. Stack may consist of number of register or part of main memory. Stack implementation is important from multiprogramming point of view.

Intermediate data generated by computer cannot be accommodated in registers. Since register are very limited in numbers. Hence there must be some mechanism so that bulk of intermediate data can be stored and can be retrieved easily. That can be achieved by implementing a part of memory unit as stack. Hence stack implementation is always there in the computer that supports multiprogramming. Stack pointer (SP) keeps track of top most item of stack. The process of inserting a new data item into stack is termed as PUSH operation. That is performed by first incrementing the stack pointer to next location. Then new data item is pushed at that location. DR is the data register that holds the data.

$$SP \leftarrow SP + 1$$
$$M[SP] \leftarrow DR$$

Before inserting a new data item, it should be checked whether stack could accommodate new data item. Overflow is the condition resulted when we try to push data item in the stack, which is already completely filled. Similarly an item can be removed from the top of stack. The process of removing an item from the top of stack is termed as POP operation. That is performed by first transferring the data from the top of stack to data register (DR). Then stack pointer (SP) is decremented to its lower value.

$$DR \leftarrow M[SP]$$
$$SP \leftarrow SP - 1$$

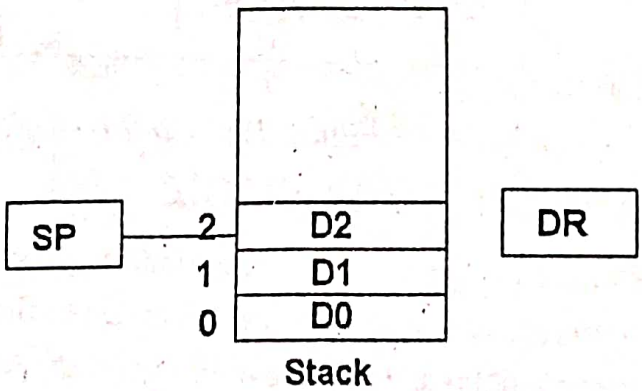


Figure 10.7 Stack Organization

Before accessing the data item from stack, it should be checked that stack should not be empty. Underflow is the condition when we try to delete (POP) data item from empty

stack. Stack can be implemented to grow by increasing the memory address as shown in figure 10.7. Stack can also be implemented by decreasing the memory address as shown in figure 10.8.

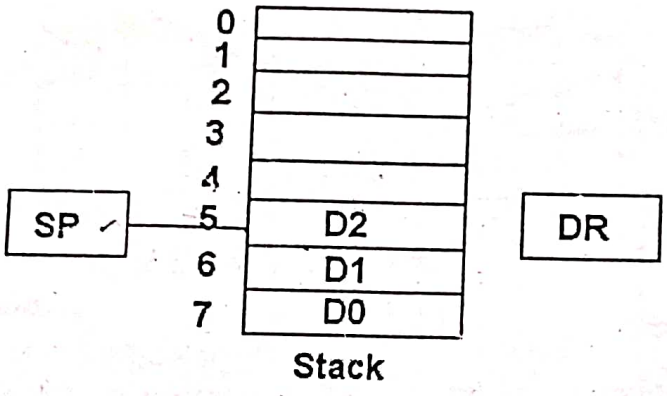


Figure 10.8 Stack Organization

In decreasing address stack, PUSH operation is performed at highest address of memory stack. When a new data item has to push, stack pointer (SP) is decremented.

$SP \leftarrow SP - 1$

$M[SP] \leftarrow DR$

When a data item is removed from stack using POP, stack pointer (SP) is incremented. The removed item from top of stack is stored in data register.

$DR \leftarrow M[SP]$

$SP \leftarrow SP + 1$

This type of stack is more commonly implemented in memory. The application of stack is there in scientific calculator, computer and other computing devices.

Problem 10.8: Write an assembly program to execute X: = (A + B) – (C + D) using stack organization.

Solution:

Instruction	Stack Contents	Stack Pointer
PUSH A	A	1
PUSH B	A, B	2
ADD	A + B	1
PUSH C	(A + B), C	2
PUSH D	(A + B), C, D	3
ADD	(A + B), (C + D)	2
SUB	(A + B) – (C + D)	1
POP X	Empty	0

Chapter 8.

INTERRUPTS.

Definition:-

An Interrupt is an asynchronous signal from H/W indicating the need for attention or a synchronous event in s/w indicating the need for a change in execution.

Interrupt Mechanism.

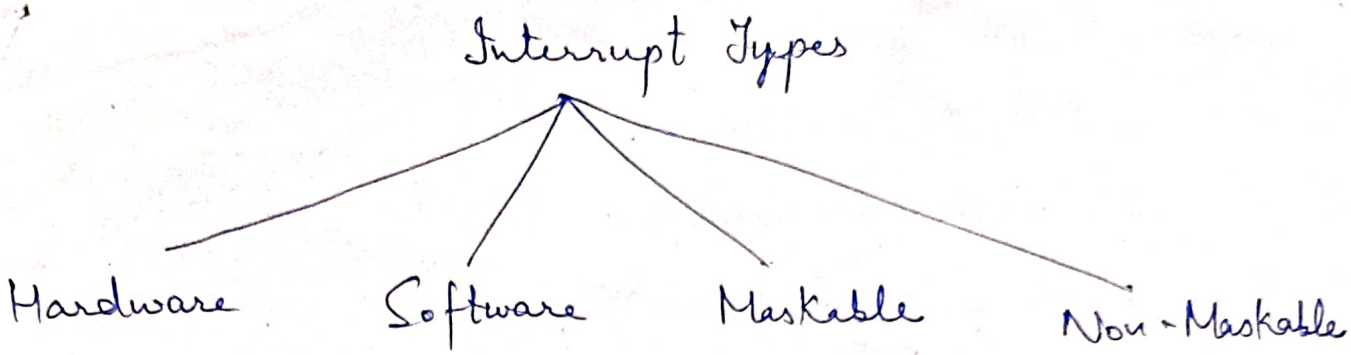
Program Interrupt can be described as a transfer of program control from a currently running program to another service program on a request generated externally or internally. After the service program is executed, the control returns to the original program.

Purpose of Interrupt:-

(i) To provide full utilization of hp speed when slow peripheral devices are interfaced to microprocessor unit.

(ii) To allow the microcomputer to handle exceptional, internal situations resulting from performing certain arithmetic op^{n}.

(iii) To allow the microcomputer to handle urgent external events.



(i) Hardware Interrupts :- When an interrupt is initiated by the Hardware in response to special internal or external conditions, a hardware interrupt is said to have occured.

Two types of H/w Interrupt

a) External

b) Internal

a) External Interrupt :- These are received from external peripheral devices (like Input or Output)

Examples :-

- → I/O device requesting transfer of data.
- → I/O device finished transfer of data.
- → Time out Interrupt (program in endless loop)
- → Power failure.

b) Internal Interrupt :- These (also known as Traps or exceptions) are hardware interrupts that are generated internally to the processor, generally on the occurance of an erroneous condition during the program execution.

Examples :- (They are not maskable)

- → Divide by zero error.
- → Overflow error.
- → Breakpoint.
- → Use of Invalid operation code
- → Protection violations
- → Out of Bound.

(ii) Software Interrupts :- Software interrupts are initiated by executing some special instructi (INT). These are special call instructions tha behave like interrupts rather than subroutine call instructions.

(iii) Maskable & Non-Maskable Interrupts :-

Maskable interrupts can be masked out or locked out for short periods of time by the software to allow the CPU to perform critical op". They can be disabled by clearing the Interrupt Enable Flag using 'Clear Interrupt enable flag' CLI Instruction. To Enable it, 'Set Int. enable flag' STI instruction is used.

Non-Maskable interrupts cannot be masked out. They are used for conditions that require immediate attention by the CPU.

Examples :-

- → Power failure
- → Memory Read Error.

3 2 2

Program Status Word :- The collection of all status bit conditions in the CPU is known as PSW. The PSW is stored in a separate Hardware register & ~~the~~ contains the status information that characterizes the state of the CPU.

PSW includes :-

i) the status bits from the last ALU operation

ii) Specifies the interrupts that are allowed to occur.

iii) Also tells whether the CPU is operating in a supervisor or user mode.

Supervisor Mode or Master Mode :- An operating System controls & supervises all other programs in the Computer. There is no restriction. All instructions will be used. It is also called System mode

User Mode or Slave Mode :- The CPU is normally in the user mode when executing user programs. Some instructions are restricted in this mode.

Status bits (sometimes also known as flags) are bit values that indicate various information about the processor's state.

Common flags in PSW are :-

C (Carry) : Set to 1 if the end carry out of ALU is 1. It is cleared to 0 if end carry is 0.

S (Sign) :- Set to 1 if the MSB of ALU output is 1. It is set to 0 if the MSB of the ALU output is 0.

Z (Zero) : Set to 1 if all the bits of the ALU ~~or~~ output are 0.

V (overflow): Set to 1 if the overflow condition is satisfied i.e if the XOR of last two carries from the ALU is equal to 1 & cleared to zero otherwise.