Name- Sumit Kumar Giri

Uni. roll No. - 2000213 (CS-2)

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Subject- Computer organization and Assembly language Programming (COALP)

Subject Code- (ACCS-16303)

Assignment- 1st.

Section-A

Q1.

(a) what do you mean by micro operations?

Ans:- The operations executed on data stored in registers are called micro-operations. Ex- Shift, Count, clear, load and Add.

The operations performed on the data stored in register is faster than the data stored in memory.

(b) what do you mean by register transfer language?

Ans:- **Register transfer language:-**

The symbolic notation used to describe the micro-operation transfers amongst registers is called Register tranfer language. The term register transfer means the availability of hardware logic circuits that can perform a stated micro-operation and transfer the result of the operation to the same or another register.

(C) what is the difference between direct and indirect addressing mode?

Ans:- There are some common difference between direct and indirect addressing mode.

Direct addressing mode	indirect addressing mode.
(i) A direct address instruction is placed at address 22 in memory.	The instruction in address 35 has a mode bit I = 1, recognized as an indirect address instruction.
(ii) The I bit is 0, so the instruction is recognized as a direct address instruction.	The address of the operand in this case is 1350.

Direct addressing mode	indirect addressing mode.
(iii) The opcode specifies an ADD instruction, and the address part is the binary equivalent of 457.	The address part is the binary equivalent of 300.
(iv) The control finds the operand in memory at address 457 and adds it to the Content of AC.	The control goes to address 300 to find the address of the operand and the operand found in address 1350 is then added to the Content of AC.

(d) Differentiate between Hardwired and micro programmed unit.

Ans:- There are many differentiate between Hardwired and micro programmed unit.

	Hardwired control unit	Microprogrammed Control unit
01	Hardwired control unit generates the control signals needed for the processor using logic circuits.	Microprogrammed Control unit generates the Control signals with the help of micro instructions stored in Control memory.
02	Hardwired Control unit is faster when compared to microprogrammed Control unit as the required control signals are generated with the help of hardwares.	This is slower than the other as micro instructions are used for generating signals here.

	Hardwired control unit	Microprogrammed Control unit
03.	Difficult to modify as the control signals that need to be generated are hard wired.	Easy to modify as the modification need to be done only at the instruction level.
04.	more costlier as everything has to be realized in terms of logic gates.	Less costlier than hardwired control as only micro instructions are used for generating control signals.
05.	It cannot handle complex instructions as the circuit design for it becomes complex.	It can handle complex instructions.
06.	only limited number of instructions are used due to the hardware implementation.	Control signals for many instructions can be generated.
07.	used in Computer that makes use of Reduced Instruction Set Computers (RISC).	used in Computer that makes use of Complex Instruction Set Computers (CISC).
08.	Control memory absent	Control memory present.

(e) Explain various types of register used in a system.

Ans:- * Accumulator :- This is the most common register, used to store data taken out from the memory. It is in different numbers in different microprocessors.

* General purpose Registers :- This is used to store data intermediate results during program execution. It can be accessed via assembly programming.

* Special purpose Registers :- Users do not access these registers. These registers are for Computer System.

* Memory Address Registers (MAR) :- Memory Address Register are those registers that holds the address for memory unit.

* PC (program Counter) :- program counter points to the next instruction to be executed. PC points to the address of the next instruction to be fetched from the main memory when the previous instruction has been succesfully completed.

* IR (Instruction Register) :- Instruction Register holds the instruction to be excuted. The instruction from PC is fetched and stored in IR.

(f) what do you mean by Instruction code?

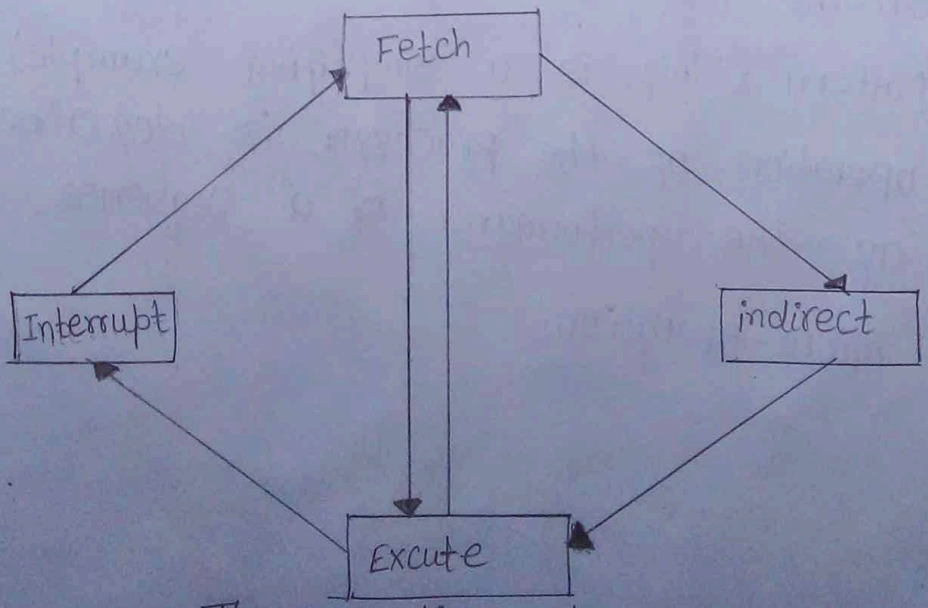
Ans:- An instruction code is a group of bits that instruct the computer to perform a specific task. It is usually divided into parts each having its own particular Interpretation. They are two types.
(i) operation code (ii) operands.

Section-B

Q2. Explain instruction cycle. How the instruction cycle is used to determine the type of instruction with flowchart?

Ans:- Instruction cycle :-

Each Phase of Instruction cycle can be decomposed into sequence of elementary micro-operations. In the above examples, there is one sequence each for the fetch, Execute and Interrupt cycles.



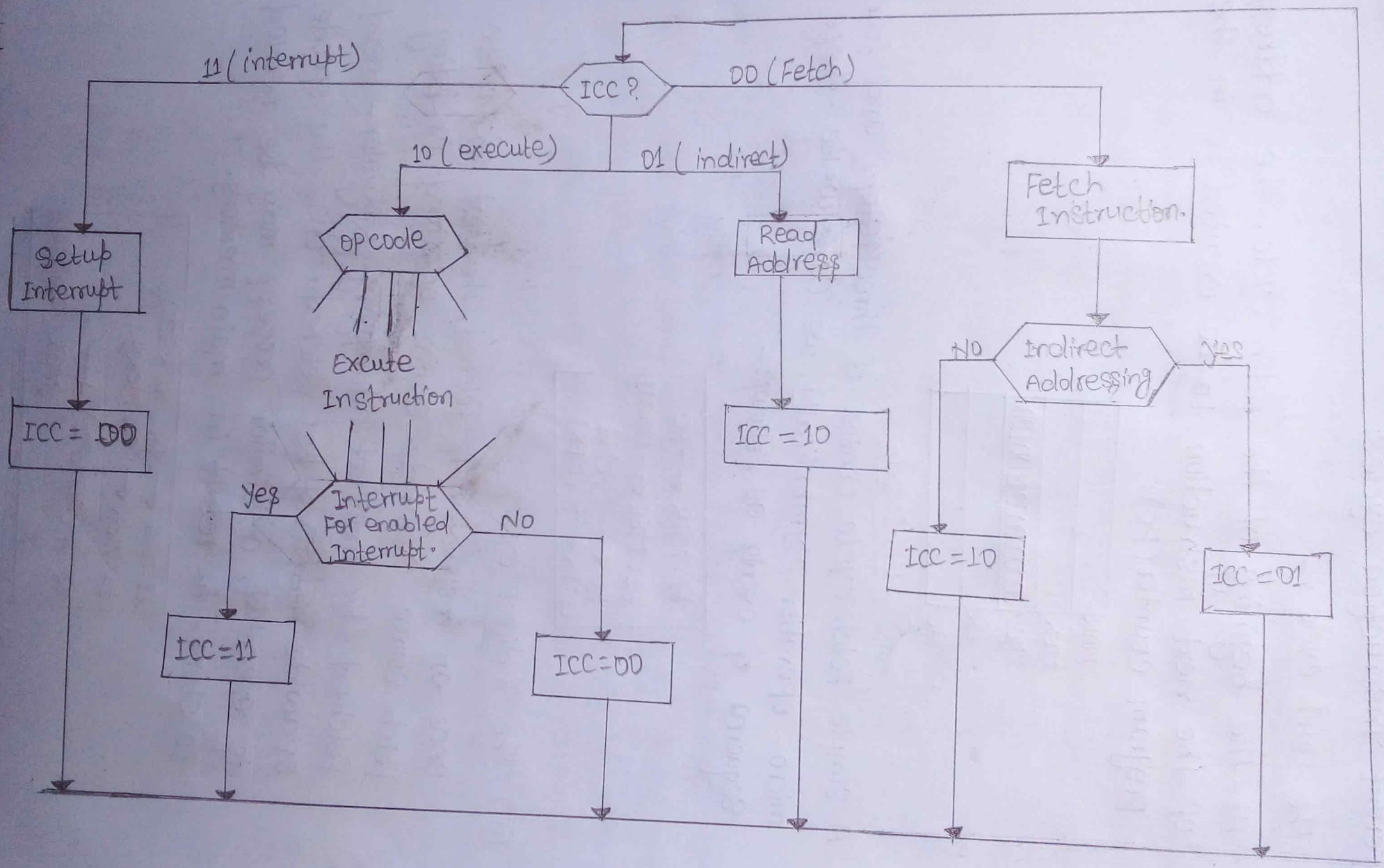
The Instruction cycle.

The Indirect cycle is always followed by the Execute cycle. The Interrupt cycle is always followed by the Fetch cycle. For both Fetch and execute cycles, the next cycle depends on the state of the system.

we assumed a new 2-bit register called Instruction cycle Code (ICC). The ICC designates the State of processor in terms of which portion of the cycle It is in:-

00: Fetch cycle.
01: Indirect cycle
102: Excute cycle.
11: Interrupt cycle.

At the end of the each cycles, the ICC is Set appropriately. The above Flowchart of Instruction cycle describes the Complete Sequence of micro-operations, depending only on the instruction sequence and the interrupt pattern (This is a simplified example). The operation of the processor is described as the performance of a sequence of micro-operation.



Flowchart For Instruction cycle:

Different Instruction cycles:

(i) The Fetch cycle :-

At the begining of the fetch cycle, the address of the next instruction to be excuted is in the program counter (PC).

MAR	
MBR	
PC	0000000001100100
IR	
AC	

BEGINING.

A Simple Fetch cycle consist of three steps and four micro-operation. Symbolically, we can write these sequence of events as follows:-

```
t1 : MAR ← PC
t2 : MBR ← Memory
     PC ← (PC) + 1
t3 : IR ← (MBR)
```

(ii) The Indirect cycles :-

once an instruction is fetched, the next step is to fetch source operands. Source operand is being fetched by indirect addressing. Register-based operands need not be fetched. once the opcode is executed, a similar process may be needed to store the result in main memory.

```
t1 : MAR ← (IR (ADDRESS))
t2 : MBR ← MEMORY
t3 : IR (ADDRESS) ← (MBR (ADDRESS))
```

(iii) The Interrupt cycle :-

At the completion of the Excute cycle, a test is made to determine whether any enabled interrupt has occurred or not. If an enabled interrupt has occurred then interrupt cycle occurs. Lets take a sequence of micro-operation:

```
t1: MBR ← (PC)
t2: MAR ← SAVE ADDRESS
    PC  ← ROUTINE ADDRESS
t3: MEMORY ← (MBR)
```

(iv) The Execute cycle :-

The other three cycles (fetch, indirect and Interrupt) are simple and predictable. Each of them requires simple, small. and fixed sequence of micro-operation are repeated each time around. Excute cycle is different from them. Like, for a machine with N different opcodes there are N different sequence of micro-operations that can occur.

```
t1: MAR ← (IR(ADDRESS)
t2: MBR ← MEMORY.
t3: R   ← (R) + (MBR)
```

Q3. Explain the following instructions with examples.

(i) LHLD 16 addr.

Ans:- In 8085 Instruction set LHLD is a mnemonic that stands for load HL pair using Direct addressing From memory location whose 16-bit address is denoted as a16. So the previous content of HL register pair well get updated with the new 16-bits value. AS HL pair has to be updated, so data comes from two Consecutive memory locations starting at the address a16 and also from next address location. It occupies 3-Bytes in the memory.

Mnemonics, operand	opcode (in HEX)	Bytes
LHLD Address	2A	3

Let us Consider one example instruction LHLD 4050H falling in this category. This instruction will occupy 3-Bytes and so 3 memory locations.

	Before	After
(4050H)	BBH	BBH
(4051H)	AAH	AAH
(H)	CCH	AAH
(L)	DDH	BBH

Address	Hex codes	Mnemonic	Comment
200B	2A	LHLD	initialize HL register pair from 4050H and 4051H memory locations contents.
200C	50		Low order Byte of the address.
200D	40		High order Byte of the address.

Note that there are no instructions in 8085 like LBCD a16 and LDED a16. As HL pair is the most important register pair,

(ii) LXI rp, 16 addr:-

The instruction loads 16-bit data in the register pair designated in the operand.

Eg:- LXI H, 2034H (2034H is stored in HL pair so that it act as memory pointer.)

(iii) STAX rp :-

The contents of the accumulator are copied into the memory location specified by the contents of the operand (register pair). The contents of the accumulator are not altered.

Eg:- STAX B (The content of accumulator is stored into the memory location specified by the BC register pair.

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Q4. Explain various types of Computer instruction formats.

Ans:- A Computer performs a task based on the instruction provided. Instruction in computers comprises groups called fields. These fields contain different information as for computers everything is in 0 and 1 so each field has different significance based on which a CPU decides what to perform. The most common fields are:

- operation field specifies the operation to be performed like addition.
- Address field which specifies how operand is to be founded.

Instruction is of variables length depending upon the number of addresses it contains. Generally, CPU organization is of three types based on the number of address fields:

(1). Single Accumulator organization.
(2). General register organization.
(3). Stack organization.

In the first organization, the operation is done involving a special register called the accumulator. In second on multiple registers are used for the computation purpose.
Note that we will use $X = (A+B) * (C+D)$ expression to showcase the procedure.