Sumit Mondal

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OBJECTIVE

ECE Master's student with a focus in Hardware Design, Digital Signal Processing, and Wireless Communications seeking full-time employment starting Summer/Fall 2020.

EDUCATION

GEORGIA INSTITUTE OF TECHNOLOGY, Atlanta, Georgia **GPA: 4.0** *Jan 2019 - May 2020*

- Candidate for Master of Science in Electric and Computer Engineering

GEORGIA INSTITUTE OF TECHNOLOGY, Atlanta, Georgia **GPA: 3.7** *Aug 2015 - Dec 2018*

- Bachelor of Science in Electric Engineering, *Summa cum laude*
- Honors: Warren Batts & Austin Brown Innovation Award, Zell Miller Scholarship

SKILLS

Programming: SystemVerilog, MATLAB, Python, C/C++, VHDL
Hardware: FPGAs(Intel/Xilinx/MicroSemi), ARM mbed, Oscilloscope, Network Analyzer
Software: Cadence Simvision, Cadence Innovus, Xilinx Vivado**,** NI LabView, Altera Quartus II, Synopsys, Git, SVN

EXPERIENCE

Maxim Integrated | San Jose, California *May 2019-Aug 2019*
Digital IC Design Intern

- Created and debugged System Verilog directed tests with randomized stimulus in UVM
- Wrote assertions to verify the timing of digital to analog interfaces of a healthcare IC
- Evaluated code coverage and wrote additional tests in order to reach sufficient coverage
- Analyzed a digital decimation filter using MATLAB and developed a design plan for area reduction

Harris Corporation | Melbourne, Florida *May 2018-Aug 2018*
Digital Design and Digital Signal Processing Intern

- Designed a SPI Master Interface in VHDL for interfacing with 16 high speed Digital-to-Analog Converters (DAC) and 4 Analog-to-Digital Converters (ADC) for a Small Satellite Mission
- Implemented Digital Signal Processing (DSP) algorithms (such as correlations, FFTs, and RRC filters) in MATLAB to assist in system engineering challenges
- Modeled and tested the the Doppler effect on the signal integrity of wide-band communication signals via a customized MATLAB GUI

PROJECTS

Vertically Integrated Projects (VIP) Research Program – *Aug 2016-Present*
Graduate Research Assistant for Intelligent Digital Communications *Jan 2019-Present*

- Lead a diverse team of undergraduates to conduct research in the area of Software-Defined-Radio (SDR), Wireless Communications, and Digital Signal Processing
- Manage and maintain an SDR sensor network in Bobby Dodd Stadium designed to record Game-Day Wireless Spectrum data

DSP Hardware Design Project *Nov 2018*

- *Edge Detection:* Designed a Sobel Edge Detection Algorithm in VHDL for a static image (320x240) with a VGA output on a Basys 3 FPGA Board
- Implemented a 2D Convolutional filter on an input image loaded and stored in FPGA block RAM

Advanced C++ Design Project *March 2018*

- *FFT Implementation:* Designed a parallel processing (Multi-threading) algorithm to perform the Fast Fourier transform, an O(n) implementation of the Discrete Fourier Transform

Statistical Machine Learning Project (Marine Voice Recognition) *March 2019*

- Created a Random Forest Model able to differentiate marine mammal voices with up to 95% accuracy
- Developed a frequency transform to emphasize marine whistles, and reduce hydrophone/ocean noise

ACTIVITIES, AWARDS, and LEADERSHIP

Undergraduate Teaching Assistant *Jan 2017-Dec 2018*

- Assist students in Digital Design Laboratory understand concepts such as FPGA prototyping, VHDL Simulations, Oscilloscopes, Logic analyzers, and State Machine design