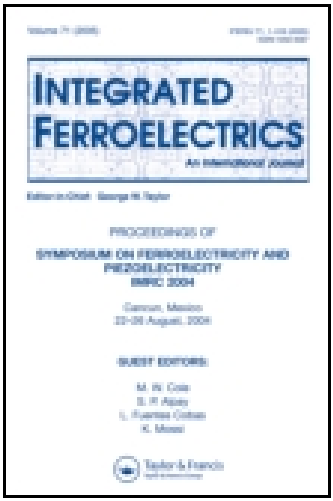

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A Ferroelectric Capacitor Mathematical Model for Spice Simulation

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A behavioral ferroelectric capacitor model based on Q-V expression with model parameters extracted from experimental hysteresis loops is proposed. A compact equivalent circuit of this model is described for spice simulation of nonvolatile memories. Excellent agreement was achieved between our measurements and simulation results. The runtime for simulation of a hysteresis loop with 10,000 points is 1.55 seconds, which is similar to 1.15 seconds for a normal capacitor.

Keywords: ferroelectric capacitor; Q-V expression; hysteresis loop; equivalent circuit

INTRODUCTION

In recent years ferroelectric random access memories (FeRAMs) have attracted considerable attention as a possible next generation nonvolatile memory technology due to the benefits of small cell size, low voltage operation, fast access time and high read/write endurance with nonvolatile data storage [1, 2]. An accurate model expressing the electrical properties of a ferroelectric capacitor is especially important for the design and optimization of ferroelectric memories. There have been many attempts at modeling ferroelectric capacitors, and significant progress has been made [3–6]. However, a compact dynamic ferroelectric capacitor model with high accuracy which can be easily introduced to existing EDA tools is still absent. Some physically based models provide satisfying intuition into the material behavior but are too complicated for simulation by existing EDA tools. Other behavioral models are not consummate enough to be flexible for different ferroelectric capacitors with different parameters. Otherwise, some models spend too long time in simulation, which is disadvantageous for simulation of large scale FeRAMs.

In this paper, we propose a compact mathematical ferroelectric capacitor model with good compatibility to existing circuit simulation tools, fine

flexibility for different capacitors with different parameters, short simulation time and sufficient accuracy. The model is based on the mathematical basis of Q-V relationship which are assumed to be determined by the past extremum values of the voltage input and initial polarization. Parameters of the model can be extracted by curve fitting a measured hysteresis loop. The transitions between the loops under different voltage patterns show a high accuracy with measured results over a wide range of operation. The time required for the polarization reversal is substantially fast so that the polarization reversal time of the ferroelectric capacitors does not affect the operational speed of the practical memories [7]. For simplicity, frequency effect caused by dipole switching time delay and other time dependent effects such as polarization fatigue and relaxation are neglected.

MATHEMATICAL BASIS

Q-V Expression for Primary Hysteresis

The Q-V curve of a ferroelectric capacitor is similar to its P-E (polarization-electric field) hysteresis curve [8]. Thus in point of circuit simulation a ferroelectric capacitor can be regarded as a voltage-controlled nonlinear capacitor whose Q-V relation presents a hysteresis loop.

The Preisach model [9] is an appropriate macroscopic model describing the ferroelectric material as a set of elementary dipoles that contribute to the total polarization. However, it requires the time-consuming numerical evaluation of double integrals. Thus this approach is difficult to be applied for circuit simulation directly. In fact, for generic simulation Q-V expressions can take any functional form as long as they fit the experimental loops. The hyperbolic tangent is often chosen [4, 10]. Here we select the arc tangent as the Q-V expression form because the derivative of the arc tangent is more simply and spends less time in circuit simulation than that of the hyperbolic tangent. And the Q-V expression based on the arc tangent function gives better agreements with our experimental results than that based on the hyperbolic tangent according to our practical simulations.

A saturated hysteresis loop can be divided into two branches as lower branch and upper branch, as illustrated in Fig. 1. The Q-V expressions of the two branches are described as:

$$Q_1(V) = \frac{c}{2a}\left[arc\tan\left(\frac{V_m + V_c}{a}\right) - arc\tan\left(\frac{V_m - V_c}{a}\right)\right] + \frac{c}{a}\cdot arc\tan\left[\frac{(V - V_c)}{a}\right] \quad \text{for lower branch} \tag{1}$$

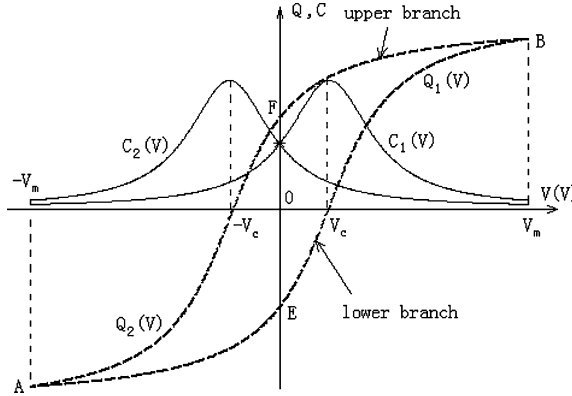

FIGURE 1 Hysteresis loop and C-V curve of a ferroelectric capacitor.

$$Q_2(V) = \frac{c}{2a}\left[arc\tan\left(\frac{V_m - V_c}{a}\right) - arc\tan\left(\frac{V_m + V_c}{a}\right)\right] + \frac{c}{a}\cdot arc\tan\left[\frac{(V + V_c)}{a}\right] \quad \text{for upper branch} \tag{2}$$

where a, c are curve fitting parameters to be extracted from experimental hysteresis loops. V_c is the macroscopic coercive voltage of hysteresis loops.

In actual circuit simulation, the total charge or polarization of a ferroelectric capacitor must be calculated by integrating its differential capacitance, which is equal to the derivative of charge on the capacitor electrode with respect to the voltage across the capacitor as illustrated in Fig. 1. According to Eqs. (1) and (2), the C-V expressions are described as:

$$C_1(V) = \frac{dQ_1(V)}{dV} = \frac{c}{a^2 + (V - V_c)^2} \tag{3}$$

$$C_2(V) = \frac{dQ_2(V)}{dV} = \frac{c}{a^2 + (V + V_c)^2} \tag{4}$$

where $C_1(V)$ is implemented when the capacitor bias changes from $-V_m$ to V_m, and $C_2(V)$ is implemented when the capacitor bias changes from V_m to $-V_m$. The two branches switch to each other when the Q-V curve changes direction or when dV/dt changes sign (see Fig. 1). We import a return sign

function:

$$\text{sgn(x)} = -1 \text{ (if } x < 0); \text{or } 0 \text{ (if } x = 0); \text{or } 1 \text{ (if } x > 0) \tag{5}$$

Combining Eqs. (3)–(5), $C(V)$ can be written in the uniform expression

$$C(V) = C_1(V) \cdot \frac{[1 + \text{sgn}(dV/dt)]}{2} + C_2(V) \cdot \frac{[1 - \text{sgn}(dV/dt)]}{2} \tag{6}$$

Q-V Expression for Minor Hysteresis Loops Under Arbitrary Bias

From experimental results, when the amplitude of the stimulated voltage decreases from V_m to V_x, a minor hysteresis loop (C-G-D-H-C) is generated in the major hysteresis loop (A-E-B-F-A) as illustrated in Fig. 2. We suppose $Q_1'(V)$ and $Q_2'(V)$ denote the lower branch and the upper branch of the minor hysteresis loop respectively. Referring to Eqs. (1) and (2), $Q_1'(V)$ and $Q_2'(V)$ can be formulated as

$$Q_1'(V) = \frac{c'}{2a}\left[arc\tan\left(\frac{V_x + V_c}{a}\right) - arc\tan\left(\frac{V_x - V_c}{a}\right)\right] + \frac{c'}{a} \cdot arc\tan\left[\frac{(V - V_c)}{a}\right] \tag{7}$$

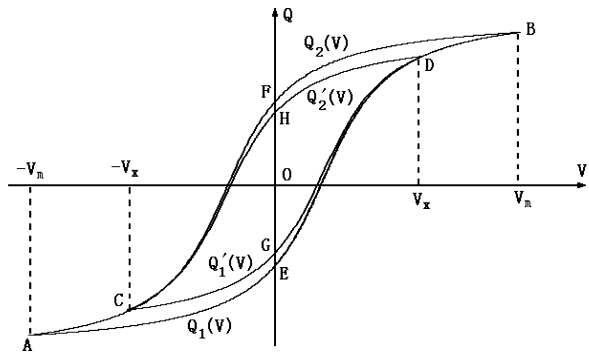

FIGURE 2 The transition between the major loop (A-E-B-F-A) and a minor loop (C-G-D-H-C).

$$Q'_2(V) = \frac{c'}{2a}\left[arc\tan\left(\frac{V_x - V_c}{a}\right) - arc\tan\left(\frac{V_x + V_c}{a}\right)\right] + \frac{c'}{a}\cdot arc\tan\left[\frac{(V + V_c)}{a}\right] \tag{8}$$

where c' is described as

$$c' = \frac{c\cdot\left[arc\tan\left(\frac{V_m+V_c}{a}\right) - arc\tan\left(\frac{V_m-V_c}{a}\right) + 2\cdot arc\tan\left(\frac{V_x-V_c}{a}\right)\right]}{arc\tan\left(\frac{V_x+V_c}{a}\right) + arc\tan\left(\frac{V_x-V_c}{a}\right)} \tag{9}$$

The C-V expression for the minor hysteresis loop generated by stimulation of voltages with amplitude of V_x is formulated as

$$C'(V) = C'_1(V)\cdot\frac{[1 + \mathrm{sgn}(dV/dt)]}{2} + C'_2(V)\cdot\frac{[1 - \mathrm{sgn}(dV/dt)]}{2} \tag{10}$$

where

$$C'_1(V) = \frac{c'}{a^2 + (V - V_c)^2} \tag{11}$$

$$C'_2(V) = \frac{c'}{a^2 + (V + V_c)^2} \tag{12}$$

where c' is described as Eq. (9), and V_x is an arbitrary positive number denoting the amplitude of the arbitrary biases across the ferroelectric capacitor. The remnant polarization corresponding to stimulation of voltage with the amplitude of V_x is given as

$$Q'_r|_{Vx} = \pm\frac{c'}{2a}\left[arc\tan\left(\frac{V_x - V_c}{a}\right) - arc\tan\left(\frac{V_x + V_c}{a}\right) + 2\cdot arc\tan\left(\frac{V_c}{a}\right)\right] \tag{13}$$

A ferroelectric capacitor in a FeRAM cell is always history dependent and remains remnant polarization state before operation. The initial remnant polarization can be specified by setup of the initial voltage across the

ferroelectric capacitor as below:

$$V_{init} = init \cdot \frac{(a^2 + V_c^2)}{2a} \cdot \left[arc\tan\left(\frac{V_x - V_c}{a}\right) - arc\tan\left(\frac{V_x + V_c}{a}\right) + 2 \cdot arc\tan\left(\frac{V_c}{a}\right)\right] \tag{14}$$

here $init = 1$ when the capacitor is polarized to positive state or $init = -1$ when the capacitor is polarized to negative state.

MACROMODEL FOR SPICE SIMULATION

A circuit representation of this mathematical model with the input port $in+$ and $in-$ is shown in Fig. 3. C_x is a voltage-controlled nonlinear capacitor with the capacitance expressed by Eq. (10), which is the core to represent the nonlinear and hysteretic characteristics of the ferroelectric capacitor. Some other behavioral elements are used in the equivalent circuit serving as control portion. We define V_f as the voltage bias across the ferroelectric capacitor. Ecap is a voltage-controlled voltage source to transform V_f into the voltage of node *cout*. Gswitch is a voltage-controlled switch with the controlling voltage of V_{dout}, which is opened only when V_{dout} is near zero in a little range $(-\delta V, \delta V)$. Ecomp is an ideal op-amp element. Ecomp and Capacitor c1, Resistor r1 form a differential circuit for differential operation of V_{cout}

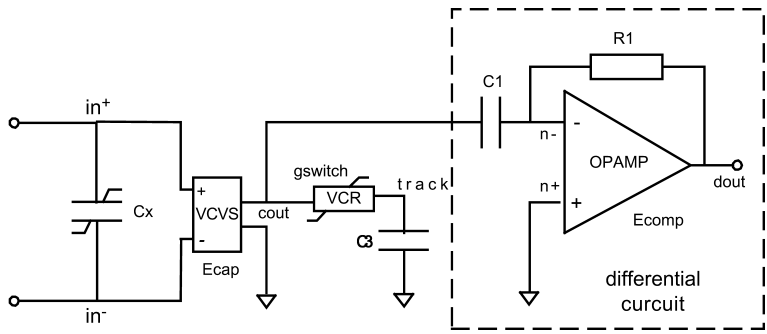

FIGURE 3 A circuit representation of the mathematical ferroelectric capacitor model.

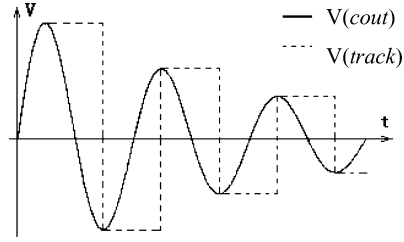

FIGURE 4 V(*track*) keeps the last extremum of the capacitor biases.

to V_{dout}:

$$V_{dout} = -R_1 C_1 \frac{dV_{cout}}{dt} = -R_1 C_1 \frac{dV_f}{dt} \tag{15}$$

Though the voltage bias across the ferroelectric capacitor is continuously changing, Gswitch and Capacitor c3 enable the node of *track* to keep the last extremum of the voltage biases, as illustrated in Fig. 4. Therefore, V(*track*) is regarded as the amplitude of the arbitrary biases applied to the ferroelectric capacitor. In the input netlist file for simulation Eq. (9) becomes

$$c' = \frac{c \cdot \left[arc\tan\left(\frac{V_m + V_c}{a}\right) - arc\tan\left(\frac{V_m - V_c}{a}\right) + 2 \cdot arc\tan\left(\frac{V_{track} - V_c}{a}\right)\right]}{arc\tan\left(\frac{V_{track} + V_c}{a}\right) + arc\tan\left(\frac{V_{track} - V_c}{a}\right)} \tag{16}$$

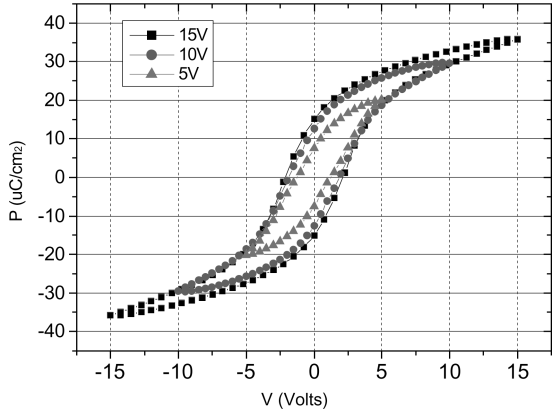

FIGURE 5 P-V hysteresis loops measured at different voltages from a PZT capacitor. (See color plate IV)

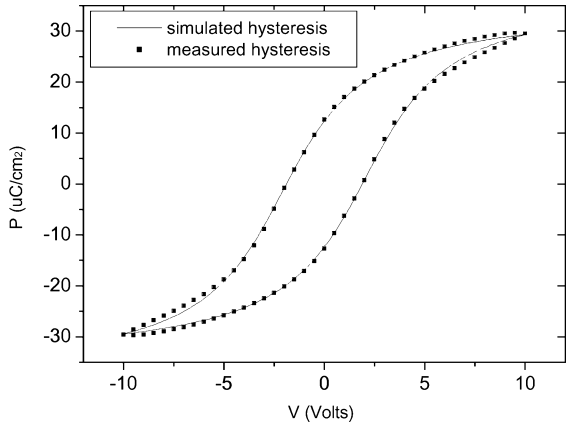

FIGURE 6 Simulated and measured hysteresis loop at 10 V.

SIMULATION RESULTS AND DISCUSSIONS

The ferroelectric capacitor samples were prepared by sol-gel method with Pt electrodes of 100×100 um^2 size fabricated by RIE (Reactive Ion Etching) and PZT dielectric thickness of about 400 nm. Figure 5 shows the measured hysteresis loops by stimulation of triangular waveforms at different voltages.

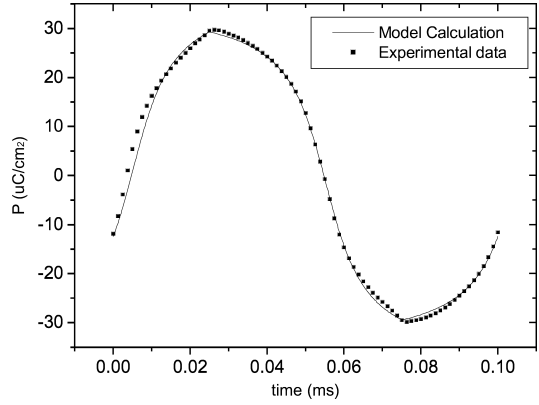

FIGURE 7 Simulated and measured polarization-time curve at 10 V.

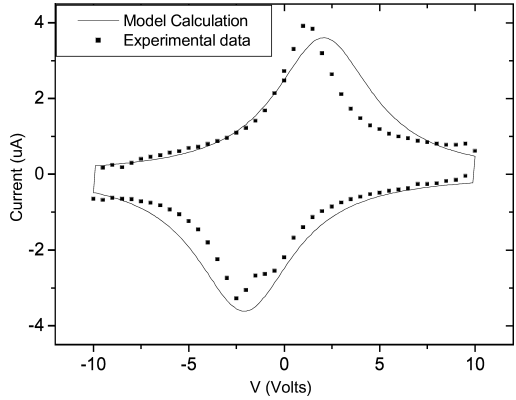

FIGURE 8 Simulated and measured current-voltage curve at 10 V.

The parameters extracted by curve fitting the measured hysteresis at 10 V is: a = 3.1024, $V_m = 10$, $V_c = 2.08677$, $c = A*0.7236$, where A is the area of ferroelectric capacitor. Figure 6 shows the comparison between simulated and measured hysteresis loop at 10 V by Sawyer-Tower circuit. Figure 7 shows the comparison between simulated and measured Polarization-Time curve during a period of triangular stimulated waveform. Comparison between simulated and measured Current-Voltage relationship is shown in Fig. 8. Some disagreement exists in Fig. 8 between simulation

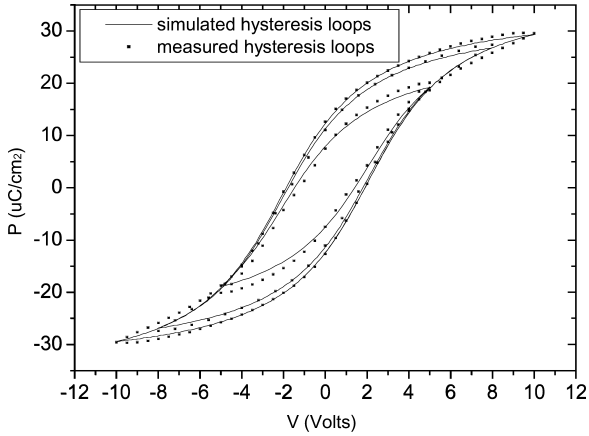

FIGURE 9 Simulated and measured hysteresis loops at 10 V, 8 V and 5 V.

and experiment probably due to measurement error and neglect of dipole switching time.

A set of hysteresis loops at different voltages of 10 V, 8 V and 5 V were simulated and compared with experimental results in Fig. 9. The transitions between the simulated loops show good agreement with experimental data.

CONCLUSION

Based on the above agreement, we conclude that the complex behavior and history dependence of a ferroelectric capacitor can be described as a voltage-controlled nonlinear capacitor with behavioral elements as control portion. This compact model is conveniently introduced to existing tools such as Spice for FeRAM circuit simulation with short simulation runtime. The model will demonstrate high accuracy and good agreement with actual ferroelectric capacitors in circuit simulation as long as the Q-V (or C-V) mathematical expression is adequately precise. Based on this mathematical model, future enhancement is easily imported to handle dynamic responses and other higher-order effects, such as imprint, fatigue, and asymmetry of hysteresis loops due to various defects.

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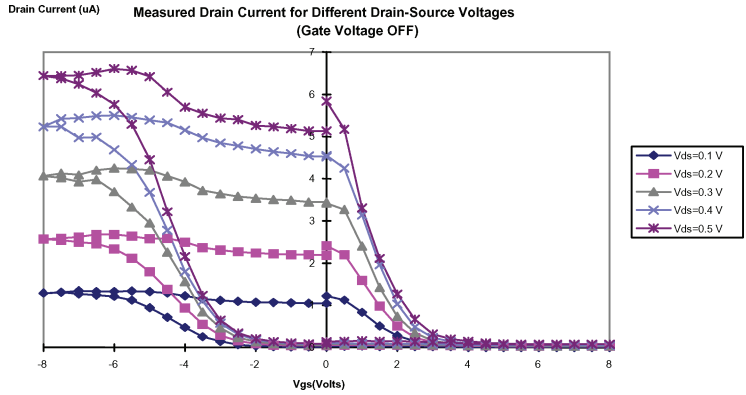
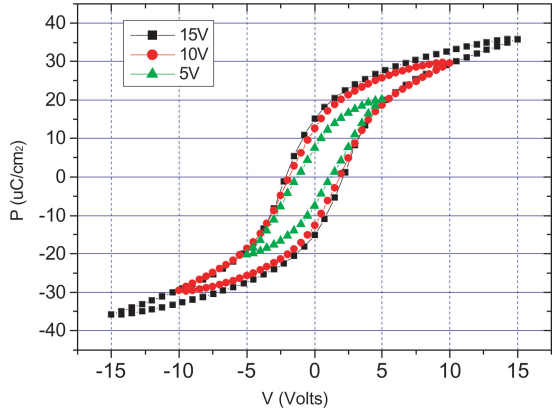


Color Plate III. See Figure 9 on page 98.—Measured drain current for Remnant mode.



Color Plate IV. See Figure 5 on page 108.—P-V hysteresis loops measured at different voltages from a PZT capacitor.