Experiment 9
Basic Combinatorial Circuits

Introduction

Logic gates are the basic building blocks in digital circuits. In this experiment, you will study the characteristics of basic logic gates and also implement some simple combinatorial circuits. Logic gates and several other digital functions are available in the form of IC (Integrated Circuit) chips. These ICs belong to several ***Logic Families***, such as TTL, CMOS, ECL, etc., of which ***TTL*** (***Transistor-Transistor Logic***) is the most popular one. The basic differences between these logic families arise from their speed and power consumption. The TTL family itself has several sub-families, such as, ***Standard TTL***, ***Schottky TTL*** (***STTL***), ***Low-Power Schottky TTL*** (***LSTTL***), ***Fast TTL*** (***FTTL***), etc. Among the TTL families, the ones that are the most popular are LSTTL and FTTL.

The commercial versions of the TTL ICs have numbers 74YYXXXX, where YY (up to 2 two characters) represents the sub-family and XXXX (up to 4 digits) represents a particular number. These numbers were arrived at as and when various manufacturers designed different functions into ICs. This number may have 2, 3, or 4 digits. Thus 7404 is a ***Hex-Inverter*** of the Standard TTL technology, whereas 74S04 is a Hex-Inverter using the Schottky technology. All TTL family ICs use +5 V as the power supply. The ***Logical HIGH*** output (V_{OH}) is typically > 2.4 V, while the ***Logical LOW*** output (V_{OL}) is < 0.4 V. The output signal levels can vary with the temperature and load. However, the manufacturer specifies the V_{OH} and V_{OL} levels for the worst-case conditions, i.e., for the maximum load condition and over the entire temperature range (0-70°C).

1. Inverter Characteristic

In this experiment, we first study the transfer characteristic of a TTL inverter and the effect of load on the V_{OH} and V_{OL} levels. The recommended load for an output is specified in terms of its *fan out*, which is defined as the maximum number of identical inputs that the specified output can drive.

Experiment

A. Inverter Characteristic Using DMM

(i) Wire the inverter circuit of Fig.1. Note that this is one of the gates of the 7404 Hex Inverter IC, as shown in Fig. 3.

(ii) Using the DMM, obtain several input voltages (V_i) (0.4 V, 0.8 V, 1 V, 1.2 V, 1.4 V, 1.6 V, 1.8 V, 2 V, 2.5 V, 3 V, 4 V, and 5 V) by varying the potentiometer R. Tabulate the corresponding values of the output voltage V_0.

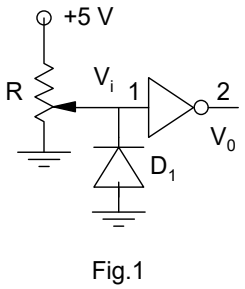


Fig.1

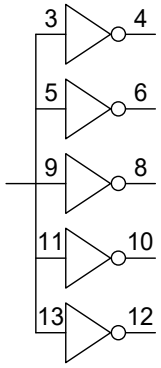


Fig.2

(iii) Now connect the remaining 5 gates of the IC as load to the inverter under test by connecting the inverter output of Fig.1 to the inputs as indicated in Fig.2. Tabulate the values of V_0 for V_i of 0.4 V and 2.5 V. Note the change in the values of V_0 with load.

B. Inverter Characteristic using FG and CRO

Remove the potentiometer R, and the +5 V DC power supply from Fig.1, and connect a ***triangular waveform*** (f = 1 kHz) going from 0 to 5 V to the input of the inverter (pin 1). Keep the load connected to the inverter output (pin 2) as in part A.(iii). Use the XY mode of the CRO to display the transfer characteristic (i.e., pin 2 versus pin 1 voltages, or, V_0 vs. V_i) and sketch it.

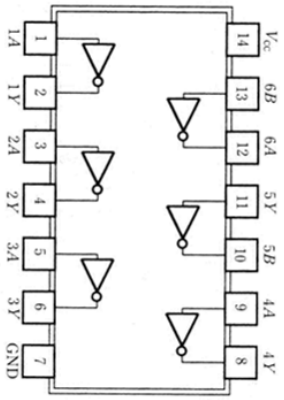


Fig. 3

2. Familiarization with the Digital Test Board

Refer to the details of the *Digital Test Board* given at the end. This board will be used in all the experiments on digital circuits.

Experiment

(i) Connect V_{CC} (+5 V) and GND to the Test Board through the microboard.

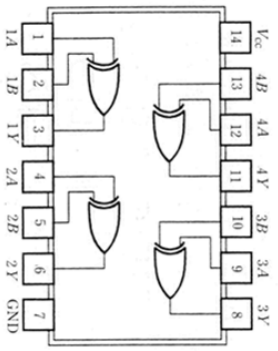
(ii) Verify the working of all the data switches by connecting their outputs individually to the Logic Probe (LP) input. For each of the data switches, check that both logic ***0*** and ***1*** levels are obtained by toggling the switch.

(iii) Connect any 4 data switch outputs to the 7-segment display driver inputs. Check the display for all the 16 input combinations. Note that for binary inputs 0000 to 0111, the display should show the corresponding decimal numbers from 0 to 7. For binary inputs 1000 to 1111, the decimal point at the top left corner of the display would also light up in addition to the numerals 0 to 7.

(iv) Connect the CLOCK output to the LP input, and verify the clock functions. N***ote that the red LED glows whenever CLOCK output is at logic '0'.***

3. Realization of Half-Adder

The half-adder is one of the basic combinatorial circuits. The aim of this part of the experiment is to design and test a half-adder circuit.



7486 Quad Ex-OR

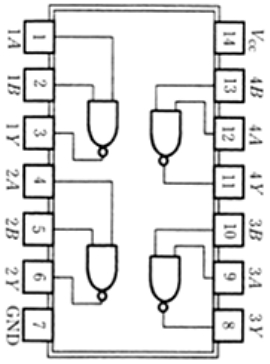
Lab Preparation

Before coming to the lab, write the truth table for a half-adder and design its circuit implementation ***using only EX-OR and NAND gates***. The details of the ICs giving the EX-OR and NAND functions (7486 and 7400, respectively) are as shown. Draw a neat circuit diagram (a functional diagram showing gates). Indicate the pin numbers against all the input and output connections of the gates in the circuit. This is very important and will save time while wiring the circuit and also during debugging (in case it does not work as per the specifications).

Experiment

(i) Wire the designed half-adder circuit. Use two of the data switches as the inputs.

(ii) Using the LP, test the SUM and CARRY outputs for various combinations of the input. Verify that your half-adder circuit is working properly.



7400 Quad NAND

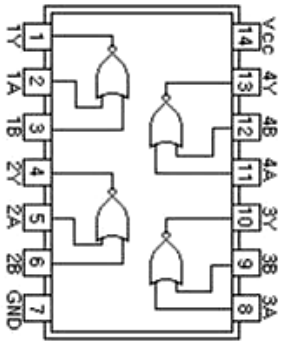
4. Realization of the CARRY function of a Full Adder

Write the truth table for a full-adder CARRY function and design its circuit implementation ***using only NAND and NOR gates***. Draw a neat functional circuit diagram with the pin numbers.

Experiment

(i) Wire the designed CARRY function of the full-adder circuit. Use three of the data switches as the inputs.

(ii) Using the LP, test the CARRY output for various combinations of the input. Verify that CARRY function is working properly.



7402 Quad NOR

5. Realization of 3-bit decoders

Design three 3-bit decoders capable of decoding the following 3-bit words (CBA) using only NAND and NOR functions (ICs 7400 and 7402). In each circuit, the decoder should give logical '1' output only for the specified input word.

(i) 111 (ii) 101 (iii) 001

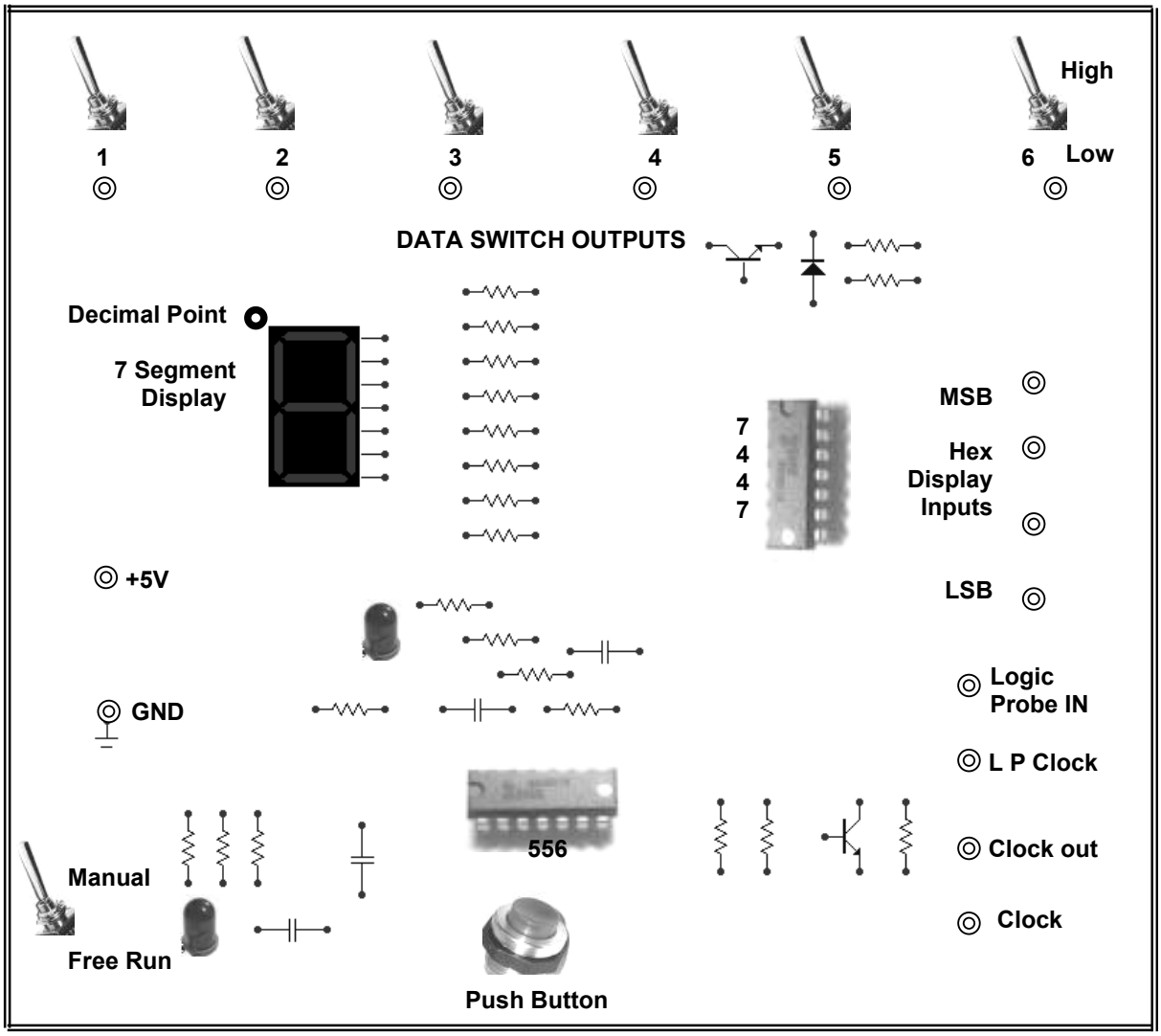
Write the truth table for the above decoder circuits. Draw neat functional circuit diagrams of the three decoder circuits with pin numbers.

Experiment

(i) Wire the designed decoder circuits and test them one by one using the

(ii) LP and three data switches. Choose the extreme left switch as be the MSB.

DIGITAL TEST BOARD



Description:

Data Switches (1,2,3,3,4,5,6)	For use as DATA inputs to Digital Circuits
Logic Probe IN	Logic '0': Green LED is OFF; Logic '1' Green LED is ON; Open (neither '1' nor '0'): Green LED flickers
LP Clock	Clock used in the Logic Probe circuit (556 IC output)
Clock OUT	Normal TTL Clock output
Clock	Complement of Clock output
Push Button	For Manual Clock; Generates one Clock pulse per push
Manual/Free Run	Switch to select either 'Manual Clock' or 'Free-Running Clock'
Hex Inputs	4 inputs for the 7-segment Decoder
7 Segment Display	7-segment LED display with a decimal point. Decimal point is

	ON for Hex inputs 1000 and above.

Half Adder

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Full Adder

A	B	C_i	S	C_o
0	0	0	0	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	1	1	1

$$C_0 = A \cdot B \cdot \overline{C_i} + \overline{A} \cdot B \cdot C_i + A \cdot \overline{B} \cdot C_i + A \cdot B \cdot C_i$$
$$C_0 = A \cdot B + C_i \cdot (A + B)$$
$$C_0 = \overline{\overline{C_0}} = \overline{\{A \cdot B\} \cdot \{C_i \cdot (A + B)\}}$$