Experiment 3
Time and Frequency Response of RC and RL Circuits

Introduction

Step response (or time response) of RC and RL circuits is of great importance in the design of pulse (or digital) circuits. The aim of this experiment is to study the time response of RC and RL circuits. In order to get the time response, square-wave signals are applied to the input of these circuits, and the output measured as a function of frequency. The results obtained are then compared with the theory.

A RC Circuits

1.1 RC Integrator Circuit

Wire the circuit of Fig.1. Connect signal from the OUTPUT socket of the FG to the RC circuit, and also to the CH-1 input of the DSO. Choose square wave signal and adjust the amplitude control to obtain a waveform going from −5 V to +5 V. Connect the output of the RC circuit to CH-2 input of the CRO. Be sure to choose the ***DC*** mode for both CH-1and CH-2 inputs so as to observe the dc levels of the signals. Use DSO to set the frequency of FG.

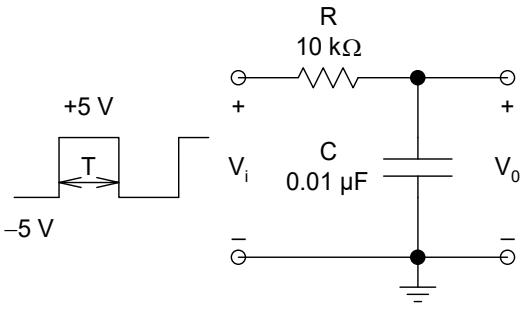

Figure 1 RC Integrator Circuit

(i) ***Time response when T << τ*** : Choose the waveform frequency (f) to be ***25 kHz***. Observe and sketch V_i and V_0 with respect to time. Note down the salient features of V_0.

(ii) ***Time response when T ≈ τ*** : Choose f to be ***5 kHz***. Observe and sketch V_i and V_0 with respect to time. Note down the salient features of V_0. Choose any two convenient points on the rising and falling parts of V_0 and measure the corresponding voltages and the time intervals. From these readings, obtain the time constant τ of the circuit. Compare the result with that obtained using the values of the components (R and C) used in the circuit.

(iii) ***Time response when T >> τ*** : Choose f = ***500 Hz***. Observe and sketch V_i and V_0.

1.2 RC Differentiator Circuit

Wire the circuit of Fig.2. As in the case of the RC integrator circuit, obtain time response of this circuit for the following three cases. Sketch V_i and V_0 for each case.

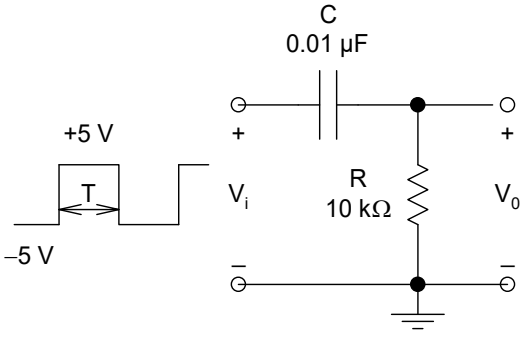

Figure 2 RC Differentiator Circuit

(i) ***Step response when T << τ*** (use f = ***25 kHz***).
(ii) ***Step response when T ≈ τ*** (use f = ***5 kHz***).
(iii) ***Step response when T >> τ*** (use f = ***500 Hz***).
(iv) Increase the input signal frequency beyond 40 kHz and note the minimum frequency at which the linear tilt (droop) seen in the V_0 waveform is negligible.

B RL Circuits

2.1 RL Integrator Circuit

Wire the circuit of Fig.3. Connect signal from the OUTPUT socket of the FG to the RL circuit, and also to the CH-1 input of the DSO. Choose square wave signal and adjust the amplitude control to obtain a waveform going from −1 V to +1 V. Connect the output of the RL circuit to CH-2 input of the DSO. Be sure to choose the ***DC*** mode for both CH-1 and CH-2 inputs so as to observe the dc levels of the signals.

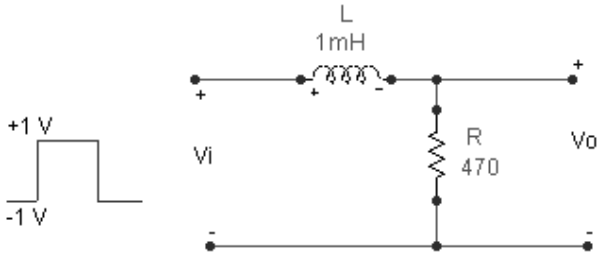

Figure 3 RL Integrator Circuit

(i) Choose the following waveform frequencies (f): ***10 kHz, 40 kHz and 100 kHz***. In each case observe and sketch V_i and V_0 with respect to time. Note down the salient features of V_0.
(ii) Choose a convenient frequency, say ***f = 40 kHz***. Observe and sketch V_i and V_0 with respect to time. Choose any two convenient points on the rising and falling parts of V_0 and measure the corresponding voltages and the time intervals. From these readings, obtain the time constant τ of the circuit and estimate the value of L. Compare the result with that obtained using the values of the components (R and L) used in the circuit.

2.2 RL Differentiator Circuit

Wire the circuit of Fig.4. As in the case of the RL integrator circuit, obtain the time response of this circuit for the

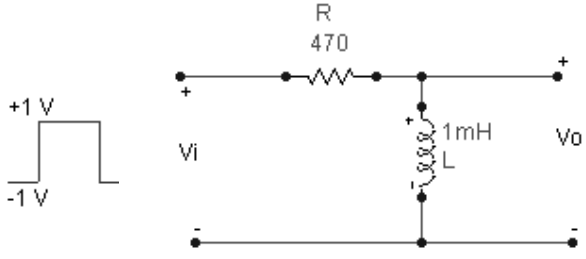

Figure 4 RL Differentiator Circuit

following three frequencies: ***10 kHz, 40 kHz and 100 kHz***. In each case sketch V_i and V_0 with respect to time. Note down the salient features of V_0.

C Frequency Response

1. Connect up the circuit in Fig.5(a) (this is also called an *RC lowpass filter*).
2. Set up the scope to display on both channels and connect the points indicated in Fig.1(a) to the respective channels.
3. Apply a sine wave from the MAIN output of the FG to the input point of the circuit. Ensure that input coupling mode for both channels is ac (both ac/dc coupling buttons pressed OUT). Let the sine wave be 2V p-p with zero dc offset.
4. **At frequencies of 200Hz, 500Hz, 1kHz, 2kHz, 5kHz, 10kHz, 20kHz, 50kHz, 100kHz, 200kHz, note the amplitudes of v_o and v_i. In the range 1kHz to 2kHz, take readings every 100Hz.**
5. **Calculate the phase angle between v_o and v_i using the cursors in the DSO to measure the time difference between two corresponding zero crossings on v_o and v_i. if this is T' and the period is T, then the phase difference (positive or negative) is given (in deg.)by 360T'/T.**
6. From the table of amplitudes and phase readings obtained from 4, 5 above, **plot the logarithmic gain A_V = 20 log[v_o/v_i] and the phase θ against frequency on semilog graph paper.**
7. **Repeat the above steps. for the *RL* circuit in Fig.1(b). Now take readings of amplitude and phase at 2kHz, 5kHz, 10kHz, 20kHz, 50kHz, 100kHz, 200kHz, 500kHz.**

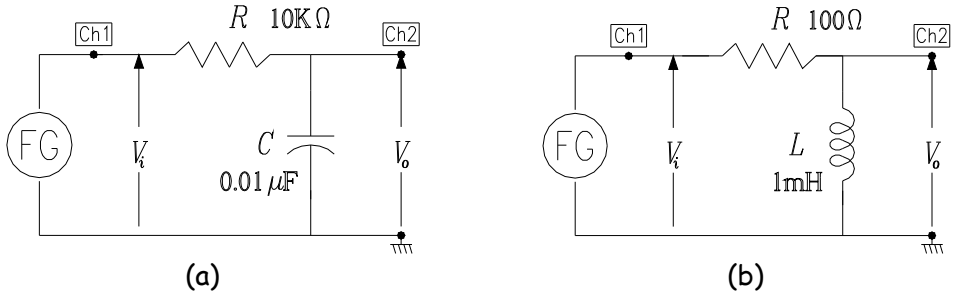

Fig.5

8. For each of the above frequency settings, also display v_o *vs* v_i in X-Y mode. You will need to first ground the two inputs, set the scope in X-Y mode, *center the dot on the screen*, and then reintroduce the channel inputs for this. You should see a figure such as shown in

Fig.6. Look at the phase as calculated in the previous steps and the appearance of the X-Y diagram (called a Lissajous diagram) and understand how the phase angle between the input and output affects the shape of the Lissajous diagram.

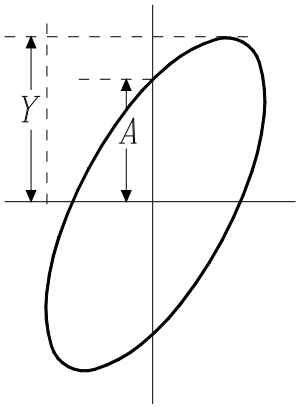

Fig.6