Experiment 10
Sequential Circuits

Introduction to Counters

The aim of this experiment is to familiarize you, first with the basic sequential circuit device called a flip flop, and then, with the design and implementation of simple synchronous and ripple counters. Counters are combinations of flip flops and some gates to achieve desired sequential behavior.

Some Concepts and Terminology

A basic JK flip flop has 2 binary inputs J and K, a clock terminal Clk, and 2 binary complementary outputs Q and Q` (Some more advanced flip flops, such as the ones in the CD 4027 may additionally have SET and RESET terminals). Since the second output Q' depends entirely upon (being complementary to) the first output Q, we need consider only Q in the discussion, The 'state' of a single flip flop at time *n* is simply the value of its output Q_n at time *n*. When the inputs are given, and a clock edge is applied to the Clk, terminal, the flip flop makes a transition to another state, The behavior of a flip flop is described using a truth table, which lists the outputs corresponding to each set of inputs. Also very useful is an *excitation table*, that essentially does the reverse, lists the inputs that need to be applied to make desired state transitions. The first thing you need to learn how to obtain the excitation table from the truth table.

A counter is simply an ordered interconnection of many flip flops. The 'state' of a counter is defined simply as the ordered sequence of the states of the respective outputs of the individual flip flops that constitute it. To interconnect them, the inputs of the next flip flop are derived as a combination of other signals available in the circuit, using the gates. For a certain specified sequence of counter states, we need to manipulate the inputs of the individual flip flops in order to force them to make the desired transitions at specific times.

There are two broad categories in counters. In a *synchronous* counter, the master clock signal is connected in parallel to the Clk inputs of all the flip-flops. Hence, all the outputs change simultaneously as well, or, in other words, they are synchronous with respect to the (master) clock. These counters can achieve very high speeds of operation. However, the design of these counters is, in general, difficult and time consuming, as each counter has to be carefully designed for the specified sequence of states. The other class of counters, the *ripple* counters, are made by just cascading flip-flops, where the master clock is connected only to the first flip-flop, with the output of the first flip-flop being used as the clock for the second flip-flop, and so on. These counters are also called asynchronous counters (or ripple counters) as the outputs of the flip-flops change at different times with respect to the master clock. These types of counters are easy to design, but cannot be used at higher clock speeds.

ICs USED

CD 4027 – CMOS Dual Positive-Edge Triggered JK Flip-Flops
CD 4023 – CMOS Triple 3-Input NAND Gates

Familiarize yourself with the above ICs. See the attached sheet for details. Note that in a CMOS IC, the inputs have to be clearly defined; ***you cannot leave them open***. Voltages above 2.5 V are taken as logic ***1***, and voltages below 2.5 V are taken as logic ***0***. For wiring purposes, use V_{DD} (or V_{CC}: +5 V) as logic ***1***, and GND as logic ***0***. Note that the CD4027 IC is positive-edge triggered and has two JK flip-flops. Take special note of the S_D (***SET***) and C_D (***CLEAR***) inputs. These are ***active HIGH asynchronous*** SET and CLEAR (or ***RESET***) inputs, respectively. **For normal JK flip-flop operation, these inputs must be kept at logic *0*.**

Lab Preparation

For each of the counters specified below, you have to implement the circuits for the specified sequence of states. Use the JK ***transition table*** (or ***excitation table***, which gives the required J and K inputs for a given transition from state Q_n to state Q_{n+1}) for the design. For each part of this experiment, you ***MUST*** have in your lab report. A clear circuit diagram (as well as a functional diagram) of your counter indicating all the inputs with the appropriate pin numbers.

Experiment

For each of the following parts, you need to verify that the sequence of states produced by your designed circuit for each counter follows the specification. You have to wire your circuits in the microboard and connect the outputs to the HEX display unit inputs of the digital test board, putting any of the unused inputs of the HEX display unit to ***0***. Also, use manual clock. With each application of the manual clock, the counter circuit should go through the specified sequence of states.

Useful tips:

i. A ripple counter that uses positive-edge triggered JK flip-flops with Q outputs connected as the clock inputs for the following stages will result in a ***down*** counter, while $\overline{Q}$ outputs so connected will give an ***up*** counter. Reverse will be the case when negative-edge triggered JK flip-flops are used.
ii. You should not leave the S_D and C_D inputs of the JK flip-flops unconnected.

1. Verify Basic Flip Flop operation:

On the microboard, connect up the inputs and outputs of a single JK flip flop from the CD 4027. Use the truth table of the flip flop to verify the operation, by providing different input values for J, K, S_D, C_D, and triggering using the manual clock key from the digital logic board. Data for this is given in the function tables for the CD 4027 (last page). Make the excitation table, and tabulate the results.

2. Divide-by-8 Ripple Down Counter (3 FFs)

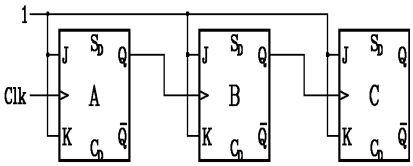
Design and verify a ÷8 ripple down counter with the sequence of states (CBA): ***111***, ***110***, ***101***, ***100***, ***011***, ***010***, ***001***, ***000***, ***111***, ***110***, … , etc., using three JK flip-flops of IC CD4027.

3. Divide-by-8 Ripple Up Counter (3 FFs)

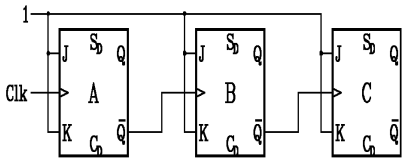
Design and verify a ÷8 ripple up counter with the sequence of states (CBA): ***000***, ***001***, ***010***, ***011***, ***100***, ***101***, ***110***, ***111***, ***000***, ***001***, … , etc., using three JK flip-flops of IC CD4027.

	Q_C	Q_B	Q_A
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

	Q_C	Q_B	Q_A
0	1	1	1
1	1	1	0
2	1	0	1
3	1	0	0
4	0	1	1
5	0	1	0
6	0	0	1
7	0	0	0



Div. by 8 Ripple Down Counter



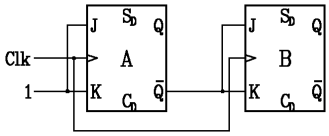
Div. by 8 Ripple Up Counter

4. **Divide-by-4 Synchronous Down Counter (2FFa)**

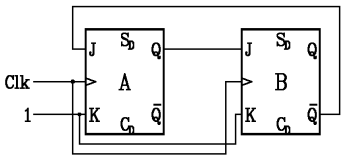
This is a synchronous counter that goes through all possible states. Hence it requires no careful design, unlike the next one. It has the sequence of states (BA): ***11***, ***10***, ***01***, ***00***, ***11***, ***10***, … , etc., using two JK flip-flops of IC CD4027.

5. **Divide-by-3 Synchronous Up Counter (2 FFs)**

This synchronous up counter is designed to skip one of its 4 states so that we get the sequence of states (BA): ***00***, ***01***, ***10***, ***00***, ***01***, … , etc., using two JK flip-flops of IC CD4027. Here is a sample Design Table.



Div. by 4 Sync. Down Counter

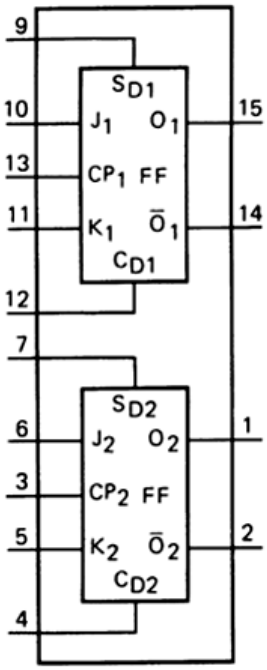


Div. by 3 Sync. Up counter and its Excitation Table

Present State		Next State		Required JK Excitations			
				FF B		FF A	
B_n	A_n	B_{n+1}	A_{n+1}	J_B	K_B	J_A	K_A
0	0	0	1	0	x	1	x
0	1	1	0	1	x	x	1
1	0	0	0	x	1	0	x
Unused State							
1	1	0	0	x	1	x	1

$J_B = Q_A \;;K_B = 1 \qquad J_A = \overline{Q}_B \;;\; K_A = 1$

FUNCTION TABLES OF CD 4027



INPUTS					OUTPUTS	
S_D	C_D	CP	J	K	Q	$\overline{Q}$
H	L	X	X	X	H	L
L	H	X	X	X	L	H
H	H	X	X	X	H	H

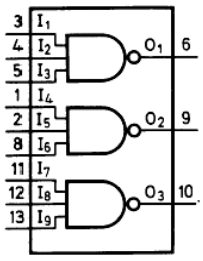
INPUTS					OUTPUTS	
S_D	C_D	CP	J	K	Q_{n+1}	$\overline{Q}_{n+1}$
L	L	↑	L	L	Q_n	$\overline{Q}_n$
L	L	↑	H	L	H	L
L	L	↑	L	H	L	H
L	L	↑	H	H	$\overline{Q}_n$	Q_n

Notes

1. H = HIGH state (the more positive voltage)
   L = LOW state (the less positive voltage)
   X = state is immaterial
   ↑ = positive-going transition
   O_{n+1} = state after clock positive transition

PINNING

J,K	synchronous inputs
CP	clock input (L to H edge-triggered)
S_D	asynchronous set-direct input (active HIGH)
C_D	asynchronous clear-direct input (active HIGH)
O	true output
$\overline{O}$	complement output



CD 4027
V_{DD}(V_{CC}) : 5V, Pin 16
GND : Pin 8

CD 4023
V_{DD}(V_{CC}) : 5V, Pin 14
GND : Pin 7