



MERL

Accelerating Engineering Innovation

DESIGN
MICROPROCESSOR
SIMPLER,
FASTER,
CHEAPER



File Edit view Go Run Terminal Help

Welcom - Suite

- □ X

Verify RTL

Upload bit stream

Upload

Export CSV

Generate report

Generate log

Generate RTL



EXPLORER

...

Get Started X





▼ FolderName

Filename1



Start

Open File

Open Folder

New File



Recents

Filename3

Filename2

Filename

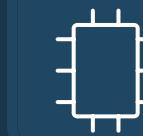
More...



Select Your Project



Custom Config Soc



Custom Config Core



Customize Core

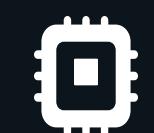


Verification

TODO

Problem

Terminal



>Select Extension

- M
- F
- C
- I

>Select ISA

- 32
- 64

>Select Devices

- Gpio
- SPI
- SPI-FLASH
- UART
- I2C
- TIMER

>Select Bus Interconnects

- TL-UL
- TL-C
- Wishbone

back

FINALIZE
SoC

Verify RTL

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EXPLORER

...

Filename1 X

Chisel code X



...

▼ FolderName

- File icon Filename1

```
5
6  import caravan.bus.tilelink.{TLRequest, TLResponse, TilelinkConfig, TilelinkDevice, TilelinkError, TilelinkHost}
7  import chisel3.experimental.Analog
8  import chisel3.stage.ChiselStage
9  import jigsaw.fpga.boards.artyA7._
10 import jigsaw.rams.fpga.BlockRam
11 import jigsaw.peripherals.gpio._
12 // import jigsaw.peripherals.spiflash._

13
14 class Picofoxy(programFile: Option[String]) extends Module {
15   val io = IO(new Bundle {
16     val gpio_io = Vec(16, Analog(1.W))
17   })
18
19   val top = Module(new Top(programFile))
20   val pll = Module(new PLL_8MHz())
21
22   pll.io.clk_in1 := clock
23   top.clock := pll.io.clk_out1
24
25   val gpioInputWires = Wire(Vec(16, Bool()))
26   val gpioOutputWires = Wire(Vec(16, Bool()))
27   val gpioEnableWires = Wire(Vec(16, Bool()))
```



PROBLEMS OUTPUT TERMINAL DEBUG CONSOLE

✖ power shell + ⌫ v X

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EXPLORER



▼ FolderName

- Filename1
- Filename1
- Filename1
- Filename1
- Filename1
- Filename1

```
Filename1 X generated RTL X
5   output [3:0] io_tlMasterTransmitter_bits_a_mask,
6   output [31:0] io_tlMasterTransmitter_bits_a_data,
7   input      io_tlSlaveReceiver_valid,
8   input [31:0] io_tlSlaveReceiver_bits_d_data,
9   input      io_reqIn_valid,
10  input [31:0] io_reqIn_bits_addrRequest,
11  input [31:0] io_reqIn_bits_dataRequest,
12  input [3:0]  io_reqIn_bits_activeByteLane,
13  input      io_reqIn_bits_isWrite,
14  output     io_rspOut_valid,
15  output [31:0] io_rspOut_bits_dataResponse
16 );
17 wire _io_tlMasterTransmitter_bits_a_opcode_T_1 = io_reqIn_bits_activeByteLane == 4'hf ? 1'h0 : 1'h1; // @[TilelinkHost.scala 49:38]
18 assign io_tlMasterTransmitter_valid = io_reqIn_valid; // @[TilelinkHost.scala 49:38]
19 assign io_tlMasterTransmitter_bits_a_opcode = io_reqIn_bits_isWrite ? {{2'd0},
20   _io_tlMasterTransmitter_bits_a_opcode_T_1} : 3'h4; // @[TilelinkHost.scala 36:70]
21 assign io_tlMasterTransmitter_bits_a_address = io_reqIn_bits_addrRequest; // @[TilelinkHost.scala 38:47]
22 assign io_tlMasterTransmitter_bits_a_mask = io_reqIn_bits_activeByteLane; // @[TilelinkHost.scala 47:44]
23 assign io_tlMasterTransmitter_bits_a_data = io_reqIn_bits_dataRequest; // @[TilelinkHost.scala 37:44]
24 assign io_rspOut_valid = io_tlSlaveReceiver_valid; // @[TilelinkHost.scala 88:21]
25 assign io_rspOut_bits_dataResponse = io_tlSlaveReceiver_bits_d_data; // @[TilelinkHost.scala 85:33]
26 endmodule
27 module stallUnit(
28   input  [31:0] in_bundle_in_d_data
```



PROBLEMS OUTPUT TERMINAL

Σ power shell + ⌂ v X

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EXPLORER

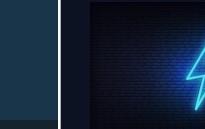


Filename1 X

Filename2 X



▼ FolderName



Verify RTL



- File icon Filename1

Select Test Cases

select your test case ▾

- test case1
- test case1
- test case1
- Select all
- customize



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RUN TEST CASES >

≡ TODO

⚠ Problem

hell + ⚡ v X

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EXPLORER

...

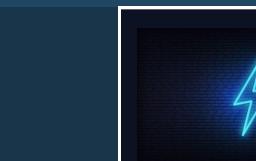
Filename1 X

Filename2 X

...

▼ FolderName

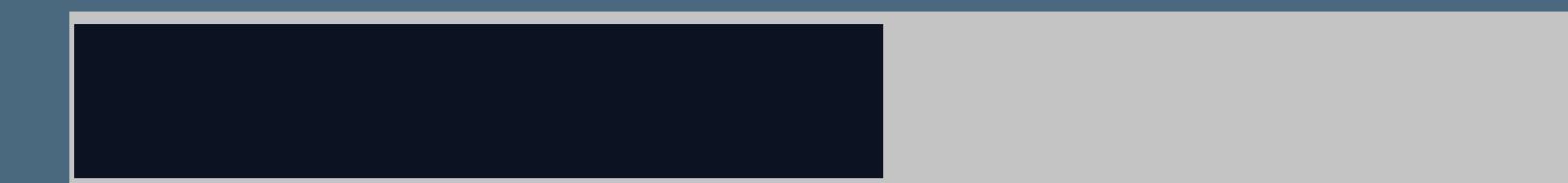
- File Name1



Verify RTL

-

Running Your Test Case



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NEXT >

PROBLEMS OUTPUT TERMINAL DEBUG CONSOLE

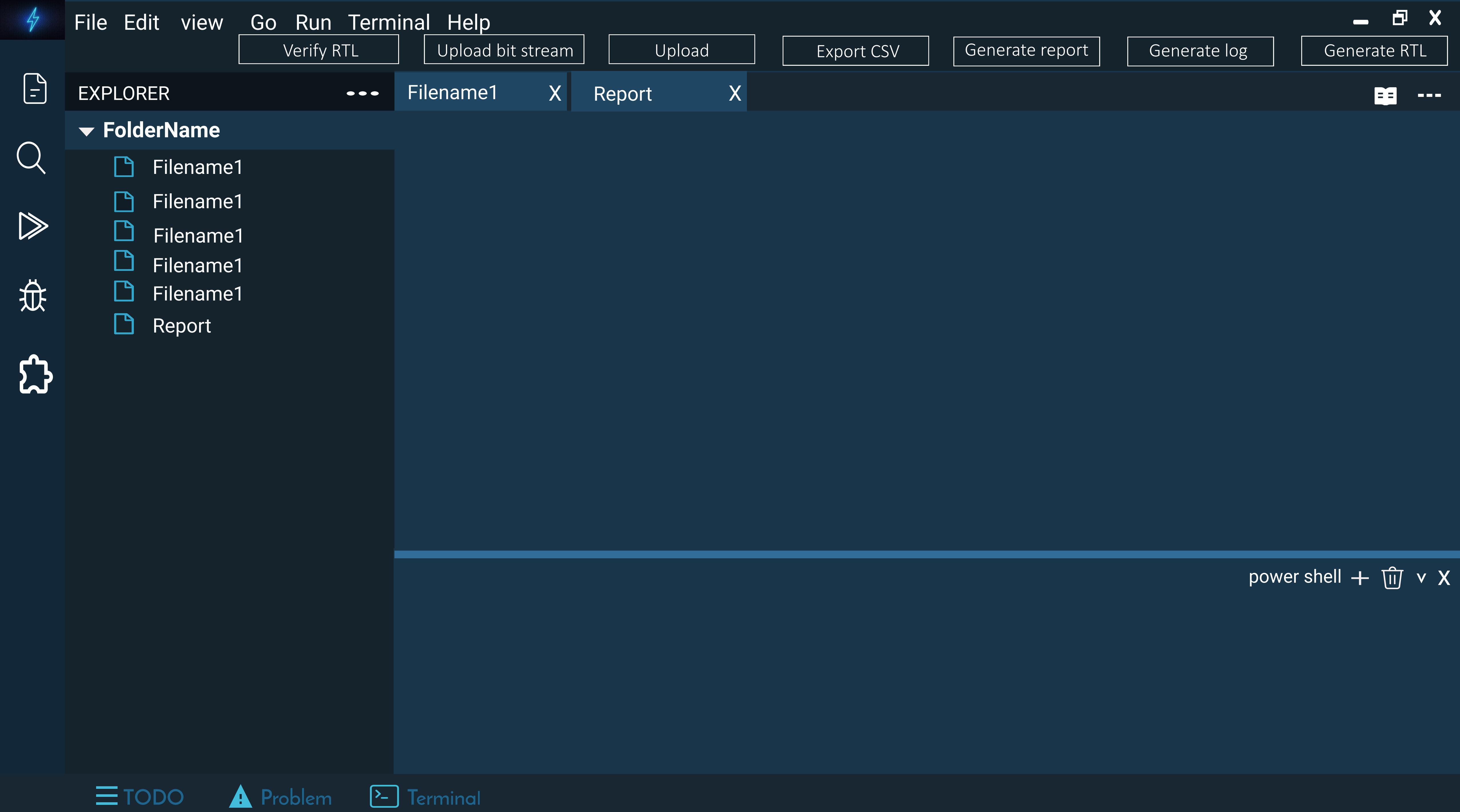
power shell + v X

show output here

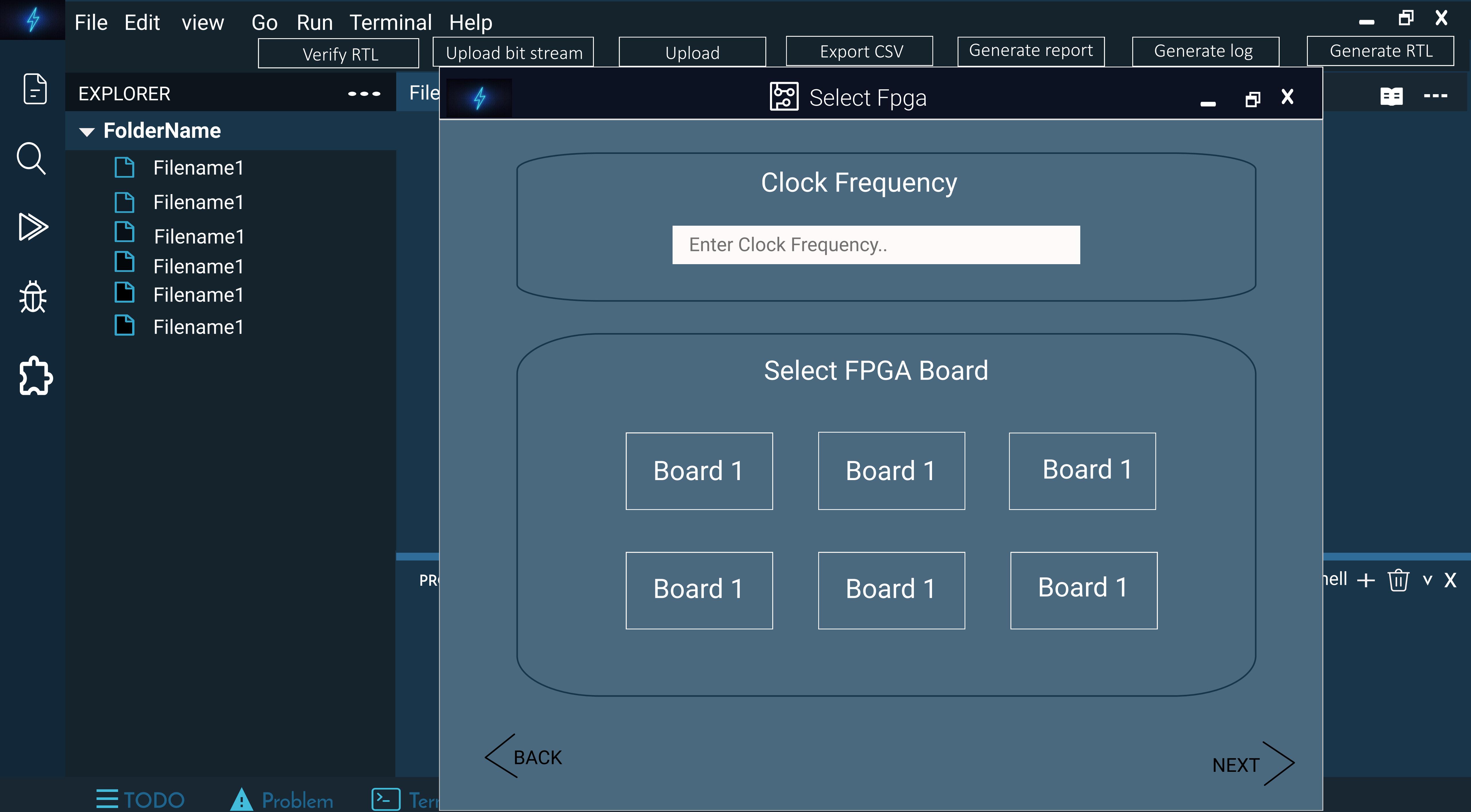
TODO

Problem

Terminal

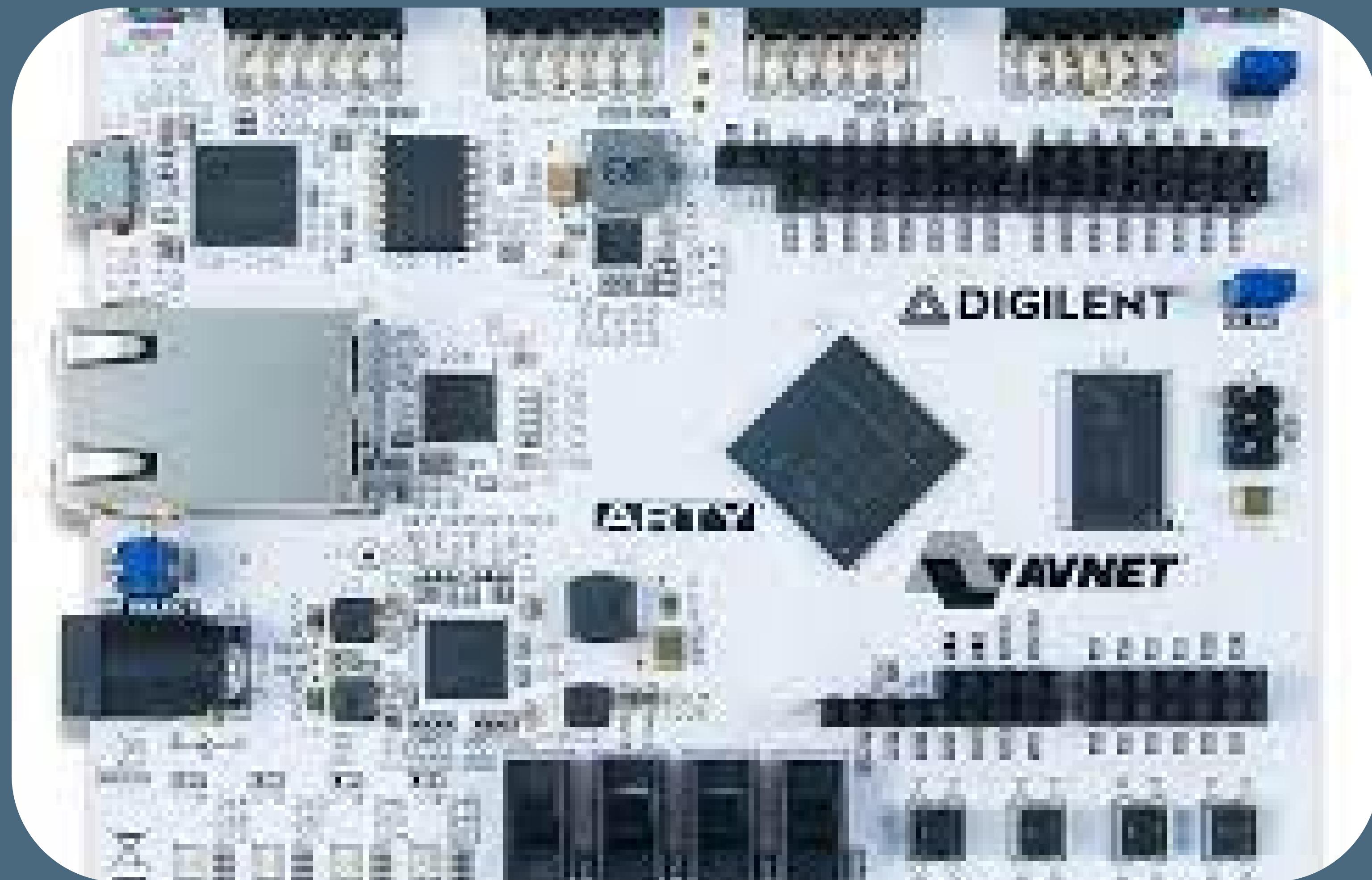


EXPLORER	...	Filename1	X	Generate Log	X	...	-	...	X	...
▼ FolderName		1	#1 0 80000000 595552b7 r 05	59555000	lui	x5, 0x59555				
		2	#2 0 80000004 55528293 r 05	59555555	addi	x5, x5, 0x555				
		3	#3 0 80000008 7c029073 c 07c0	59555555	csrrw	x0, mrac, x5				
		4	#4 0 8000000c 70041117 r 02	f004100c	auipc	x2, 0x70041				
		5	#5 0 80000010 02410113 r 02	f0041030	addi	x2, x2, 0x24				
		6	#6 0 80000014 032000ef r 01	80000018	jal	x1, . + 0x32				
		7	#7 0 80000046 7139 r 02	f0040ff0	c.addi16sp -0x4					
		8	#8 0 80000048 de22 m f004102c	00000000	c.swsp	x8, 0x3c				
		9	#9 0 8000004a 0080 r 08	f0041030	c.addi4spn	x8, 0x10				
		10	#10 0 8000004c f00407b7 r 0f	f0040000	lui	x15, -0xffff0				
		11	#11 0 80000050 00078793 r 0f	f0040000	addi	x15, x15, 0x0				
		12	#12 0 80000054 438c r 0b	0000000b	c.lw	x11, 0x0(x15)				
		13	#13 0 80000056 43d0 r 0c	0000001d	c.lw	x12, 0x4(x15)				
		14	#14 0 80000058 4794 r 0d	00000053	c.lw	x13, 0x8(x15)				
		15	#15 0 8000005a 47d8 r 0e	0000006d	c.lw	x14, 0xc(x15)				
		16	#16 0 8000005c 4b9c r 0f	00000009	c.lw	x15, 0x10(x15)				
		17	#17 0 8000005e fcb42a23 m f0041004	0000000b	sw	x11, -0x2c(x8)				
		18	#18 0 80000062 fcc42c23 m f0041008	0000001d	sw	x12, -0x28(x8)				
		19	#19 0 80000066 fcd42e23 m f004100c	00000053	sw	x13, -0x24(x8)				
		20	#20 0 8000006a fee42023 m f0041010	0000006d	sw	x14, -0x20(x8)				
		21	#21 0 8000006e fef42223 m f0041014	00000009	sw	x15, -0x1c(x8)				
		22	#22 0 80000072 f00407b7 r 0f	f0040000	lui	x15, -0xffff0				
		23	#23 0 80000076 01478793 r 0f	f0040014	addi	x15, x15, 0x14				
		24	#24 0 8000007a 438c r 0b	00000059	c.lw	x11, 0x0(x15)				
		25	#25 0 8000007c 43d0 r 0c	0000003e	c.lw	x12, 0x4(x15)				
		26	#26 0 8000007e 4794 r 0d	00000049	c.lw	x13, 0x8(x15)				
		27	#27 0 80000080 47d8 r 0e	0000005a	c.lw	x14, 0xc(x15)				
		28	#28 0 80000082 4b9c r 0f	00000007	c.lw	x15, 0x10(x15)				
		29	#29 0 80000084 fcb42023 m f0040ff0	00000059	sw	x11, -0x40(x8)				
		30	#30 0 80000086 fcc42223 m f00410ff1	0000003a	sw	x12, -0x2c(x8)				





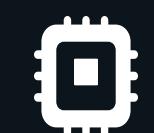
Mapped I\O



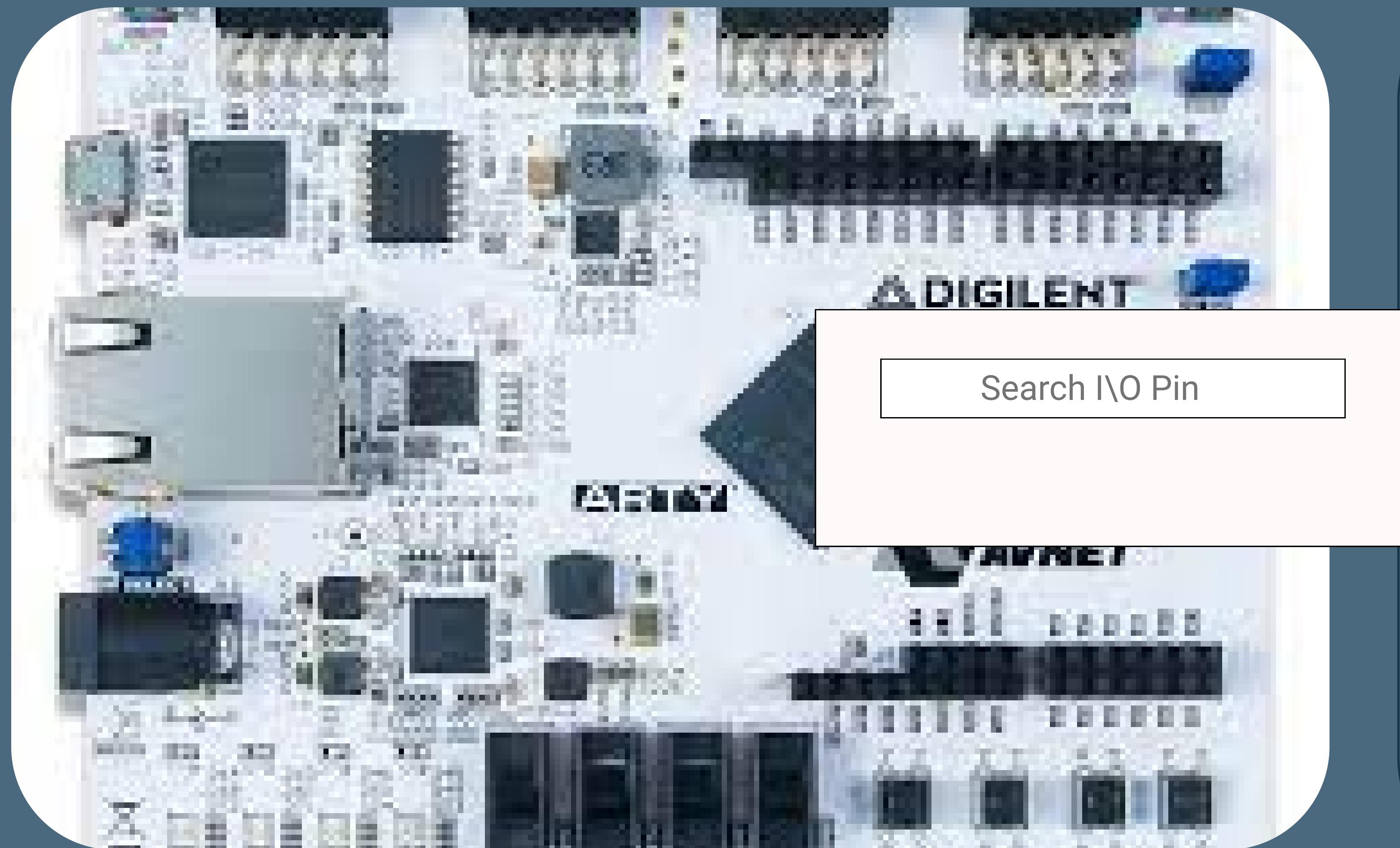
< BACK

MAPPED

NEXT >



Mapped I\O

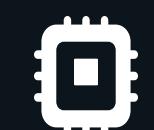


LED <--> I\O
LED <--> I\O
LED <--> I\O
LED <--> I\O

< BACK

MAPPED

NEXT >



Show Mapped I\O

< BACK

UPLOAD BIT STREAM >



Show connection

BACK

Write Code

Upload



Verify RTL

Upload bit stream

Export CSV

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Generate RTL



EXPLORER

...

Filename1 X

write test case X

▼ FolderName

- Filename1
- Filename1
- Filename1
- Filename1
- Filename1
- write test case



PROBLEMS OUTPUT TERMINAL DEBUG CONSOLE

power shell + v X

TODO

Problem

Terminal

Verify RTL

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EXPLORER

...

Filename1 X

Filename2 X



▼ FolderName

- File: Filename1

VERIFICATION - ⌂ X

Select Core

CORE ▾

CORE1
CORE2
CORE3
ADD CORE

Select ISS

ISS ▾

SPIKE
WHISPER
OVPSIM

NEXT >

PROBLEMS OUTPUT TERMINAL DEBUG CONSOLE

power shell + ⌂ v X

File Edit view Go Run Terminal Help

Verify RTL Upload bit stream Export CSV Upload Generate report Generate log Generate RTL

EXPLORER ... Filename1 X Filename2 X

FolderName

- Filename1
- Filename1
- Filename1
- Filename1
- Filename1
- Filename1

PROBLEMS

VERIFICATION

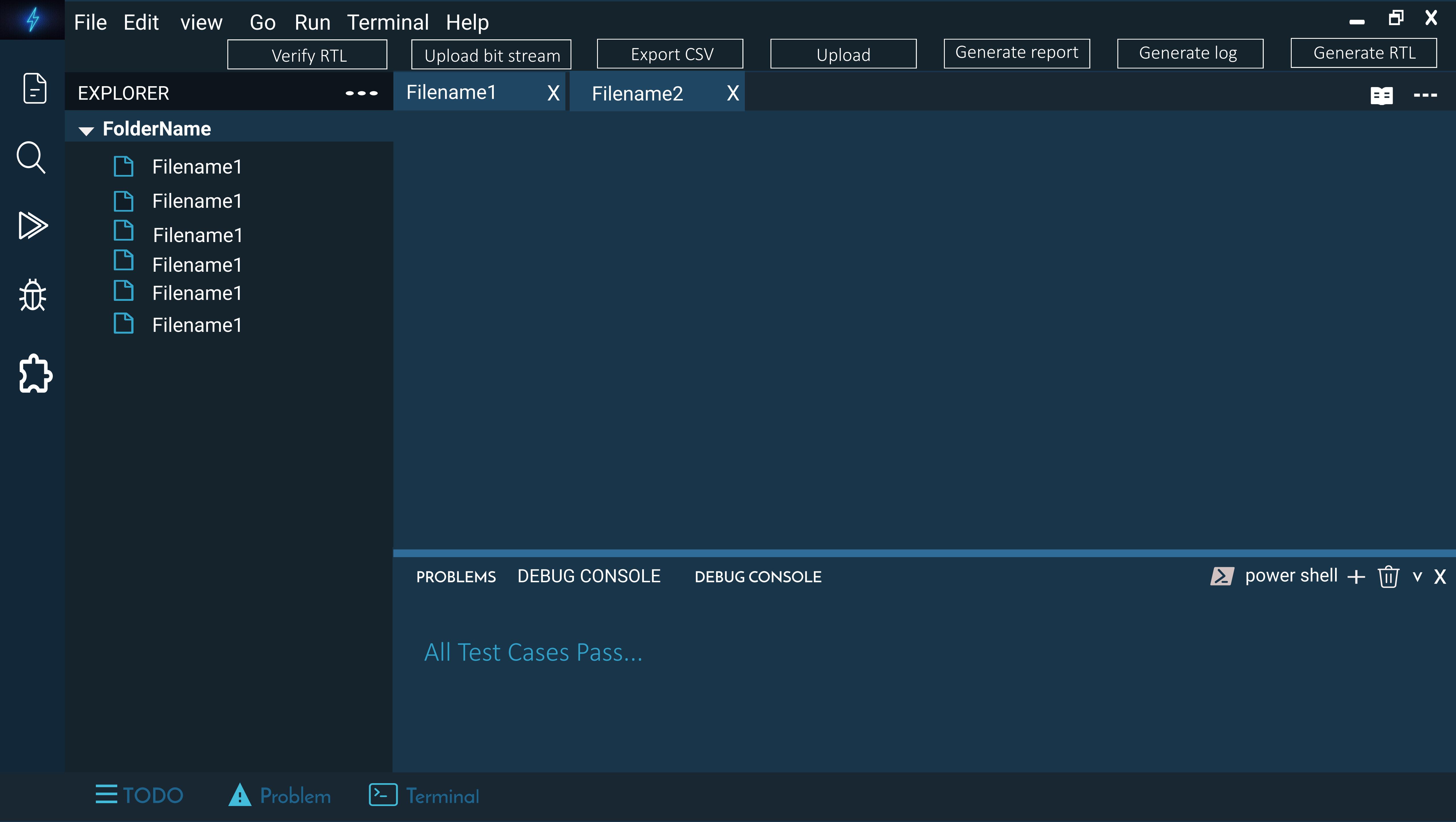
Select Test Case

- test case1
- test case2
- test case3
- test case4
- test case1
- test case2
- test case3
- test case4
- Select All
- Customize

BACK NEXT

power shell + ⚡ v X

TODO Problem Terminal



Verify RTL

Upload bit stream

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Generate RTL



3 Test Case Failed

an error occurred during processing Test case

the test case you are trying to run can not be run because
of the authenticity of the received data could not be verified

error line number 2,3 ,5,6 and 7

Try Again