



## 1. Description

### 1.1. Project

Project Name	stm32f1_ros_node
Board Name	custom
Generated with:	STM32CubeMX 6.3.0
Date	11/06/2021

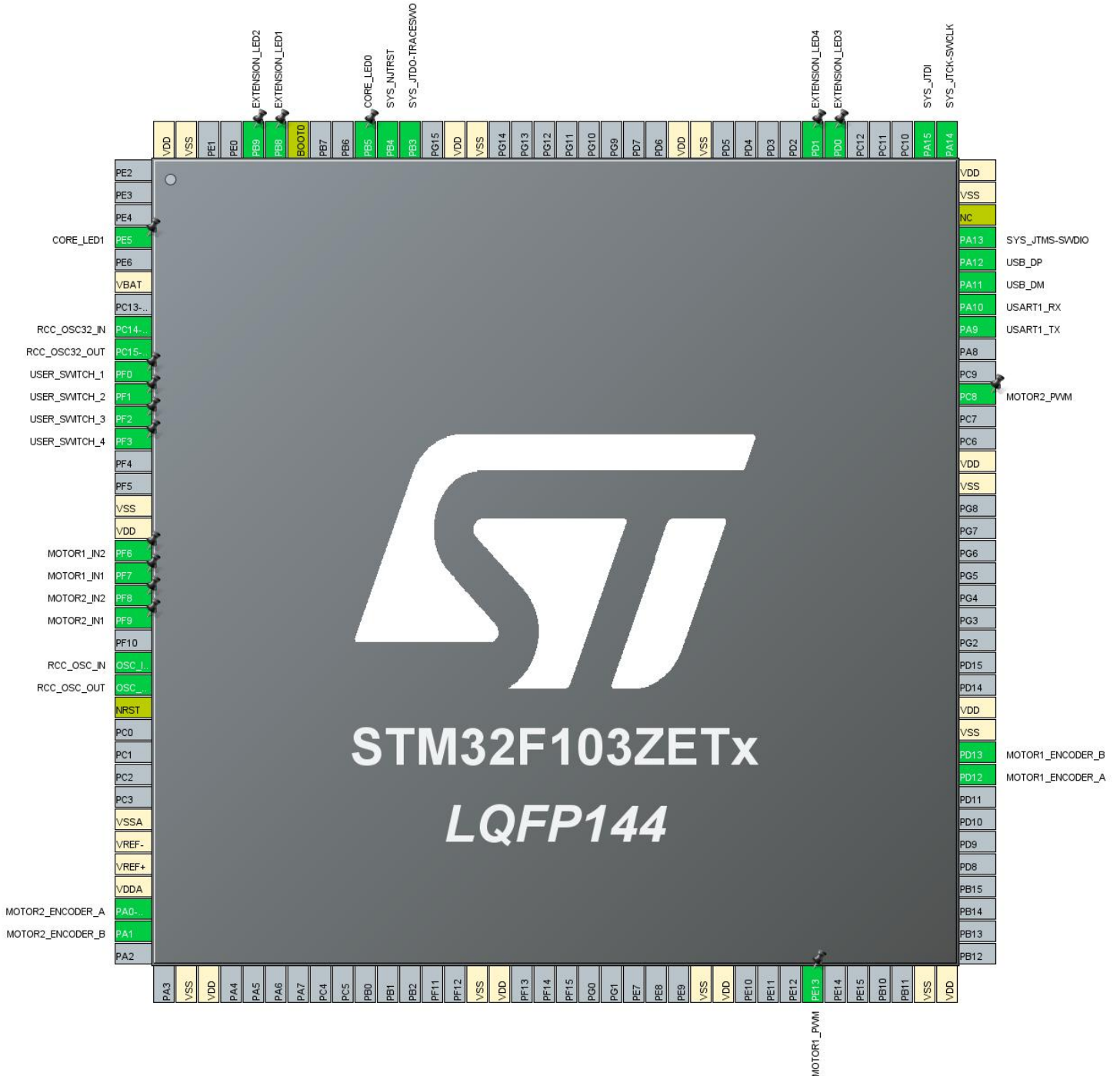
### 1.2. MCU

MCU Series	STM32F1
MCU Line	STM32F103
MCU name	STM32F103ZETx
MCU Package	LQFP144
MCU Pin number	144

### 1.3. Core(s) information

Core(s)	Arm Cortex-M3
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## 2. Pinout Configuration



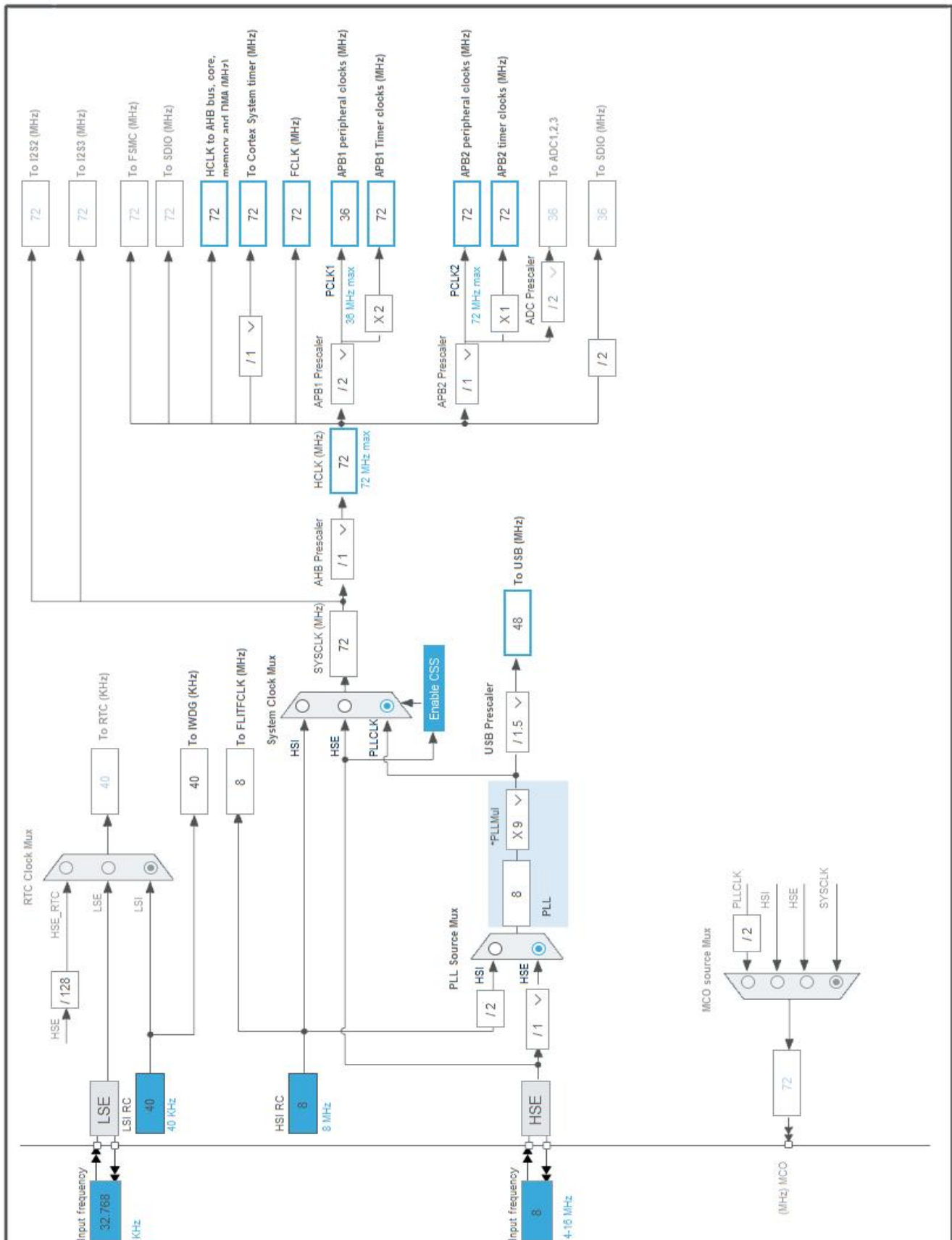
### 3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
4	PE5 *	I/O	GPIO_Output	CORE_LED1
6	VBAT	Power		
8	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
9	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
10	PF0 *	I/O	GPIO_Input	USER_SWITCH_1
11	PF1 *	I/O	GPIO_Input	USER_SWITCH_2
12	PF2 *	I/O	GPIO_Input	USER_SWITCH_3
13	PF3 *	I/O	GPIO_Input	USER_SWITCH_4
16	VSS	Power		
17	VDD	Power		
18	PF6 *	I/O	GPIO_Output	MOTOR1_IN2
19	PF7 *	I/O	GPIO_Output	MOTOR1_IN1
20	PF8 *	I/O	GPIO_Output	MOTOR2_IN2
21	PF9 *	I/O	GPIO_Output	MOTOR2_IN1
23	OSC_IN	MonolO	RCC_OSC_IN	
24	OSC_OUT	MonolO	RCC_OSC_OUT	
25	NRST	Reset		
30	VSSA	Power		
31	VREF-	Power		
32	VREF+	Power		
33	VDDA	Power		
34	PA0-WKUP	I/O	TIM5_CH1	MOTOR2_ENCODER_A
35	PA1	I/O	TIM5_CH2	MOTOR2_ENCODER_B
38	VSS	Power		
39	VDD	Power		
51	VSS	Power		
52	VDD	Power		
61	VSS	Power		
62	VDD	Power		
66	PE13	I/O	TIM1_CH3	MOTOR1_PWM
71	VSS	Power		
72	VDD	Power		
81	PD12	I/O	TIM4_CH1	MOTOR1_ENCODER_A
82	PD13	I/O	TIM4_CH2	MOTOR1_ENCODER_B
83	VSS	Power		
84	VDD	Power		

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
94	VSS	Power		
95	VDD	Power		
98	PC8	I/O	TIM3_CH3	MOTOR2_PWM
101	PA9	I/O	USART1_TX	
102	PA10	I/O	USART1_RX	
103	PA11	I/O	USB_DM	
104	PA12	I/O	USB_DP	
105	PA13	I/O	SYS_JTMS-SWDIO	
106	NC	NC		
107	VSS	Power		
108	VDD	Power		
109	PA14	I/O	SYS_JTCK-SWCLK	
110	PA15	I/O	SYS_JTDI	
114	PD0 *	I/O	GPIO_Output	EXTENSION_LED3
115	PD1 *	I/O	GPIO_Output	EXTENSION_LED4
120	VSS	Power		
121	VDD	Power		
130	VSS	Power		
131	VDD	Power		
133	PB3	I/O	SYS_JTDO-TRACESWO	
134	PB4	I/O	SYS_NJTRST	
135	PB5 *	I/O	GPIO_Output	CORE_LED0
138	BOOT0	Boot		
139	PB8 *	I/O	GPIO_Output	EXTENSION_LED1
140	PB9 *	I/O	GPIO_Output	EXTENSION_LED2
143	VSS	Power		
144	VDD	Power		

\* The pin is affected with an I/O function

## 4. Clock Tree Configuration



## 5. Software Project

### 5.1. Project Settings

Name	Value
Project Name	stm32f1_ros_node
Project Folder	D:\002-Work\001-PolyU-IC\002-Courses\IC382-2122-
Toolchain / IDE	MDK-ARM V5.32
Firmware Package Name and Version	STM32Cube FW_F1 V1.8.4
Application Structure	Advanced
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0x1000
Minimum Stack Size	0x800

### 5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

### 5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	SystemClock_Config	RCC
3	MX_DMA_Init	DMA
4	MX_USART1_UART_Init	USART1
5	MX_TIM1_Init	TIM1
6	MX_TIM3_Init	TIM3
7	MX_TIM4_Init	TIM4
8	MX_TIM5_Init	TIM5
9	MX_USB_DEVICE_Init	USB_DEVICE
10	MX_IWDG_Init	IWDG





## 6. Power Consumption Calculator report

### 6.1. Microcontroller Selection

Series	STM32F1
Line	STM32F103
MCU	STM32F103ZETx
Datasheet	DS5792_Rev12

### 6.2. Parameter Selection

Temperature	25
Vdd	3.3

### 6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

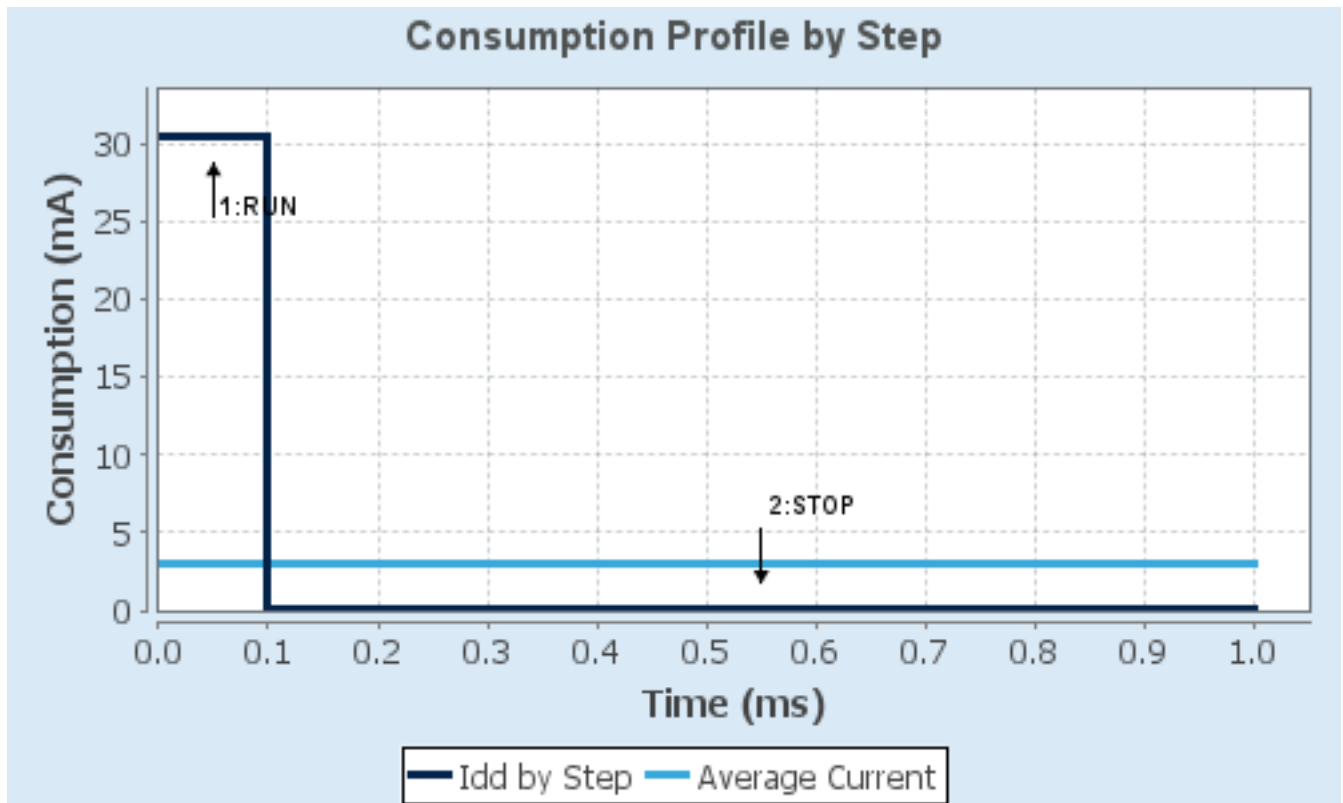
#### 6.4. Sequence

<b>Step</b>	Step1	Step2
<b>Mode</b>	RUN	STOP
<b>Vdd</b>	3.3	3.3
<b>Voltage Source</b>	Battery	Battery
<b>Range</b>	No Scale	No Scale
<b>Fetch Type</b>	FLASH	n/a
<b>CPU Frequency</b>	72 MHz	0 Hz
<b>Clock Configuration</b>	HSE PLL	Regulator LP
<b>Clock Source Frequency</b>	8 MHz	0 Hz
<b>Peripherals</b>		
<b>Additional Cons.</b>	0 mA	0 mA
<b>Average Current</b>	30.5 mA	25 $\mu$ A
<b>Duration</b>	0.1 ms	0.9 ms
<b>DMIPS</b>	90.0	0.0
<b>Ta Max</b>	101.98	105
<b>Category</b>	In DS Table	In DS Table

#### 6.5. Results

Sequence Time	1 ms	Average Current	3.07 mA
Battery Life	1 month, 15 days, 15 hours	Average DMIPS	61.0 DMIPS

#### 6.6. Chart



## 7. *Peripherals and Middlewares Configuration*

### 7.1. IWDG

**mode: Activated**

#### 7.1.1. Parameter Settings:

**Clocking:**

IWDG counter clock prescaler	<b>128 *</b>
IWDG down-counter reload value	4095

### 7.2. RCC

**High Speed Clock (HSE): Crystal/Ceramic Resonator**

**Low Speed Clock (LSE) : Crystal/Ceramic Resonator**

#### 7.2.1. Parameter Settings:

**System Parameters:**

VDD voltage (V)	3.3
Prefetch Buffer	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

**RCC Parameters:**

HSI Calibration Value	16
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

### 7.3. SYS

**Debug: JTAG (5 pins)**

**Timebase Source: SysTick**

### 7.4. TIM1

**Clock Source : Internal Clock**

**Channel3: PWM Generation CH3**

#### 7.4.1. Parameter Settings:

**Counter Settings:**

Prescaler (PSC - 16 bits value)	<b>20 *</b>
Counter Mode	Up

Counter Period (AutoReload Register - 16 bits value ) **3600 \***

Internal Clock Division (CKD) No Division

Repetition Counter (RCR - 8 bits value) 0

auto-reload preload Disable

#### Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection Reset (UG bit from TIMx\_EGR)

#### Break And Dead Time management - BRK Configuration:

BRK State Disable

BRK Polarity High

#### Break And Dead Time management - Output Configuration:

Automatic Output State Disable

Off State Selection for Run Mode (OSSR) Disable

Off State Selection for Idle Mode (OSSl) Disable

Lock Configuration Off

#### PWM Generation Channel 3:

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable

Fast Mode Disable

CH Polarity High

CH Idle State Reset

## 7.5. TIM3

**Clock Source : Internal Clock**

**Channel3: PWM Generation CH3**

### 7.5.1. Parameter Settings:

#### Counter Settings:

Prescaler (PSC - 16 bits value) **20 \***

Counter Mode Up

Counter Period (AutoReload Register - 16 bits value ) **3600 \***

Internal Clock Division (CKD) No Division

auto-reload preload Disable

#### Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection Reset (UG bit from TIMx\_EGR)

#### PWM Generation Channel 3:

Mode PWM mode 1

Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

## 7.6. TIM4

### Combined Channels: Encoder Mode

#### 7.6.1. Parameter Settings:

##### Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value )	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

##### Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

##### Encoder:

Encoder Mode

##### Encoder Mode TI1 and TI2 \*

\_\_\_\_ Parameters for Channel 1 \_\_\_\_

Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

\_\_\_\_ Parameters for Channel 2 \_\_\_\_

Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

## 7.7. TIM5

### Combined Channels: Encoder Mode

#### 7.7.1. Parameter Settings:

##### Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up

Counter Period (AutoReload Register - 16 bits value ) 65535

Internal Clock Division (CKD) No Division

auto-reload preload Disable

### Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection Reset (UG bit from TIMx\_EGR)

### Encoder:

Encoder Mode

### Encoder Mode TI1 and TI2 \*

\_\_\_\_ Parameters for Channel 1 \_\_\_\_

Polarity Rising Edge

IC Selection Direct

Prescaler Division Ratio No division

Input Filter 0

\_\_\_\_ Parameters for Channel 2 \_\_\_\_

Polarity Rising Edge

IC Selection Direct

Prescaler Division Ratio No division

Input Filter 0

## 7.8. USART1

### Mode: Asynchronous

#### 7.8.1. Parameter Settings:

#### Basic Parameters:

Baud Rate 115200

Word Length 8 Bits (including Parity)

Parity None

Stop Bits 1

#### Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples

## 7.9. USB

### mode: Device (FS)

#### 7.9.1. Parameter Settings:

#### Basic Parameters:

Speed Full Speed 12MBit/s

**Power Parameters:**

Low Power Disabled  
Link Power Management Disabled  
Battery Charging Disabled

## 7.10. USB\_DEVICE

### Class For FS IP: Communication Device Class (Virtual Port Com)

#### 7.10.1. Parameter Settings:

**Basic Parameters:**

USBD\_MAX\_NUM\_INTERFACES (Maximum number of supported interfaces) 1  
USBD\_MAX\_NUM\_CONFIGURATION (Maximum number of supported configuration) 1  
USBD\_MAX\_STR\_DESC\_SIZ (Maximum size for the string descriptors) 512  
USBD\_SELF\_POWERED (Enabled self power) Enabled  
USBD\_DEBUG\_LEVEL (USBD Debug Level) 0: No debug message

**Class Parameters:**

USB CDC Rx Buffer Size 1000  
USB CDC Tx Buffer Size 1000

#### 7.10.2. Device Descriptor:

**Device Descriptor:**

VID (Vendor Identifier) 1155  
LANGID\_STRING (Language Identifier) English(United States)  
MANUFACTURER\_STRING (Manufacturer Identifier) STMicroelectronics

**Device Descriptor FS:**

PID (Product Identifier) 22336  
PRODUCT\_STRING (Product Identifier) STM32 Virtual ComPort  
CONFIGURATION\_STRING (Configuration Identifier) CDC Config  
INTERFACE\_STRING (Interface Identifier) CDC Interface

\* User modified value



## 8. System Configuration

### 8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
	PA15	SYS_JTDI	n/a	n/a	n/a	
	PB3	SYS_JTDO-TRACESWO	n/a	n/a	n/a	
	PB4	SYS_NJTRST	n/a	n/a	n/a	
TIM1	PE13	TIM1_CH3	Alternate Function Push Pull	n/a	Low	MOTOR1_PWM
TIM3	PC8	TIM3_CH3	Alternate Function Push Pull	n/a	Low	MOTOR2_PWM
TIM4	PD12	TIM4_CH1	Input mode	No pull-up and no pull-down	n/a	MOTOR1_ENCODER_A
	PD13	TIM4_CH2	Input mode	No pull-up and no pull-down	n/a	MOTOR1_ENCODER_B
TIM5	PA0-WKUP	TIM5_CH1	Input mode	No pull-up and no pull-down	n/a	MOTOR2_ENCODER_A
	PA1	TIM5_CH2	Input mode	No pull-up and no pull-down	n/a	MOTOR2_ENCODER_B
USART1	PA9	USART1_TX	Alternate Function Push Pull	n/a	High *	
	PA10	USART1_RX	Input mode	No pull-up and no pull-down	n/a	
USB	PA11	USB_DM	n/a	n/a	n/a	
	PA12	USB_DP	n/a	n/a	n/a	
GPIO	PE5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CORE_LED1
	PF0	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	USER_SWITCH_1
	PF1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	USER_SWITCH_2
	PF2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	USER_SWITCH_3
	PF3	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	USER_SWITCH_4
	PF6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR1_IN2
	PF7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR1_IN1
	PF8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR2_IN2
	PF9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR2_IN1
	PD0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	EXTENSION_LED3
	PD1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	EXTENSION_LED4
	PB5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CORE_LED0

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PB8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	EXTENSION_LED1
	PB9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	EXTENSION_LED2

## 8.2. DMA configuration

DMA request	Stream	Direction	Priority
USART1_RX	DMA1_Channel5	Peripheral To Memory	<b>High *</b>
USART1_TX	DMA1_Channel4	Memory To Peripheral	<b>High *</b>

### USART1\_RX: DMA1\_Channel5 DMA request Settings:

Mode: **Circular \***  
Peripheral Increment: Disable  
Memory Increment: **Enable \***  
Peripheral Data Width: Byte  
Memory Data Width: Byte

### USART1\_TX: DMA1\_Channel4 DMA request Settings:

Mode: Normal  
Peripheral Increment: Disable  
Memory Increment: **Enable \***  
Peripheral Data Width: Byte  
Memory Data Width: Byte

### 8.3. NVIC configuration

#### 8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
DMA1 channel4 global interrupt	true	0	0
DMA1 channel5 global interrupt	true	0	0
USB low priority or CAN RX0 interrupts	true	0	0
USART1 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
USB high priority or CAN TX interrupts	unused		
TIM1 break interrupt	unused		
TIM1 update interrupt	unused		
TIM1 trigger and commutation interrupts	unused		
TIM1 capture compare interrupt	unused		
TIM3 global interrupt	unused		
TIM4 global interrupt	unused		
TIM5 global interrupt	unused		

#### 8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
DMA1 channel4 global interrupt	false	true	true
DMA1 channel5 global interrupt	false	true	true
USB low priority or CAN RX0 interrupts	false	true	true
USART1 global interrupt	false	true	true

\* User modified value

## 9. System Views

### 9.1. Category view

#### 9.1.1. Current

#### Middleware

USB\_DEVICE 

#### System Core

DMA 

GPIO 

IWDG 

NVIC 

RCC 

SYS 

#### Analog

#### Timers

TIM1 

TIM3 

TIM4 

TIM5 

#### Connectivity

USART1 

USB 

#### Multimedia

#### Computing

## 10. Docs & Resources

Type	Link
Datasheet	<a href="http://www.st.com/resource/en/datasheet/CD00191185.pdf">http://www.st.com/resource/en/datasheet/CD00191185.pdf</a>
Reference manual	<a href="http://www.st.com/resource/en/reference_manual/CD00171190.pdf">http://www.st.com/resource/en/reference_manual/CD00171190.pdf</a>
Programming manual	<a href="http://www.st.com/resource/en/programming_manual/CD00228163.pdf">http://www.st.com/resource/en/programming_manual/CD00228163.pdf</a>
Programming manual	<a href="http://www.st.com/resource/en/programming_manual/CD00283419.pdf">http://www.st.com/resource/en/programming_manual/CD00283419.pdf</a>
Errata sheet	<a href="http://www.st.com/resource/en/errata_sheet/CD00197763.pdf">http://www.st.com/resource/en/errata_sheet/CD00197763.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00160362.pdf">http://www.st.com/resource/en/application_note/CD00160362.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00164185.pdf">http://www.st.com/resource/en/application_note/CD00164185.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00167594.pdf">http://www.st.com/resource/en/application_note/CD00167594.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00200423.pdf">http://www.st.com/resource/en/application_note/CD00200423.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00211314.pdf">http://www.st.com/resource/en/application_note/CD00211314.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00249778.pdf">http://www.st.com/resource/en/application_note/CD00249778.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00259245.pdf">http://www.st.com/resource/en/application_note/CD00259245.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00264321.pdf">http://www.st.com/resource/en/application_note/CD00264321.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00264342.pdf">http://www.st.com/resource/en/application_note/CD00264342.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00264379.pdf">http://www.st.com/resource/en/application_note/CD00264379.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00024853.pdf">http://www.st.com/resource/en/application_note/DM00024853.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00032987.pdf">http://www.st.com/resource/en/application_note/DM00032987.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00033267.pdf">http://www.st.com/resource/en/application_note/DM00033267.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00033344.pdf">http://www.st.com/resource/en/application_note/DM00033344.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00042534.pdf">http://www.st.com/resource/en/application_note/DM00042534.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00052530.pdf">http://www.st.com/resource/en/application_note/DM00052530.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00073742.pdf">http://www.st.com/resource/en/application_note/DM00073742.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00080497.pdf">http://www.st.com/resource/en/application_note/DM00080497.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00129215.pdf">http://www.st.com/resource/en/application_note/DM00129215.pdf</a>

Application note [http://www.st.com/resource/en/application\\_note/DM00156964.pdf](http://www.st.com/resource/en/application_note/DM00156964.pdf)

Application note [http://www.st.com/resource/en/application\\_note/DM00160482.pdf](http://www.st.com/resource/en/application_note/DM00160482.pdf)

Application note [http://www.st.com/resource/en/application\\_note/DM00209695.pdf](http://www.st.com/resource/en/application_note/DM00209695.pdf)

Application note [http://www.st.com/resource/en/application\\_note/DM00220769.pdf](http://www.st.com/resource/en/application_note/DM00220769.pdf)

Application note [http://www.st.com/resource/en/application\\_note/DM00236305.pdf](http://www.st.com/resource/en/application_note/DM00236305.pdf)

Application note [http://www.st.com/resource/en/application\\_note/DM00257177.pdf](http://www.st.com/resource/en/application_note/DM00257177.pdf)

Application note [http://www.st.com/resource/en/application\\_note/DM00272912.pdf](http://www.st.com/resource/en/application_note/DM00272912.pdf)

Application note [http://www.st.com/resource/en/application\\_note/DM00296349.pdf](http://www.st.com/resource/en/application_note/DM00296349.pdf)

Application note [http://www.st.com/resource/en/application\\_note/DM00315319.pdf](http://www.st.com/resource/en/application_note/DM00315319.pdf)

Application note [http://www.st.com/resource/en/application\\_note/DM00325582.pdf](http://www.st.com/resource/en/application_note/DM00325582.pdf)

Application note [http://www.st.com/resource/en/application\\_note/DM00327191.pdf](http://www.st.com/resource/en/application_note/DM00327191.pdf)

Application note [http://www.st.com/resource/en/application\\_note/DM00354244.pdf](http://www.st.com/resource/en/application_note/DM00354244.pdf)

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