LAB 1 BOOLEAN ALGEBRA

CDA 3201C, Section 003

SEPTEMBER 24, 2019

PROFESSOR PETRIE
Summer Poissonnier
Z23492880

• CDA3201 • Intro to Logic Design • Lab Assignment **1**

Name: Summer Poissonnier Z#: 23492880 Grade: /100

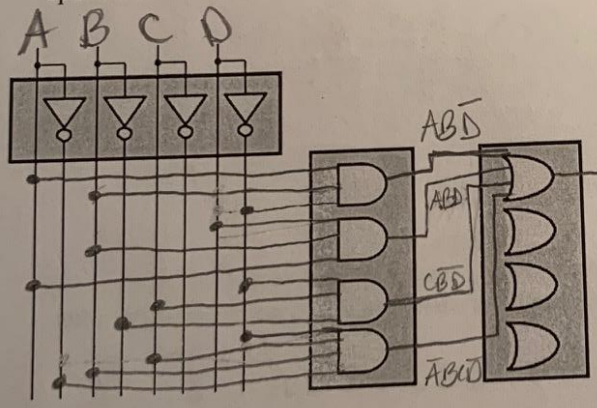
1. [100] To get all your lab points you need to get your lab grader by the Teaching Assistant (TA) and submit under Canvas > Assignment > Lab 1 a **portfolio** consisting of one pdf file that includes:
   - Header: Cover page or header with your name, my name, number, Logic Design class and class section
   - Handwork: copy of planning work you did by hand (take picture of this worksheet or annotate this pdf with Edge)
   - Simulation: a copy of the work you did in Altera Quartus
     - Schematic do all 3 circuits in one schematic window, must include comment with your name and Z#, the file name must include your name as part of the file name so it appears on the schematic screen window. You can take a picture of the screen or use Snipping Tool under Start menu to capture the pertinent part of the screen.
     - Vector Waveform simulation (simulated timing diagram) that include output for all 3 circuits in one screen
   - Wiring: a picture of your breadboard with the wired circuit and your FAU OWL Card (if you got it graded in the lab also include with TA OWL card and the lab grade sheet in the background)

1.1 [10] Given the following Boolean Algebra Equation, complete the Truth Table at right

$$X = A B \overline{D} + A B D + C \overline{B} \overline{D} + \overline{A} B C \overline{D}$$

ABCD	$AB\overline{D}$	ABD	$C\overline{B}\overline{D}$	$\overline{A}BC\overline{D}$	X
0000	001	000	011	1001	0
0001	000	001	010	1000	0
0010	001	000	111	1011	1
0011	000	001	110	1010	0
0100	011	010	001	1101	0
0101	010	011	000	1100	0
0110	011	010	101	1111	1
0111	010	011	100	1110	0
1000	101	100	011	0001	0
1001	100	101	010	0000	0
1010	101	100	111	0011	1
1011	100	101	110	0010	0
1100	111	110	001	0101	1
1101	110	111	000	0100	1
1110	111	110	101	0111	1
1111	110	111	100	0110	1

1.2 [10] Utilizing the NOT AND OR gates provided below, label the input that you need to put through NOT, determine how many inputs are needed for each gate and use the number of gates you need (there may be extras). Draw the circuit connections to implement X exactly as specified.



$$X = A B \overline{D} + A B D + C \overline{B} \overline{D} + \overline{A} B C \overline{D}$$

1.3 [10] Create a project in Altera Quartus called **lab1-PETRIE-yourlastname** following Dr. Petrie's step by step guide and verify the circuit you designed in 1.2 works according to 1.1 Truth Table. If it does not work as specified by the Truth Table, then determine if error is in the Truth Table or your design. Create with same name a Block Diagram/Schematics (.bdf) of your design in 1.3. Is there a 4-input OR gate available? If there is not then figure out how you will change the design using 2 input OR gates. Generate with same name a Waveform file (.vwf), group the inputs and set the counter to step through all the values, Compile, and Simulate. Make sure to save the project, the .bdf and .vwf files often. Check the .vwf to verify it produces same results as the Truth Table 1.1. Keep the project and files to expand the Block Diagram to include the other 2 circuits in the rest of lab 1.

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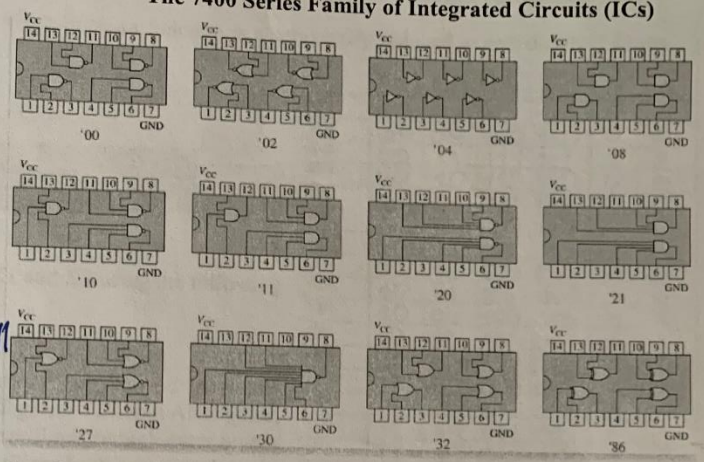
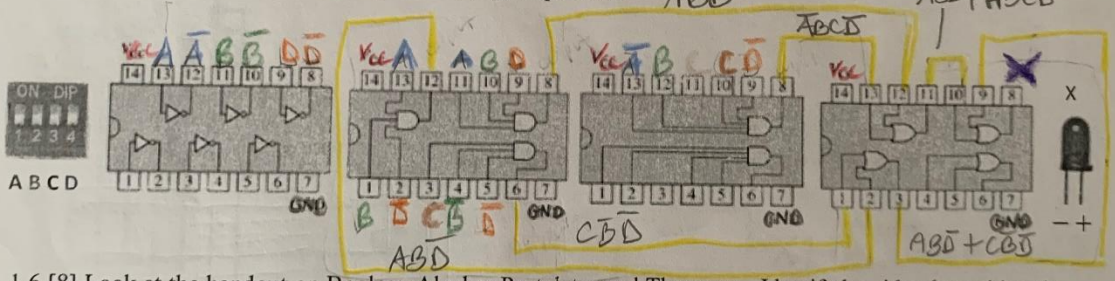
1.4 [5] Gates are packaged in ICs. Determine which and how many ICs from the 7400 Series family at right you will need to implement the circuit as you specified in 1.3 (Note there are no 4 input ORs in your kit so use 2 input OR ICs instead:

Quantity needed?	7400 Series IC #
1	7411
1	7432
1	7404
1	7421

The 7400 Series Family of Integrated Circuits (ICs)



1.5 [10] Plan out the layout by labeling inputs and outputs of the gates or drawing the wiring use blue-A, Green-B, Brown-C, Orange-D, use the same color dashed wire for NOT. Note we don't have 4 input ORs in the kit, so we need to make due with using 2 input ORs:



1.6 [8] Look at the handout on Boolean Algebra Postulates and Theorems. Identify by either by writing the name or the equation of the postulate(s) or theorem(s) used to simplify.

$$X = AB\overline{D} + ABD + C\overline{B}\,\overline{D} + \overline{A}BC\overline{D}$$

Factoring

$$= AB(\overline{D} + D) + (\overline{B} + \overline{AB})C\overline{D}$$

Additive Complement / Absorption

$$= AB(1) + (\overline{B} + \overline{A})C\overline{D} = AB + \overline{B}C\overline{D} + A\overline{C}\overline{D}$$

Multiplicative Identity / Distribution

Or

$$= AB + (\overline{AB})C\overline{D} = AB + C\overline{D}$$

DeMorgan's Law / Absorption

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As you verified in 1.a.6, the following Boolean function is algebraically reduced to two different forms denoted as X1 and X2 as follows.

$X = A B \overline{D} + A B D + C \overline{B} \overline{D} + \overline{A} B C \overline{D}$

$= AB(\overline{D} + D) + (\overline{B} + \overline{A}B) C\overline{D}$

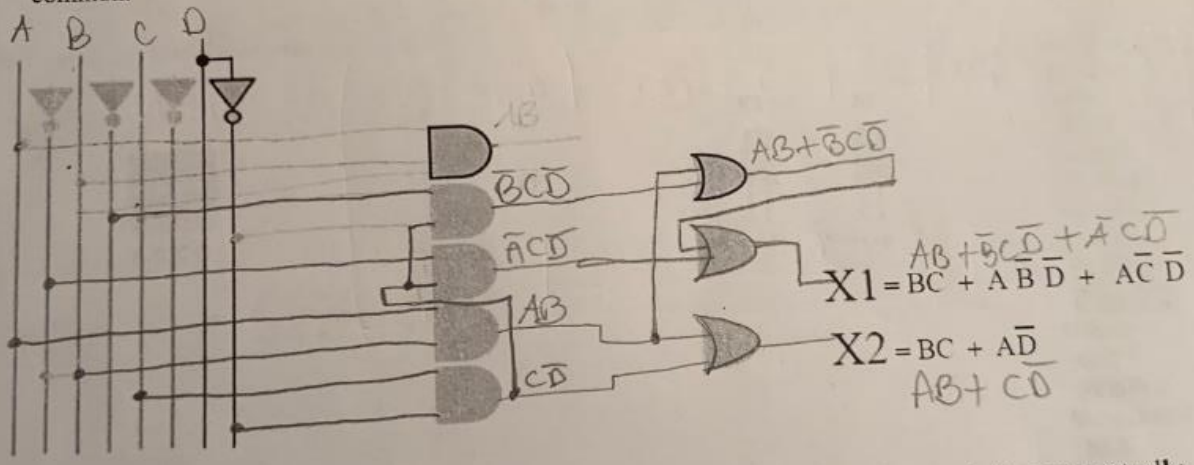
$= AB + (\overline{B} + \overline{A}) C\overline{D} = \underline{AB + \overline{B} C \overline{D} + \overline{A} C \overline{D} = X1}$

or $= AB + \overline{(AB)} C\overline{D} = \underline{AB + C\overline{D} = X2}$

1.7) [5] Verify the equivalence of X1 and X2 using the following truth table:

ABCD	AB	$C\overline{D}$	$\overline{B}C\overline{D}$	$\overline{A}C\overline{D}$	X1	X2
0000	00	01	101	101	0	0
0001	00	00	100	100	0	0
0010	00	11	111	111	1	1
0011	00	10	110	110	0	0
0100	01	01	001	101	0	0
0101	01	00	000	100	0	0
0110	01	11	011	111	1	1
0111	01	10	010	110	0	0
1000	10	01	101	001	0	0
1001	10	00	100	000	0	0
1010	10	11	111	011	1	1
1011	10	10	110	010	0	0
1100	11	01	001	001	1	1
1101	11	00	000	000	1	1
1110	11	11	011	011	1	1
1111	11	10	010	010	1	1

1.8) [7] Design the circuit for the above two reduced functions, X1 and X2, using exactly 3 NOT gates, 4 2-input AND gates, 3 2-input OR gates. Note, there will not enough gates unless you are able to reuse by finding things both equations have in common.



1.9) [10] Verify the circuit design/behavior by implementing the circuit using Quartus before you actually build the circuit on the breadboard. Open the Quartus project you build in 1.a.3 and add the X1 and X2 circuits to the X circuit Block Diagram / Schematics. Add the X1 and X2 inputs to the Waveform File and Compile and Simulate, check if all X = X1 = X2. You will show the TA you have these files and submit the .bdf and .vwf to the Lab 1 together with the scan of this completed Lab with all your work. Dr. Petrie will adjust your grade – these 2 points will be converted to 20 points total for this section and 1.a.3.

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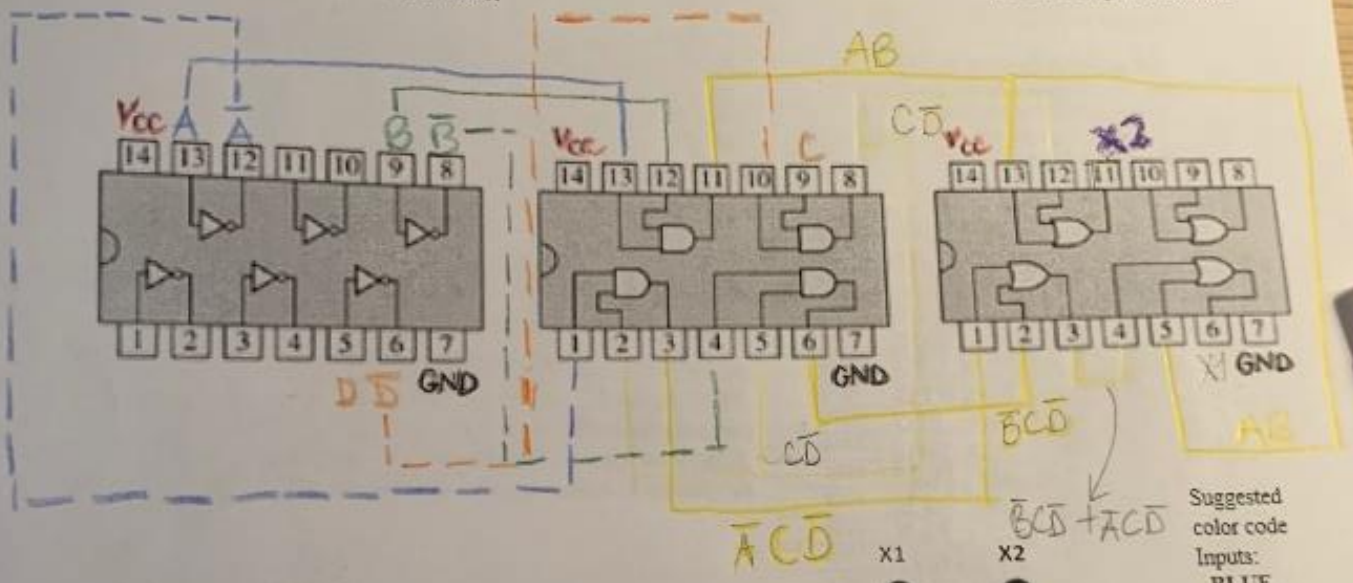
1.10) [20] Use the following chip pin-out to conveniently plan your wiring to build the above 2-output circuit for X1 and X2 on your breadboard using exactly 1/2 7404, 1 7408 and 3/4 7432 chips on your breadboard and then connect inputs ABCD to 4 DIP switched and the outputs X1 X2 to two LED indicators. Test all the 16 different input combinations and observe the two outputs to be equivalent and matching the 1.7 Truth Table.



A B C D

X1 X2

− + − +

Suggested color code

Inputs:
BLUE
GREEN
BROWN
ORANGE

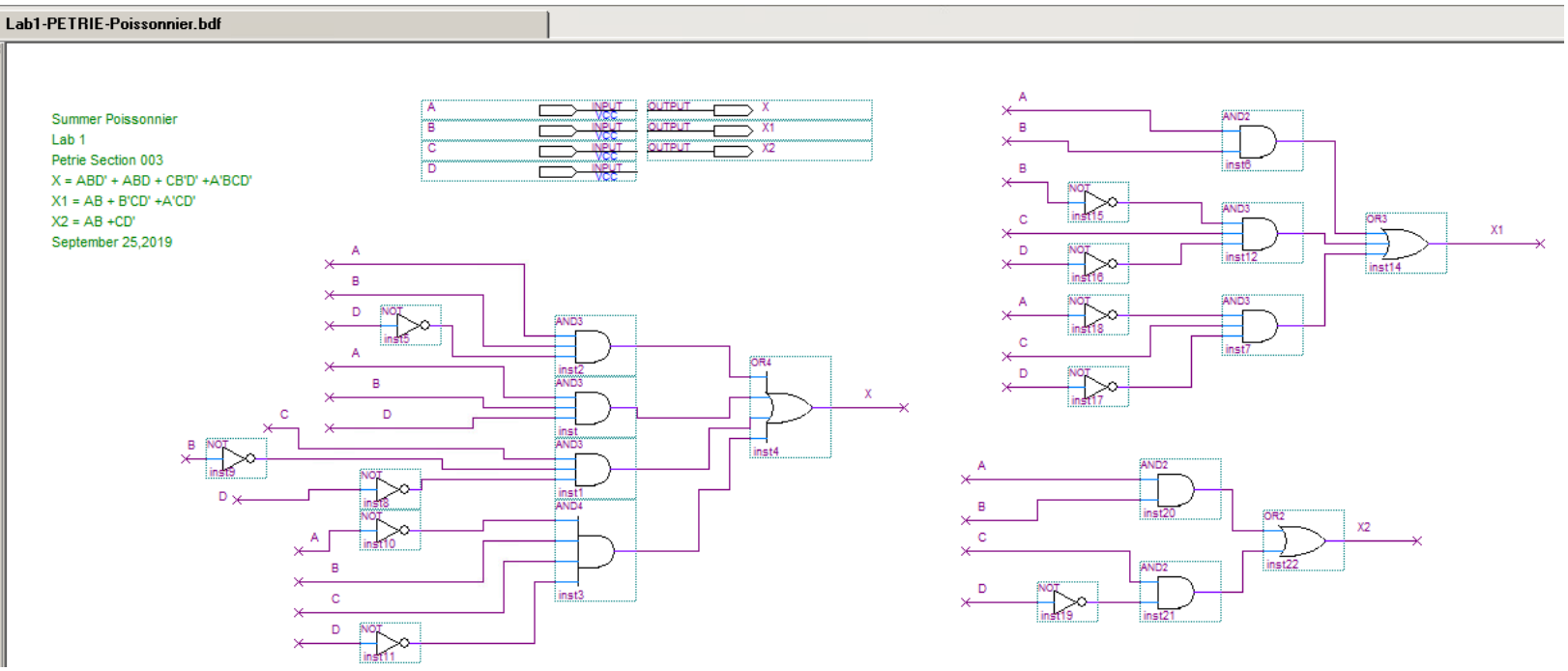
In-Between:
WHITE
YELLOW

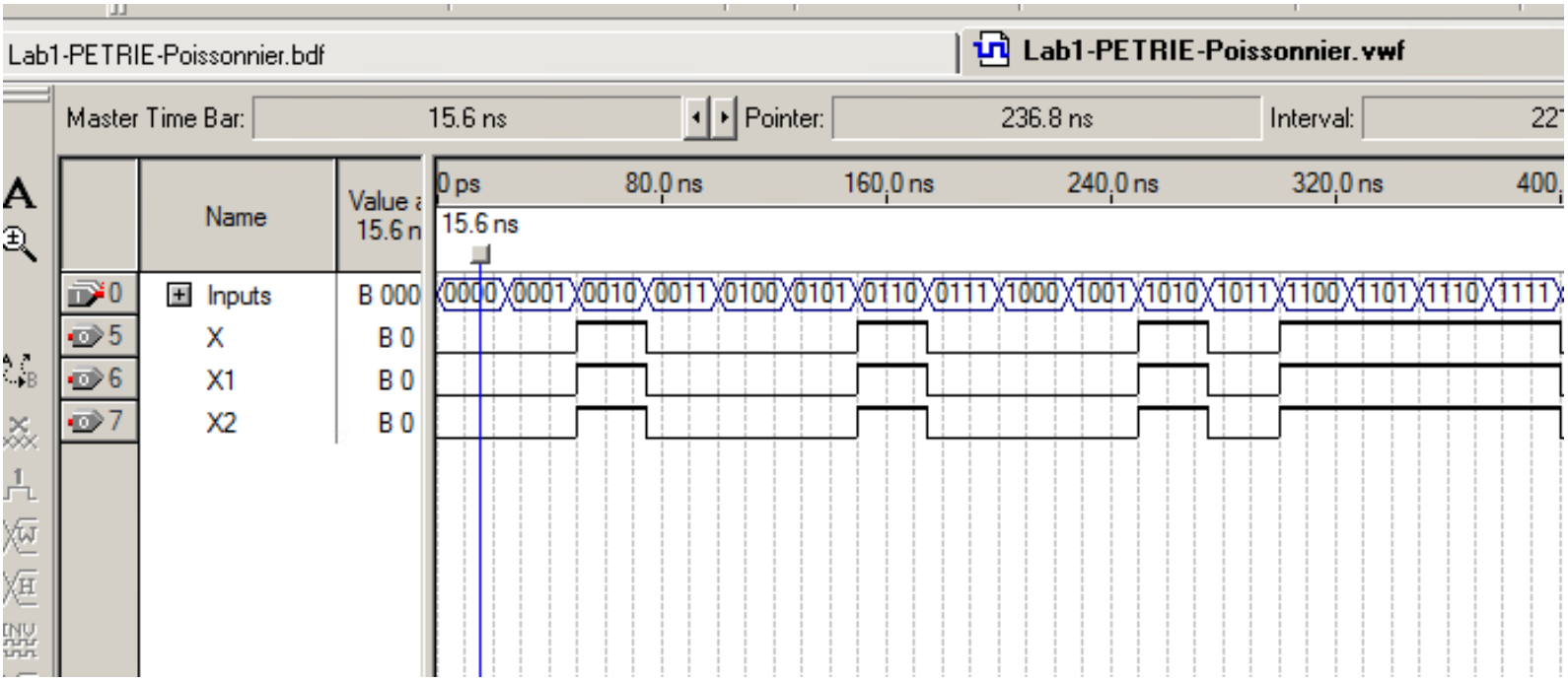
Outputs:
GREY
PURPLE

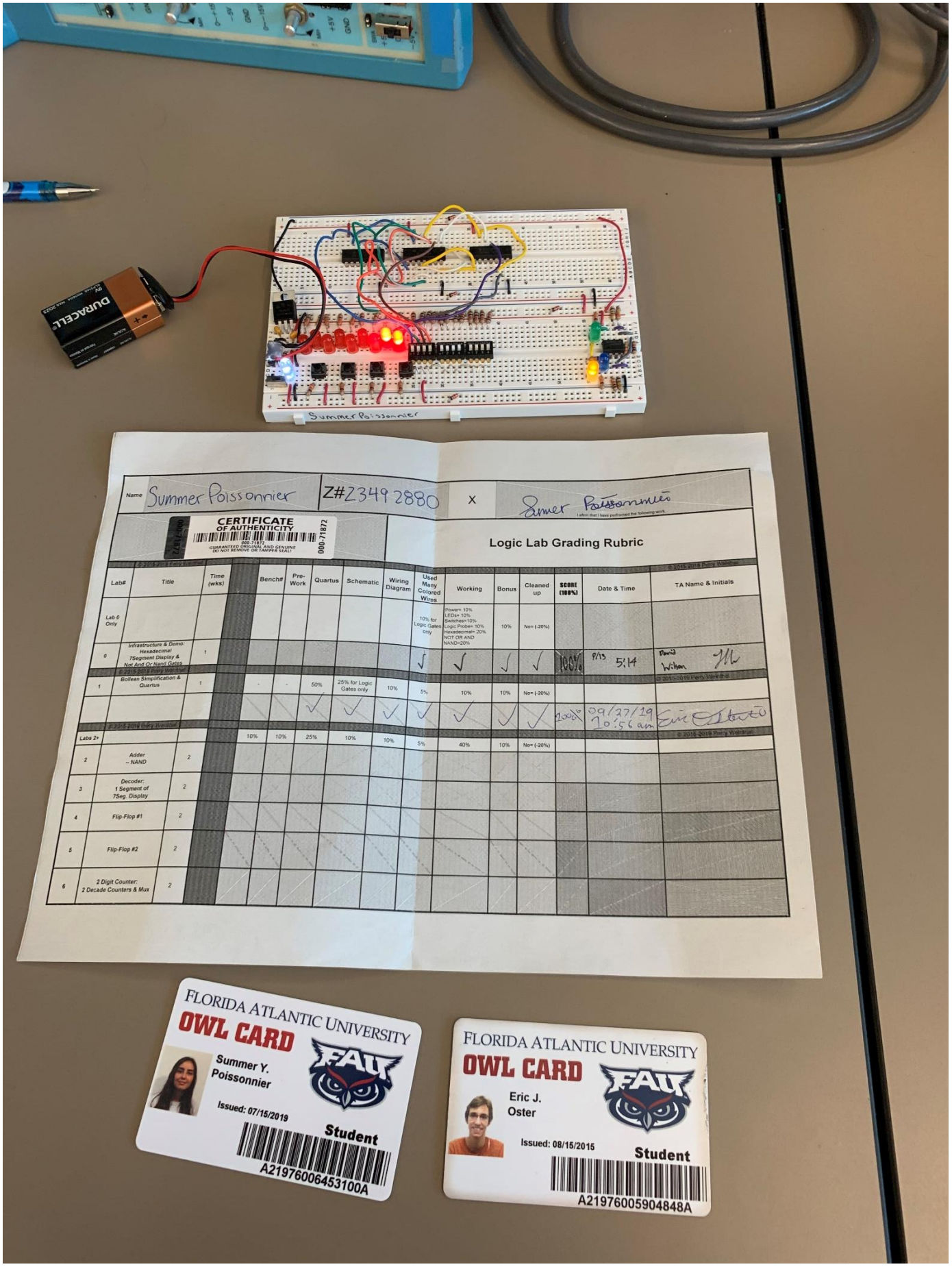
Vcc and GND:
RED
BLACK

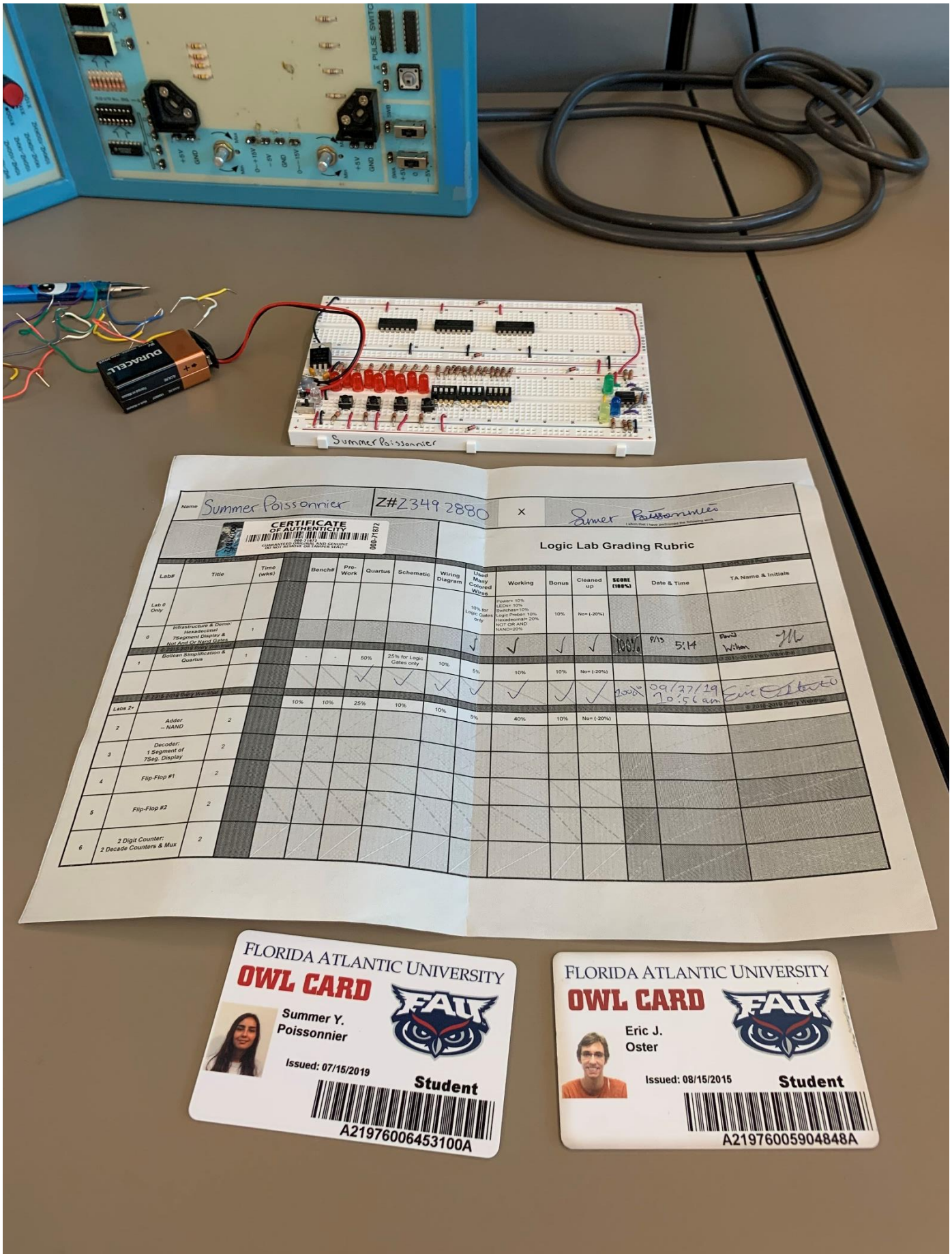
Note that = white!!

After you get it to work but before the TA grades it, take a picture of your breadboard to submit as part of Lab 1 documentation. After it is graded take a picture of the gradesheet, then, except for the ground and power wires, pull the wires attached to the three the three ICs on the upper breadboard you used for this experiment (*Do NOT* pull the lab platform wires just the ones in the upper breadboard), leaving the three ICs plugged into your board with power and ground connected. **KEEP THE WIRE TO REUSE FOR NEXT LAB.** Upload the portfolio of your labwork to Canvas to validate your lab grade.


Lab1-PETRIE-Poissonnier.bdf
Summer Poissonnier
Lab 1
Petrie Section 003
X = ABD' + ABD + CB'D' +A'BCD'
X1 = AB + B'CD' +A'CD'
X2 = AB +CD'
September 25,2019


Lab1-PETRIE-Poissonnier.bdf
Lab1-PETRIE-Poissonnier.vwf
Master Time Bar:
15.6 ns
Pointer:
236.8 ns
Interval:
Name
Value a
15.6 n
0 ps
80.0 ns
160.0 ns
240.0 ns
320.0 ns
400
15.6 ns
0 Inputs B 000
5 X B 0
6 X1 B 0
7 X2 B 0
0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111


Summer Poissonnier
Name Summer Poissonnier
Z#Z3492880
X
Summer Poissonnier
I affirm that I have performed the following work.
CERTIFICATE OF AUTHENTICITY
000-71872
Logic Lab Grading Rubric
Lab#
Title
Time (wks)
Bench#
Pre-Work
Quartus
Schematic
Wiring Diagram
Used Many Colored Wires
Working
Bonus
Cleaned up
SCORE (100%)
Date & Time
TA Name & Initials
Lab 0 Only
10% for Logic Gates only
Power= 10%
LEDs= 10%
Switches=10%
Logic Probe= 10%
Hexadecimal= 20%
NOT OR AND
NAND=20%
Nos= (-20%)
0
Infrastructure & Demo: Hexadecimal 7Segment Display & Not And Or Nand Gates
1
100%
9/13
5:14
David Wilson
1
Boolean Simplification & Quartus
1
50%
25% for Logic Gates only
10%
5%
10%
10%
Nos= (-20%)
100%
09/27/19 10:56 am
Labs 2+
10%
10%
25%
10%
10%
5%
40%
10%
Nos= (-20%)
2
Adder – NAND
2
3
Decoder: 1 Segment of 7Seg. Display
2
4
Flip-Flop #1
2
5
Flip-Flop #2
2
6
2 Digit Counter: 2 Decade Counters & Mux
2
FLORIDA ATLANTIC UNIVERSITY
OWL CARD
Summer Y. Poissonnier
Issued: 07/15/2019
Student
A21976006453100A
FLORIDA ATLANTIC UNIVERSITY
OWL CARD
Eric J. Oster
Issued: 08/15/2015
Student
A21976005904848A


PULSE SWITCH
DURACELL
Summer Poissonnier
Name Summer Poissonnier Z#23492880
CERTIFICATE OF AUTHENTICITY
Logic Lab Grading Rubric
Lab# Title Time (wks) Bench# Pre-Work Quartus Schematic Wiring Diagram Used Many Colored Wires Working Bonus Cleaned up SCORE [100%] Date & Time TA Name & Initials
Lab 0 Only
0 Infrastructure & Demo: Hexadecimal 7Segment Display & Not And Or Nand Gates 1
1 Boolean Simplification & Quartus 1
Labs 2+
2 Adder -- NAND 2
3 Decoder: 1 Segment of 7Seg Display 2
4 Flip-Flop #1 2
5 Flip-Flop #2 2
6 2 Digit Counter: 2 Decade Counters & Mux 2
10% for Logic Gates only
Power= 10% LEDs= 10% Switches=10% Logic Probe= 10% Hexadecimal= 20% NOT OR AND NAND=20%
10% No= (-20%)
100%
9/13 5:14
25% for Logic Gates only
50%
10%
5%
40%
09/27/19 10:56 am
FLORIDA ATLANTIC UNIVERSITY
OWL CARD
Summer Y. Poissonnier
Issued: 07/15/2019
Student
A21976006453100A
FLORIDA ATLANTIC UNIVERSITY
OWL CARD
Eric J. Oster
Issued: 08/15/2015
Student
A21976005904848A

Name	Summer Poissonnier	Z# Z3492880	X	Summer Poissonnier

I affirm that I have performed the following work.

CERTIFICATE OF AUTHENTICITY
000-71872
GUARANTEED ORIGINAL AND GENUINE
DO NOT REMOVE OR TAMPER SEAL!
000-71872 000-71872

Logic Lab Grading Rubric

Lab#	Title	Time (wks)		Bench#	Pre-Work	Quartus	Schematic	Wiring Diagram	Used Many Colored Wires	Working	Bonus	Cleaned up	SCORE (100%)	Date & Time	TA Name & Initials
Lab 0 Only									10% for Logic Gates only	Power= 10% LEDs= 10% Switches=10% Logic Probe= 10% Hexadecimal= 20% NOT OR AND NAND=20%	10%	No= (-20%)			
0	Infrastructure & Demo: Hexadecimal 7Segment Display & Not And Or Nand Gates	1							√	√	√	√	100%	9/13 5:14	David Wilson
1	Bollean Simplification & Quartus	1		-	-	50%	25% for Logic Gates only	10%	5%	10%	10%	No= (-20%)			
						√	√	√	√	√	√	√	100%	09/27/19 10:56 am	Eric Stanton
Labs 2+				10%	10%	25%	10%	10%	5%	40%	10%	No= (-20%)			
2	Adder -- NAND	2													
3	Decoder: 1 Segment of 7Seg. Display	2													
4	Flip-Flop #1	2													
5	Flip-Flop #2	2													
6	2 Digit Counter: 2 Decade Counters & Mux	2													