LAB 3 DECODER

CDA 3201C Section 003

OCTOBER 22, 2019

PROFESSOR PETRIE
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Z 23492880

CDA3201 x Intro to Logic Design x

Lab Assignment **3**

/100

Name: Summer Boissonnier

Grade:

3) **[Petrie-100]** Consider the following two functions:

$$X = \bar{A}BCD + \bar{A}B\bar{C}D + A\bar{B}\bar{C}D + BCD$$

$$Y = A\bar{B}CD + AB\bar{C} + ACD + ABD$$

3.1) [Petrie – 10] In the past we started with a Truth Table and simplified using K-maps to build a simplified circuit. In this lab we are given an equation which is not simplified, so in order to construct a K-map, you need to reverse-engineer the Truth Table or Sum of Minterms. This is equivalent to finding the Canonical Sum of Products from a Simplified Boolean Expression. There are two methods, you can either create the Truth Table or find the Minterms associated with the following products to find the Sum of Minterm equation for X and for Y. Do both methods here:

Truth Table [10]

Term	Minterm#	A B C D	A'BCD	A'BC'D	AB'C'D	BCD	X
0	0	0000	0	0	0	0	0
1	1	0001	0	0	0	0	
2	2	0010	0	0	0	0	
3	3	0011	0	0	0	0	
4	4	0100	0	0	0	0	1
5	5	0101	0	1	0	0	
6	6	0110	0	0	0	1	1
7	7	0111	1	0	0	0	
8	8	1000	0	0	0	0	1
9	9	1001	0	0	0	0	
10	10	1010	0	0	0	0	
11	11	1011	0	0	0	0	
12	12	1100	0	0	0	0	
13	13	1101	0	0	0	0	
14	14	1110	0	0	0	1	1
15	15	1111	0	0	0	1	

Find minterms number(s) associated with each term and Sum of Minterm efor X and Y [10]

A' B C D $\Sigma m(7)$
0 1 1 1
1 1 1 1

A' B C' D $\Sigma m(5)$
0 1 0 1
1 1 1 1

A B' C' D $\Sigma m(9)$
1 0 0 1
1 1 1 1

B C D $\Sigma m(7,15)$
0 1 1 1
1 1 1 1

$X = \Sigma m(5, 7, 9, 15)$)

Term	Minterm#	A B C D	AB'CD	ABC'	ACD	ABD	Y
0	0	0000	0	0	0	0	0
1	1	0001	0	0	0	0	0
2	2	0010	0	0	0	0	0
3	3	0011	0	0	0	0	0
4	4	0100	0	0	0	0	0
5	5	0101	0	0	0	0	0
6	6	0110	0	0	0	0	0
7	7	0111	0	0	0	0	0
8	8	1000	0	0	0	0	0
9	9	1001	0	0	0	0	0
10	10	1010	0	0	0	0	1
11	11	1011	1	0	1	0	1
12	12	1100	0	1	0	0	1
13	13	1101	0	1	0	1	1
14	14	1110	0	0	0	0	0
15	15	1111	0	0	1	1	1

AB' C D $\Sigma m(11)$
1 0 1 1

A B C' $\Sigma m(12,13)$
1 1 0 0
1 1 0 1

A C D $\Sigma m(12,15)$
1 0 1 1
1 1 1 1

A B D $\Sigma m(13,15)$
1 1 0 1
1 1 1 1

$Y = \Sigma m(11, 12, 13, 15)$)

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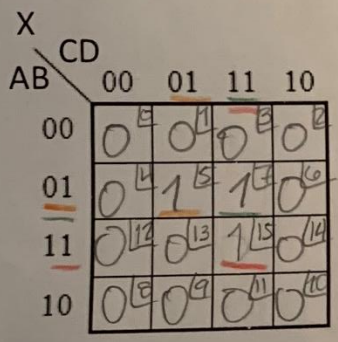
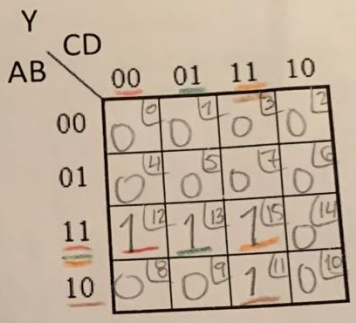
$$X = \bar{A}B\,CD + \bar{A}B\,\bar{C}D + A\bar{B}\bar{C}D + B\,CD$$

$$Y = A\bar{B}\,CD + AB\bar{C} + ACD + ABD$$

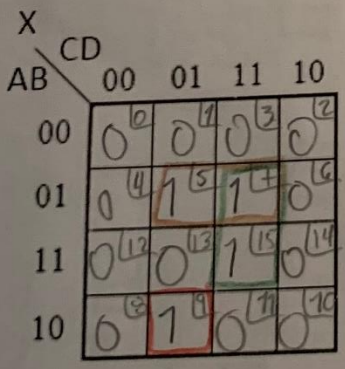
3.2) [Petrie 10] Expand the above functions to sum of Minterm using K-maps.

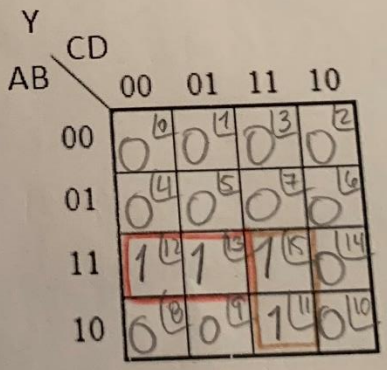
We could also reverse-engineer what region each term covers using the K-maps figuring out which row(s) and which column(s) the term and putting 1s in the intersection. Underline each term (Product) in X in a different color and mark in the X K-Map in that color the 1s each term represents. Repeat for Y.





To check your work, label each cell in the following K-Maps with the Minterm # of the cell, then put the 1s where indicated in the Sum of Minterms equations for X and Y done previously in 3.1.





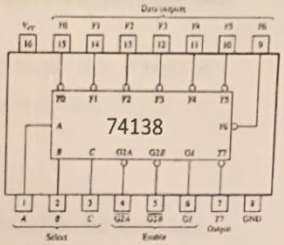
If they agree, you write the Sum of Minterms for X and Y below

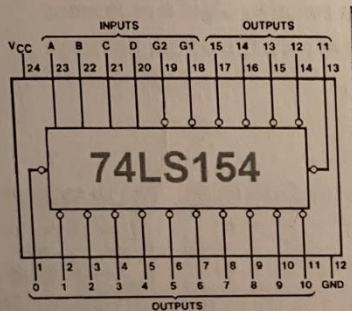
X = f (A, B, C, D) = ∑m (5, 7, 9, 15)

Y = f (A, B, C, D) = ∑m (11, 12, 13, 15)

Name: Grade:

3.3) [TA-4, Petrie-30] The Functional Diagrams of the 74HC154 4 to 16 Decoder and of the 74138 3-8 Decoder are given, along with the PinOut Diagrams and the Truth Table for each. Plan the circuits for X and Y given in page 1. First by using the 74HC154 4-16 decoder and 1 7420 4-input NAND. You do not have a 4-16 decoder in your kit, plan the same circuits for X and Y using exactly two 3-to-8 Decoders, (2 of 74138 chips) and two 4-input NAND gates (1 - 7420 chip). No other gates are allowed.

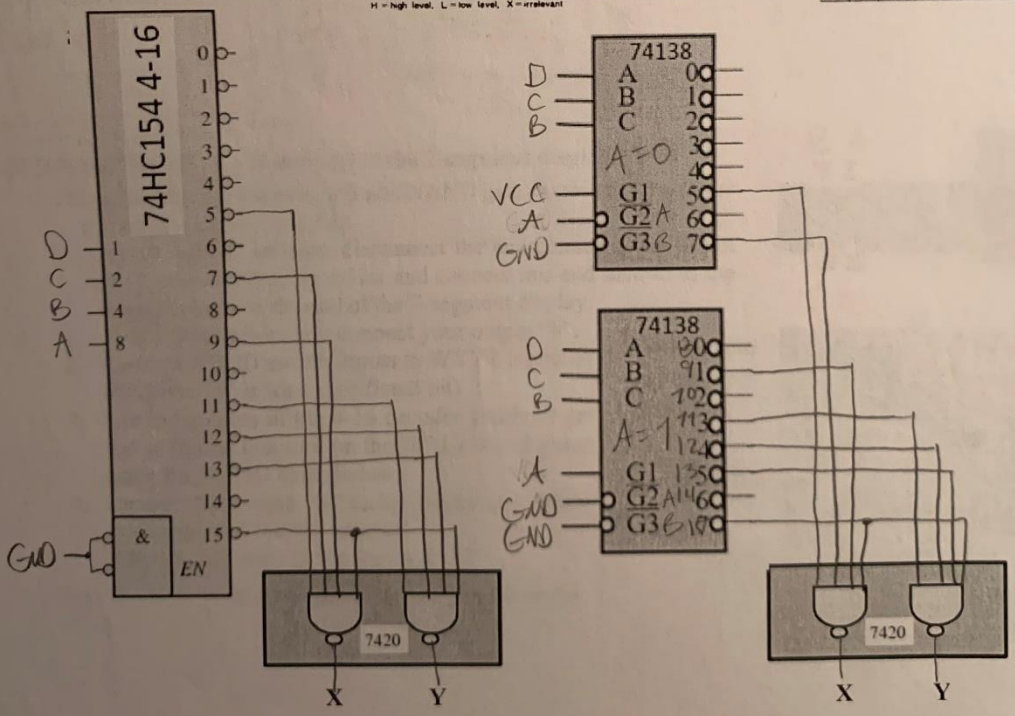




INPUTS					OUTPUTS													
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = high level, L = low level, X = irrelevant

Inputs						Output							
Enable			Select										
G2A	G2B	G1	C	B	A	0	1	2	3	4	5	6	7
1	X	X	X	X	X	1	1	1	1	1	1	1	1
X	1	X	X	X	X	1	1	1	1	1	1	1	1
X	X	0	X	X	X	1	1	1	1	1	1	1	1
0	0	1	0	0	0	0	1	1	1	1	1	1	1
0	0	1	0	0	1	1	0	1	1	1	1	1	1
0	0	1	0	1	0	1	1	0	1	1	1	1	1
0	0	1	0	1	1	1	1	1	0	1	1	1	1
0	0	1	1	0	0	1	1	1	1	0	1	1	1
0	0	1	1	0	1	1	1	1	1	1	0	1	1
0	0	1	1	1	0	1	1	1	1	1	1	0	1
0	0	1	1	1	1	1	1	1	1	1	1	1	0

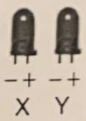


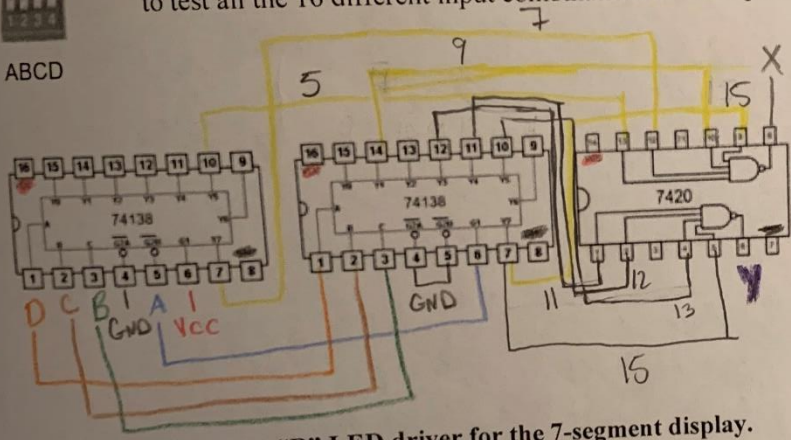
Name: Grade:

3.d) [4] Verify the circuit design/behavior for X and Y by implementing the 74138 circuit using Quartus and checking against the truth tables for X and Y on page 1. Do this before you actually build the 74138 circuit on the breadboard.

3.c) [10] Plan and build the above circuit using the specified logic chips on your breadboard and then connect to 4 logic switches as inputs A, B, C, D and 2 LEDs as outputs X and Y. You need to test all the 16 different input combinations of the inputs

ABCD



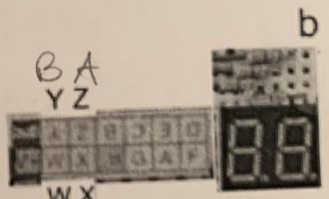


3.3) [10] Build a "B" LED driver for the 7-segment display.

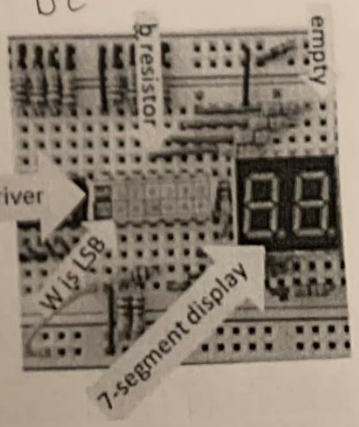
Using the two decoders on left add NAND gates to also build a driver circuit to control "b" LED.

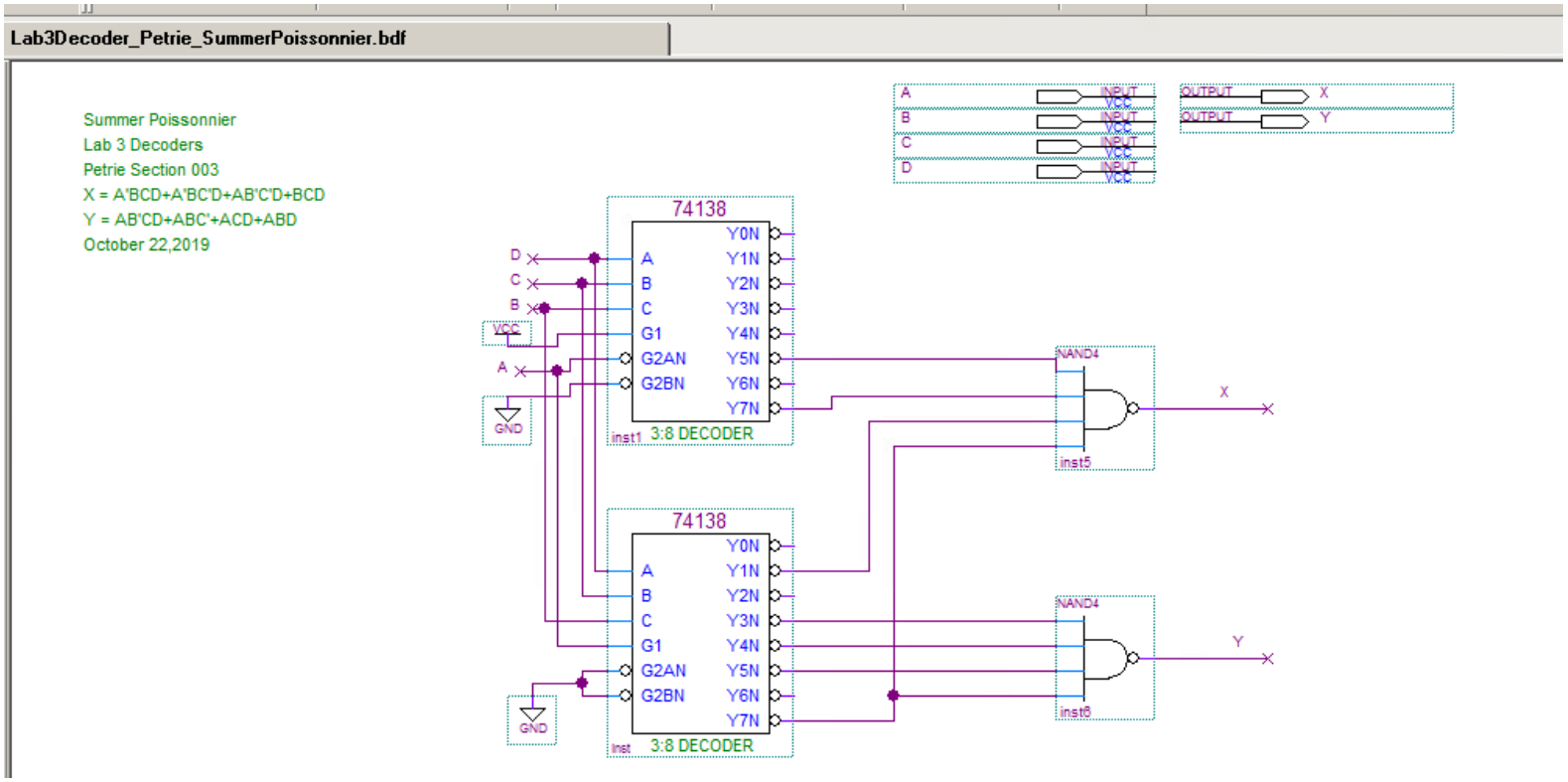
1. Locate b LED resistor, disconnect the end connected to "B" in the 7-segment display driver and connect this end instead to the empty column at the end of the 7-segment display. This will be where you connect your output "b".
2. Connect ABCD switch inputs to WXYZ inputs of the driver (W is least significant bit)
3. Use the outputs of the 4-16 decoder you built get the minterms that turn on the "b" LED and group using the NAND chips below.
4. Connect the output "b" to the empty row where you connected the "b" resistor
5. Test running through the inputs 0 to 9

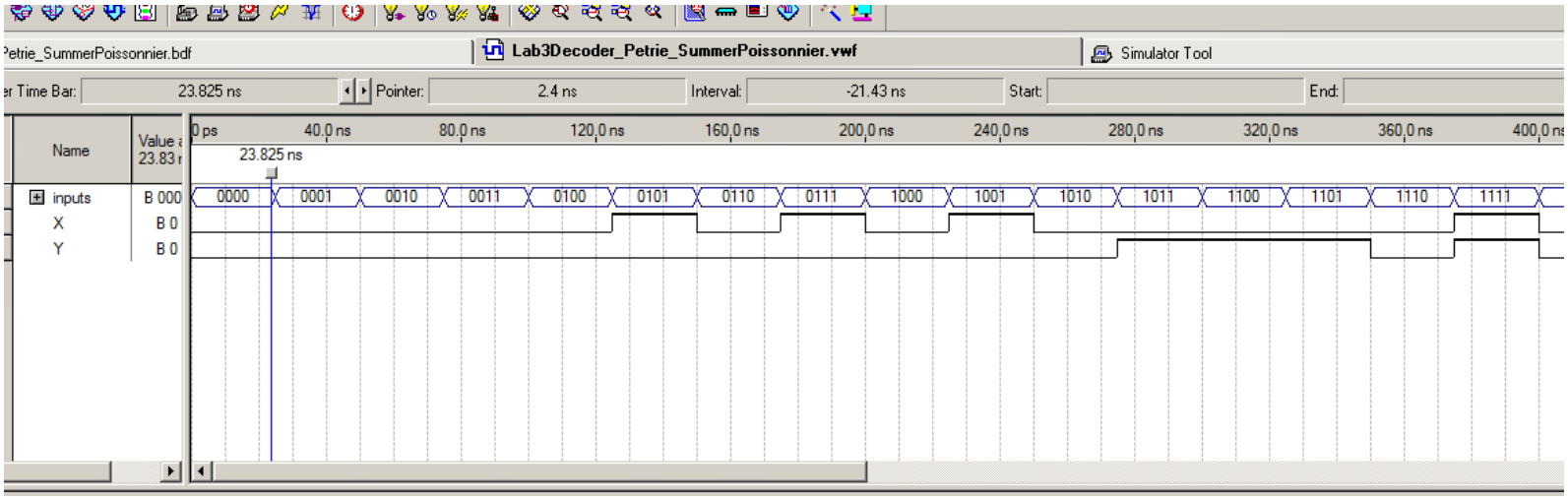
You do not have to do Quartus for this part of the lab.

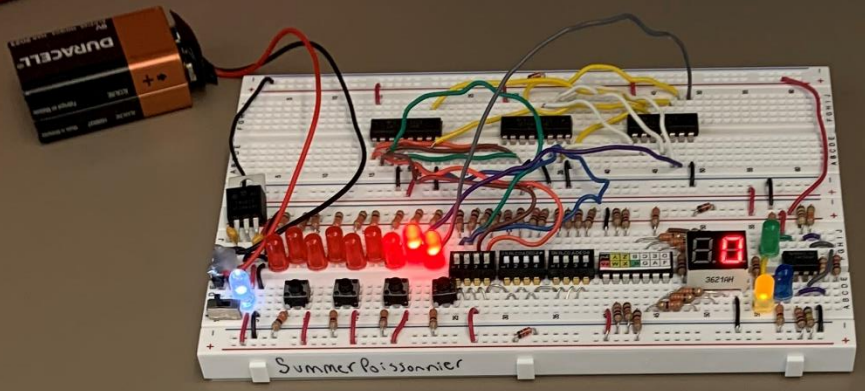


Find on your breadboard platform:




Lab3Decoder_Petrie_SummerPoissonnier.bdf
Summer Poissonnier
Lab 3 Decoders
Petrie Section 003
X = A'BCD+A'BC'D+AB'C'D+BCD
Y = AB'CD+ABC'+ACD+ABD
October 22,2019
A
B
C
D
INPUT
VCC
OUTPUT
X
Y
74138
Y0N
Y1N
Y2N
Y3N
Y4N
Y5N
Y6N
Y7N
G1
G2AN
G2BN
VCC
GND
inst1 3:8 DECODER
NAND4
inst5
inst6
inst 3:8 DECODER


Petrie_SummerPoissonnier.bdf
Lab3Decoder_Petrie_SummerPoissonnier.vwf
Simulator Tool
Time Bar: 23.825 ns
Pointer: 2.4 ns
Interval: -21.43 ns
Start:
End:
Name
Value
inputs
X
Y
0 ps
40.0 ns
80.0 ns
120.0 ns
160.0 ns
200.0 ns
240.0 ns
280.0 ns
320.0 ns
360.0 ns
400.0 ns
23.825 ns
0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111

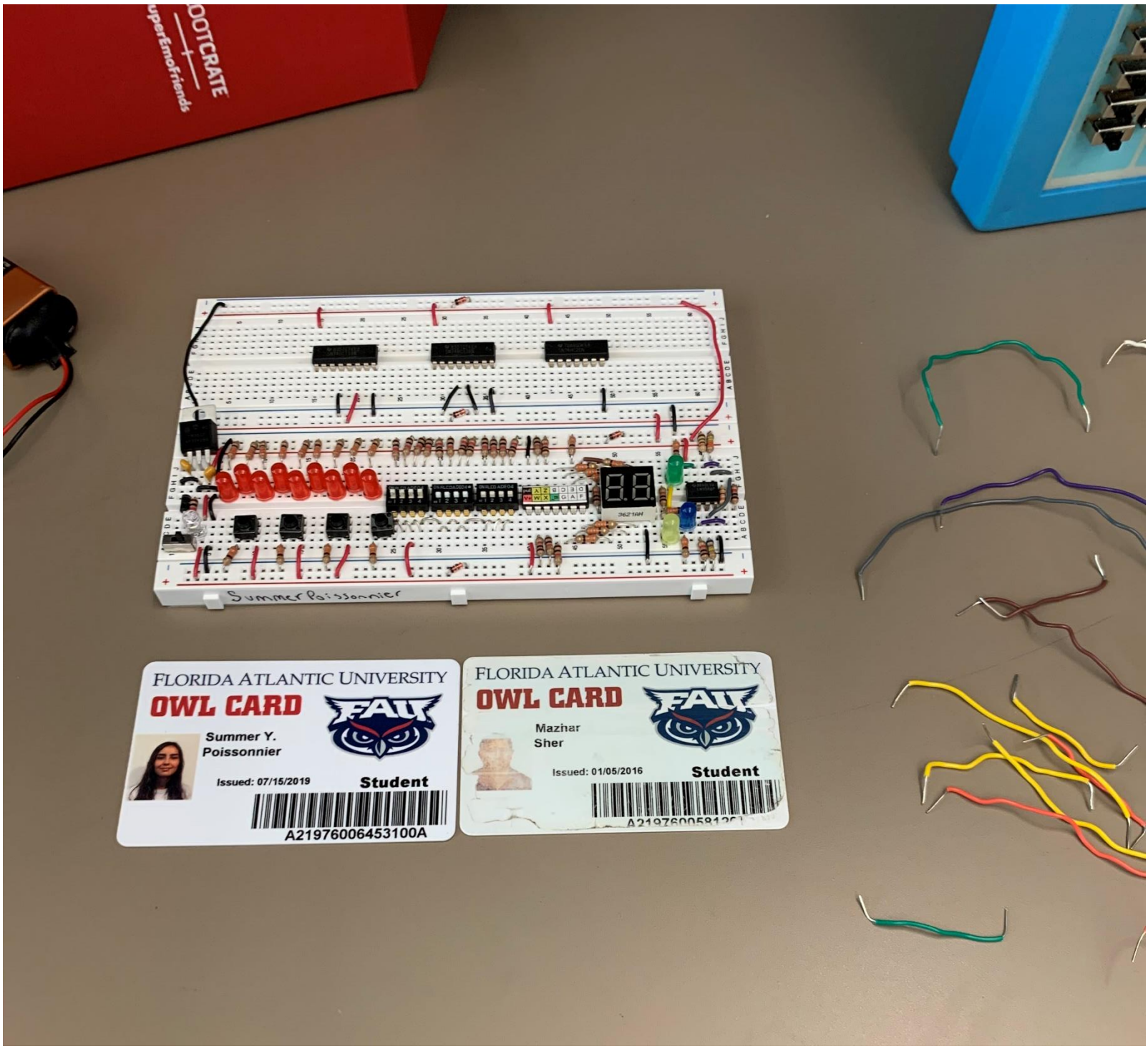


Name: Summer Poissonnier | Z#23492880 | X: Samer Poissonnier — I affirm that I have performed the following work

CERTIFICATE OF AUTHENTICITY 000-71872 — GUARANTEED ORIGINAL AND GENUINE DO NOT REMOVE OR TAMPER SEAL!

Logic Lab Grading Rubric

Lab#	Title	Time (wks)	Bench#	Pre-Work	Quartus	Schematic	Wiring Diagram	Used Many Colored Wires	Working	Bonus	Cleaned up	SCORE (100%)	Date & Time	TA Name & Initials
Lab 0 Only								10% for Logic Gates only	Power= 10% LEDs= 10% Switches=10% Logic Probe= 10% Hexadecimal= 20% NOT OR AND NAND=20%	10%	No= (-20%)			
0	Infrastructure & Demo: Hexadecimal 7Segment Display & Not And Or Nand Gates	1						√	√	√	√	100%	9/13 5:14	David Wilson
1	Bollean Simplification & Quartus	1	-	-	50%	25% for Logic Gates only	10%	5%	10%	10%	No= (-20%)			
					√	√	√	√	√	√	√	100%	09/27/19 10:56 am	Eric Olsten
Labs 2+			10%	10%	25%	10%	10%	5%	40%	10%	No= (-20%)			
2	Adder -- NAND	2	7	√	√	√	√	√	√	√	√	100%	10/18/19 11:06 am	Eric Olsten
3	Decoder: 1 Segment of 7Seg. Display	2	49	—	—	—	—	—	—	—	—	100	10-25-19 11:21	M.S.
4	Flip-Flop #1	2												
5	Flip-Flop #2	2												
6	2 Digit Counter: 2 Decade Counters & Mux	2												


FLORIDA ATLANTIC UNIVERSITY
OWL CARD
Summer Y.
Poissonnier
Issued: 07/15/2019
Student
A219760064531OOA
FLORIDA ATLANTIC UNIVERSITY
OWL CARD
Mazhar
Sher
Issued: 01/05/2016
Student

Name: Summer Poissonnier | Z#Z3492880 | X | Summer Poissonnier — I affirm that I have performed the following work.

CERTIFICATE OF AUTHENTICITY
000-71872
GUARANTEED ORIGINAL AND GENUINE
DO NOT REMOVE OR TAMPER SEAL!

Logic Lab Grading Rubric

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Lab 0 Only								10% for Logic Gates only	Power= 10% LEDs= 10% Switches=10% Logic Probe= 10% Hexadecimal= 20% NOT OR AND NAND=20%	10%	No= (-20%)			
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1	Bollean Simplification & Quartus	1	-	-	50%	25% for Logic Gates only	10%	5%	10%	10%	No= (-20%)			
					√	√	√	√	√	√	√	100%	09/27/19 10:56 am	Eric Oberto
Labs 2+			10%	10%	25%	10%	10%	5%	40%	10%	No= (-20%)			
2	Adder -- NAND	2	7	√	√	√	√	√	√	√	√	100%	10/18/19 11:06 am	Eric Oberto
3	Decoder: 1 Segment of 7Seg. Display	2	49	—	—	—	—	—	—	—	—	100	10-25-19 11:21	MS-A Blas
4	Flip-Flop #1	2												
5	Flip-Flop #2	2												
6	2 Digit Counter: 2 Decade Counters & Mux	2												