LAB 4 WALTZ COUNTER

CDA 3201C Section 003

NOVEMBER 7, 2019

PROFESSOR PETRIE
Summer Poissonnier
Z23492880

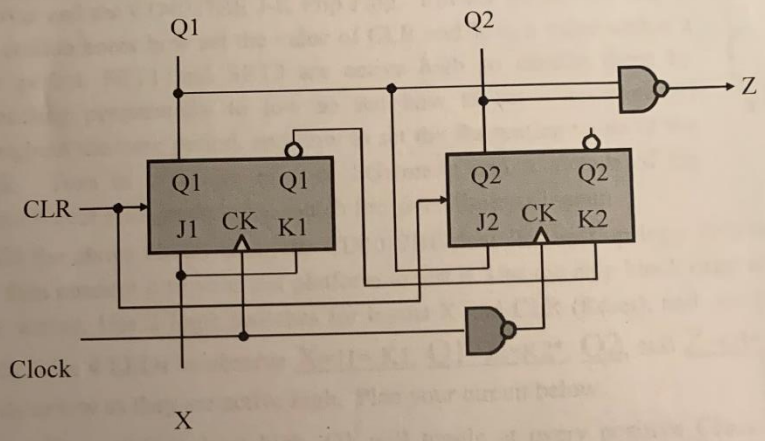
• CDA3201 • Intro to Logic Design •

Lab Assignment 4

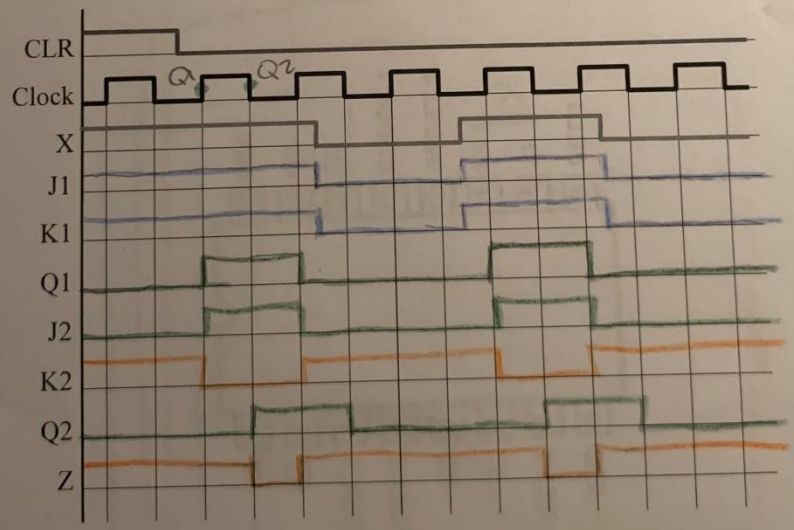
Name: Summer Poissonnier

Grade: /100

4) [40] Consider the following sequential circuit with two positive-edge-triggered JK flip-flops.



4.a) [4] Trace the timing diagram for the above circuit by hand.



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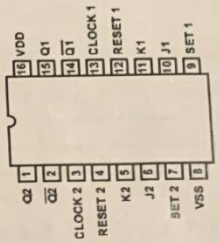
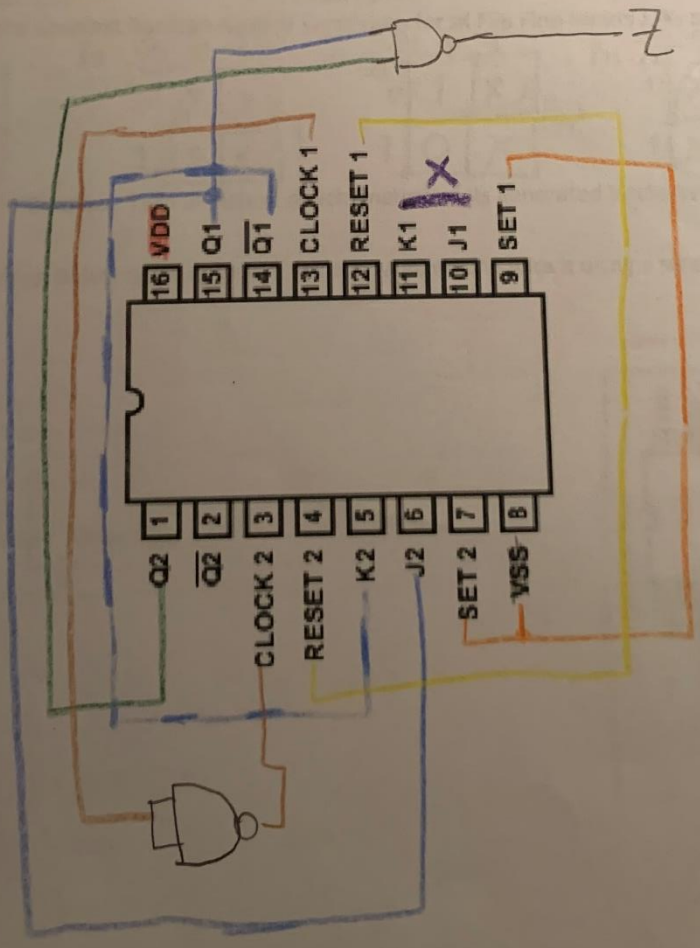
Name: **Grade:** /100



4.c) [8] Verify the circuit design/behavior by implementing the circuit using Quartus and the CD4027BE J-K Flip Flop. Review the PowerPoint in this section know how set the value of CLR and X to a value within a time period. SET1 and SET2 are active high so disable them by connecting permanently to low so see how to set a constant (0) throughout the time period, and how to set the fluctuating value of the clock. Turn in a picture of your Schematic and a picture of the VectorWaveForm generated to match the given timing diagram

4.b) [16] Build the above circuit using the CD4027BE dual JK flip-flop logic chip on your breadboard and then connect it to your test platform to test it. Use the chip block diagram below to plan for your wiring. Use 2 logic switches for inputs X and CLR (Reset), and one pulse switch for the Clock. Use 4 LEDs to observe X=J1= K1, Q1=J2=K2*, Q2, and Z=Q1*+Q2*. Tie the SET inputs to low as they are active high. Plan your circuit below.

Observation: If X is kept high, Q1 will toggle at every positive Clock transition because J1=K1=X=1 (toggle mode).



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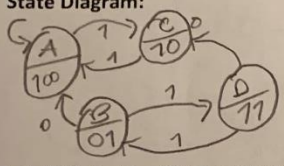
Lab Assignment 4

Name:

Grade: /100

4.d) [12] From the analysis of the circuit above, draw the State Table and the State Diagram.

State Diagram:

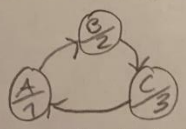


Present State		Input	Output	Next State	Flip Flop Transition
State	Q_2 Q_1	i	Z	Q_2^+ Q_1^+	J_2K_2 J_1K_1
A	00		1	0 1	01 01 0 01
B	01		1	1 0	1 01 01 01
C	10		1	1 1	01 1 01 01
D	11		0	0 0	01 01 01 01

4.e) [60] Build a "Waltz Counter", the Waltz is a dance where you keep time by counting 1, 2, 3, 1, 2, 3, 1, 2, 3, 1...

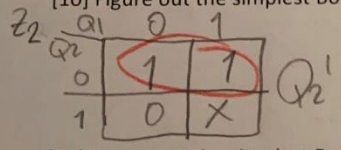
[10] Draw the State Diagram and Table

State Diagram:



Present State		Input	Output	Next State	Flip Flop Transition
State	Q_2 Q_1	i	Z_2 Z_1	Q_2^+ Q_1^+	J_2K_2 J_1K_1
A	00		11	B 0 1	0X 1X
B	01		10	C 1 0	1X X1
C	10		01	A 0 0	X1 0X
	11		XX	X X X	XX XX

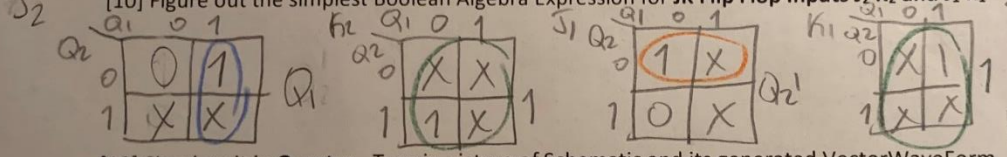
[10] Figure out the simplest Boolean Algebra Expression for 2 **Output bits Z_2 and Z_1**



$Z_2 = Q_2'$

$Z_1 = Q_1'$

[10] Figure out the simplest Boolean Algebra Expression for **JK Flip Flop Inputs J_2 K_2 and J_1 K_1**



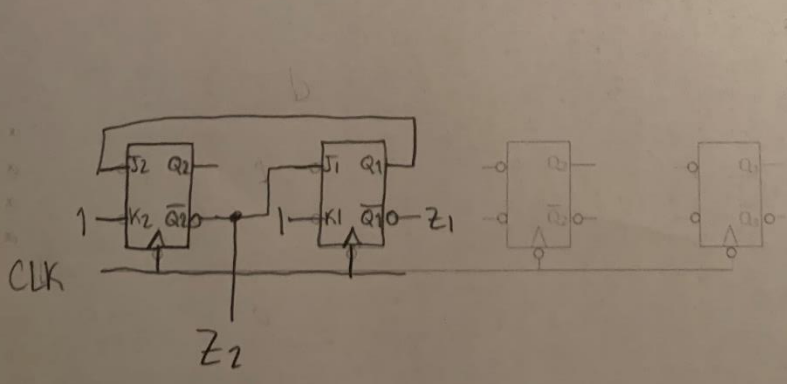
$J_2 = Q_1$

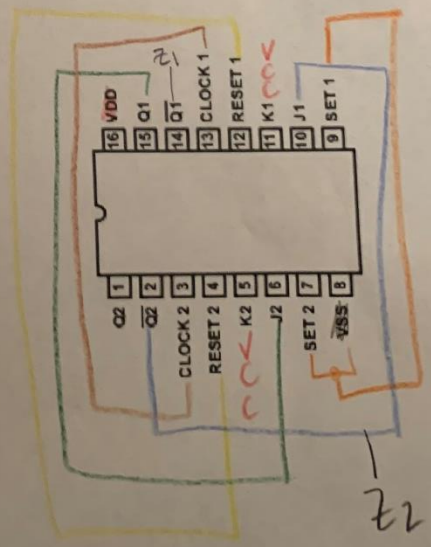
$J_1 = Q_2'$

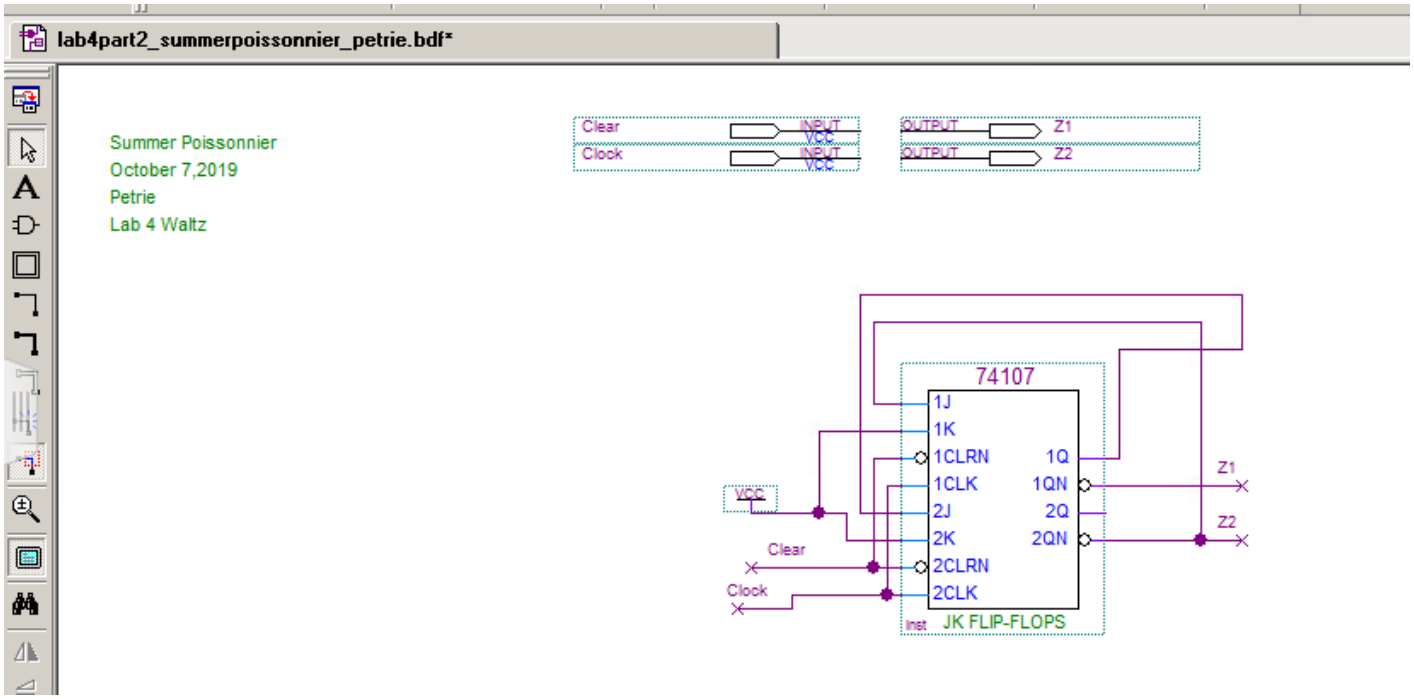
$K_2 = 1$ $K_1 = 1$

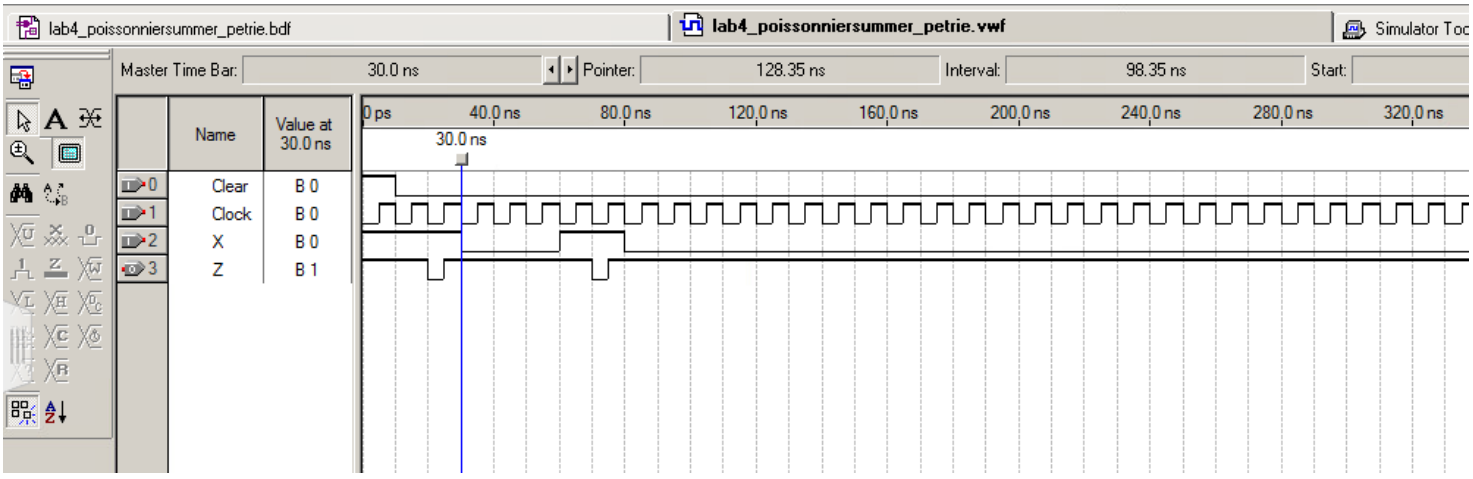
[10] Simulate it in **Quartus**. Turn in picture of Schematic and its generated VectorWaveForm

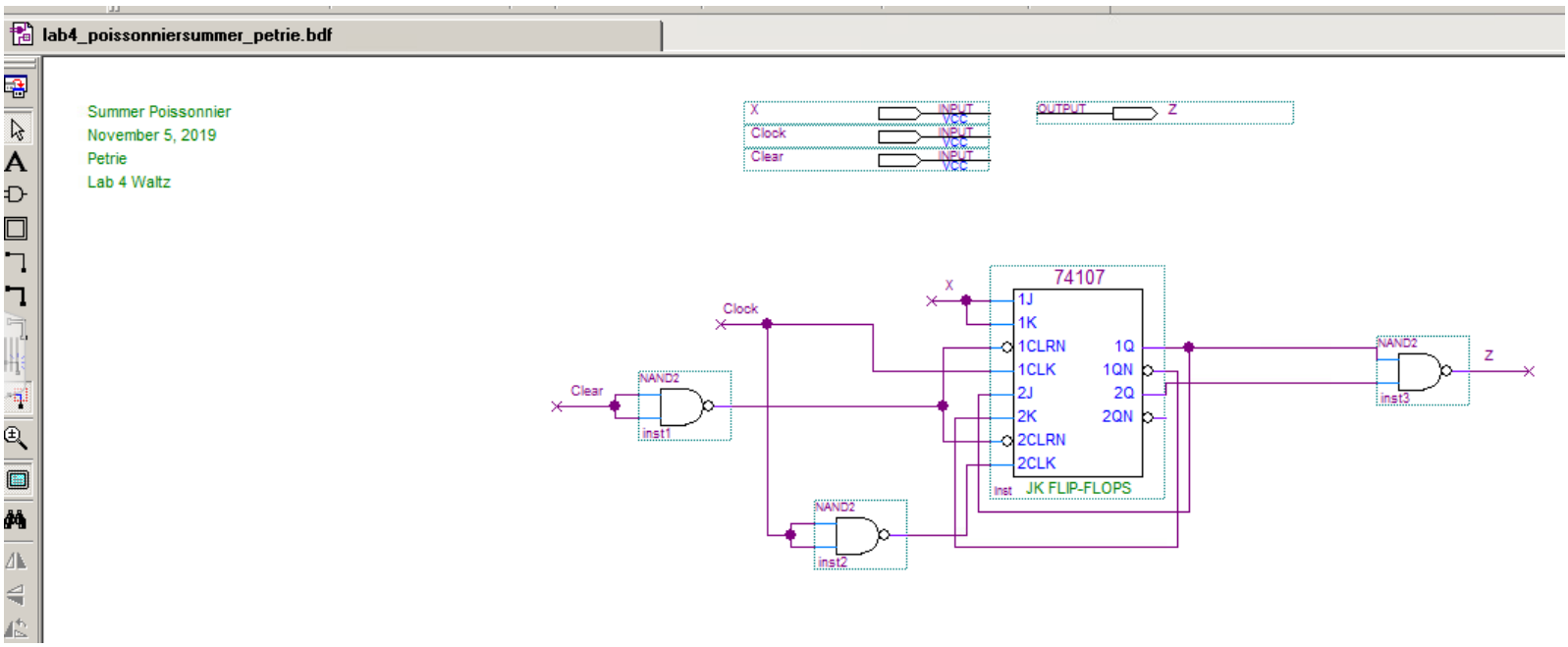
[20] Plan your wiring below using template below as a guide and wire it using a second CD4027BE J-K Flip

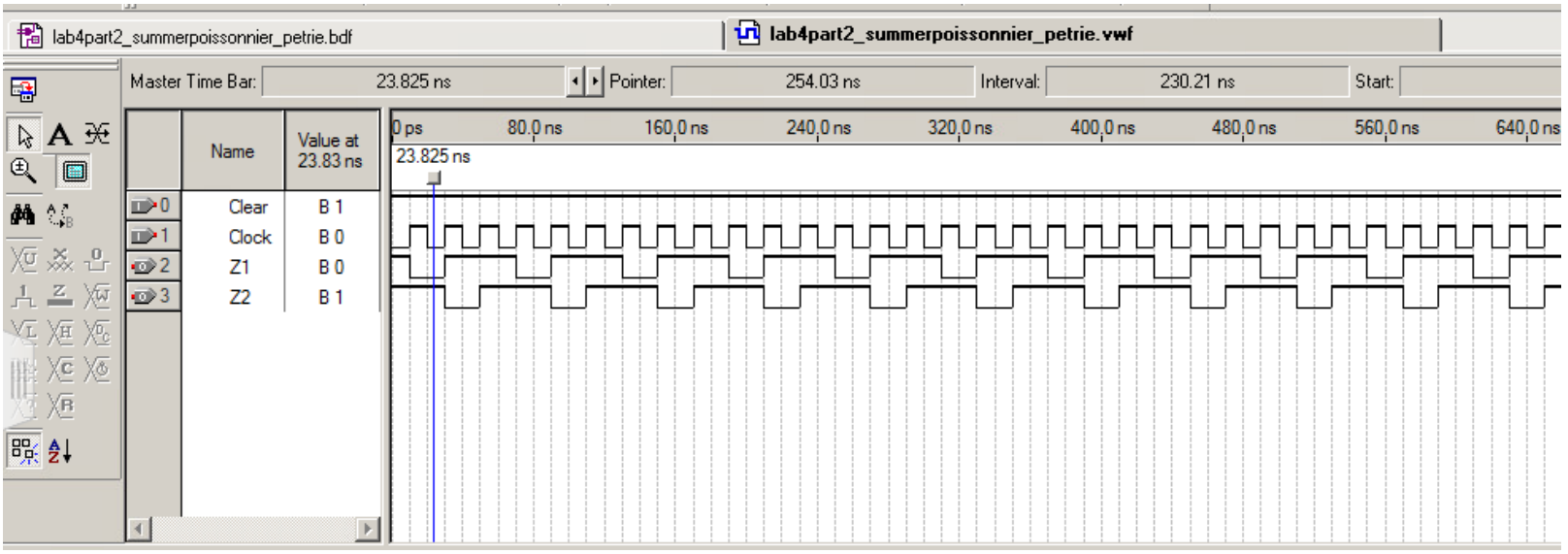





lab4part2_summerpoissonnier_petrie.bdf*
Summer Poissonnier
October 7,2019
Petrie
Lab 4 Waltz
Clear
Clock
INPUT
VCC
OUTPUT
Z1
Z2
74107
1J
1K
1CLRN
1CLK
2J
2K
2CLRN
2CLK
1Q
1QN
2Q
2QN
JK FLIP-FLOPS
inst


lab4_poissonniersummer_petrie.bdf
lab4_poissonniersummer_petrie.vwf
Simulator Too
Master Time Bar:
30.0 ns
Pointer:
128.35 ns
Interval:
98.35 ns
Start:
Name
Value at 30.0 ns
Clear
Clock
X
Z
B 0
B 0
B 0
B 1
0 ps
40.0 ns
80.0 ns
120.0 ns
160.0 ns
200.0 ns
240.0 ns
280.0 ns
320.0 ns
30.0 ns


lab4_poissonniersummer_petrie.bdf
Summer Poissonnier
November 5, 2019
Petrie
Lab 4 Waltz
X
Clock
Clear
INPUT
VCC
OUTPUT
Z
74107
1J
1K
1CLRN
1CLK
2J
2K
2CLRN
2CLK
1Q
1QN
2Q
2QN
JK FLIP-FLOPS
inst
NAND2
inst1
inst2
inst3


lab4part2_summerpoissonnier_petrie.bdf
lab4part2_summerpoissonnier_petrie.vwf
Master Time Bar:
23.825 ns
Pointer:
254.03 ns
Interval:
230.21 ns
Start:
Name
Value at 23.83 ns
0 Clear B 1
1 Clock B 0
2 Z1 B 0
3 Z2 B 1
0 ps
80.0 ns
160.0 ns
240.0 ns
320.0 ns
400.0 ns
480.0 ns
560.0 ns
640.0 ns
23.825 ns


Summer Poissonnier
Name Summer Poissonnier
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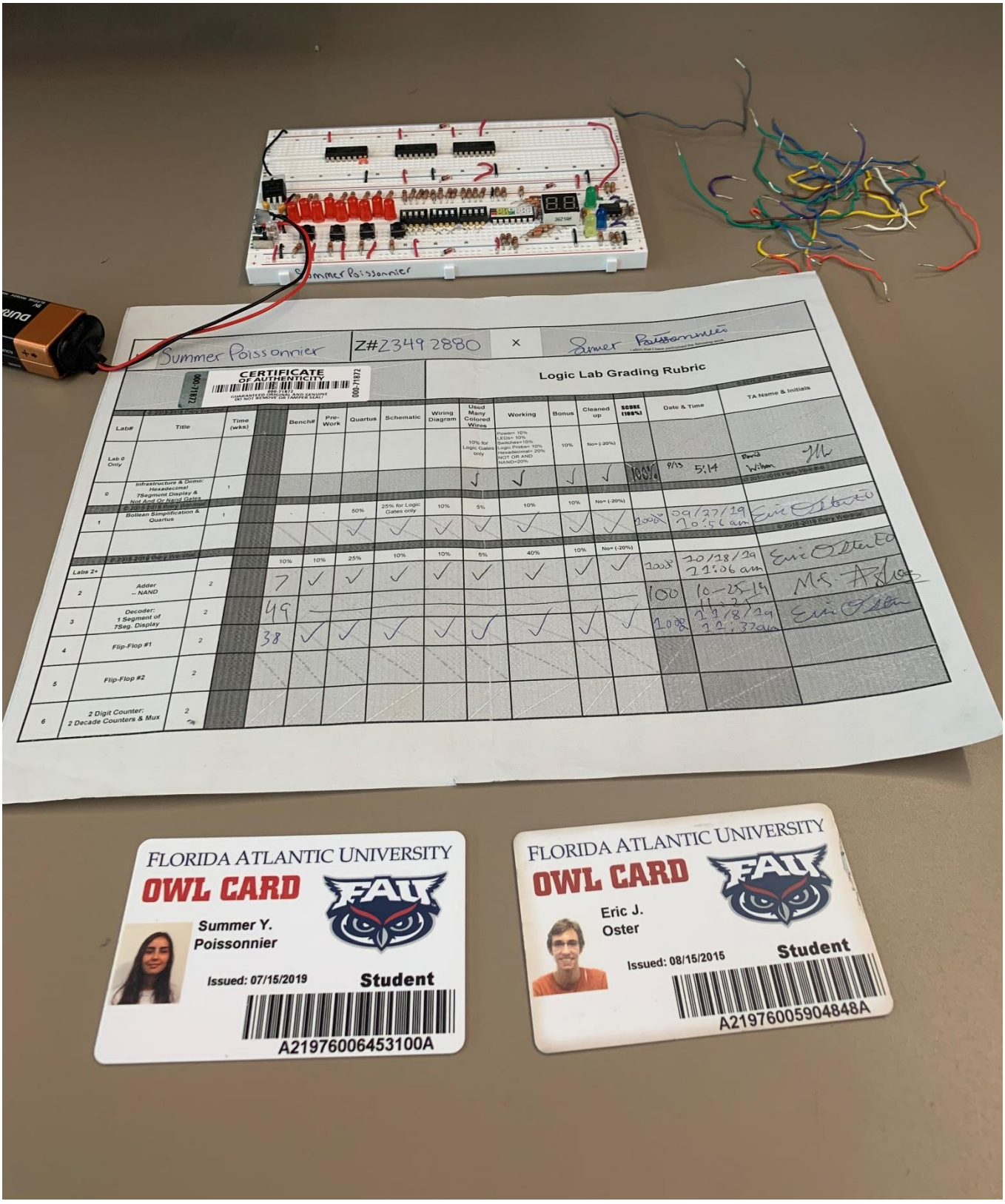
Logic Lab Grading Rubric
CERTIFICATE OF AUTHENTICITY
FLORIDA ATLANTIC UNIVERSITY
OWL CARD
Summer Y. Poissonnier
Issued: 07/15/2019
Student
A21976006453100A
FLORIDA ATLANTIC UNIVERSITY
OWL CARD
Eric J. Oster
Issued: 08/15/2015
Student
A21976005904848A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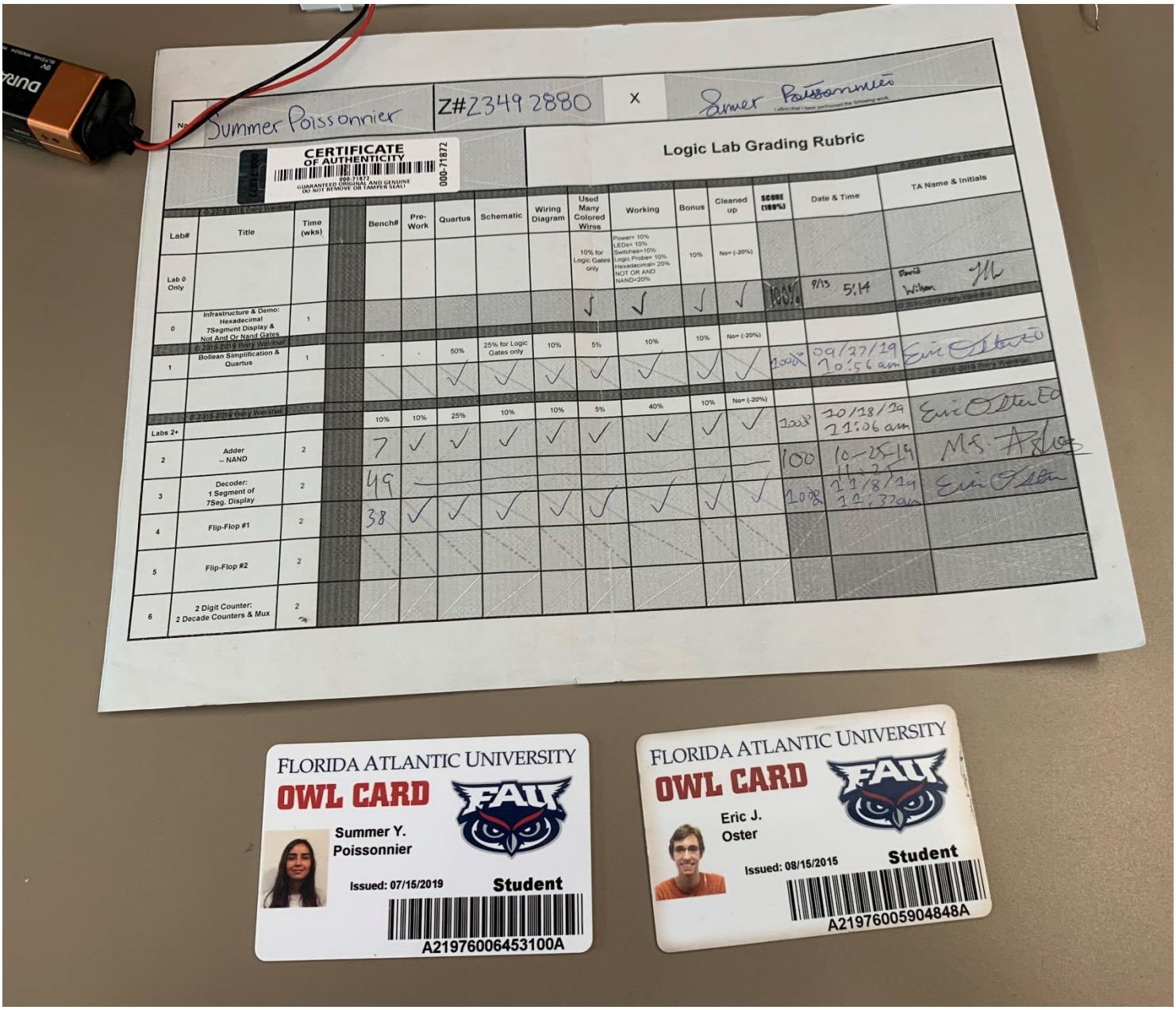

Name: Summer Poissonnier Z#Z3492880 X Summer Poissonnier
I affirm that I have performed the following work.

CERTIFICATE OF AUTHENTICITY
000-71872
GUARANTEED ORIGINAL AND GENUINE
DO NOT REMOVE OR TAMPER SEAL!

Logic Lab Grading Rubric

Lab#	Title	Time (wks)	Bench#	Pre-Work	Quartus	Schematic	Wiring Diagram	Used Many Colored Wires	Working	Bonus	Cleaned up	SCORE (100%)	Date & Time	TA Name & Initials
								10% for Logic Gates only	Power= 10% LEDs= 10% Switches=10% Logic Probe= 10% Hexadecimal= 20% NOT OR AND NAND=20%	10%	No= (-20%)			
Lab 0 Only								√	√	√	√	100%	9/13 5:14	David Wilson
0	Infrastructure & Demo: Hexadecimal 7Segment Display & Not And Or Nand Gates	1												
1	Boolean Simplification & Quartus	1	-	-	50%	25% for Logic Gates only	10%	5%	10%	10%	No= (-20%)			
					√	√	√	√	√	√	√	100%	09/27/19 10:56 am	Eric Oster
Labs 2+			10%	10%	25%	10%	10%	5%	40%	10%	No= (-20%)			
2	Adder -- NAND	2	7	√	√	√	√	√	√	√	√	100%	10/18/19 21:06 am	Eric Oster
3	Decoder: 1 Segment of 7Seg. Display	2	49	—							—	100	10-25-19 11:25	MS-A&L
4	Flip-Flop #1	2	38	√	√	√	√	√	√	√	√	100%	11/8/19 11:37am	Eric Oster
5	Flip-Flop #2	2												
6	2 Digit Counter: 2 Decade Counters & Mux	2												

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