LAB 6 DUAL COUNTER

CDA 3201C Section 003

DECEMBER 3, 2019

PROFESSOR PETRIE
Summer Poissonnier
Z23492880

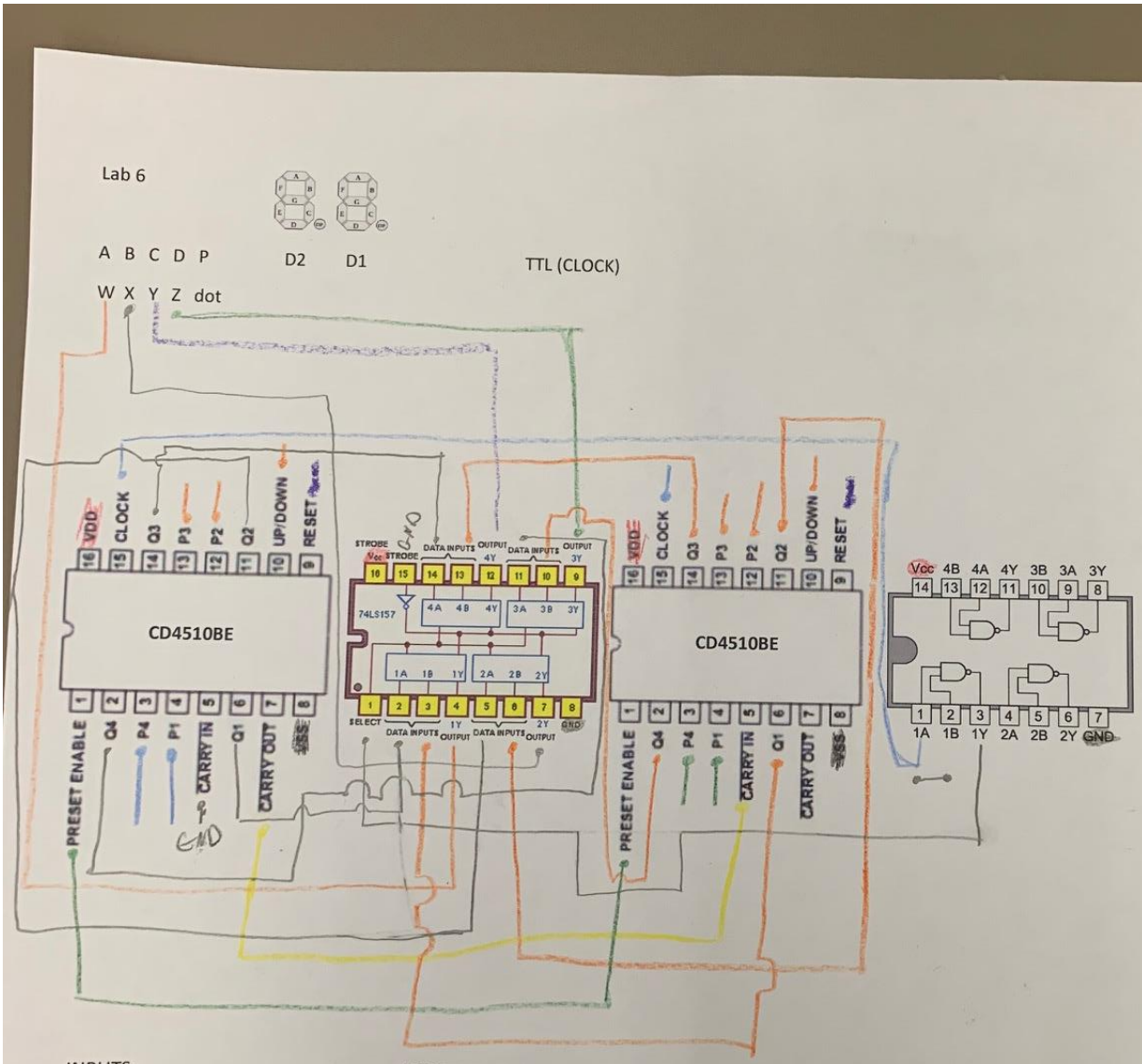
Lab 6

A B C D P

W X Y Z dot

D2 D1

TTL (CLOCK)



INPUTS: PRESET-ENABLE RESET UP/DOWN SW1 [8 4 2 1] SW2 [8 4 2 1]

Inputs				Output Y	
Strobe	Select	A	B	LS157	LS158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = High Level, L = Low Level, X = Don't Care

74LS157

Pin 1 Select = Clock

Pin 15 Strobe = GND

Pin 4, 7, 9 12 = outputs, go to LE figure out if to A,B,C,D or D,C,B,A

Clock = is TTL in Clock section of Blue Logic Analyzer, put through NOT. To attach clock to D2 and NOT clock to D1. Make one line on breadboard clock signal, ther take from there, you will need 5 Clock and 1 NOT Clock connections

CD4510BE

Pin 1 Preset Enable = Parallel Load, attach both to switch. loads when 1.

Pin 9 Reset = attach both to switch. It clears when 1.

Clock = TTL

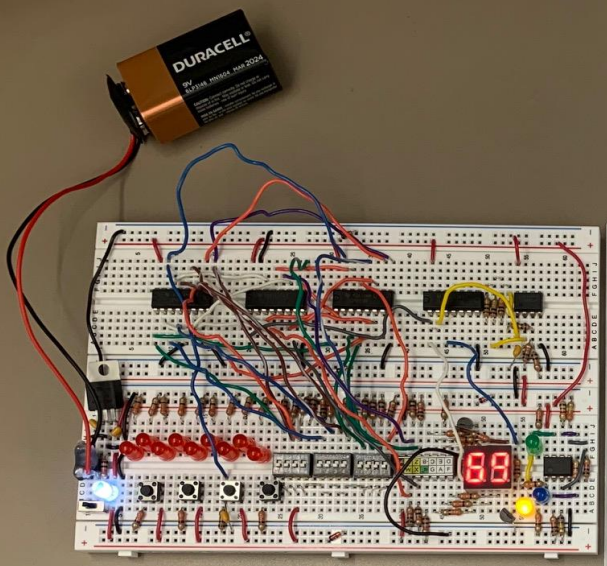
Pin 10 Up/Down = attach to switch, Counts up when 1, otherwise counts down.

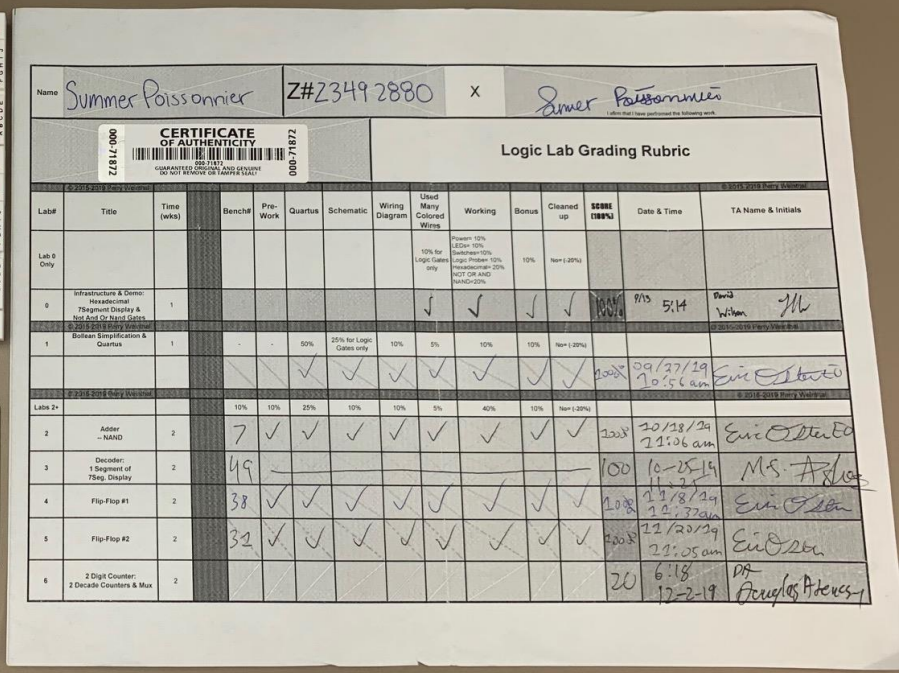
Pin 4, 12, 13, 3 = inputs, attac each chip to 4 switches, one for the LSD One's Digit (Right or B in MUX), and one for MS Ten's Digit (Left or A in MUX)

Pin 6, 11, 14, 2 = outputs go t MUX as shown in lab manua

Pin 5,7 = Carry (active low) in LSD, Carry In=GND,

in MSD, Carry In of MSD = Carry Out of LSD





Name: Summer Poissonnier | Z#Z3492880 | X: Summer Poissonnier — I affirm that I have performed the following work.

CERTIFICATE OF AUTHENTICITY 000-71872 — GUARANTEED ORIGINAL AND GENUINE DO NOT REMOVE OR TAMPER SEAL!

Logic Lab Grading Rubric

Lab#	Title	Time (wks)	Bench#	Pre-Work	Quartus	Schematic	Wiring Diagram	Used Many Colored Wires	Working	Bonus	Cleaned up	SCORE (100%)	Date & Time	TA Name & Initials
Lab 0 Only								10% for Logic Gates only	Power= 10% LED= 10% Switches=10% Logic Probes 10% Hexadecimal= 20% NOT OR AND NAND=20%	10%	No= (-20%)			
0	Infrastructure & Demo: Hexadecimal 7Segment Display & Not And Or Nand Gates	1						√	√	√	√	100%	9/13 5:14	David Wilson
1	Boolean Simplification & Quartus	1	-	-	50%	25% for Logic Gates only	10%	5%	10%	10%	No= (-20%)			
					√	√	√	√	√	√	√	100%	09/27/19 10:56 am	Eric Olten
Labs 2+				10%	10%	25%	10%	10%	5%	40%	10%	No= (-20%)			
2	Adder – NAND	2		7	√	√	√	√	√	√	√	√	100%	10/18/19 11:06 am	Eric Olten
3	Decoder: 1 Segment of 7Seg. Display	2		49	—							—	100	10-25-19 11:21	M.S. A
4	Flip-Flop #1	2		38	√	√	√	√	√	√	√	√	100%	11/8/19 10:32am	Eric Olten
5	Flip-Flop #2	2		32	√	√	√	√	√	√	√	√	100%	11/20/19 11:05 am	Eric Olten
6	2 Digit Counter: 2 Decade Counters & Mux	2											20	6:18 12-2-19	DA Douglas Athenosy

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3	Decoder: 1 Segment of 7Seg. Display	2	49	—	—	—	—	—	—	—	—	100	10-25-19 11:25	M.S.
4	Flip-Flop #1	2	38	√	√	√	√	√	√	√	√	100%	11/8/19 12:37pm	Eric Olsen
5	Flip-Flop #2	2	32	√	√	√	√	√	√	√	√	100%	11/20/19 11:05 am	Eric Olsen
6	2 Digit Counter: 2 Decade Counters & Mux	2										20	6:18 12-2-19	DA Douglas Athenosy

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