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Verilog Code

H0_counter

```
module H0_counter(count,TC,clr_, enb, clk, h11) ;
output reg [3:0] count ;
output reg TC ;
input clr_, enb, clk, h11 ;

always @ (*)
        if(enb && count >= (h11 ? 3 : 9))
                TC = 1;
        else
                TC = 0;

always @ (posedge clk or negedge clr_) // combinational+sequential
        if (~clr_)
                count = 0 ;
        else if (enb)
                if (TC)
                        count = 0;
                else
                        count = count + 1;
endmodule
```

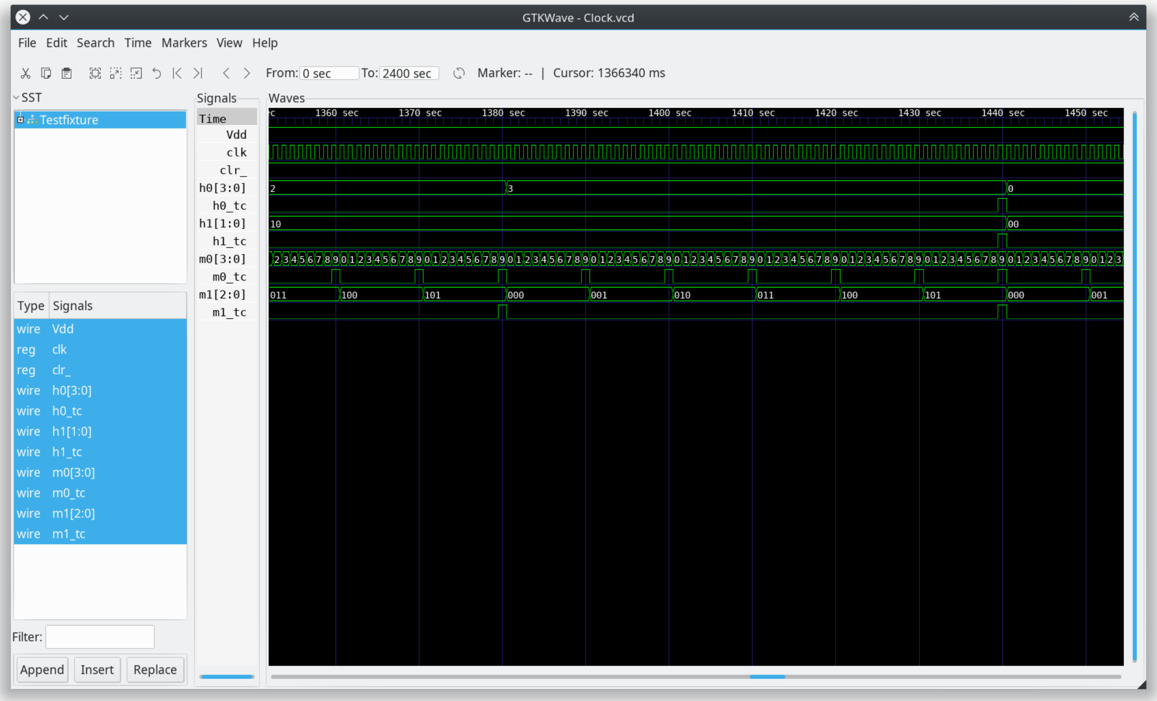
H1_counter

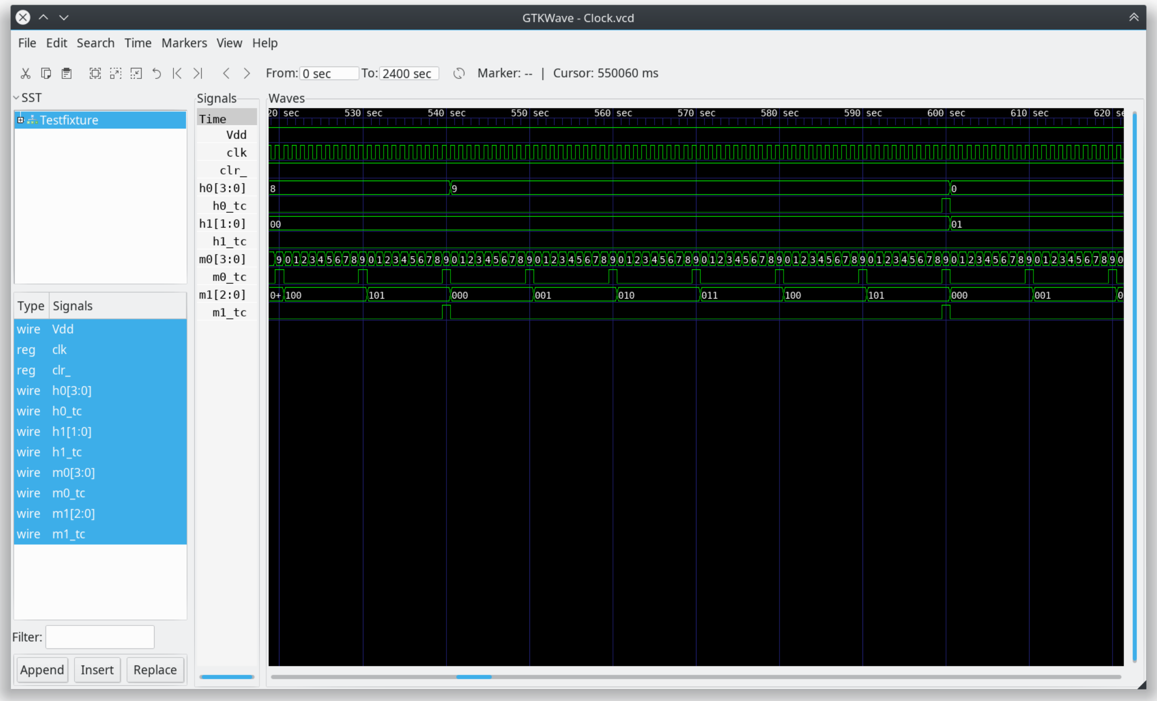
```
module H1_counter(count,TC,clr_, enb, clk) ;
output reg [1:0] count ;
output reg TC ;
input clr_, enb, clk ;

always @ (*)
        if(enb && count >= 2)
                TC = 1;
        else
                TC = 0;

always @ (posedge clk or negedge clr_) // combinational+sequential
        if (~clr_)
                count = 0 ;
        else if (enb)
                if (TC)
                        count = 0;
                else
                        count = count + 1 ;
endmodule
```

Testfixture

```
module Testfixture ;
wire Vdd = 1'b1;
reg clk, clr_;
wire [3:0] m0 ;
wire [2:0] m1 ;
wire [3:0] h0 ;
wire [1:0] h1 ;

BCD_counter M0 (m0,m0_tc,clr_, Vdd, clk) ;
Hex_counter M1 (m1,m1_tc,clr_, m0_tc, clk) ;
H1_counter H1 (h1,h1_tc,clr_, h0_tc, clk) ;
H0_counter H0 (h0,h0_tc,clr_, m1_tc, clk, h1[1]) ;


//Stimulus
initial
begin
        clk = 1'b0 ;
        repeat(4800)
                #5 clk = ~clk ;
        $finish ;
end

initial
begin
  clr_ = 0;
  #6  clr_ = 1'b1;
end

initial
begin
$dumpfile("Clock.vcd");
$dumpvars;
end

endmodule
```

Timing diagram


GTKWave - Clock.vcd
File Edit Search Time Markers View Help
From: 0 sec To: 2400 sec
Marker: -- | Cursor: 1366340 ms
SST
Testfixture
Type Signals
wire Vdd
reg clk
reg clr_
wire h0[3:0]
wire h0_tc
wire h1[1:0]
wire h1_tc
wire m0[3:0]
wire m0_tc
wire m1[2:0]
wire m1_tc
Filter:
Append Insert Replace
Signals
Time
Vdd
clk
clr_
h0[3:0]
h0_tc
h1[1:0]
h1_tc
m0[3:0]
m0_tc
m1[2:0]
m1_tc
Waves
1360 sec 1370 sec 1380 sec 1390 sec 1400 sec 1410 sec 1420 sec 1430 sec 1440 sec 1450 sec
2 3 0
10 00
011 100 101 000 001 010 011 100 101 000 001


GTKWave - Clock.vcd
File Edit Search Time Markers View Help
From: 0 sec To: 2400 sec
Marker: -- | Cursor: 550060 ms
SST
Testfixture
Type Signals
wire Vdd
reg clk
reg clr_
wire h0[3:0]
wire h0_tc
wire h1[1:0]
wire h1_tc
wire m0[3:0]
wire m0_tc
wire m1[2:0]
wire m1_tc
Filter:
Append Insert Replace
Signals
Time
Vdd
clk
clr_
h0[3:0]
h0_tc
h1[1:0]
h1_tc
m0[3:0]
m0_tc
m1[2:0]
m1_tc
Waves
20 sec 530 sec 540 sec 550 sec 560 sec 570 sec 580 sec 590 sec 600 sec 610 sec 620 se
8 9 0
00 01
0+ 100 101 000 001 010 011 100 101 000 001 0