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Verilog Code

(Modified Part)

```
module GCDdatapath (clk, operand_A, operand_B, result_data, A_en, B_en,
A_sel, B_sel, B_zero, A_lt_B);
parameter A_sel_In= 2'b00;
parameter A_sel_B=2'b01;
parameter A_sel_Sub=2'b10;
parameter A_sel_X=2'bxx;
parameter B_sel_In= 1'b0;
parameter B_sel_A= 1'b1;
parameter B_sel_X=1'bx;
parameter W = 16;
input clk;
// Data signals
input [W-1:0] operand_A, operand_B;
output [W-1:0] result_data;
// Control signals (ctrl->dpath)
input A_en, B_en;
input [1:0] A_sel;
input B_sel;
// Control signals (dpath->ctrl)
output B_zero, A_lt_B;

reg [W-1:0] A_out;
reg [W-1:0] A;
reg [W-1:0] B_out;
reg [W-1:0] B;
wire [W-1:0] sub_out;
wire [W-1:0] sub_out_2;

always @(*)
        case (A_sel)
        A_sel_In: A_out = operand_A ;
        A_sel_B: A_out = sub_out_2;
        A_sel_Sub: A_out = sub_out;
        default: A_out = 16'bx ;
        endcase

always @(posedge clk)
        if (A_en)
                A = A_out;
```

```
always @(*)
        case(B_sel)
        B_sel_In: B_out = operand_B ;
        B_sel_A: B_out = A ;
        default: B_out = 16'bx ;
        endcase

always @(posedge clk)
        if (B_en)
                B = B_out ;

assign B_zero = (B==0);
assign A_lt_B = (A < B);
assign sub_out = A - B;
assign sub_out_2 = B - A;
assign result_data = A;
endmodule
```

Timing diagram