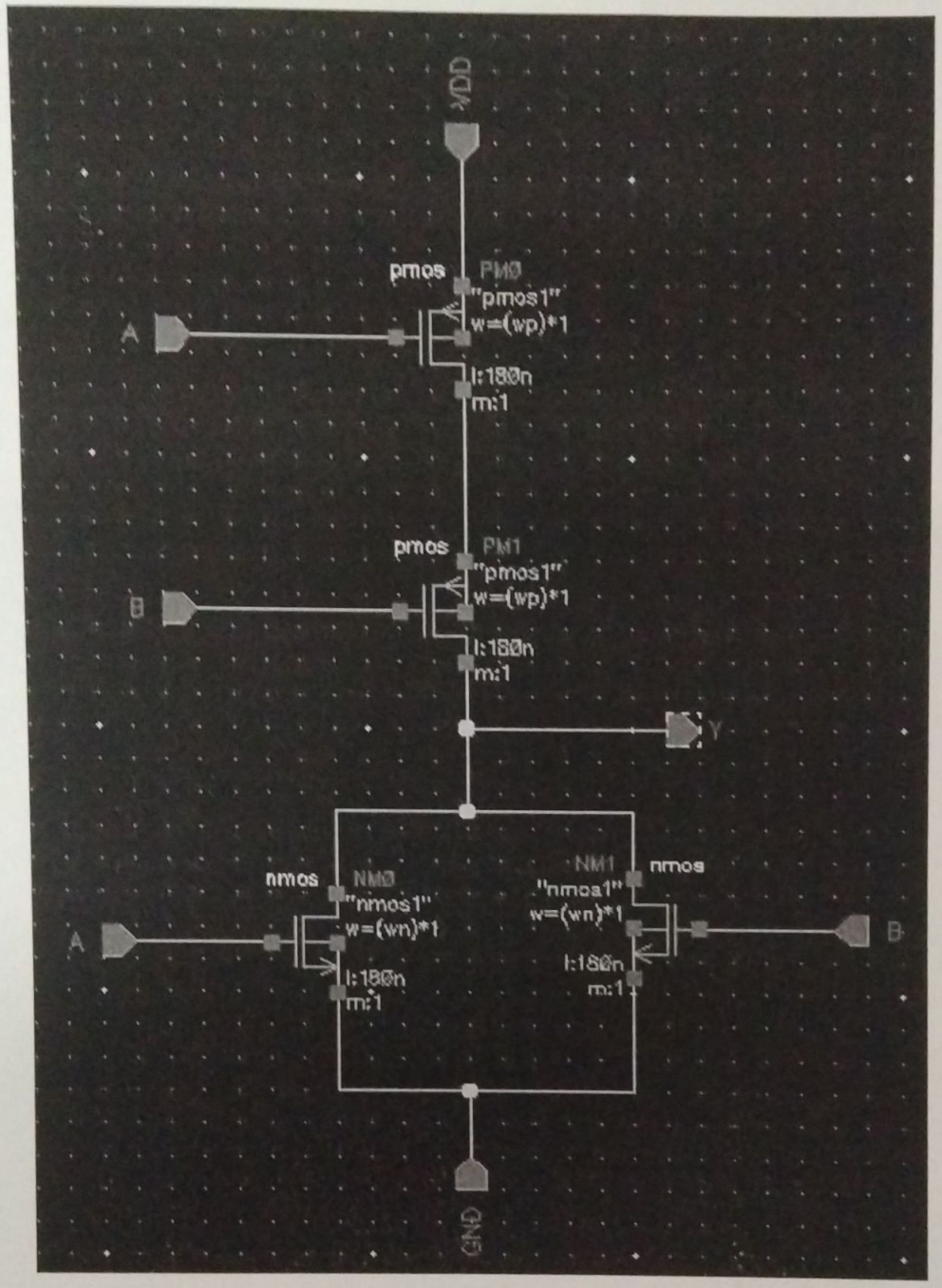
EXPERIMENT - 9

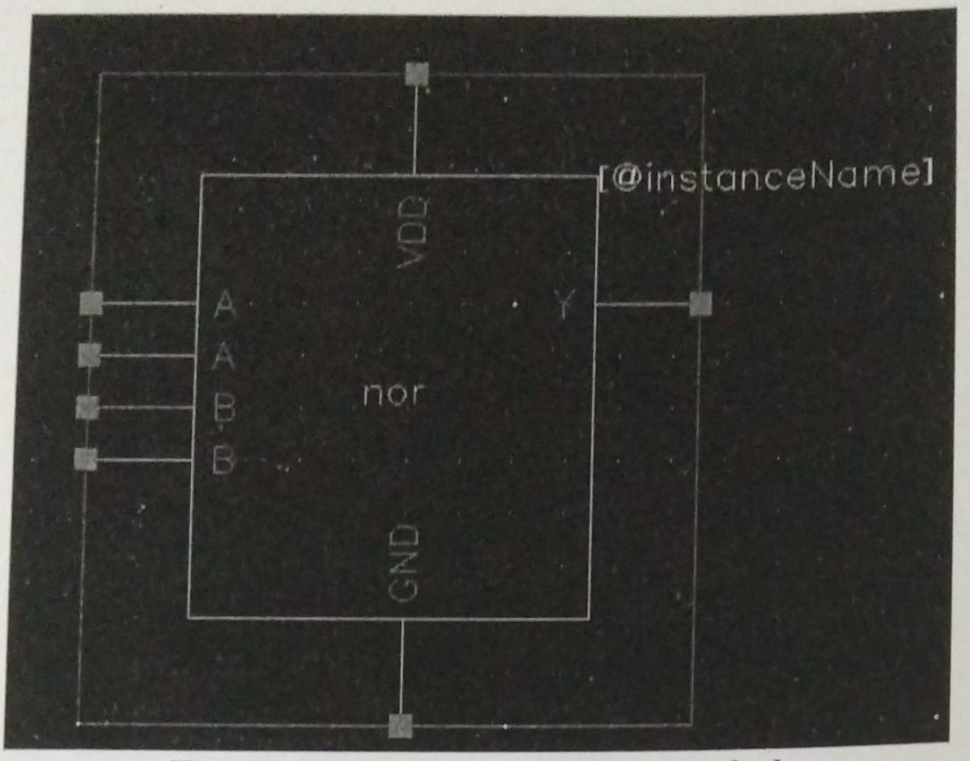
Capture the schematic of 2-input CMOS NOR gate having similar delay as that of CMOS inverter computed in experiment 1. Verify the functionality of NOR gate and also find out the delay t_d for all four possible combinations of input vectors. Tabulate the result. Increase the drive strength to 2X and 4X and tabulate the result.



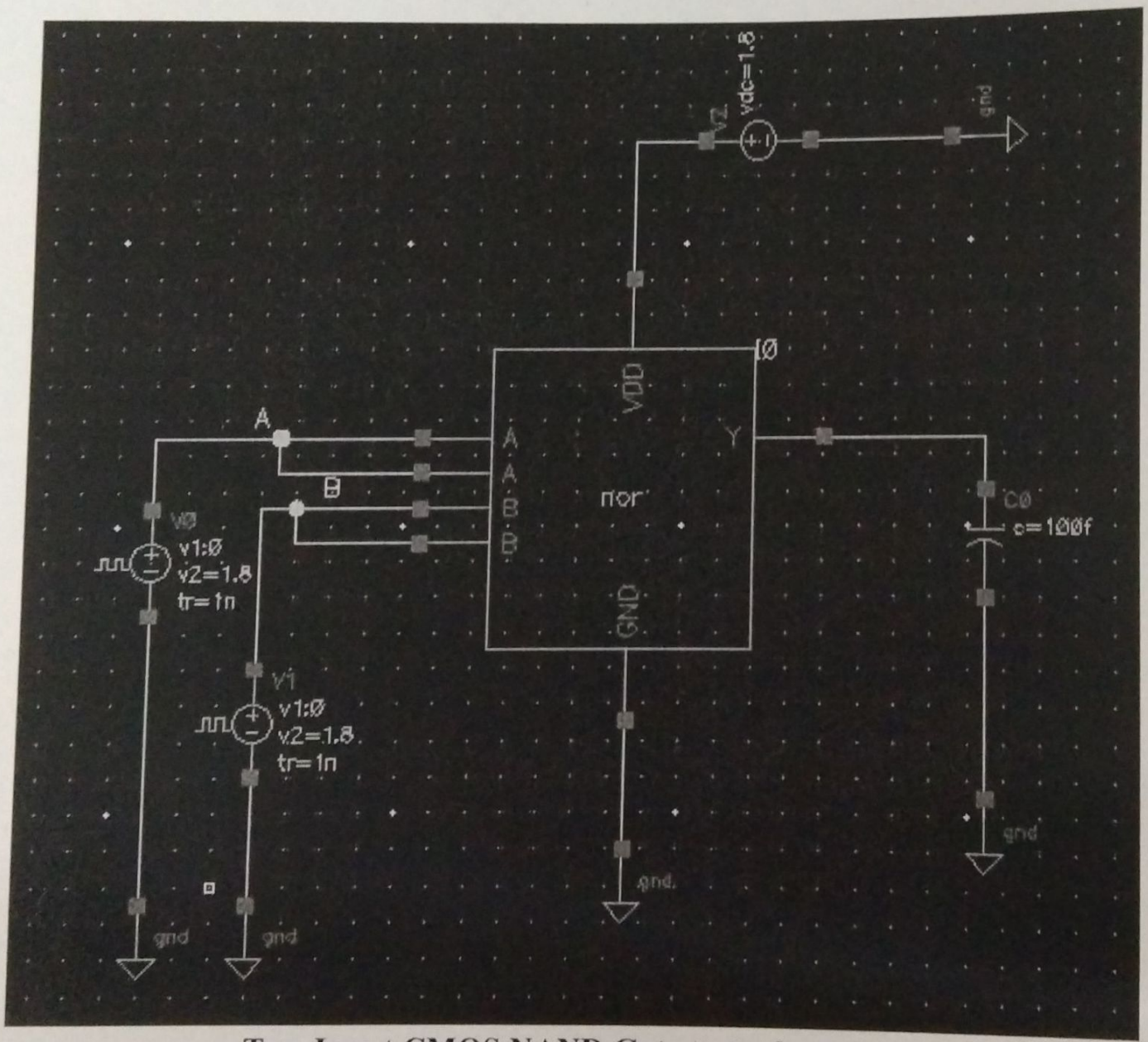
Two Input CMOS NOR Gate schematic

Table of components for building the schematic:

Library Name	Cell Name	Properties
gpdk180	pmos	W = Wp, L = 180n
gpdk180	nmos	W = Wn, L = 180n



Two Input CMOS NOR Gate symbol



Two Input CMOS NAND Gate test schematic

Table of components for building the test schematic:

Library Name	Cell Name	Properties
analogLib	Vpulse	V1 = 0, V2 = 1.8, Period = 20n, Rise time = 1n, Fall time = 1n, Pulse width = 10n
analogLib	Vpulse	V1 = 0, V2 = 1.8, Period = 50n, Rise time = 1n, Fall time = 1n, Pulse width = 25n
analogLib	Vdc	Vdc = 1.8
analogLib	gnd	
analogLib	cap	100pF

Table of values to setup for different analysis:

Analysis Name	Settings	Properties
Transient	trans	Stop time = 50n, moderate

Analog Simulation with spectre for Two Input CMOS NOR Gate:

b) Transient Response

Tabulated Values of Delay:

Values of t_{phl}, t_{plh} and t_{pd} for different geometries

MOSFET	Width	t_{phl} (ps)	t_{plh} (ps)	t_{pd} (ps)
pmos	4u			
nmos	1u			
pmos	8u			
nmos	2u			
pmos	16u			
nmos	4u			

Tabulated Values of Delay:

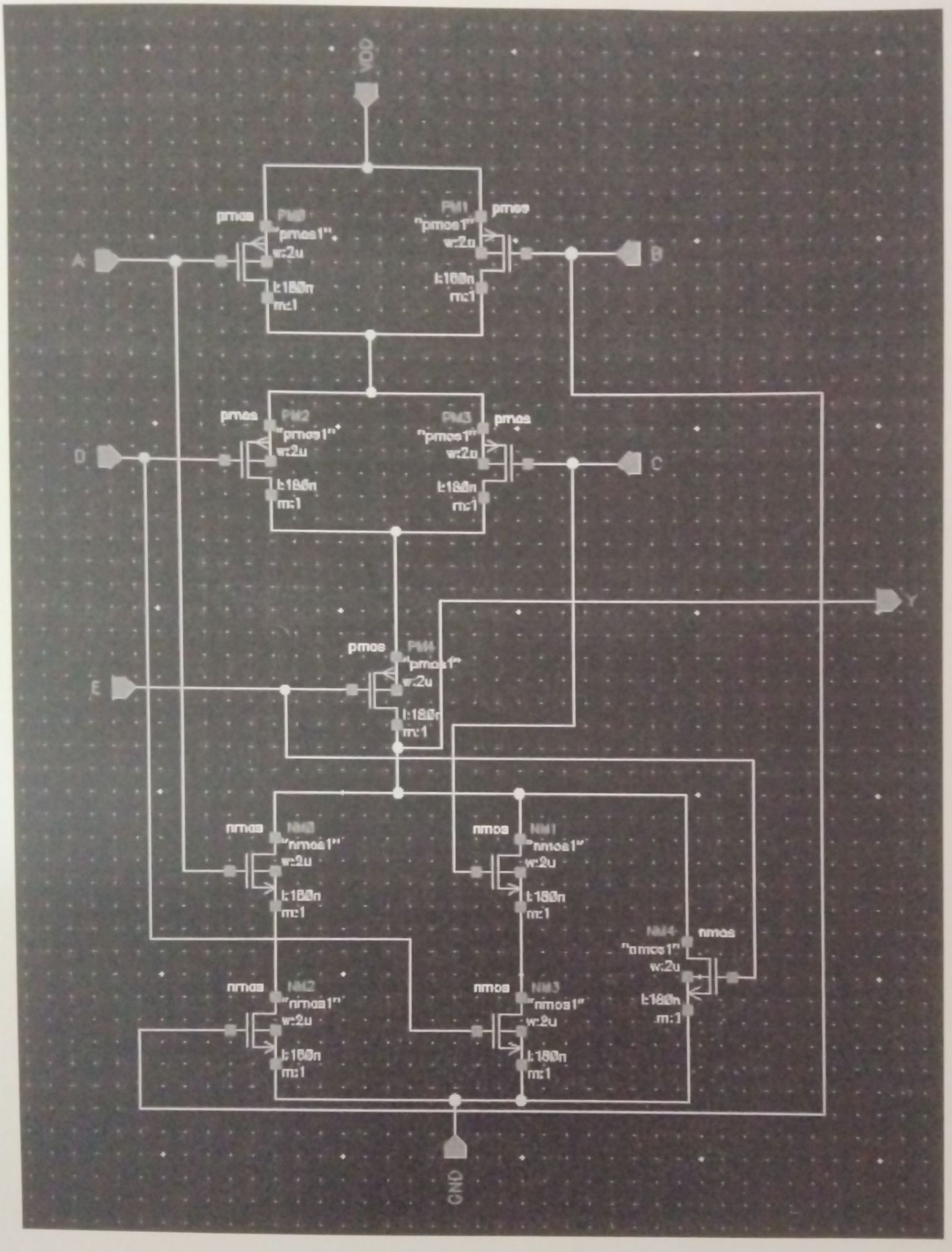
Values of t_{phl}, t_{plh} and t_{pd} for different geometries

	t_{phl} (ps)	t_{plh} (ps)	t_{pd} (ps)
Two Input CMOS NOR Gate Test Schematic			

Conclusion/Inference: (To be written by students)
Faculty Signature:

EXPERIMENT - 10

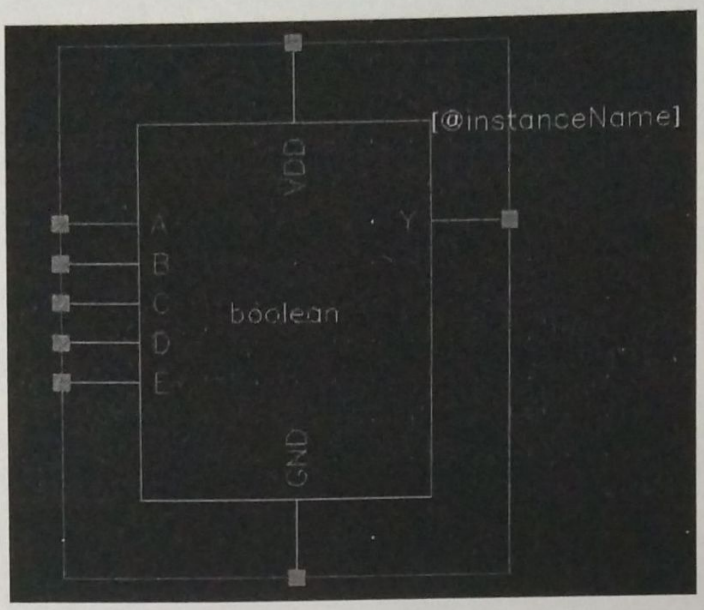
Capture the schematic of the Boolean Expression Y= AB+CD+E using CMOS Logic. Verify the functionality of the expression find out the delay td for some combination of input vectors. Table the results.



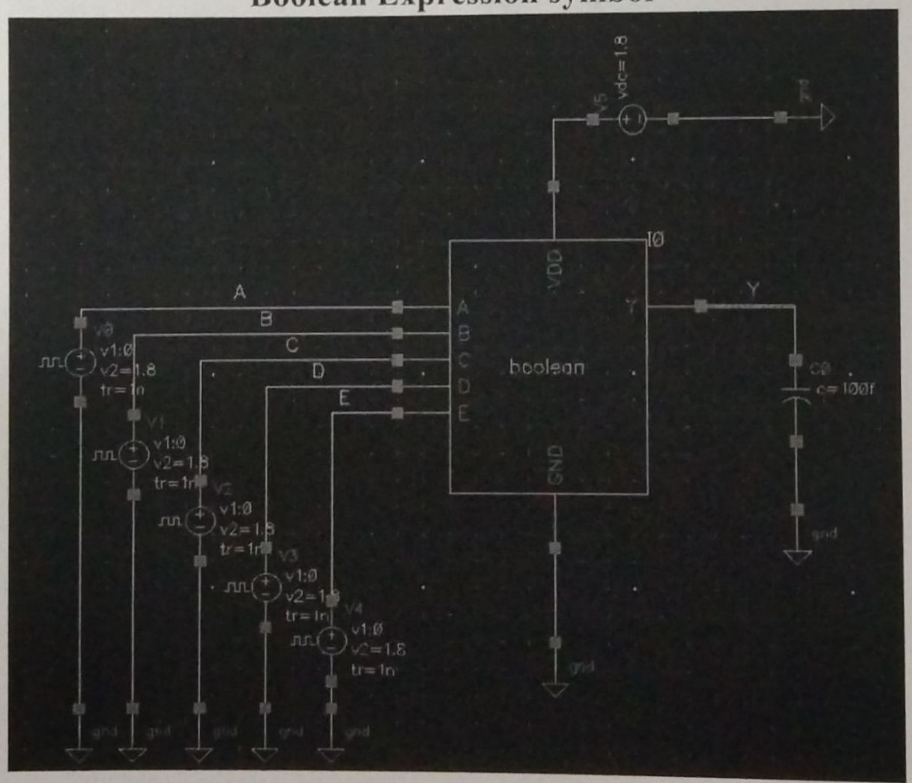
Boolean Expression schematic

Table of components for building the schematic:

Library Name	Cell Name	Properties
gpdk180	pmos	W = Wp, L = 180n
gpdk180	nmos	W = Wn, L = 180n



Boolean Expression symbol



Boolean Expression test schematic

Table of components for building the test schematic:

Library Name	Cell Name	Properties
analogLib	Vpulse	V1 = 0, V2 = 1.8, Period = 20n, Rise time = 1n, Fall time = 1n, Pulse width = 10n
analogLib	Vpulse	V1 = 0, V2 = 1.8, Period = 40n, Rise time = 1n, Fall time = 1n, Pulse width = 20n
analogLib	Vpulse	V1 = 0, V2 = 1.8, Period = 50n, Rise time = 1n, Fall time = 1n, Pulse width = 25n
analogLib	Vpulse	V1 = 0, V2 = 1.8, Period = 60n, Rise time = 1n, Fall time = 1n, Pulse width = 30n
analogLib	Vpulse	V1 = 0, V2 = 1.8, Period = 70n, Rise time = 1n, Fall time = 1n, Pulse width = 35n
analogLib	Vdc	Vdc = 1.8
analogLib	gnd	
analogLib	cap	100fF

Table of values to setup for different analysis:

Analysis Name	Settings	Properties
Transient	trans	Stop time = 200n, moderate

Analog Simulation with spectre for Boolean Expression

Transient Response

Tabulated Values of Delay:

Values of t_{phl}, t_{plh} and t_{pd} for different geometries

MOSFET	Width	t_{phl} (ps)	t_{plh} (ps)	t_{pd} (ps)
pmos	4u			
nmos	1u			
pmos	8u			
nmos	2u			
pmos	16u			
nmos	4u			

Tabulated Values of Delay:

Values of t_{phl}, t_{plh} and t_{pd}

	t_{phl} (ps)	t_{plh} (ps)	t_{pd} (ps)
Boolean Expression Schematic			

Conclusion/Inference: (To be written by students)
Faculty Signature: