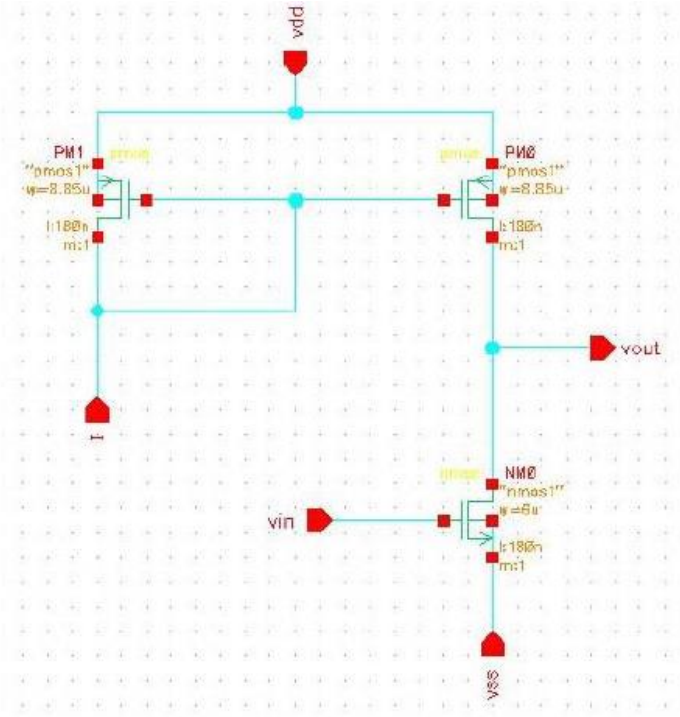
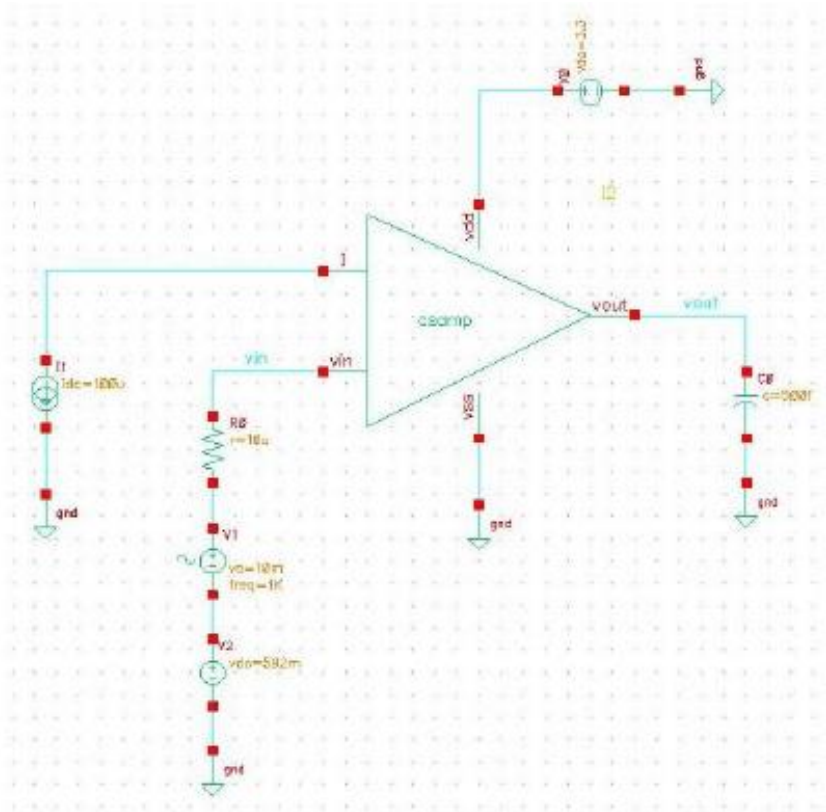



Common Source Amplifier schematic

**Table of components for building the schematic:**

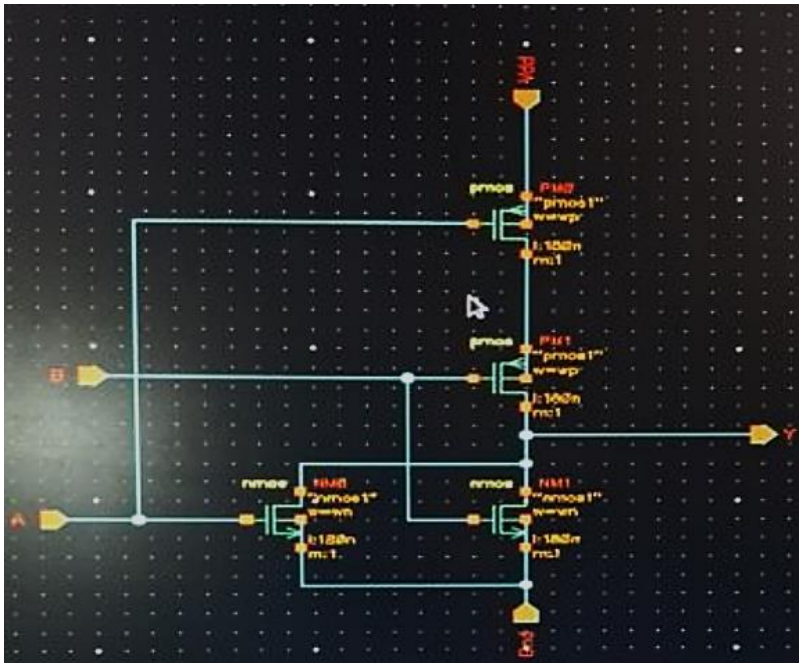
| Library Name | Cell Name | Properties |
|---|---|---|
| gpdk180 | pmos | W = 8.85u, L = 180n |
| gpdk180 | nmos | W = 6u, L = 180n |



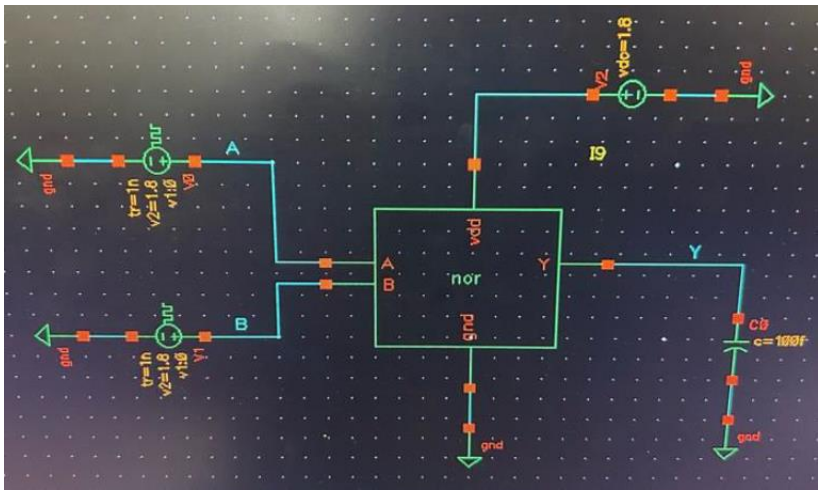

Common Source Amplifier test schematic

**Table of components for building the test schematic:**

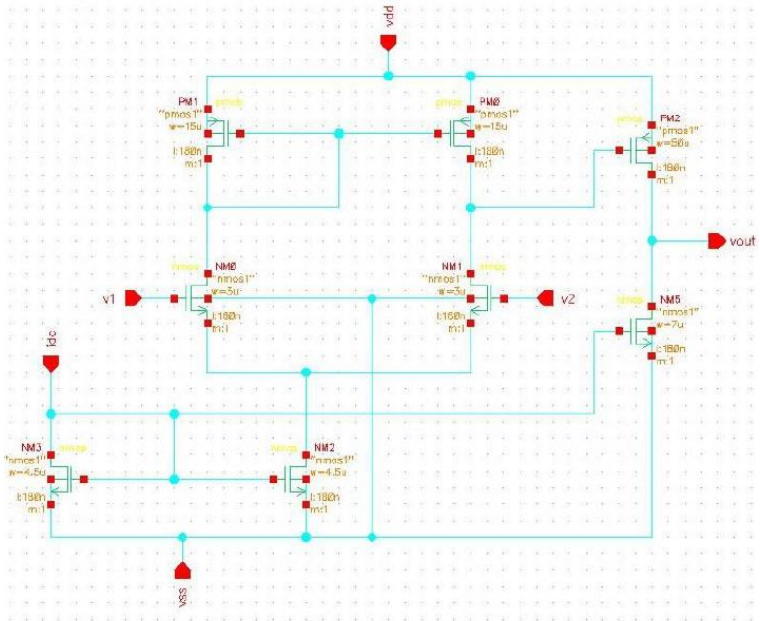
| Library Name | Cell Name | Properties |
|---|---|---|
| analogLib | Vdc | DC Voltage = 3.3 V ($V_{dd}$) |
| analogLib | Vsin | AC Magnitude = 1 V, Amplitude = 10u V, Frequency = 1K Hz |
| analogLib | Vdc | DC Voltage = 592m V |
| analogLib | res | Resistance = 10u Ohms |
| analogLib | idc | DC Current = 100u A |
| analogLib | cap | 500f F |



NOR GATE



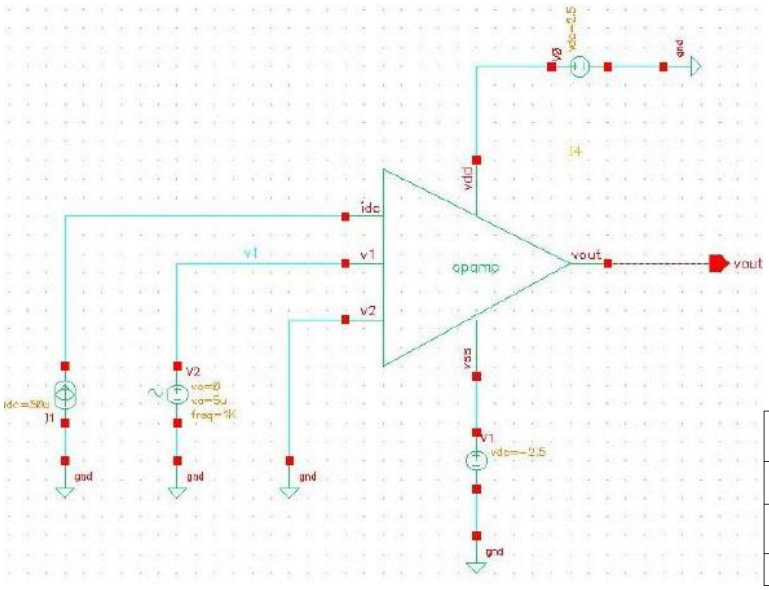

| Library Name | Cell Name | Properties |
|---|---|---|
| analogLib | Vpulse | V1 = 0, V2 = 1.8, Period = 30n, Rise time = 1n, Fall time = 1n, Pulse width = 15n |
| analogLib | Vpulse | V1 = 0, V2 = 1.8, Period = 20n, Rise time = 1n, Fall time = 1n, Pulse width = 10n |
| analogLib | Vdc | Vdc = 1.8 |
| analogLib | gnd | |
| analogLib | cap | 0.1pF |



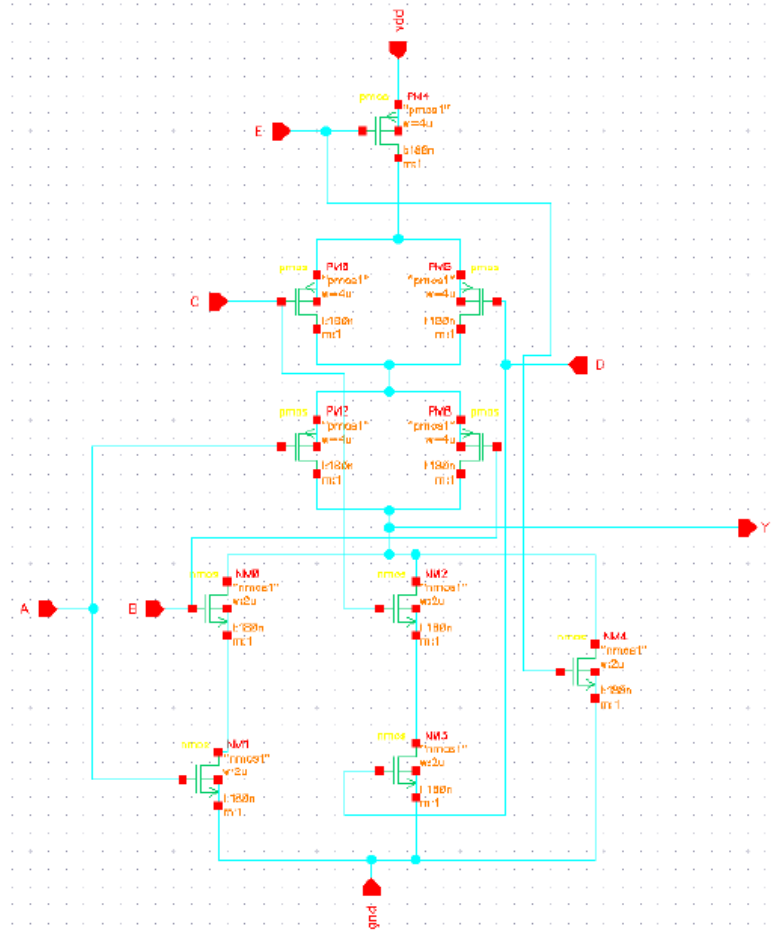

Operational Amplifier schematic

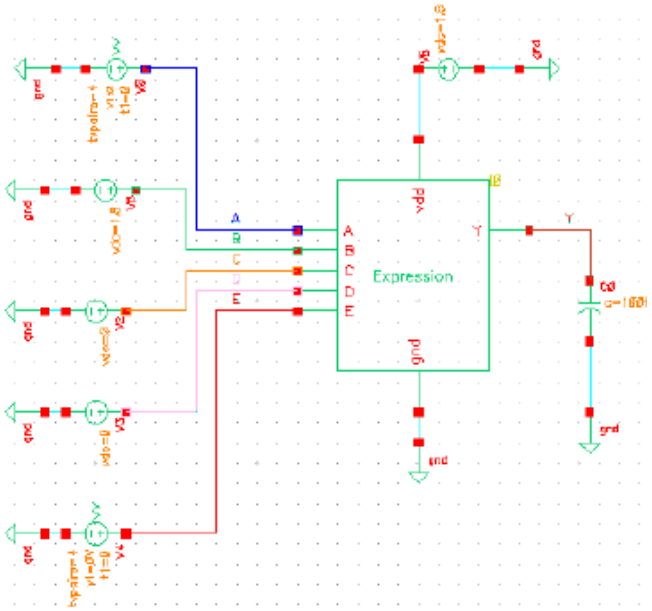
| Library Name | Cell Name | Properties |
|---|---|---|
| gpdk180 | pmos | W = 15u, L = 180n<br>W = 50u, L = 180n |
| gpdk180 | nmos | W = 3u, L = 180n<br>W = 4.5u, L = 180n<br>W = 7u, L = 180n |

CS AMP TEST SCHEMATIC




| Library Name | Cell Name | Properties |
|---|---|---|
| analogLib | Vdc | DC Voltage = 2.5 V ($V_{dd}$)<br>DC Voltage = -2.5 V ($V_{ss}$) |
| analogLib | Vsin | AC Magnitude = 1 V, DC Voltage = 0 V, Offset Voltage = 0 V<br>Amplitude = 5u V, Frequency = 1K Hz |
| analogLib | idc | DC Current = 30u A |




| | | |
|---|---|---|
| analogLib | Vpulse | For **input A**, V1 = 0, V2 = 1.8, Period = 160n, Rise time = 1n, Fall time = 1n, Pulse width = 80n |
| | Vpulse | For **input B**, V1 = 0, V2 = 1.8, Period = 80n, Rise time = 1n, Fall time = 1n, Pulse width = 40n |
| | Vpulse | For **input A**, V1 = 0, V2 = 1.8, Period = 40n, Rise time = 1n, Fall time = 1n, Pulse width = 20n |
| | Vpulse | For **input A**, V1 = 0, V2 = 1.8, Period = 20n, Rise time = 1n, Fall time = 1n, Pulse width = 10n |
| | Vpulse | For **input A**, V1 = 0, V2 = 1.8, Period = 10n, Rise time = 1n, Fall time = 1n, Pulse width = 5n |
| analogLib | Vdc | Vdc = 1.8 |
| analogLib | gnd | |
| analogLib | cap | 0.1pF |

boolean