

ECGR4101/s101 - Fall 2018 - Lab 3

Pin mapping

0 Vcc	Vcc	GND	GND	0
0 P1.0 (A0)	PB5 (AIN11)	PB2	P2.7	0
0 P1.1 (A1)	PB0	P2.0	P2.6	0
0 P1.2				0
0 P1.3 (sw2)	PE4 (AIN9)			0
0 P1.4	PES (AIN8)			0
0 P1.5	PB4 (AIN10)	PDO (AIN7)		0
0 P2.0	PA5	PA4	P2.50	
0 P2.1	PA6	PA3	P2.4	0
0 P2.2	PA7	PA2	P2.3	0

J1 ↑

Note

Your action item:

Will need to add a wire so that the daughterboard will work on both the MSP430 & Tiva boards.