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A design example of a 65 nm CMOS operational amplifier

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SUMMARY

In this paper, we discuss the properties of new nanometer-size CMOS technologies being important for the circuit designer. Thereby we concentrate on analogue circuit design. In the literature, the gain reduction by the high output conductance of the transistors is discussed. In detail, we further describe gain reduction due to gate-leakage current. Finally, we present a design example of a fully differential operational amplifier in a 65 nm CMOS technology including results. Copyright © 2007 John Wiley & Sons, Ltd.

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KEY WORDS: nanometer CMOS; gate leakage; tunnelling currents; operational amplifier; cascodes; gain boost; common-mode control

1. INTRODUCTION

The applications of semiconductor electronics always ask for more performance at a lower price. The constant progress in semiconductor technologies makes better and cheaper electronics feasible. New technologies enable the development of circuits with much more transistors. Especially digital circuits benefit most by structure size reduction. Because of the greater advantage in area reduction of smaller-structure-size CMOS processes for digital circuits, the tendency is to realize more and more functionality in digital circuits. The shrinking of the transistors leads to faster transistors which enable faster circuits and open up additional applications. The faster transistors enable also analogue circuits with higher speed [1, 2]. The process shrink however leads also to some

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disadvantages for the designs. The very short transistors can only withstand low drain–source voltages and also the very thin gate insulator limits the maximal useable supply voltage.

For digital circuits as for instance inverters, the minimum gain according to [3] is about 10 (20 dB). The low supply voltages and the finite sub-threshold swing lead to a static power consumption of digital CMOS circuits. For 65 nm and smaller structure-size processes, gate tunnelling currents occur through the ultra-thin gate insulator.

For analogue circuits, the impacts of these imperfections have much more influence. The output conductance of short-channel transistors is very large. The channel-length modulation factor is very large in 65 nm technology or in other words the Early voltage of transistors with gate lengths L of 360 nm is about 4 V and of shortest-channel transistors ($L = 65$ nm) it is below 1 V. This leads to a very low gain per amplifier stage. Reduced signal swing follows from the reduced supply voltage. To ensure the same performance (signal-to-noise ratio), the noise has to be reduced which makes higher current necessary. So the analogue circuits do not automatically consume less power with reduced supply voltage at the same performance. The reduced supply voltages complicate or prohibit the use of some circuit structures, e.g. cascode circuits. Instead of cascoding sometimes cascading or a combination of cascading and cascoding of amplifier stages has to be used to reach high gain.

Unfortunately, there is another aspect to be considered for the design of analogue 65 nm (and smaller structure-size) circuits. The gate leakage increases the mismatch [3]. The conventional way to reduce mismatch is to spend more gate area [4, 5]. However, if the speed of the circuit has to be constant, then the wider transistors need more power, because the additional capacitance has to be charged/discharged [6]. According to [3], the following formula can be used for estimation of mismatch under consideration of gate leakage:

$$\frac{\sigma_{id}^2}{i_D^2} = \left(\frac{A_{VT} \cdot g_m}{\sqrt{W \cdot L} \cdot i_D}\right)^2 + \left(\frac{X_{IGS} \cdot i_G}{\sqrt{W \cdot L} \cdot i_D}\right)^2 \tag{1}$$

where A_{VT} is $2-3\,\text{mV}\,\mu\text{m}$ [7], $X_{IGS} \approx 0.03/\sqrt{\text{Area}}$ and Area is the gate area $W \cdot L$ in square-microns [3]. In this formula, i_D denotes the drain current and i_G the gate leakage current. The second term on the right-hand side of the equation considering gate leakage induced mismatch has been added to the well-known expression for larger structure-size MOSFETs.

In addition to the noise sources of MOSFETs, also the gate-leakage current in 65 nm CMOS technology generates noise. The shot noise current density is $S_{IG} = 2 \times q \times i_G$ (q = electron charge). This noise is equivalent to the noise of the base current in bipolar transistors. This noise comes on top of the induced gate noise [8, 9]. The gate-current noise limits the noise performance in nanometer-scale technologies [10]. Furthermore, gate leakage limits the hold times of sample and hold circuits and also has severe consequences on integrators, which hardly can use MOS capacitors any more or cannot be used for 'gate frequencies' below 1 MHz at 65 nm [3]. Poly–poly capacitors become necessary leading to more process complexity compared to pure digital processes.

In addition to these aspects, gain reduction of amplifiers occurs due to the gate leakage and tunnelling currents. As a consequence, known methods like gain enhancement with the help of gain boosting with regulated cascodes are reduced in their effectiveness. This aspect will be discussed in the next section in detail. A simplified model of a gain-boosted cascode considering this gain reduction will be derived.

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2. GAIN REDUCTION BY GATE CURRENTS

The voltage gain of the cascode circuit is the product of transconductance of the input transistor and of the transimpedance of the cascode stage. In the literature, however, mainly the gain reduction by the output conductance of deep-sub-micrometer MOS transistors is discussed. For the modelling of a cascoded amplifier, this approach is not sufficient. The output node of a gain-boosted cascode amplifier needs a very high impedance to achieve a very high gain and that is why the gain of a gain-boosted amplifier stage is limited by the gate currents of the cascode transistors. Without the gate currents, the gain is only limited by the gain of the gain-boost amplifier and the impedance of the load circuit. The impedance of the load circuit can also be increased with a gain-boost amplifier. This means that the gain of an amplifier stage with gain boost is finally limited by the complexity of the gain-boost amplifier and parasitic feedback like thermal feedback. The schematic of the gain-boosted amplifier stage for the simplified calculation is shown in Figure 1. The two resistors corresponding to g_{GD} and g_{GS} represent the leakage currents. A_{Gb} is the gain of the gain-boost amplifier. G_1 is the conductance of the input transistor in a plain cascode or the conductance of the input transistor and the current source of a folded cascode. The input current I_i is generated by the input transistor of the cascode circuit ($V_{in} \times g_m$). G_L represents the summarized conductance of the load circuit (current source) and following circuits (e.g. the next amplifier stage).

In a cascode amplifier stage a high gain is reached by delivering the input current to the output node with high impedance. The gate leakage current of the following amplifier stage increases the conductance G_L and reduces thereby the gain the amplifier stage. The gain-boost amplifier together with the cascode transistor forms a circuit with extremely high transimpedance. By solving the mesh and node equations, the transimpedance of the simplified amplifier stage is obtained as

$$\frac{V_o}{I_i} = \frac{(g_m - g_{GD}) \cdot A_{Gb} + g_m + g_{DS}}{N} \tag{2}$$

with

$$\begin{aligned} N = {} & ((g_{GD}+G_L) \cdot g_m - g_{GS}(g_{GD}+G_L+g_{DS}) + g_{DS} \cdot g_{GD}) \cdot A_{Gb} + (g_{GD}+G_L) \cdot g_m \\ & + 2 \cdot G_1 \cdot (G_L+g_{GD}) + g_{DS}(2 \cdot G_1 + g_{GD} - g_{GS} + G_L) - g_{GS} \cdot (G_{GL}+g_{GD}) \end{aligned} \tag{3}$$

With infinite gain in the gain-boost amplifier, the transimpedance of the cascode stage can reach

$$\frac{V_o}{I_i} = \frac{g_{GD} - g_m}{(g_{GS} - g_m) \cdot G_L - g_m \cdot g_{GD} + g_{GS} \cdot g_{DS} + g_{GS} \cdot g_{GD} - g_{DS} \cdot g_{GD}} \tag{4}$$

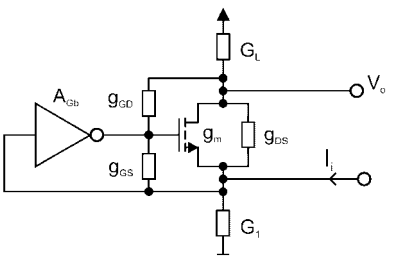

Figure 1. Simplified schematic of gain-boosted cascode amplifier.

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Without the gate currents, the gain is only limited by the load. The theoretical limit (gain of the gain-boost amplifier is infinite) for the reachable transimpedance without gate leakage is

$$\frac{V_o}{I_i} = \frac{1}{G_L} \tag{5}$$

The load circuit (represented as G_L in this calculation) can also be realized with a gain-boosted cascode. This means that in nanometer-scale technologies also the gate leakage of the load acts gain reducing.

The gate leakage current in a standard 65 nm CMOS is in the order of up to 100 nA/μm^2. According to a rough estimation, this leads to a reduction of the transimpedance to 4 MΩ compared to a value of 30 MΩ for a gain-boost amplifier with infinite gain. As a consequence, the gain of the gain-boosted amplifier stage in the 65 nm operational amplifier is reduced by about 10–20 dB by the gate leakage currents.

3. DESIGN EXAMPLE

The design example was simulated with a BSIM4 model and with the parameters of a 65 nm low-power process. This process has a somewhat thicker gate oxide to be able to use a supply voltage of 1.2 V instead of 1.0 V of the standard or base 65 nm process and to reduce the gate leakage. The technology is optimized to realize systems on a chip with digital and analog circuits. Despite the thicker gate oxide, there is a gate current of up to 1 nA/μm^2. In the base process, the gate currents are approximately 100 times larger. The threshold voltages for the NMOS and PMOS transistors are approximately 0.4 V. The nominal supply voltage is 1.2 V. Despite this low voltage, the used reference current source is described in a standard textbook [11].

Originally, the operational amplifier was designed for a pipelined analog-to-digital converter but the operational amplifier can be used for all purposes. The input-voltage range is in the middle of the power supply and the outputs are driven rail-to-rail. The block diagram of the operational amplifier shows three main amplifier stages and is shown in Figure 2. The operational amplifier is realized fully differential. For simplicity, however, only one signal line is drawn in Figure 2 for each differential connection. The amplifier stage A1 is realized as a folded cascode with gain boost. The gain-boost technique is also known as regulated cascode. In the two-path concept, A2h forms the high-frequency path with low gain and A2–A3 form the low-frequency high-gain path. Simultaneously, the amplifier stages A2h and A3 are the output stage.

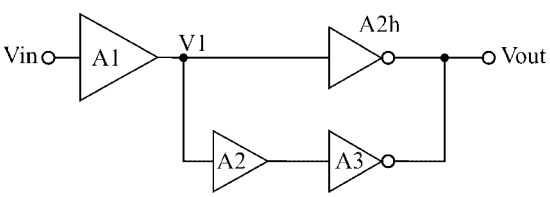

Figure 2. Block diagram of the operational amplifier.

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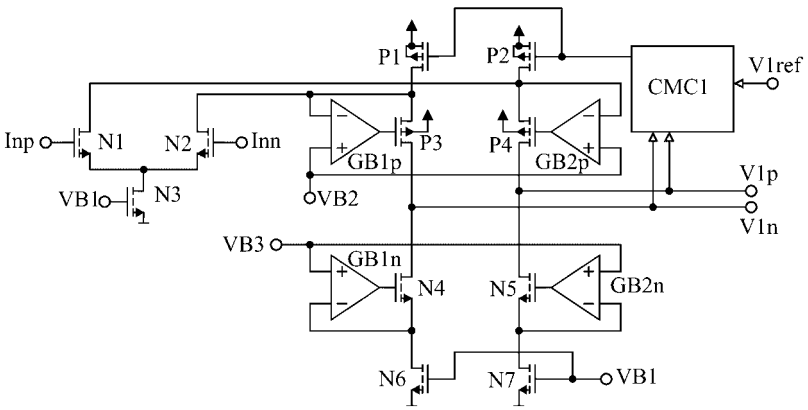

Figure 3. Schematic of the input stage.

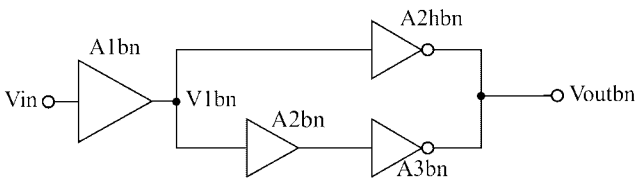

Figure 4. Block diagram of the N-channel gain-boost amplifier.

3.1. The amplifier stage A1

The amplifier stage A1 is realized as shown in Figure 3. The common-mode level of the first amplifier stage is controlled by the common-mode controller CMC1. The operating point of the amplifier stage is defined by the current sources N3, N6 and N7. With the gain-boost amplifiers GB1p, GB1n, GB2p and GB2n, the gain of the folded cascodes is increased. Because of the simpler realization, the gain-boost amplifiers of the N-channel cascodes are described first in the following.

3.1.1. The gain-boost amplifier of the N-channel cascodes. The block diagram of the gain-boost amplifier is shown in Figure 4. To reach sufficient gain, the amplifier is realized with three amplifier stages. Because of the nested Miller compensation, the second amplifier stage has to be non-inverting.

The detailed schematic of the N-channel gain-boost amplifiers is shown in Figure 5. The gain-boost amplifier is a complete operational amplifier. The amplifier stages are marked with dotted lines. The currents in the amplifier stage are preset by the current source P5. The current mirror N8–N9 is compensated with the resistor R1 between the drain and the gate of the FET diode connected transistors N8. The resistor reduces the capacitive load on the input node of the current mirror and the feedback *via* N8 is delayed. The load reduction and the delayed feedback increase the pole frequency of the current mirror. The compensation of the current mirrors is described in [12]. In the same way, the current mirror P8, P9 is compensated with R2. P-channel input

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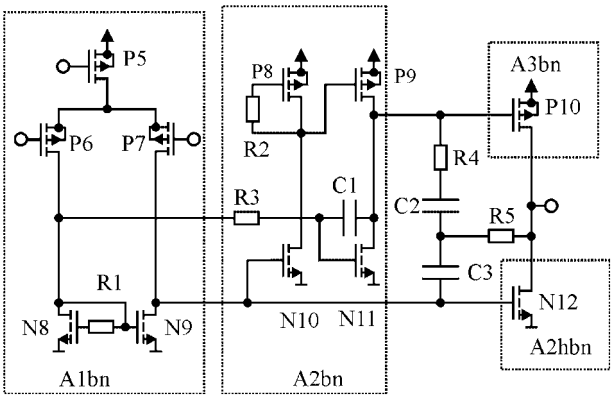

Figure 5. Schematic of the N-channel gain-boost amplifiers.

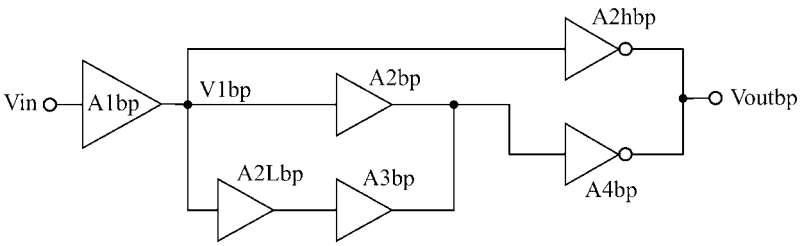

Figure 6. Block diagram of the gain-boost amplifier for the P-channel transistors.

transistors are used, because the source voltages of the N-channel cascodes N4, N5 in Figure 3 are near the negative supply voltage. The gate of N11 is connected *via* R3 to the amplifier stage A1bn. This signal path is mainly to set the operating point and has a negligible influence on the gain-boost amplifier gain. A2hbn and A3Bn are the output stage of the gain-boost amplifier and are the load circuit of one another. The compensation is done according to [13]. The values of C1 and R3 have to fulfil the condition that $1/(2\pi \cdot \mathrm{R3} \cdot \mathrm{C1})$ is slightly larger than the -3 dB frequency of the complete gain-boost amplifier.

3.1.2. The gain-boost amplifier for the P-channel cascode transistors. The signal current is flowing *via* the P-channel cascode transistors to the output of the first amplifier stage. For this reason, a higher gain is necessary in the gain-boost amplifier for the P-channel cascodes. This extra gain is reached with additional amplifier stages A2Lbp and A3bp as shown in the block diagram (Figure 6).

The input voltages for these gain-boost amplifiers are near VDD, therefore, N-channel input transistors (N13, N14) are used (Figure 7). The amplifier stage A2Lbp is similar to A2bn (Figure 5), only the polarity of the transistors and the supply rails are exchanged.

The amplifier stages A2bp and A3bp consist of a signal summing stage (P15, N17) and an inverting amplifier stage (N18, P16). A2Lbp and the summing amplifier stage are compensated by R8 as well as R9, R10 and C4. All other amplifier stages of the gain-boost amplifier are compensated according to [13] with R12, R13, C6 and C7.

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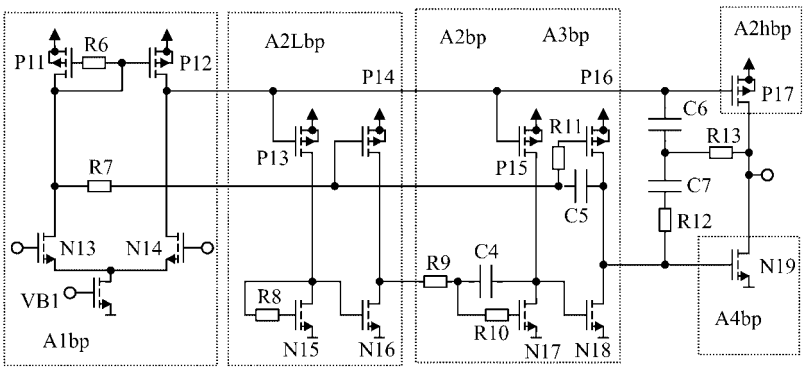

Figure 7. Schematic of the gain-boost amplifier of the P-channel cascode transistors.

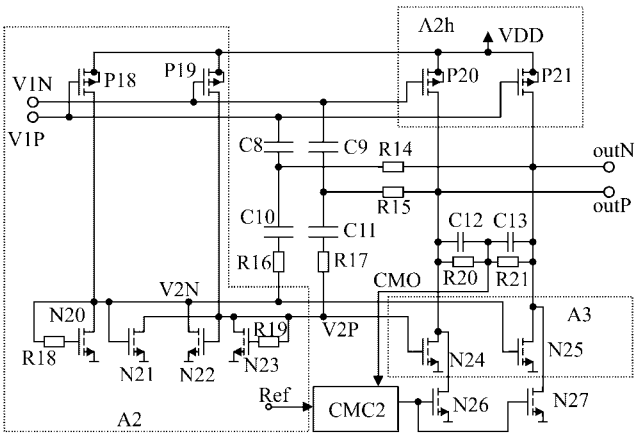

Figure 8. Schematic of the second stage and the output stage.

3.2. A2 and the output stage (A2h and A3)

The schematic of the second stage and the output stage is shown in Figure 8. The amplifier stage A2 mirrors the current of the P-channel transistors P18 and P19 *via* the loads N20 and N23 to the N-channel output transistors N24 and N25. The positive feedback transistors N21 and N22 introduce an additional gain. To assure a positive feedback factor smaller than 1, the transistors N21 and N22 have a smaller width than the transistors N20 and N23. The FET-diode connected transistors N20 and N23 are compensated with the resistors R18 and R19. The common-mode controller CMC2 controls the common-mode level at the output via transistors N26 and N27. The control-loop for the common-mode level at the output consists of only two amplifier stages (N26, N27 in series with CMC2, which is a single-stage differential amplifier) and is therefore very robust.

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3.3. Design methodology

The node and mesh equations with poles and zeros are very lengthy and complex. A closed solution is not possible and approximations to obtain a compact form cannot be done easily. Therefore, an iterative procedure for the design of the 65 nm operational amplifier with certain start assumptions for the different circuit blocks was used. As a base for the design, the statement 'For the overall system stability it is sufficient (but not necessary) that each of the structures in the set is stable' in [14] is used, that the complete operational amplifier is stable, when each circuit block is stable. To our own experience stability is assured, if all the settling behaviours (over technology, temperature and supply variation) show a well-damped settling without oscillation. The design flow was the following.

First, the width of the output transistors is chosen by the necessary output current and the (low) drain source saturation voltage (rail-to-rail output) for the output transistors. The output transistors have minimal gate length for high-speed circuits. The necessary transconductance of the output transistors can be calculated from the specified unity-gain frequency and the capacitive load. The necessary transconductance leads to a minimal bias current in the output stage.

The input stage dominates the noise and the offset voltage. So from the maximal offset voltage, a minimum gate area of the input transistors can be estimated. The maximal input noise gives the minimal current in the input stage. In the amplifier stage A2 (Figure 8), the condition $W_{P19}/W_{P21} = (W_{N22} + W_{N23})/W_{N25}$ (W is transistor width, gate length L is minimum for all these transistors) has to be observed, in order to achieve a good common-mode behaviour.

In a first approach, the complete operational amplifier inclusive common-mode controllers [15] is simulated with 'ideal' gain-boost amplifiers (gain = 60 dB, −20 dB/frequency decade, phase margin = 90°). Because of the shorter simulation time and the simpler evaluation of the simulation results, the AC response is optimized. Thereby, the values of the compensation components are estimated according to [12] first and are optimized by AC simulations. In a second step, the transient behaviour is optimized. Because of the nonlinearity of the circuits, AC simulation is not sufficient for the assurance of stability. For the transient behaviour, the optimization to achieve robust operating points is important, i.e. the transistors must not leave saturation for all technology, temperature and supply variations. Then, the gain-boost amplifiers are simulated as real amplifiers and the behaviour is optimized by a few iterations and when the results are good, then the recovery from extreme operating conditions is checked by transient simulation. E.g. if the output voltage of the first stage was set to VDD or VSS, the operational amplifier had to reach its regular operating point in a well-damped behaviour without oscillations.

4. RESULTS

The frequency and phase responses of the 65 nm CMOS operational amplifier are shown in Figure 9 for a supply voltage of 1.2 V. These results are valid for the nominal parameter set at a temperature of 100°C. A load of 0.5 pF is assumed. This means that no electrostatic discharge (ESD) protection circuits are present, which of course are not necessary for systems-on-chip applications. The DC gain is 110 dB. In the first stage, a gain of 90 dB is realized. The gain-boost amplifiers for the P-channel transistors have a gain of 89 dB and the gain-boost amplifiers for the N-channel transistors have a gain of 60 dB. The transit frequency f_t is 2.5 GHz. A phase margin φ_R of 55° is present at this frequency. The total power consumption of the operational amplifier is 15 mW at 1.2 V supply voltage.

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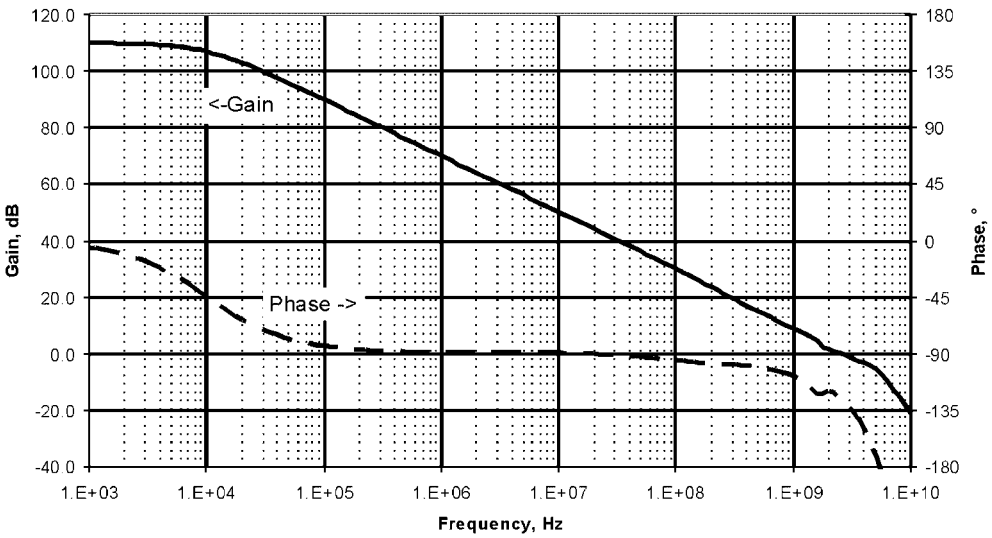

Figure 9. Bode diagram of the 65 nm operational amplifier.

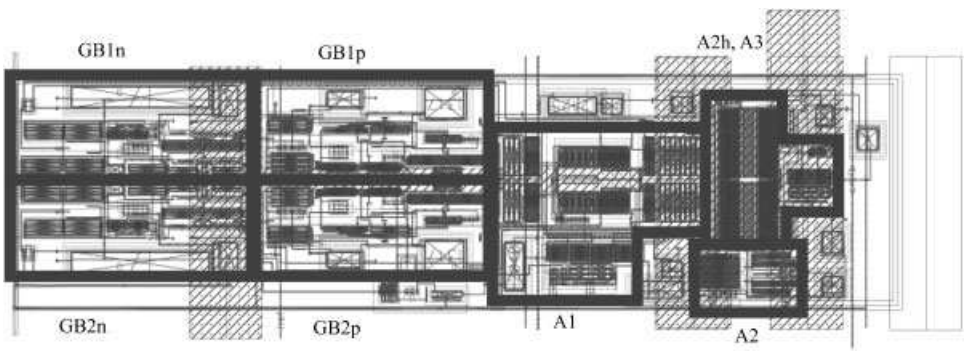

Figure 10. Layout of the 65 nm operational amplifier.

Figure 10 shows the layout plot of the 65 nm operational CMOS amplifier. In the left half of the chip, the gain-boost amplifiers can be seen. The total chip area of the operational amplifier is 130 μm × 30 μm. Each gain-boost amplifier occupies a chip area of 35 μm × 15 μm. The amplifier stages A1, A2, A2h and A3 need a chip area of 60 μm × 30 μm. That means that more chip area is necessary to reach high gain than for high speed only. Another conclusion is that chip area for supporting circuits (70 μm × 30 μm) is larger than chip area of the actual core of the operational amplifier (60 μm × 30 μm).

Table I summarizes the properties of the operational amplifier. The output voltage range is 1.14 V for a load of 10 kΩ between both outputs. The 0.5 pF capacitors were present from each output to ground for all simulation results. The slew rate of 1650 V/μs is achieved with an input voltage step of 0.1 V between the inputs. This large value is possible because the output stage is of class-AB type. The output stage has a bias current of 1.8 mA in each branch of the differential structure.

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Table I. Summarized performance of the presented operational amplifier.

Gain	110 dB
Unity-gain frequency	2.51 GHz
Phase margin	55°
Supply voltage	1.2 V
Power consumption	15 mW
Slew rate (0.1 V overdrive)	1650 V/μs
Input-noise density ($\mu V/\sqrt{Hz}$)	3.9/1 kHz 1.2/10 kHz 0.39/0.1 MHz 0.13/1 MHz
Harmonic distortion, $V_o = 0.8\ V_p$, $f_1 = 10$ MHz	$HD_3 = -64$ dB $HD_5 = -73.8$ dB $HD_7 = -97$ dB

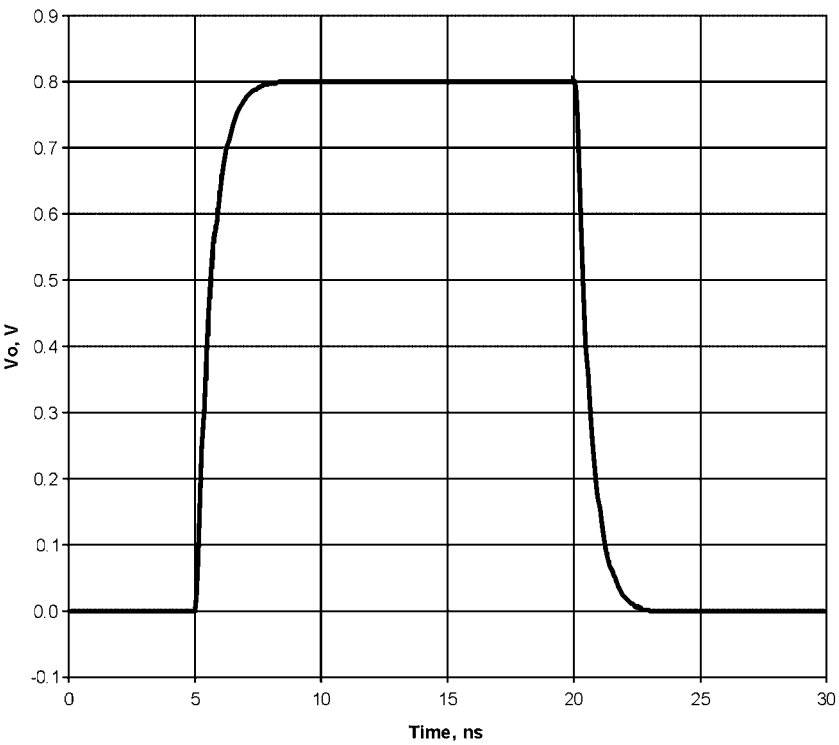

Figure 11. Step response of the 65 nm operational amplifier.

With a large overdrive, the output stage can deliver 13 mA. Therefore, the slew rate is not limited by the output stage. The limiting factor for the slew rate comes from the compensation capacitors C8 = C9 = 80 fF (Figure 8) and the current in N3 (Figure 3), which is 220 μA. According to this simple estimation, which neglects further parasitics, the slew rate is limited to 2700 V/μs.

The step response (Figure 11) was simulated with a differential amplifier with resistive feedback for a gain of 2. The same circuit was used for the investigation of the harmonic distortions. The

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settling time is 2.54 ns for 1% and 3.3 ns for 1 for an output voltage step of 0.8 V. The slew rate in Figure 11 is 1050 V/μs; because the overdrive reduces very fast to zero due to the feedback for the gain factor of 2. Therefore, the high value of 1650 V/μs for a 0.1 V input overdrive in Table I simulated for the open-loop case with 0.5 pF loads is not present in Figure 11.

The input noise is dominated by $1/f$ noise up to a frequency of 5 MHz. The thermal noise level is 36 nV/$\sqrt{\text{Hz}}$. Because of the low currents in the gain-boost amplifiers the gain-boost amplifiers have a relatively large contribution to the noise. The shot noise of the gate-leakage current has no noteworthy contribution to the noise.

The harmonic distortions of even order are nearly perfectly suppressed because of the fully differential realization and the absence of mismatch in the simulations. The values for the harmonic distortion listed in Table I have been simulated with an output-voltage amplitude of $0.8\,V_{\text{peak}}$.

The common-mode distortion is at least reduced by 23 dB in a feedback circuit with a gain of 2 (the same circuit as for settling simulation). This means that the common-mode output voltage changes by 7 mV, if the common-mode input voltage (both inputs connected to each other) changes by 100 mV.

5. CONCLUSION

The effect of gain reduction by gate leakage currents and by gate tunnelling currents was addressed. An expression for the quantitative reduction of the gain-boost transimpedance was derived and its effect on the gain reduction of amplifier stages was discussed for the first time at the example of a 65 nm CMOS operational amplifier. In the presented operational amplifier design, we use a robust common-mode control circuit, which leads to a class-AB behaviour of the output stage. Compared to the seemingly simpler realization with one common-mode controller in [16] the presented common-mode control technique is proven in 120 nm CMOS test chips [15, 17] and is not sensitive to mismatch. With this design example, we showed that it is possible to reach high gain with a three-stage two-signal-path concept. At the same time, high speed is achievable with such a topology. This means that in all useable digital technologies, it will be possible to realize high-gain amplifiers and therewith high-precision analogue circuits for high-speed applications. The area of the analogue circuits will not shrink as much as digital circuits. In many cases, even a larger chip area will be necessary for the same performance due to supporting circuits such as additional gain-boost amplifiers and common-mode controllers.

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