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A High-Speed Fully Differential Telescopic Op-Amp for Active Filter Designs in V2X Applications*

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In this paper, an ultra-wideband fully differential two-stage telescopic 65-nm CMOS op-amp is presented, which uses low-voltage design techniques such as level shifter circuits and low-voltage cascode current mirrors. The designed op-amp consists of two stages. While the telescopic first stage provides high speed and low swing, the second stage provides high gain and large swing. Common-mode feedback circuits (CMFB), which contain five transistors OTA and sensing resistors, are used to set the first-stage output to a known value. The designed two-stage telescopic operational amplifier has 41.04 dB lower frequency gain, 1.81 GHz gain-bandwidth product (GBW) and 51.9° phase margin under 5 pF load capacitance. The design consumes a total current of 11.9 mA from a 1.2-V supply voltage. Presented fully differential two-stage telescopic op-amp by using low-voltage design techniques is suitable for active filter in vehicle-to-everything (V2X) applications with 120 μm×55 μm layout area.

Keywords: Common-mode feedback; fully differential op-amp; telescopic first stage; ultra-wideband; V2X.

1. Introduction

WITH the advancements in the CMOS deep sub-μm technology, transistor sizes continuously scaled down, which led designers to construct faster analog–digital mixed circuits. This rapid development opened a new era that devices communicate

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with each other and share information. Vehicle-to-everything (V2X) systems aim to achieve an intelligent transportation system by using this excessive information transmit rate in the near future.

V2X applications use a 5.9 GHz frequency band to communicate. This standard contains 10 and 20 MHz channel sizes with several wideband options such as 60, 80 and 100 MHz.[1] In the active filter designing, fully differential op-amps are usually used in negative feedback, so high speed and high gain become essential parameters in these circuits to satisfy the V2X applications' requirements. There are several active filter topologies such as Rauch filter (Multiple-Feedback Filter), Tow–Thomas filter, Akerbeng–Mossberg filter and Sallen–Key filter. The Sallen–Key topology requires a Differential Difference Amplifier (DFF) for implementation in fully differential form, so this topology cannot be used for this paper. So, we implemented a bandwidth programmable fourth-order Multiple-Feedback filter, as can be seen in Fig. 1. Equal-R method is used to create the filter transfer functions. Also, bandwidth programmability is achieved by using programmable capacitor arrays, as can be seen in Fig. 1.

Nowadays, CMOS devices work with very low supply voltages. However, unlike digital circuits, analog circuits cannot take advantage of it because transistors' threshold values inevitably become high in short channel designs. This poses a significant challenge to design cascode devices to work correctly. In this paper, to reduce this effect in the input stage, low threshold PMOS transistors are used.

CMFB circuits are the most critical parts of the fully differential op-amp designing. If CMFB circuits are not properly designed, the circuit can oscillate or shutdown itself because of the insufficient common-mode voltage at output nodes. Furthermore, common-mode sensing is done with complex circuits such as source follower stages or MOSFETs working in the triode region in the long channel process.

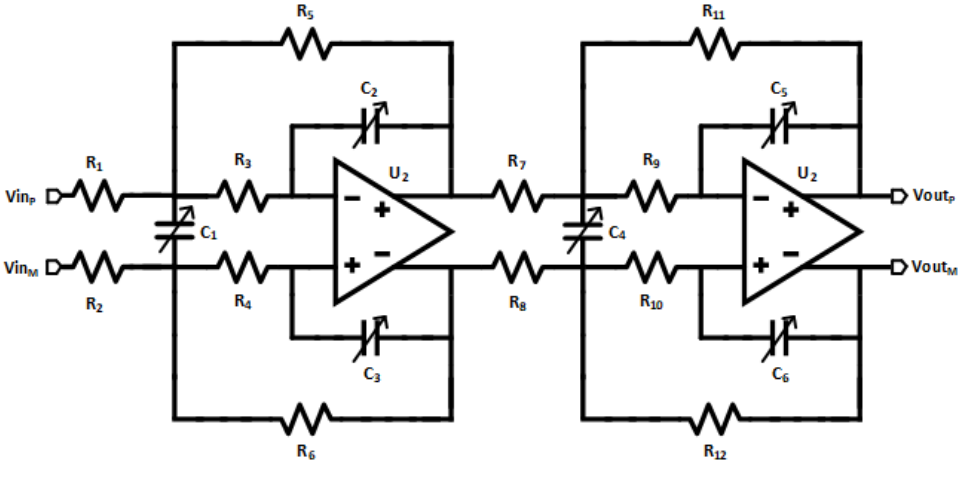

Fig. 1. Fourth-order programmable MFB filter.

However, in the short channel process, resistive structures can be used due to small r_O values. In this work, a resistive feedback method and five-transistor OTA-based CMFB circuit adjust the output nodes to a known common-mode value.

Unlike the other works that have been done over the years, in this work, PMOS transistors are used as the input stage, and a higher transition frequency value is achieved.[2,3] PMOS transistors are used in the input stage because the noise immunity of the PMOS transistor is better than the NMOS transistor.[4]

This paper is organized as follows. Section 2 presents the fully differential telescopic two-stage op-amp design. The simulation results of the op-amp are given in Sec. 3. Finally, the paper is finished with a conclusion in Sec. 4.

2. Fully Differential Telescopic Op-Amp Design

In this paper, a fully differential operational amplifier is used instead of its signed-ended counterpart. Fully differential op-amps have differential inputs the same as the single-ended counterparts, but the main difference is the fully differential op-amps produce differential outputs.

These topologies have many advantages over single-ended op-amps. Since fully differential op-amps have very high CMRR values and have a large swing, they can be considered a perfect choice for filter circuit applications. Moreover, the total harmonic distortion (THD) value is significantly reduced, due to even-order nonlinearities that are not present in these topologies. Disadvantages of fully differential op-amps can be considered as their need for matched feedback networks and common-mode feedback circuits.[5]

As shown in Fig. 2, the designed fully differential op-amp consists of two main amplifier stages. The compensation is done by connecting the second-stage output to the first-stage output with a capacitor and zero-nulling resistor.[6]

2.1. *First-stage design*

The designed op-amp circuit has a telescopic cascode structure in the input stage, as shown in Fig. 3. The main advantage of telescopic cascode structure against other

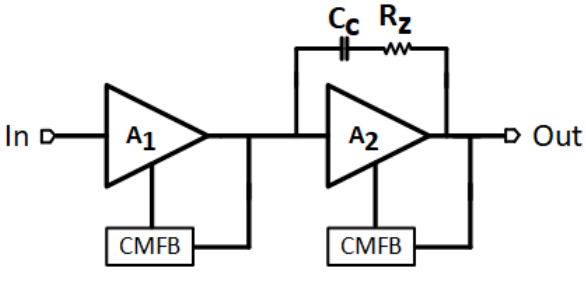

Fig. 2. Block diagram of the overall operational amplifier.

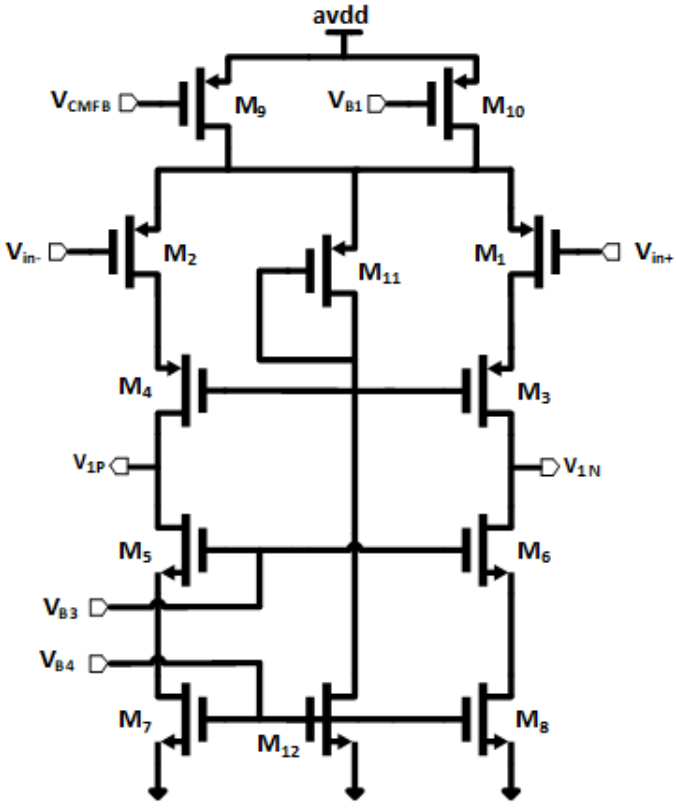

Fig. 3. Schematic of telescopic first stage.

op-amp structures is that it has the highest speed performance. Also, the telescopic op-amp structure has low power dissipation and low noise.[3] Low-voltage design causes headroom limitations and makes the op-amp designs challenging. In order to overcome these limitations, low threshold M_1, M_2 PMOS transistors are used in the input stage.

Furthermore, the fully differential op-amp cut-off frequency strongly depends on the circuit's dominant pole due to the miller effect. In this work, an 850 fF capacitor is used as a pole-splitting capacitor. The dominant pole's approximate location can be shown as the function of the first-stage output resistance, compensation capacitance, and the second-stage gain, as depicted in (1)

$$P_1 = \frac{-1}{(1 + gm_2 * R_2) * C_c * R_1}, \tag{1}$$

where g_{m2} is the second-stage transconductance.

To achieve maximum cut-off frequency and overcome headroom limitations, M_5, M_6, M_7 and M_8 transistors are designed as low-voltage high-swing cascode current

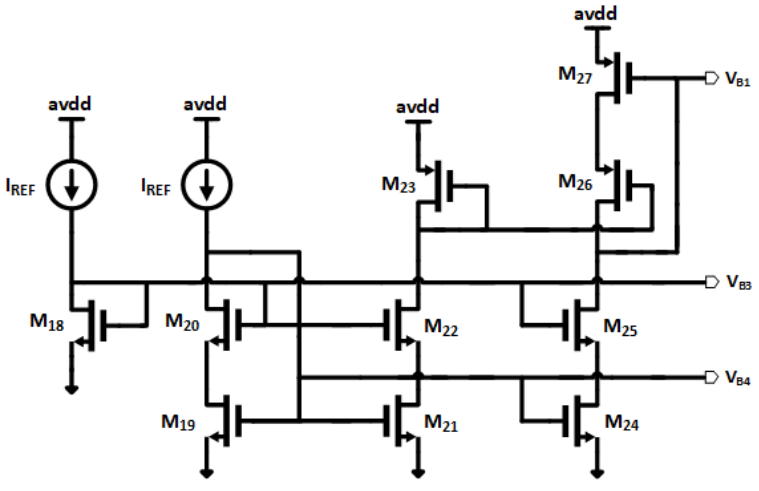

Fig. 4. The bias circuit.

mirror with minimum length values. In this work, the op-amp's cut-off frequency is calculated as 14.39 MHz under 5 pF load.

The bias circuit of the system is shown in Fig. 4. As we can see, M_{22} and M_{27} transistors are used to generate drain voltages of M_{23}, M_{25}, M_{28} and M_{31} transistors by using M_{24}, M_{26}, M_{29}, M_{30} transistors. I_{REF} refers to the current that is generated from the bandgap circuitry.

The change in common-mode input level affects the M_1, M_2 transistor's VDS, and M_3, M_4 transistor's VGS values. Hence, gain also drops with the common-mode input voltage. To have the gain constant, M_{11} and M_{12} transistors are used as a level shifter circuit.[4] For minimal power dissipation, the level shifter circuit is designed to draw minimum current from the bias circuit.

2.2. *CMFB circuit for the first stage*

Fully differential amplifiers need a common-mode feedback network to ensure that the common-mode voltage level between two output nodes is at the wanted "V_{REF}" reference voltage value. There are several methods to sense the common-mode levels in general. These methods can be realized as resistive sensing, sensing with the source-follower stage and sensing with MOSFETs that are operating in the deep triode region.[4] In this paper, the resistive sensing method is adapted. The common-mode sensing stage's resistor values are chosen relatively high not to affect the telescopic first-stage gain. C_{S1} and C_{S2} capacitors are used to cancel the parasitic effects of the sensing resistors in high-frequency operations.

The sensed common-mode voltage level through R_1, R_2 resistors is compared with a reference voltage. Five-transistor OTA with a gain of 7 is designed for this operation. The amplified error value is used to control the telescopic first-stage tail

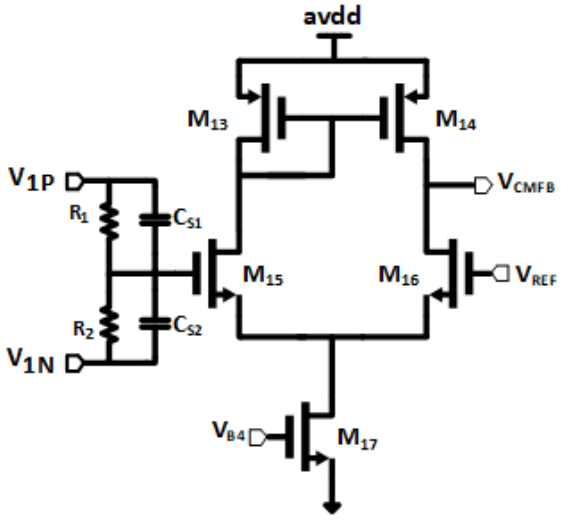

Fig. 5. The first-stage common-mode feedback circuit.

current. OTA's output controls 30% of the main tail current through the M_9 transistor to avoid stability issues in the common-mode feedback loop. Figure 5 depicts the designed five transistor OTA and common-mode sensing resistors.

2.3. *Second-stage design*

Although the telescopic first stage has advantages like its high-speed operation and high gain, the output swing of telescopic cascode configuration is small. Thus, using only the telescopic cascode stage is not suitable for low-voltage op-amp design. The second stage is designed as a common source amplifier with an active load to overcome small swing problems encountered in the first stage. As illustrated in Fig. 6, the second stage consists of C_{C1}, C_{C2}, R_{Z1} and R_{Z2} as a compensation network and R_3, R_4 as a common-mode feedback structure alongside the common-source stage. C_{S3} and C_{S4} capacitors are used to cancel the parasitic effects of R_3, R_4 resistances in high-frequency operations.

The second stage exhibits a nondominant pole and right half-plane zero due to pole-splitting capacitor C_C and the first- and second-stage output capacitances C_1 and C_2. The second-stage transconductance has an important role in determining the locations of the nondominant pole and the right half-plane zero.[5] These locations are approximately defined as

$$P_2 = \frac{-g_{m2} * C_c}{C_1 * C_c + C_2 * C_1 + C_c * C_2}, \tag{2}$$

$$Z = +\frac{g_{m2}}{C_c}. \tag{3}$$

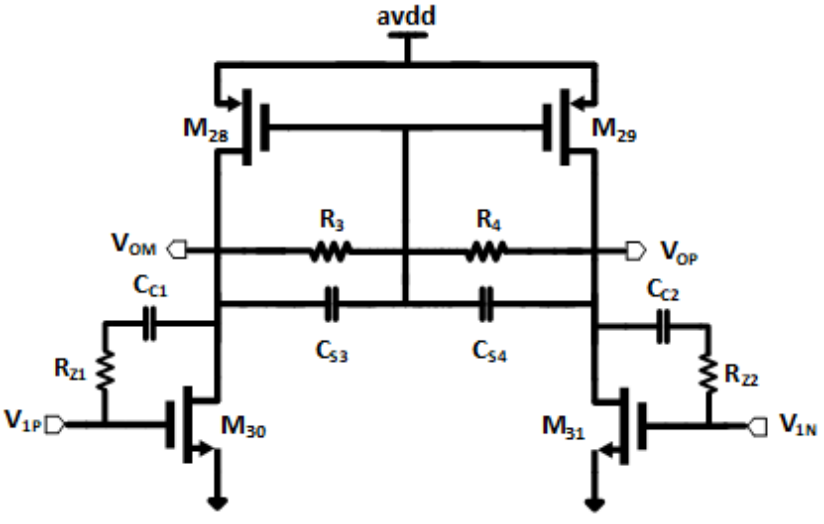

Fig. 6. Schematic of the second stage.

If the first-stage parasitic capacitance is small compared to the compensation capacitor and the load capacitance C_L is approximately five times bigger than the compensation capacitor, the nondominant pole becomes highly dependent on the load capacitance.[4] This can be expressed as

$$P_2 = \frac{-g_{m2}}{C_L}. \tag{4}$$

Right half-plane zero appears on the circuits because the pole-splitting capacitor shorts the first- and second-stage outputs at high frequencies. The right half-plane zero has the same magnitude response as the left half-plane zero. However, the phase response of the right half-plane zero behaves the same as the left half-plane pole. Thus, the stability of the system is decreased.[7]

The simplest method to reduce the right half-plane zero effect is connecting a zero-nulling resistor series with the compensation capacitor.[6] With this approach, the zero location of the system becomes as

$$Z = \frac{1}{C_c * \left(\frac{1}{g_{m2}} - R_z\right)}. \tag{5}$$

If the zero-nulling resistor is made equal to $1/g_{m2}$, the right half-plane zero disappears from the system. However, the zero-nulling resistor can be used to cancel the effect of the nondominant pole.[6] As shown in Fig. 7, increasing the R_Z value carries the zero from the right half-plane to the left half-plane. A 180 Ω zero nulling resistor is used to reduce the nondominant pole's effect in this work.

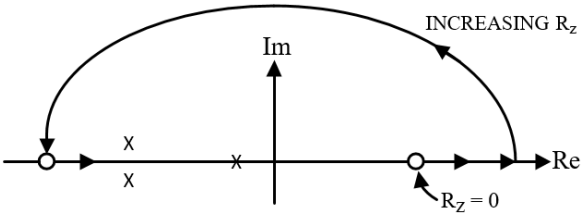

Fig. 7. Movement of the RHP zero with zero-nulling resistor.

The second-stage common-mode feedback loop only consists of resistors, unlike the first stage. This is due to the fact that the second stage only contains minimum length transistors. So, the resistive sensing method does not disturb the second-stage gain. R_3 and R_4 resistors with 30 kΩ value are used as the second-stage common-mode feedback loop. The sensed common-mode voltage of the outputs is directly applied to the gates of the M_{18} and M_{19} transistors. The main advantage of this common-mode feedback loop is that this structure does not suffer from any stability problem.[4]

3. Post-Layout Simulation Results

The op-amp is designed in TSMC 65 nm process using core and low threshold devices. As shown in Fig. 8, the layout was drawn with the Cadence Virtuoso computer-aided design (CAD) tool and includes common-mode feedback circuits, compensation capacitors, first and second stages. The common-centroid method is used for every stage in design to reduce the gradient-induced mismatches. The active layout area has been measured as 120 μm×55 μm. Table 1 summarizes the component sizes of the op-amp.

As shown in Figs. 9 and 10, the op-amp's open-loop magnitude and phase responses for TT, FF and SS corners are plotted. The circuit has a low-frequency gain of 41.04 dB, transition frequency of 1.81 GHz and a phase margin of about 51.9° for 5 pF capacitive loads per output stage in TT corner. Also, gain and phase variations for different temperatures and supply voltages in the TT corner are shown in Figs. 11 and 12, respectively. The op-amp's gain, phase margin, GBW and power consumption for these variations are summarized in Table 2.

The DC characteristic of the operational amplifier is shown in Fig. 13. A good linearity is achieved within an input voltage range of ±5 mV. The DC differential gain of 41.04 dB is observed from the post-layout simulation.

The post-layout input-referred spectral noise density simulation is shown in Fig. 14. Flicker noise (1/f) frequency corner is approximately estimated as 300 Hz. The input-referred spectral noise density at 100 MHz calculated as 1.961 nV/$\sqrt{\text{Hz}}$

In Fig. 15, the results of the PSRR and CMRR simulations are shown. The PSRR and CMRR are extremely important analog design parameters because they describe how well an amplifier rejects noises in common-mode input or power supply and

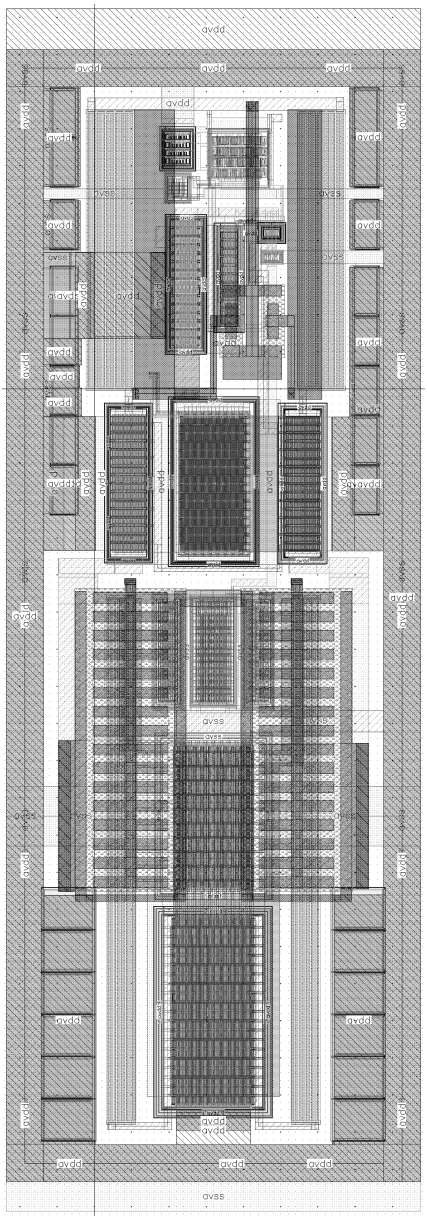

Fig. 8. Layout of the operational amplifier.

ground. Ideally, a fully differential amplifier has infinite CMRR and PSRR, but due to mismatches that is caused by parasitic extraction, the designed op-amp exhibits 72.26 dB CMRR, 87.91 dB PSRR+ and 60.41 dB PSRR−. PSRR+ and PSRR− denote the noises that are originated from power supply and ground, respectively.

Table 1. Device sizes.

Device (s)	Sizes (W/L)	Device(s)	Sizes (W/L)
M_1/M_2	(122.88 μm/60 nm)	M_{17}	(5.76 μm/180 nm)
M_3/M_4	(122.88 μm/60 nm)	M_{18}	(1.44 μm/720 nm)
$M_5/M_6/M_7/M_8$	(28.8 μm/60 nm)	$M_{19}/M_{21}/M_{24}$	(1.44 μm/60 nm)
M_9	(31.68 μm/60 nm)	$M_{20}/M_{22}/M_{25}$	(1.44 μm/60 nm)
M_{10}	(86.4 μm/60 nm)	M_{23}	(2.88 μm/720 nm)
M_{11}	(1.64 μm/180 nm)	M_{26}/M_{27}	(2.88 μm/60 nm)
M_{12}	(1.44 μm/60 nm)	M_{28}/M_{29}	(240 μm/60 nm)
M_{13}/M_{14}	(3.84 μm/60 nm)	M_{30}/M_{31}	(240 μm/60 nm)
M_{15}/M_{16}	(15.36 μm/180 nm)		

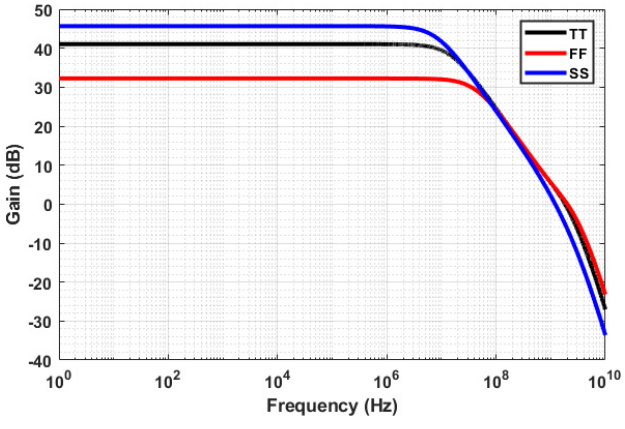

Fig. 9. Magnitude responses of the operational amplifier for TT, FF, and SS corners.

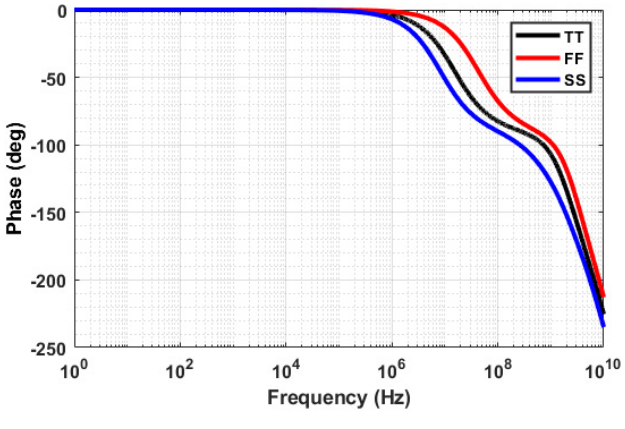

Fig. 10. Phase responses of the operational amplifier for TT, FF and SS corners.

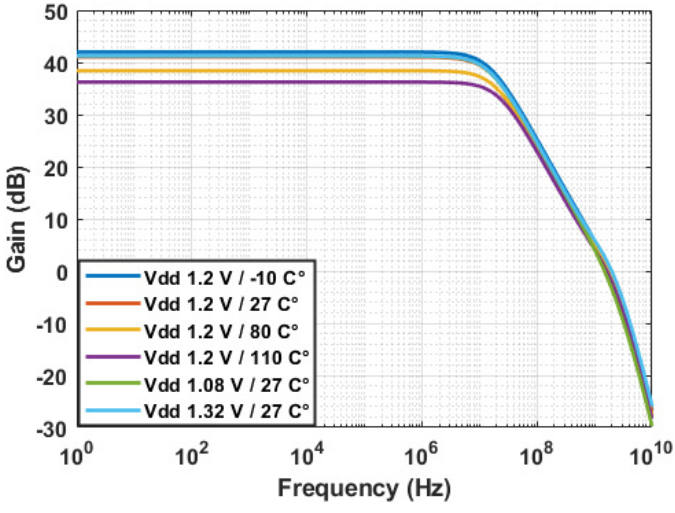

Fig. 11. Effect of temperature and supply voltage variations on the operational amplifier's gain.

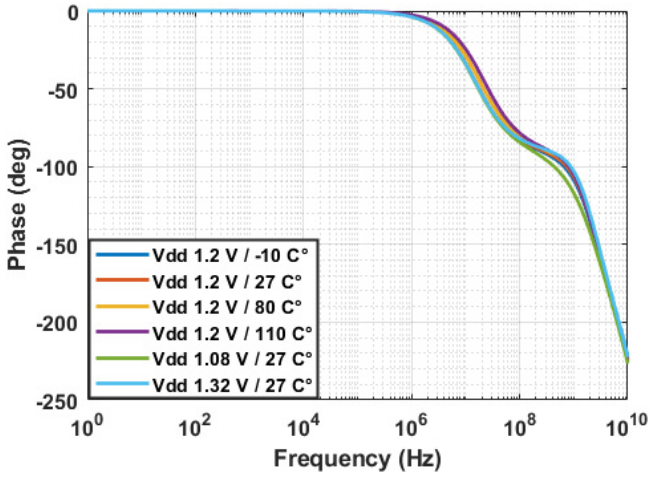

Fig. 12. Effect of temperature and supply voltage variations on the operational amplifier's phase.

Table 2. The op-amp's specifications for various supply voltage and temperature variations.

Supply voltage/temperature	Gain	GBW	Phase margin	Power consumption
1.08 V/27°C	41.19 dB	1.5 GHz	49.91°	9.34 mW
1.2 V/−10°C	42 dB	1.863 GHz	48.51°	11.97 mW
1.2 V/27°C	41.04 dB	1.81 GHz	51.9°	14.3 mW
1.2 V/80°C	38.42 dB	1.715 GHz	54.32°	16.95 mW
1.2 V/110°C	36.23 dB	1.625 GHz	56.84°	18.44 mW
1.32 V/27°C	41.24 dB	1.98 GHz	50.15°	17.64 mW

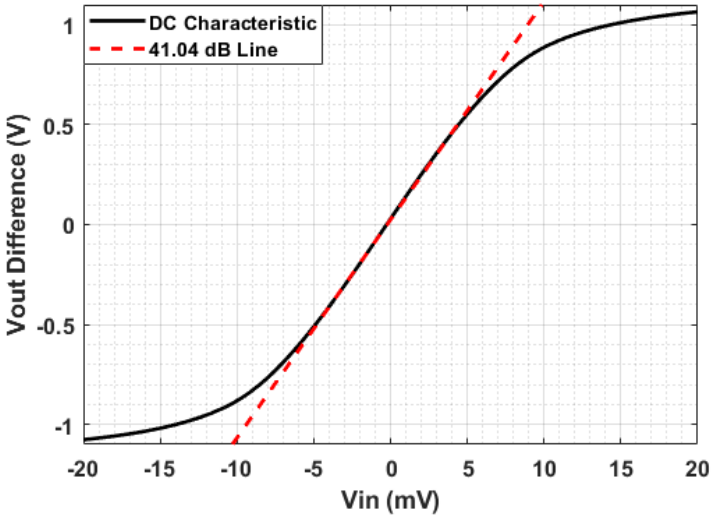

Fig. 13. DC transfer characteristic of the operational amplifier.

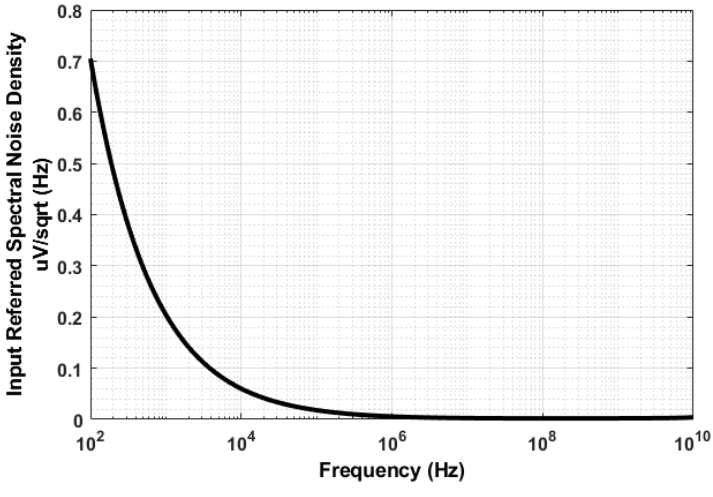

Fig. 14. Simulated input-referred noise density.

Figure 16 depicts the THD of the designed operational amplifier from 100 kHz to the 500 MHz frequency. To achieve a trustworthy result, the first five harmonics are included in the THD calculation. 2 kΩ feedback resistors and 5 pF and 10 kΩ loads are used in post-layout THD simulation. −55 dB THD value is achieved at 100 MHz frequency.

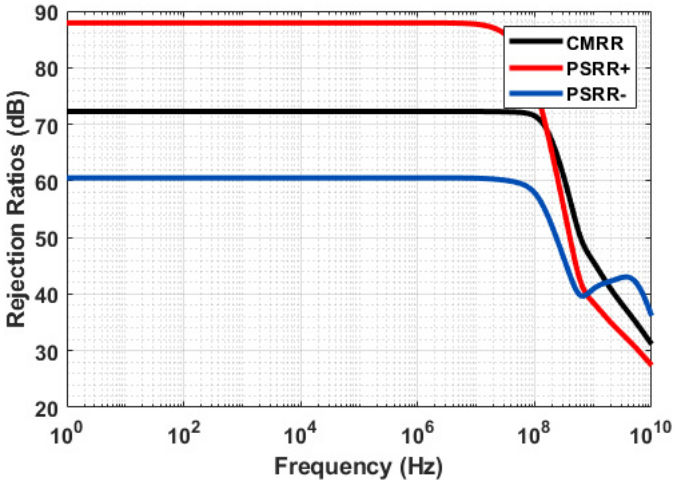

Fig. 15. PSRR and CMRR of the operational amplifier.

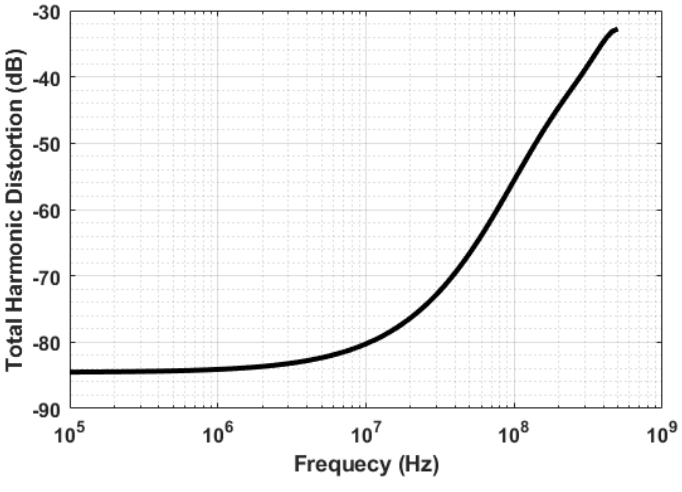

Fig. 16. Total harmonic distortion versus frequency.

The post-layout transient simulation of the op-amp is shown in Fig. 17. 100 mV peak-to-peak (V_{pp}) sinusoidal signal with 100 MHz frequency is applied to the op-amp differential inputs for 10 periods. 2 kΩ feedback resistor is used as a unity gain feedback network. THD value is calculated as −55 dB for 10 periods as previously simulated in the THD simulation.

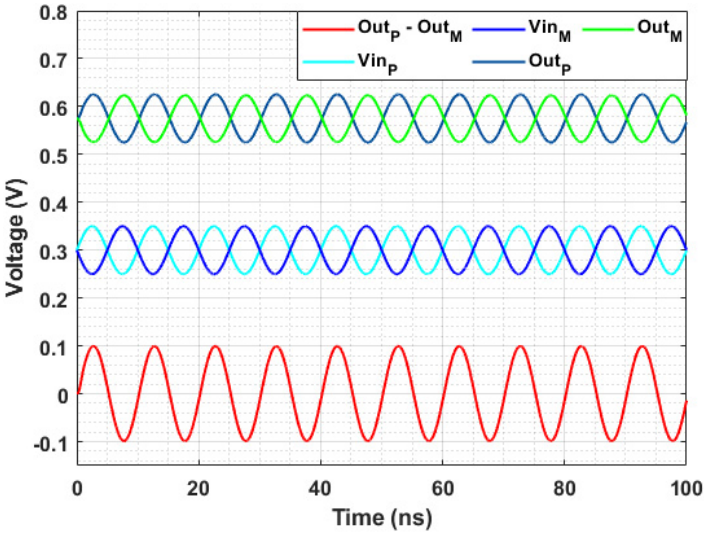

Fig. 17. Closed-loop transient simulation with unity feedback.

In Table 3, recent works and their performance characteristics can be seen. The Figure of Merit (FoM) method is used to compare the designed op-amps with their certain characteristics. There are several ways to calculate the FoM, but in this work, it is calculated as presented in Ref. 8.

$$\text{FoM} = \frac{\text{GBW[MHz]} * C_L\text{[pF]}}{W\text{[mW]}}. \tag{6}$$

In Eq. (6), the power consumption can be changed as total current consumption. This FoM calculation method is usable for the compared op-amp designs apart from the process.

In this work, the FoM value is calculated as 632.86 MHz·pF/mW, and the best FoM value is achieved among the other papers that have been published.

In layout design, it is observed that big IR drops from the power supply disturb the circuit working. To reduce the resistance values from power supply and ground through to the op-amp circuit, metal lines with a width of 5 μm from metal1 to metal6 have been used.

Figures 18 and 19 show the post-layout Monte Carlo simulations of the gain and phase margin of the op-amp. Totally, we ran 200 Monte Carlo simulations. We achieved 40.49 dB mean and 1.67 dB standard deviation in gain and 50.31° mean and 2.54° standard deviation in phase margin.

Table 3. Comparison to op-amps in the literature.

Ref.	Technology	Gain	GBW	Phase margin	Power consumption	Supply voltage	Load	FOM $\frac{[\mathbf{MHz}]*[\mathbf{pF}]}{[\mathbf{mW}]}$	Year
2	0.12 μm	40.2 dB	1.5 GHz	45°	11 mW	1.2 V	3.2 pF	436.36	2004
3	65 nm	58 dB	1 GHz	62°	11.4 mW	1.2 V	2 × (5 pF and 10 kΩ)	438.59	2009
9	0.18 μm	86 dB	392 MHz	73°	12 mW	1.8 V	2 × (2 pF and 1 kΩ)	65.33	2004
10	65 nm	56 dB	450 MHz	77°	1.6 mW	1 V	2 pF	562.5	2011
11	0.18 μm	50 dB	2.6 GHz	35°	7.2 mW	1.8 V	2× (300 fF and 1 kΩ)	108.33	2002
12	0.18 μm	80 dB	660 MHz	73°	3.8 mW	1.8 V	1 pF	173.68	2006
13	90 nm	72.1 dB	202 MHz	63°	5.2 mW	1.2 V	2 pF	77.6	2015
14	90 nm	72.8 dB	221 MHz	61°	2.9 mW	1.2 V	2 pF	152.8	2014
15	65 nm	60 dB	45 MHz	45°	158.4 μW	1.2 V	1 pF	284.1	2019
This work	65 nm	41.04 dB	1.81 GHz	51.9°	14.3 mW	1.2 V	2 × (5 pF and 10 kΩ)	632.86	

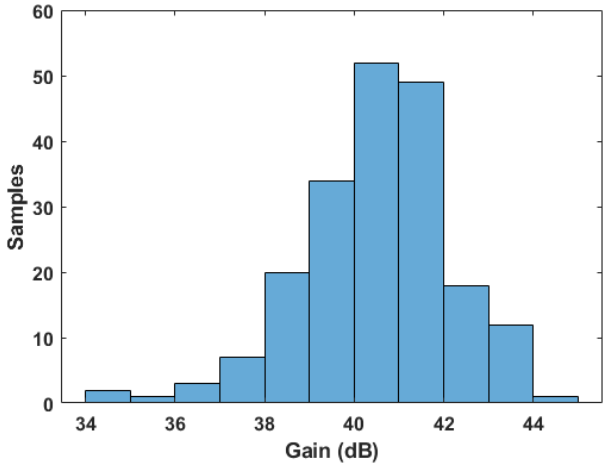

Fig. 18. Op-amp gain histogram.

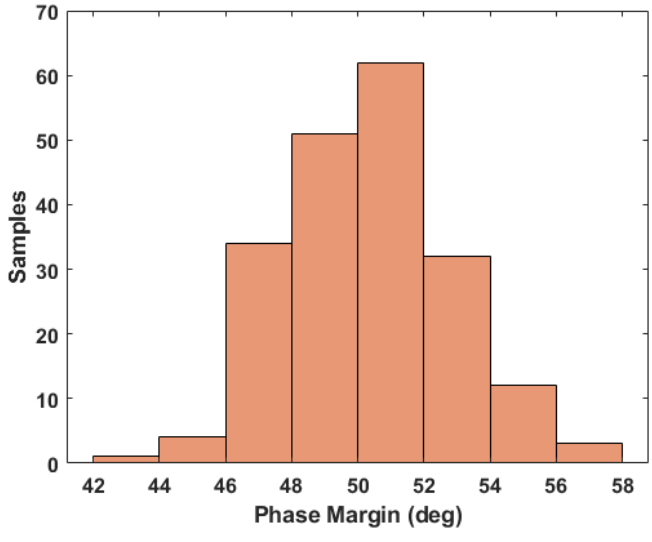

Fig. 19. Op-amp phase margin histogram.

4. Conclusion

In this paper, a fully differential telescopic operational amplifier is presented in 65 nm technology with core and low threshold voltage devices. Despite the low-voltage headroom caused by 1.2-V supply voltage, the telescopic cascode structure is properly designed with level shifter and low-voltage cascode current mirror circuits. Magnitude and phase simulations are done under TT, FF and SS corners. The

designed op-amp has a GBW of 1.81 GHz, a low-frequency gain of 41.04 dB and a phase margin of about 51.9° with 1.2-V supply voltage. Very high GBW value and comparable power dissipation of the designed op-amp to other works make this design a suitable choice for active filter designs in V2X applications. The designed op-amp can be used, where high-speed operations are the main design specifications besides the filter applications.

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