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MIXED SIGNAL LETTER

A high speed four-stage operational amplifier in 65 nm CMOS

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Abstract The paper presents a four-stage operational amplifier (OPA) with high DC gain and large bandwidth by combining no capacitor feedforward compensation and reversed nested indirect compensation. The proposed OPA is simulated in TSMC 65 nm 1.2 V CMOS process, achieving 100 dB DC gain, 330 MHz gain-bandwidth product, 266.25 V/μs slew rate and 1.56 mW power dissipation with 1.2 V supply voltage.

Keywords Multi-stage OPA · Frequency compensation · Feedforward compensation · Indirect compensation

1 Introduction

Operational amplifiers are indispensable units in analog circuits as well as mixed digital-analog circuits, whose performance directly influences the system's performance. With the improvement of CMOS processes and the scale down of transistor dimensions and supply voltages, high gain can only be realized by multi-stage amplifiers in nano-scale CMOS processes. But each stage inevitably introduces a low-frequency pole causing stability problem. We need to employ frequency compensation techniques to maintain circuit stability. For this purpose, many frequency compensation schemes [1–5] for large bandwidth have been reported. Since the no capacitor feedforward compensation (NCFF) [3, 4] scheme does not introduce any compensation capacitors, right-half-plane (RHP) zeros brought by compensation capacitors are fundamentally eliminated. This scheme uses the positive phase shift from left-half-plane (LHP) zeros created by feedforward paths, to compensate the negative phase shift due to poles. However, feedforward networks lead to higher power consumption due to extra added feedforward transconduction stages. In amplifiers with reversed nested indirect compensation (RNIC) [5] structure, the compensation capacitor is connected to an internal low-impedance node moving poles to higher frequency, thus expanding bandwidth. However, these amplifiers are sensitive to load due to the added resistors in series with compensation capacitors, which makes them impractical in applications.

A novel frequency compensation technique not only possessing the advantages of both NCFF and RNIC, but also covering their shortages, will be presented in this paper. A four-stage opamp using this novel compensation network achieves high DC open-loop gain and large gain-bandwidth product (GBW) without extra resistors, and reduces power compared with the NCFF scheme. This paper is organized as follows. Section 2 discusses the structure and the design considerations of the proposed opamp. The circuit schematic of the proposed opamp is provided in Sect. 3. The simulation results based on TSMC 65 nm 1.2 V CMOS process are illustrated in Sect. 4, and conclusions are given in Sect. 5.

2 Structure and design considerations of proposed amplifier

The proposed scheme is shown in Fig. 1. Each stage is an inverting gain stage, and G_{mi} (i = 1, 2, 3, 4) is the transconductance of the corresponding gain stage. R_i (i = 1, 2, 3, L) and C_i (i = 1, 2, 3) represent the output

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resistor and the parasitic capacitor of each stage, respectively. C_L is the load capacitor of the amplifier, much larger than the parasitic capacitor of the fourth stage C_4 so that the latter one can be neglected. Compensation capacitors C_{c1} and C_{c3} both connect to the low-impedance inverting node of the first stage at one terminal, while the other terminal is connected to the output of the second and the fourth stage, respectively. As for C_{c2} and C_{c4}, they both connect to the third stage output node at one terminal, while the other terminal is connected to the low-impedance non-inverting node of the first stage and the low-impedance node of the second stage, respectively. A feedforward path of G_{mf} is inserted between the opamp's input and the output of the third stage, creating an LHP zero to impose the pole-zero cancellation.

Figure 2 is the small-signal diagram of the proposed four-stage opamp, where $i_{c1}=\frac{V_2}{C_{c1}+R_{c1}}$,$i_{c2}=\frac{V_3}{C_{c2}+R_{c2}}$,$i_{c3}=\frac{V_{out}}{C_{c3}+R_{c3}}$,$i_{c4}=\frac{V_3}{C_{c4}+R_{c4}}$ and R_{ci} in series with C_{ci} (i = 1, 2, 3, 4) respectively is a low-value resistor.

In order to analyze the stability of the proposed amplifier, two assumptions are made to simplify the transfer function during the derivation.

(1) The gain of all stages is much greater than 1, or $G_{m1}R_1$, $G_{m2}R_2$, $G_{m3}R_3$, $G_{m4}R_L$ and $G_{mf}R_3 \gg 1$;
(2) The parasitic capacitance of all stages is much smaller than the load capacitance, or C_1, C_2, C_3 and $C_4 \ll C_L$;

Based on the assumptions above, the transfer function is given as

$$A(s) = A_{DC}\frac{b_0 + b_1 s + b_2 s^2 + b_3 s^3 + b_4 s^4 + b_5 s^5 + b_6 s^6}{a_0 + a_1 s + a_2 s^2 + a_3 s^3 + a_4 s^4 + a_5 s^5 + a_6 s^6 + a_7 s^7 + a_8 s^8} \tag{1}$$

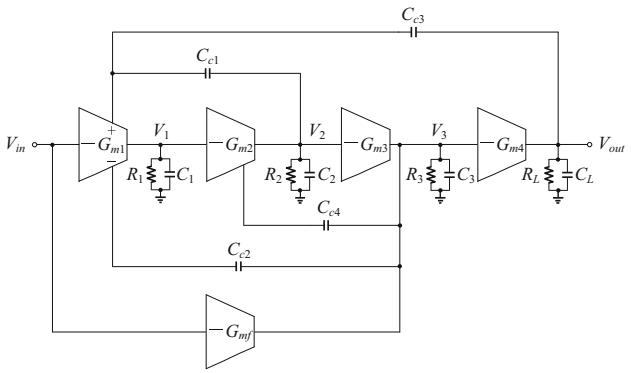

Fig. 1 Block diagram of proposed scheme

where

$$A_{DC} = \left(G_{m1}R_1G_{m2}R_2G_{m3}R_3 + G_{mf}R_3\right)G_{m4}R_4 \tag{2}$$

$$\approx G_{m1}G_{m2}G_{m3}G_{m4}R_1R_2R_3R_4. \tag{3}$$

In order to simplify the transfer function, parts of numerator coefficients are given as

$$b_0 = 1 \tag{4}$$

$$b_1 \approx R_{c1}C_{c1} + R_{c2}C_{c2} + R_{c3}C_{c3} + R_{c4}C_{c4} \tag{5}$$

$$b_2 \approx R_{c1}C_{c1}R_{c2}C_{c2} + R_{c1}C_{c1}R_{c3}C_{c3} + R_{c1}C_{c1}R_{c4}C_{c4} + R_{c2}C_{c2}R_{c3}C_{c3} + R_{c2}C_{c2}R_{c4}C_{c4} + R_{c3}C_{c3}R_{c4}C_{c4} \tag{6}$$

$$b_3 \approx R_{c1}C_{c1}R_{c2}C_{c2}R_{c3}C_{c3} + R_{c1}C_{c1}R_{c2}C_{c2}R_{c4}C_{c4} + R_{c1}C_{c1}R_{c3}C_{c3}R_{c4}C_{c4} + R_{c2}C_{c2}R_{c3}C_{c3}R_{c4}C_{c4} \tag{7}$$

$$b_4 \approx R_{c1}C_{c1}R_{c2}C_{c2}R_{c3}C_{c3}R_{c4}C_{c4} \tag{8}$$

and parts of the denominator coefficients are also given as

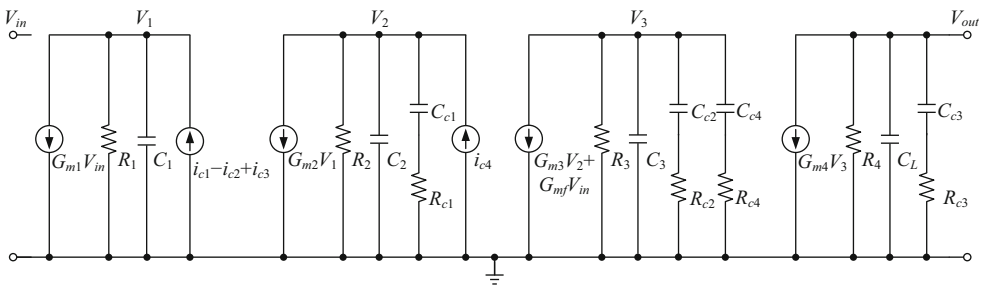

Fig. 2 Small-signal diagram of the proposed amplifier

$$a_0 = 1 \tag{9}$$

$$a_1 \approx G_{m2}G_{m3}G_{m4}R_1R_2R_3R_4C_{c3} \tag{10}$$

$$a_2 \approx G_{m2}G_{m3}G_{m4}R_1R_2R_3R_4C_{c3}(R_{c1}C_{c1} + R_{c2}C_{c2} + R_{c4}C_{c4}) \tag{11}$$

$$a_3 \approx G_{m2}G_{m3}G_{m4}R_1R_2R_3R_4C_{c3} (R_{c1}C_{c1}R_{c2}C_{c2}+R_{c1}C_{c1}R_{c4}C_{c4} + R_{c2}C_{c2}R_{c4}C_{c4}) \tag{12}$$

$$a_4 \approx G_{m2}G_{m3}G_{m4}R_1R_2R_3R_4R_{c1}R_{c2}R_{c4}C_{c1}C_{c2}C_{c3}C_{c4}. \tag{13}$$

Obviously, we can derive several poles and zeros which can cancel each other. These zero-pole doublets are located at $\frac{1}{R_{c1}C_{c1}}$,$\frac{1}{R_{c2}C_{c2}}$, and $\frac{1}{R_{c4}C_{c4}}$. They should be moved far away from the GBW to reduce the impact on large-signal settling. The dominant pole is located at

$$p_{-3dB} = -\frac{a_0}{a_1} = -\frac{1}{G_{m2}G_{m3}G_{m4}R_1R_2R_3R_4C_{c3}}. \tag{14}$$

$GBW = A_{DC} \times p_{-3\ \mathrm{dB}} = G_{m1}/C_{c3}$ is the GBW of the proposed amplifier.

The transfer function exhibits one non-dominant zero and one non-dominant pole at high frequency, which will be neglected in the analysis below because they have negligible influence on the transfer function. The transfer function expressed in Eq. (15) can be rewritten as Eq. (16)

$$p_3 = -\frac{G_{m2}G_{m3}R_{c4}}{G_{m2}C_3R_{c4} + G_{m3}C_1R_{c1}} \tag{20}$$

$$p_4 = -\frac{C_2R_{c1} + C_2R_{c4} + C_3R_{c4}}{C_2C_3R_{c1}R_{c4}}. \tag{21}$$

The load capacitor is much greater than the parasitic capacitor based on the assumptions, and G_{m4} is greater than G_{m1}, G_{m2} and G_{m3} in our design, leading to $p_2 < p_3$. If p_2 is designed to be equal to p_1 by changing the transconductance of output stage, as shown in Eq. (22)

$$\frac{G_{m4}}{C_L} = \frac{1}{R_{c3}C_{c3}}, \tag{22}$$

then G_{m4} is given, where $\frac{1}{R_{c3}C_{c3}}$ is relevant to GBW. If p_3 can cancel z_2, or

$$\frac{G_{m2}G_{m3}R_{c4}}{G_{m2}C_3R_{c4} + G_{m3}C_1R_{c1}} = \frac{G_{m1}G_{m2}G_{m3}}{G_{mf}(R_1C_1 + R_2C_2)}, \tag{23}$$

the exact cancellation will occur at

$$G_{mf} = \frac{G_{m1}(G_{m2}C_3R_{c4} + G_{m3}C_1R_{c1})}{G_{m2}(R_1C_1 + R_2C_2)}. \tag{24}$$

After the circuit design above, if zero-pole cancellations are feasible, then the phase margin (PM) of the proposed amplifier is only determined by p_4, given by

$$A(s) = \frac{A_{DC}(1 + sR_{c3}C_{c3})\left(1 + \frac{G_{mf}(R_1C_1+R_2C_2)}{G_{m1}G_{m2}G_{m3}}s\right)(1 + s/z_{non-dom})}{\left(1 + \frac{s}{p_{-3dB}}\right)\left(1 + \frac{C_L}{G_{m4}}s + \frac{C_LR_{c3}(G_{m2}R_{c4}C_3+G_{m3}R_{c1}C_1)}{G_{m2}G_{m3}G_{m4}R_{c1}R_{c4}}s^2\right)\left(1 + \frac{C_2C_3R_{c1}R_{c4}}{C_2R_{c1}+C_2R_{c4}+C_3R_{c4}}s\right)(1 + s/p_{non-dom})} \tag{15}$$

$$\approx \frac{A_{DC}(1 + sR_{c3}C_{c3})\left(1 + \frac{G_{mf}(R_1C_1+R_2C_2)}{G_{m1}G_{m2}G_{m3}}s\right)}{\left(1 + \frac{s}{p_{-3dB}}\right)\left(1 + \frac{C_L}{G_{m4}}s + \frac{C_LR_{c3}(G_{m2}R_{c4}C_3+G_{m3}R_{c1}C_1)}{G_{m2}G_{m3}G_{m4}R_{c1}R_{c4}}s^2\right)\left(1 + \frac{C_2C_3R_{c1}R_{c4}}{C_2R_{c1}+C_2R_{c4}+C_3R_{c4}}s\right)}. \tag{16}$$

Two LHP zeros can be derived from Eq. (16) as seen in Eq. (17) and Eq. (18)

$$z_1 = -\frac{1}{R_{c3}C_{c3}} \tag{17}$$

$$z_2 = -\frac{G_{m1}G_{m2}G_{m3}}{G_{mf}(R_1C_1 + R_2C_2)} \tag{18}$$

and three non-dominant poles are given as

$$p_2 = -\frac{G_{m4}}{C_L} \tag{19}$$

$$\begin{aligned} PM = {} & 180^\circ - \arctan\left(\frac{GBW}{p_{-3dB}}\right) - \arctan\left(\frac{GBW}{p_2}\right) \\ & - \arctan\left(\frac{GBW}{p_3}\right) - \arctan\left(\frac{GBW}{p_4}\right) \\ & + \arctan\left(\frac{GBW}{z_1}\right) + \arctan\left(\frac{GBW}{z_2}\right) \end{aligned} \tag{25}$$

$$\approx 90^\circ - \arctan\left(\frac{GBW}{p_4}\right). \tag{26}$$

Considering the existence of zero-pole doublets and pole p_4, all of zeros and poles should be designed

reasonably to obtain better PM and faster settling. The pole-zero doublets will cause oscillations in the time domain and the poles can reduce the phase margin of the amplifier, so their frequencies should be located higher than the GBW.

3 Circuit implementations of proposed amplifier

Split-length devices [5] can generate low-impedance nodes effectively, moving poles to higher frequency, thus expanding the bandwidth. As shown in Fig. 3, an nMOS transistor M_1 with the length of L is split into two transistors M_{1T} and M_{1B} of lengths L_1 and L_2, respectively, where $L = L_1 + L_2$. The top transistor M_{1T} is in the saturation region and the bottom one M_{1B} is in the triode region. Node A is a low-impedance node since the output resistance at node A is equal to $(1/g_{m,M_{1B}}) \| r_{on,M_{1T}} \approx 1/g_{m,M_{1B}}$.The V_{DS} of the transistor in the triode region can be designed to be very small; therefore, split-length transistor reduces the difficulty of vertically stacking transistors at low voltage. If $L_1 = L_2$, then the effective transconductance of the spilt-length transistor is given by $g_{m,eff} = 1/R_c = g_{m1}/\sqrt{2}$, where g_{m1} represents the transconductance of the individual MOS transistor with length L_1 in the saturation region.

Indirect compensation can be realized by split-length current mirror load (SLCL) or split-length diff-pair (SLDP). Figure 4(a) shows a SLCL structure for indirect compensation. Current mirror load is implemented by split-length transistors, which offers a low-impedance

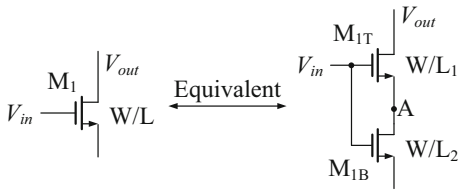

Fig. 3 Split-length transistor in nMOS configuration

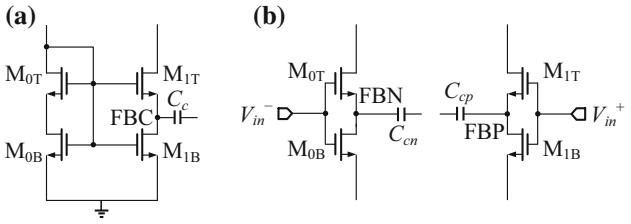

Fig. 4 Indirect compensation using split-length transistors **a** SLCL structure **b** SLDP structure

node FBC connected with compensation capacitor C_c. Figure 4(b) shows a SLDP structure where node FBP is a positive-input low-impedance node and node FBN is a negative-input low-impedance node. In-phase voltages are required to be connected to the terminals of the compensation capacitor C_{cp} and C_{cn} to perform negative feedback. When the compensation current through the compensation capacitor is fed back to the low-impedance node, the pole will be located at higher frequency than that of the high-impedance node, thus extending the bandwidth. These two structures using split-length transistors are both adopted in the proposed four-stage opamp.

The circuit schematic of the four-stage amplifier is shown in Fig. 5, in which each transistor M_i has its own transconductance g_{mi}. V_{BN} and V_{BP} are bias voltages. The input stage is realized by transistors M_0, M_{1T}, M_{1B}, M_{2T}, M_{2B}, M_3 and M_4. Split-length nMOS transistors compose a differential input pair and $G_{m1} = g_{m1T}/\sqrt{2} = g_{m2T}/\sqrt{2}$, where transistors M_{1T}, M_{1B}, M_{2T} and M_{2B} have the same length and width. The second stage ($G_{m2} = g_{m6} = g_{m7}$) is made up of transistors M_5, M_6, M_7, M_{8T}, M_{8B}, M_{9T} and M_{9B}, in which transistors M_{8T}, M_{8B}, M_{9T} and M_{9B} comprise SLCL structure connected with compensation capacitor C_{c4}. The third stage consists of transistors M_{10}, M_{11}, M_{12}, M_{16} and M_{17}, and $G_{m3} = g_{m11} = g_{m12}$. The common source amplifier M_{18} and current source load M_{19} which is biased by V_{BN} realize the fourth stage, where $G_{m4} = g_{m18}$. The feedforward path is implemented by transistors M_{13}, M_{14}, M_{15}, M_{16} and M_{17} and $G_{mf} = -g_{m14} = g_{m15}$. The compensation network is accomplished by compensation capacitors C_{c1}, C_{c2}, C_{c3}, C_{c4} and transistors connected with them. The first three compensation capacitors connected with the SLDP structure are used to indirectly feed back the compensation current to the output of the first stage, while C_{c4} connects node FBC in the SLCL structure of the second stage. It is noted that C_{c1} and C_{c3} are connected with a positive feedback node, or node FBP, while C_{c2} is connected with a negative feedback node, or node FBN.

The settling time (ts) of an amplifier can be divided into a quasi-linear region and an exponential slewing region. The pole-zero doublets do not exist within the GBW in our design. Hence, the output voltage of the four-stage opamp can settle within a short duration in the quasi-linear region. The Slew rate (SR) defines how fast a given load can be charged or discharged. The SR of the proposed amplifier is given by

$$SR = \min\left(\frac{I_{SS1}}{C_{c1}}, \frac{I_{SS1}}{C_{c2}}, \frac{I_{SS1}}{C_{c3}}, \frac{I_{SS2}}{C_{c4}}, \frac{I_L}{C_L}\right), \tag{27}$$

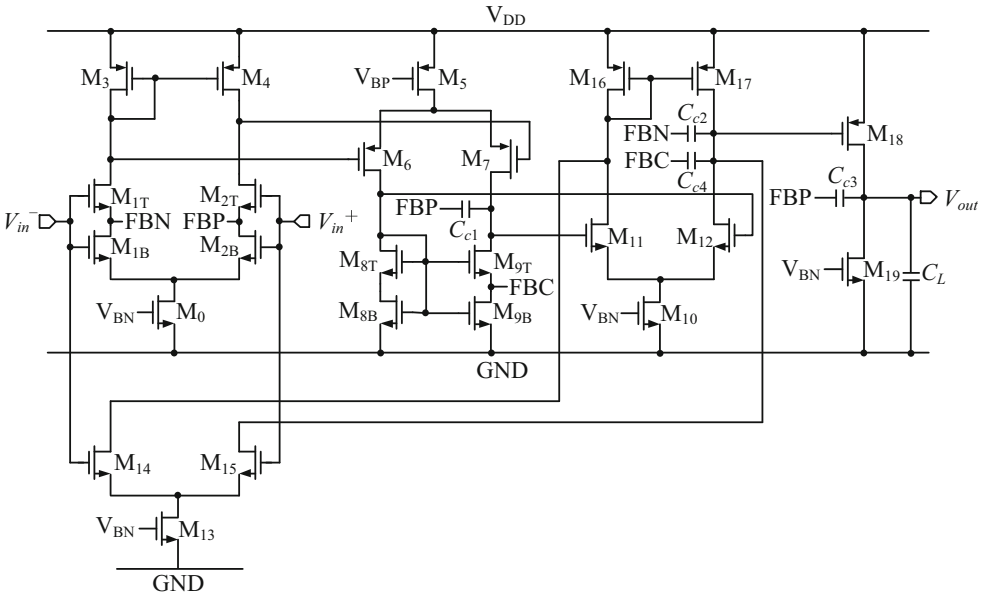

Fig. 5 Circuit schematic of the proposed amplifier

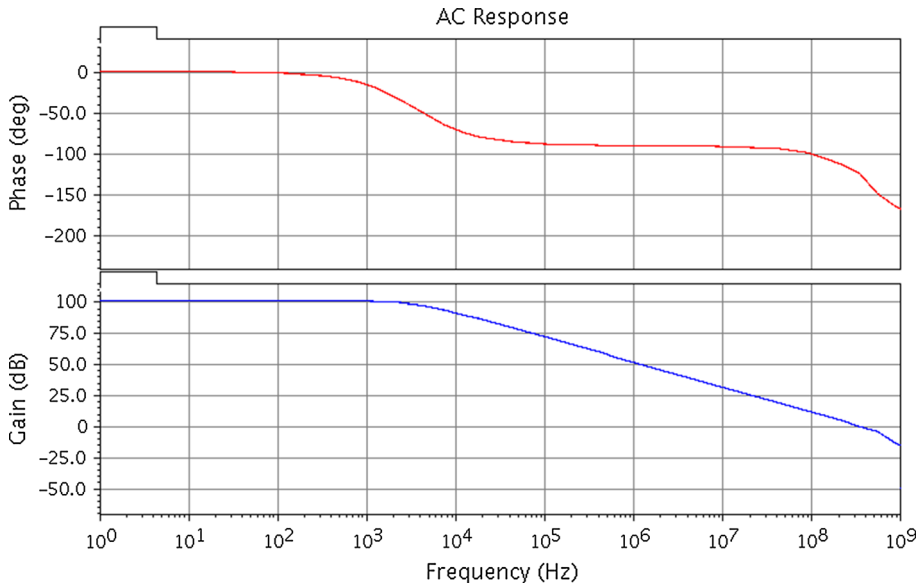

Fig. 6 Simulated gain and phase responses of the proposed amplifier

where I_{SS1} and I_{SS2} are the first and second stage tail current, respectively, and I_L is the amount of current available to charge or discharge C_L.

4 Simulation results

The amplifier with 5 pF capacitive load is simulated in TSMC 65 nm 1.2 V CMOS process. From Fig. 6, the proposed amplifier achieves a DC open-loop gain of 101.1 dB, a GBW of 330.0 MHz, a phase margin of 58.0° with a current of 1.3 mA from a 1.2 V supply voltage. Taking process variation into consideration, process corner simulations are shown in Fig. 7. The simulation results are summarized in Table 1 for three different process corner cases.

Figure 8 shows the closed-loop unity-gain step response with a 0.3 V step input. The measured result indicates that average SR is 266.3 V/μs and average 1 % ts is 9.3 ns.

Comparisons with other compensation schemes are made in Table 2. The proposed four-stage operational

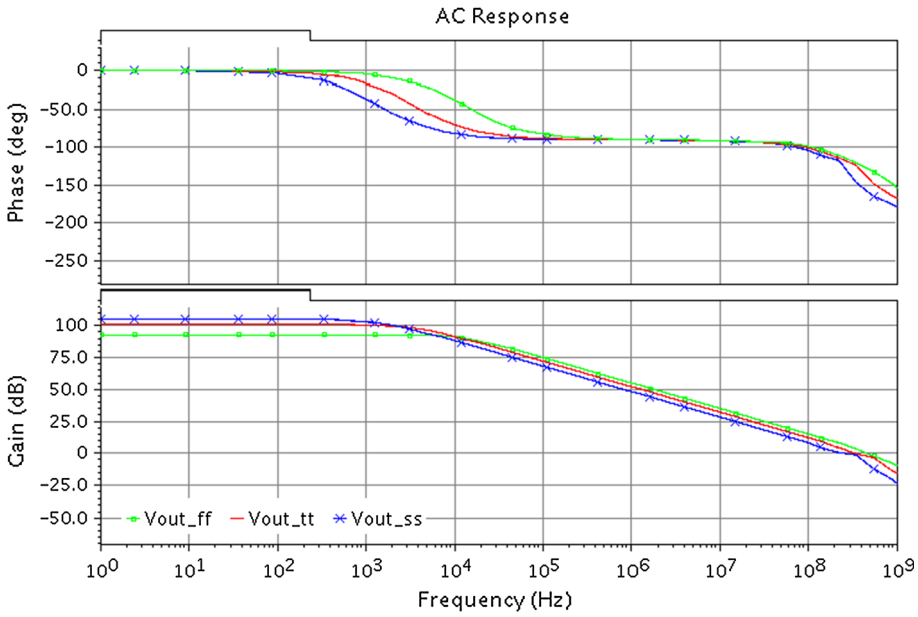

Fig. 7 AC simulations of process corner

Table 1 Summary of simulation results on process corner

Process corner	FF	TT	SS
DC gain (dB)	93.0	101.1	105.0
GBW (MHz)	430.0	330.0	234.7
PM (°)	58.4	58.0	53.5

amplifier combines competitive DC gain and GBW while its total compensation capacitance is less than 1 pF. Larger FoM_S (=*GBW* C_L/*power*), FoM_L (=*SR* C_L/*power*), FoM_S (=*GBW* C_L/I_{DD}), and IFoM_L (=*SR* C_L/I_{DD}) are also achieved than the other multi-stage amplifiers driving small on-chip capacitors, indicating the better performance of the proposed design.

5 Conclusion

A four-stage opamp with the novel compensation network, which combines indirect compensation technique and feedforward compensation technique, is presented in this paper. According to indirect compensation strategy, split-length transistors providing low-impedance node are used

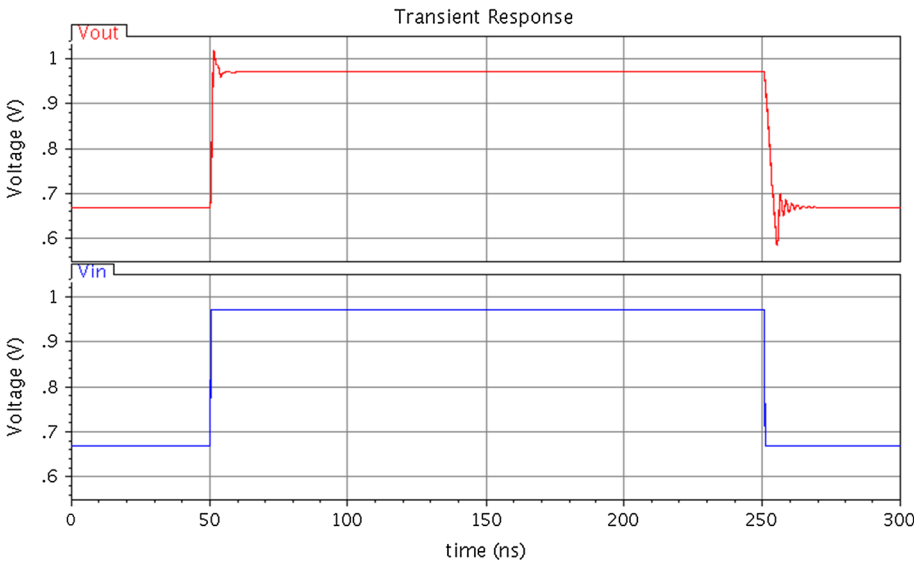

Fig. 8 Unity-gain buffer transient response

Table 2 Comparisons of different multi-stage amplifiers with small capacitive load

	This work[a]	[6][b] NCFF	[7][c] IRFC	[8][a] DFCFC	[9][a] RNMC
DC gain (dB)	101.1	91.0	64.9	72.8	72.2
GBW (MHz)	330.0	325.0	67.0	221.5	121.0
PM (°)	58.0	N/A	72.7	61.6	63.8
C_L (pF)	5.0	8.0	5.5	2.0	2.0
C_c (pF)	0.725	0	0	1	2
Power dissipation (mW@V)	1.56@1.2	18@2.5	0.36@1.2	2.9@1.2	2.5@1.2
SR (V/μs)	266.3	140.0	20.70	244.5	487.9
1 %Ts (ns)	9.3	5.1	N/A	8.4	7.5
FoM_S (MHz pF/mW)	1057.7	147.5	977.8	152.8	96.8
FoM_L (V/μs pF/mW)	853.5	63.5	316.3	168.6	390.3
$IFoM_S$ (MHz pF/mA)	1269.2	368.7	1173.3	183.3	116.2
$IFoM_L$ (V/μs pF/mA)	1024.2	158.8	379.5	202.3	468.4
CMOS process	65 nm	0.5 μm	0.13 μm	90 nm	90 nm

[a] Simulated results

[b] Post-layout results

[c] Measured results

to accomplish frequency compensation. By adjusting feedforward transconductance stage, an LHP zero can be generated to cancel a pole. The power consumption is reduced compared with conventional NCFF amplifier. The proposed opamp is simulated in TSMC 65 nm 1.2 V CMOS process, achieving 101.1 dB DC gain, 330.0 MHz GBW and 266.3 V/μs slew rate with 1.2 V supply voltage.

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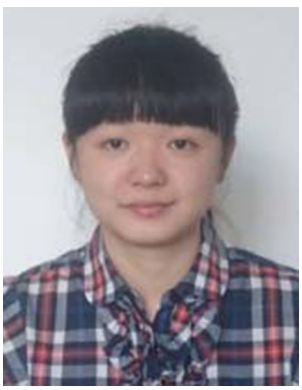

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