A 0.5V fully differential transimpedance amplifier in 65-nm CMOS technology

Hugo García-Vázquez, Fortunato Carlos Dualibe, and Grigory Popov
Analog and Mixed Signal Design Group, Electronic and Microelectronic Unit, University of Mons
31, Boulevard Dolez, 2nd building, 1st floor
7000 Mons, Belgium
{hugo.garciavazquez ; fortunato.dualibe}@umons.ac.be

***Abstract*—This paper proposes a novel fully differential ultra-low voltage transimpedance amplifier (TIA) based on a CMOS translinear circuit. Following a simple bias strategy, its transimpedance gain can be adjusted to the desired accuracy either by means of an external resistor or using internal voltage and current references. To a first order approach, the transresistance results independent from technological parameters. The amplifier does not need a common mode feedback circuit (CMFB) to set the quiescent output voltages. The circuit was sized and simulated in a 65-nm CMOS process to comply with a 10kΩ transimpedance gain and 1MHz@1pF bandwidth. For a 0.5V supply voltage the total power consumption is 78.5μW.**

Keywords—Transimpedance Amplifier, fully differential, CMOS, 65-nm, RF front end, mixer, IoT.

I. INTRODUCTION

Nowadays, the Internet of Things (IoT) is becoming a ubiquitous technology. Thanks to the IoT all objects in homes, offices, industries, hospitals, farms, public buildings, public spaces… become smart, so they can be controlled from anywhere in the world. It is expected that in the near future everything will be wirelessly interconnected for data exchange [1-2].

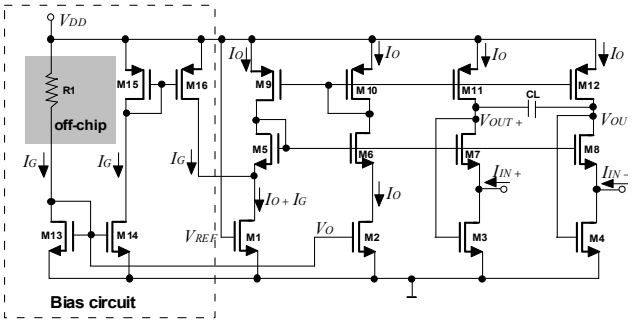
Key enabling technologies for the IoT are the short–range communication systems that must be added to sensors and actuators of the IoT's objects. These devices must normally remain operable for weeks, months or even years supplied with a single battery or even by means of energy harvesting techniques. Therefore, the use of ultra-low power and ultra-low voltage RF transceivers becomes mandatory for this kind of application. With this objective, new low-power standards have been implemented. One example is the Bluetooth low-energy that operates in the 2.4GHz ISM band with fewer channels of 1MHz bandwidth [3-8].

On the other hand, at the transceivers front-ends, the mixer is one of the most power consuming RF blocks. In recent years however, active mixers have been substituted by passive ones that feature considerably reduced power consumption. A typical passive mixer comprises four cross-coupled switching transistors driving a transimpedance amplifier [9]. The latter is normally built from a fully differential operational amplifier and two matched feedback resistors that define the transimpedance gain.

In contrast to this typical TIA implementation we introduce herein a novel MOST-only fully differential device which does not need neither internal matched resistors nor a CMFB circuit. It is based on the two-quadrant analogue divider presented by Dualibe, Verleysen and Jespers in [10] and can be used for ultra-low voltage applications.

This paper is structured as follows: in section II we introduce the circuit of the TIA and the fundamental equations describing its working principle. In section III design issues are commented. Section IV describes the simulations carried out and their results. Finally, in the conclusions, we summarize pros and cons of this achievement.

Fig. 1. Schematic of the fully differential TIA



II. CIRCUIT DESCRIPTION

The fully differential transimpedance amplifier is shown in Fig.1. It includes a bias circuit that will be explained later. The active part of the amplifier comprises transistors M_1-M_{12}, which are row-wise equally sized. Starting from the translinear circuit in [10] transistors M_4, M_8 and M_{12} must be added in order to build a fully differential device [11]. For correct operation, transistors M_1-M_4 are constrained to operate in the triode region of the strong inversion. The M_2 drain current (Io) is replicated at all branches by means of the upper PMOS multiple mirror built by M_9-M_{12}. This warrants identical V_{GS} drops in all NMOS transistors in the middle row and, consequently, the same V_{DS} for all triode transistors in the bottom row. While V_{REF} and V_0 are fixed bias voltages the gate-to-source voltages of M_3 and M_4 (i.e. V_{OUT+} and V_{OUT-})

self-adjust according to the values of the currents at the TIA's inputs (i.e. I_{IN+} and I_{IN-}). Due to the triode operation of transistors M_1-M_4 and the ultra-low voltage requirement for this particular implementation V_{REF} was connected to the maximum available voltage (i.e. V_{DD}), as shown in fig. 1. Nevertheless, in the most general case (i.e. $V_{REF} \neq V_{DD}$) we can write:

$$I_O = \mu_N Cox\left(\frac{W}{L}\right)_2 V_{DS2}\left(V_O - V_{THN} - \frac{n_N}{2}V_{DS2}\right) \quad (1)$$

$$I_O + I_G = \mu_N Cox\left(\frac{W}{L}\right)_1 V_{DS1}\left(V_{REF} - V_{THN} - \frac{n_N}{2}V_{DS1}\right) \quad (2)$$

$$I_O + I_{IN+} = \mu_N Cox\left(\frac{W}{L}\right)_3 V_{DS3}\left(V_{OUT+} - V_{THN} - \frac{n_N}{2}V_{DS3}\right) \quad (3)$$

$$I_O + I_{IN-} = \mu_N Cox\left(\frac{W}{L}\right)_4 V_{DS4}\left(V_{OUT-} - V_{THN} - \frac{n_N}{2}V_{DS4}\right) \quad (4)$$

Assuming ideal matching conditions all drain-to-source voltage drops of the triode transistors are identical. Therefore, the equations above lead to

$$\left.\begin{aligned} V_{OUT+} - V_O &= (V_{REF} - V_O)\frac{I_{IN+}}{I_G} \\ V_{OUT-} - V_O &= (V_{REF} - V_O)\frac{I_{IN-}}{I_G} \end{aligned}\right\} \rightarrow (V_{OUT+} - V_{OUT-}) = \frac{V_{REF} - V_O}{I_G}(I_{IN+} - I_{IN-}) \quad (5)$$

Thus, the fully differential transimpedance gain R_G is given by:

$$R_G = \frac{V_{OUT+} - V_{OUT-}}{I_{IN+} - I_{IN-}} = \frac{V_{OUT}}{I_{IN}} = \frac{V_{REF} - V_O}{I_G} \quad (6)$$

At first glance, R_G does not depend on technological parameters as long as V_{REF}-V_O and I_G are obtained from on-chip voltage and current reference circuits, respectively. This property makes this circuit less sensitive to process variations. But, if reference circuits are not available on-chip the biasing scheme proposed in Fig. 1 gives a simple and robust solution at the price of only one extra package pin, which is needed for connecting an external accurate resistor R_1. In this case, assume that both current mirrors at the bias circuit (i.e. M_{13}-M_{14} and M_{15}-M_{16}) have unity mirroring ratios. Since the gate-to-source voltage of M_{13} (V_O) biases the M_2´s gate and V_{REF} is connected to V_{DD} the transimpedance gain given by (6) becomes equal to R_1.

Notice that the DC levels of the TIA's outputs are settled by the negative feedback loop around transistors M_3 and M_7 for V_{OUT+} and M_4 and M_8 for V_{OUT-}. Therefore, no common mode feedback (CMFB) circuit is required. Furthermore, when multiple instances of the TIA are used in a given application (i.e. I/Q quadrature mixers) there is no need to replicate the whole circuit in Fig. 1 but only the two last transistor columns on the right. The remaining transistors can be shared by the different instances. These two latter features benefit from considerable savings on die area and current consumption for those kinds of applications [3-8].

III. CIRCUIT DESIGN

A proof-of-concept circuit was sized and simulated, following the requirements of a range of applications reported in [3-8]. It features a nominal transimpedance gain R_G=10kΩ and 1MHz of bandwidth for a differential load C_L=1pF. The design complies with V_{DD}=0.5V in a 65-nm CMOS process, with typical parameters V_{THN}=0.2V, V_{THP}=-0.2V, $\mu_N C_{OX}$=500μA/V², $\mu_P C_{OX}$=180μA/V². The extracted Body effect coefficients are n_N=n_P=1.2.

Using MOST triode equations, the current I_O is determined by

$$I_O = \frac{V_O - V_{THN} - \frac{n_N V_{DS,M2}}{2}}{R_G} \quad (7)$$

From which the size of the bottom row transistors can be calculated as

$$\left(\frac{W}{L}\right)_{1,2,3,4} = \frac{1}{\mu_N C_{OX} V_{DS,M2} R_G} \quad (8)$$

Hence, the smaller the desired transimpedance, the higher the current consumption and the larger the triode transistors.

The minimal power supply is limited by the sum of voltage drops along the column of transistors M_2-M_6-M_{10}:

$$V_{DD} \geq \left|V_{THP,M10}\right| + G_{VO,M10} + V_{DS,M6} + V_{DS,M2} \quad (9)$$

where $G_{VO,M10}$ is the gate-voltage-overdrive (i.e. V_{GS}-$|V_{THP}|$) of transistor M_{10}. For a positive R_G, equation (6) together with the biasing conditions demanded by the triode operation of the bottom transistors row, lead to the following constraints

$$V_{REF} > V_o = V_{THN} + G_{VO,M2} \quad and \quad G_{VO,M2} > n_N V_{DS,M2} \quad (10)$$

In order to define the optimal drain-to-source voltage for the triode transistors, its bounds have been investigated. The upper limit for V_{DS} results after trading the current consumption in (7) and the triode transistors size in (8) with the available voltage headroom in (9), constrained by the triode condition in (10). This must always be accomplished. The lower V_{DS} limit however, should be much greater than the standard deviation due to mismatch of the V_{GS} (σ_{VGS}) of the middle row transistors. This way, the matching properties of M_1-M_4 are improved. Hence, biasing M_5-M_8 in weak-inversion is recommended because σ_{VGS} normally results very small in such a region.

In agreement with everything explained above, the nominal V_{DS} of the triode transistors (i.e. for R_G=10kΩ) was fixed to 50mV. The V_{DSAT} of M_6 operating in week inversion (V_{DSAT}=3~4 kT/q), is around 100mV. It means that, with V_{DD}=0.5V, there is still enough room (150mV) for the gate-voltage-overdrive of M_{10}. Setting V_O=V_{THN}+0.2V=0.4V, the current I_G given by (6) is 10μA whereas I_O, from (7), rounds to 17μA.

In order to minimize the Early effect, all the transistors' lengths were set to L=1μm, which is more than ten times the minimal length allowed in this technology. Therefore, from (8) we can calculate $W_{1,2,3,4}$.

All saturated transistors were sized following the methodology presented in [12-13] which is based on the gm/ID ratio of MOS transistors. Aiming to reduce the size of the transistors M_5-M_8 that work in weak inversion we adopted a normalized current ID/(W/L)=100nA. This warrants at least gm/ID=25V^{-1}.

In order to keep the mismatch errors in the PMOS mirrors as small as possible, transistors M_9-M_{12} and M_{15}-M_{16} should be biased in strong inversion. However, due to the extremely reduced voltage room those transistors actually work in moderate inversion (gm/ID=15V^{-1}), with tolerable impact on the circuit accuracy. Finally, the mirror M_{13}-M_{14} was biased in strong inversion (gm/ID=10V^{-1}). Table I below summarizes the adopted transistor sizes and their gm/ID.

TABLE I: TIA'S TRANSISTOR SIZES

	$M_{1,2,3,4}$	$M_{5,6,7,8}$	$M_{9,10,11,12}$	$W_{13,14}$	$M_{15,16}$
W	20μm	170μm	168.6μm	0.707μm	500μm.
L	1 μm	1 μm	1 μm	1 μm	1μm
gm/ID	---------	25V^{-1}.	15V^{-1}.	10V^{-1}	15V^{-1}.

IV. SIMULATION RESULTS

Simulations were carried out using the BSIM4 MOS model. Fig. 2 shows the DC input-output characteristic of the TIA for the different corners of the technology. The maximum deviation with respect to the typical case is smaller than 12.4% within the linear range, which is defined for the interval $|I_N| \leq 20\mu A$. Also, a mismatch simulation including process variation was carried out for the transimpedance gain R_G. The deviation with respect to the nominal value is smaller than 14%. This can be appreciated in Fig. 3. It should be taken into account that the latter feature can be further improved by means of proper layout techniques.

Fig. 4 shows the frequency response of the TIA loaded with C_L=1pF for different values of the external resistor R_1 in the range 9kΩ to 11kΩ. Within the TIA passband the transimpedance gain tracks the value of the external resistor with a maximum divergence of 0.4%.

The sensitivity to power supply variation was tested by increasing V_{DD} to 0.6V. In this case, the obtained transimpedance gain exceeds its nominal value by less than 0.17%. The small-signal power supply rejection (PSR) over frequency was also simulated for the different corners. Results are shown in Fig. 5. In the worst case the PSR inside band is -42dB.

In order to evaluate the linearity of the circuit the total harmonic distortion (THD) was simulated at the typical corner (TT) for a 1MHz sinusoidal input current with amplitudes ranging from 0.1μA to 30μA. In Fig. 6 it can be appreciated that the THD is kept below 1.1% for $I_{IN} \leq 26\mu A$.

Table II summarizes the main features of this amplifier.

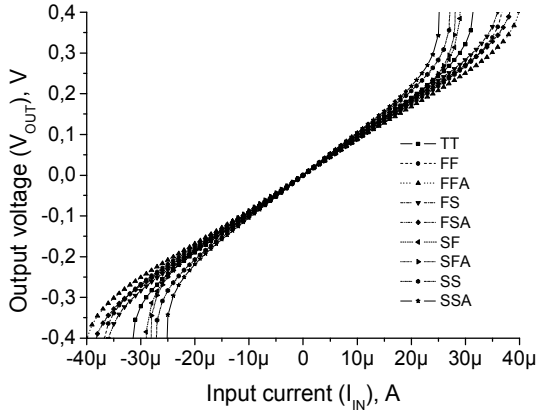


Fig. 2 Output voltage V_{OUT} versus input current I_{IN} for different corners.

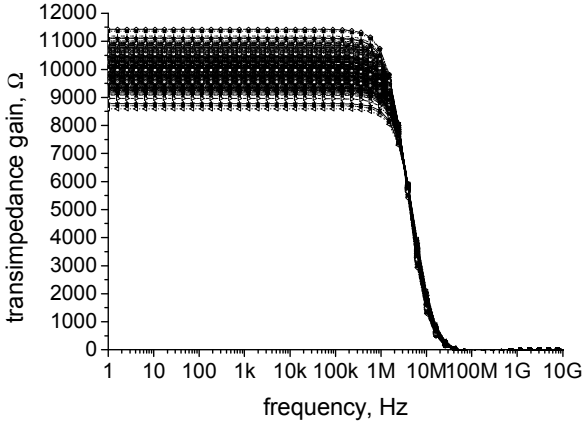


Fig. 3 TIA frequency response variations with mismatch and process.

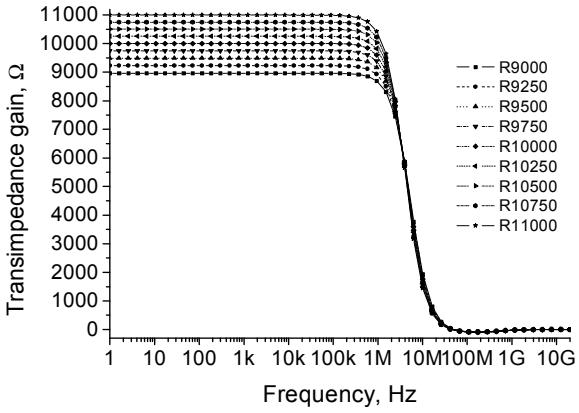


Fig. 4 TIA frequency response for R_1=9k~11kΩ.

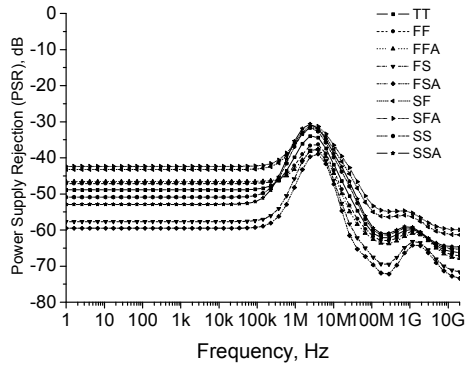


Fig. 5 Power Supply Rejection (PSR) for different corners.

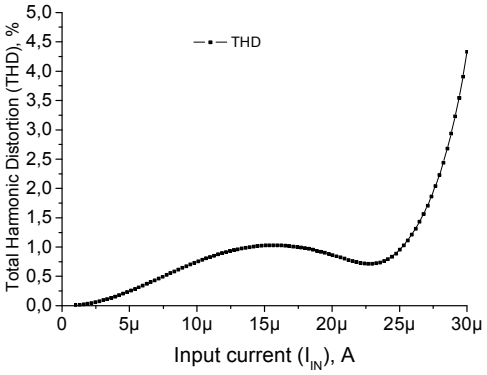


Fig. 6 Total Harmonic Distortion (THD) over I_{IN}.

TABLE II: TIA'S MAIN FEATURES

	Features
Technology:	CMOS 65-nm
Minimum Voltage Supply:	0.5V
Power consumption:	78.5µW
Active area:	2521 μm^2
Transimpedance RG:	10kΩ
Bandwidth	1MHz@C_L=1pF
THD	<1.1% @ $I_{IN} \leq$ 26µA
Power Suply Rejection (PSR)	> 42dB@1MHz
Line regulation ($\Delta R_G / \Delta V_{DD}$)	170Ω/V
Maximum mismatch deviation	14%

V. CONCLUSIONS

A novel application of the analogue divider reported in [10] has been proposed for designing a transimpedance amplifier. The presented low transistor-count fully differential version does not need an additional CMFB circuit for settling the DC voltage level of its outputs. Its transimpedance gain can be accurately set by means of on-chip voltage and current reference circuits or by an external precision resistor. Moreover, in applications where several transimpedance amplifiers are required, considerable savings on power and area can be achieved since part of the circuit can be shared among the different TIA instances. According to simulation results this circuit can be used in ultra-low voltage applications like the ones reported in [3-8].

ACKNOWLEDGMENTS

This paper is a tribute to our colleague Grigory Popov who suddenly passed away on December 2, 2016.

This work was supported by the Belgium Walloon Region, BEWARE Fellowships program (1410164-POHAR).

REFERENCES

1. S. Mumtaz, A. Alsohaily, Z. Pang, A. Rayes, K. F. Tsang and J. Rodriguez, "Massive Internet of Things for Industrial Applications: Addressing Wireless IIoT Connectivity Challenges and Ecosystem Fragmentation," in IEEE Industrial Electronics Magazine, vol. 11, no. 1, pp. 28-33, March 2017.
2. M. Wollschlaeger, T. Sauter and J. Jasperneite, "The Future of Industrial Communication: Automation Networks in the Era of the Internet of Things and Industry 4.0," in IEEE Industrial Electronics Magazine, vol. 11, no. 1, pp. 17-27, March 2017.
3. A. Selvakumar, M. Zargham and A. Liscidini, "13.6 A 600µW Bluetooth low-energy front-end receiver in 0.13µm CMOS technology," 2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers, San Francisco, CA, 2015, pp. 1-3.
4. Masuch, J.; Delgado-Restituto, M., "A 1.1-mW-RX 81.4-dBm Sensitivity CMOS Transceiver for Bluetooth Low Energy," in Microwave Theory and Techniques, IEEE Transactions on , vol.61, no.4, pp.1660-1673, April 2013.
5. Bryant, C.; Sjoland, H., "A 0.55 mW SAW-Less Receiver Front-End for Bluetooth Low Energy Applications," in Emerging and Selected Topics in Circuits and Systems, IEEE Journal on , vol.4, no.3, pp.262-272, Sept. 2014.
6. L. Liao et al., "A 1.2V, 2.7mA receiver front-end for bluetooth low energy applications," 2014 IEEE Radio and Wireless Symposium (RWS), Newport Beach, CA, 2014, pp. 37-39.
7. J. Masuch, M. Delgado-Restituto and A. Rodriguez-Vazquez, "Transformer based front-end for a low power 2.4 GHz transceiver," 2010 IEEE Asia Pacific Conference on Circuits and Systems, Kuala Lumpur, 2010, pp. 288-291.
8. D. Pietron, K. Siwiec, J. Kopanski and W. A. Pleskacz, "Implementation of the Bluetooth receiver RF front-end in the CMOS-RF 130 nm technology," 2014 Proceedings of the 21st International Conference Mixed Design of Integrated Circuits and Systems (MIXDES), Lublin, 2014, pp. 230-235.
9. Sackinger, E., "The Transimpedance Limit," in Circuits and Systems I: Regular Papers, IEEE Transactions on , vol.57, no.8, pp.1848-1856, Aug. 2010.
10. Dualibe, C.; Verleysen, M.; Jespers, P., "Two-quadrant CMOS analogue divider," in Electronics Letters , vol. 34, no. 12, pp.1164-1165, 11 Jun 1998.
11. Dualibe C., Jespers P. and Verleysen M., "Embedded fuzzy control for automatic channel equalization after digital transmissions," ISCAS 2001. The 2001 IEEE International Symposium on Circuits and Systems (Cat. No.01CH37196), Sydney, NSW, 2001, pp. 173-176 vol. 2.
12. Silveira, F.; Flandre, D.; Jespers, P.G.A., "A gm/ID based methodology for the design of CMOS analog circuits and its application to the synthesis of a silicon-on-insulator micropower OTA," in Solid-State Circuits, IEEE Journal of , vol.31, no.9, pp.1314-1319, Sept 1996.
13. Fiorelli, R.; Silveira, F.; Peralias, E., "MOST Moderate–Weak-Inversion Region as the Optimum Design Zone for CMOS 2.4-GHz CS-LNAs," in Microwave Theory and Techniques, IEEE Transactions on , vol.62, no.3, pp.556-566, March 2014.