TIMING ANALYSIS

1. Ripple Carry Adder

Timing constraint: Default path analysis
Total number of paths / destination ports: 100 / 9

Delay: 2.662ns (Levels of Logic = 7)
Source: a<1> (PAD)
Destination: sum<7> (PAD)

Data Path: a<1> to sum<7>

Cell:in->out	Gate fanout	Net Delay	Delay	Logical Name (Net Name)
IBUF:I->O	3	0.001	0.693	a_1_IBUF (a_1_IBUF)
LUT5:I0->O	2	0.097	0.299	a3/Madd_n0003_Madd_cy<0>11 (a3/Madd_n0003_Madd_cy<0>1)
LUT3:I2->O	3	0.097	0.305	a3/Madd_n0003_Madd_cy<0>12 (a3/Madd_n0003_Madd_cy<0>)
LUT5:I4->O	2	0.097	0.299	a6/Madd_n0003_Madd_cy<0>11 (a6/Madd_n0003_Madd_cy<0>1)
LUT3:I2->O	2	0.097	0.299	a6/Madd_n0003_Madd_cy<0>12 (a6/Madd_n0003_Madd_cy<0>)
LUT5:I4->O	1	0.097	0.279	a8/Madd_n0003_Madd_cy<0>11 (a8/Madd_n0003_Madd_cy<0>)
OBUF:I->O		0.000		c_out_OBUF (c_out)

Total 2.662ns (0.486ns logic, 2.176ns route)
(18.3% logic, 81.7% route)

2. Hybrid Adder

Delay: 2.571ns (Levels of Logic = 6)
Source: a<1> (PAD)
Destination: sum<6> (PAD)

Data Path: a<1> to sum<6>

Cell:in->out	Gate fanout	Net Delay	Delay	Logical Name (Net Name)
IBUF:I->O	2	0.001	0.687	a_1_IBUF (a_1_IBUF)
LUT5:I0->O	3	0.097	0.305	a1/temp_c<1><1>1 (a1/temp_c<1>)
LUT5:I4->O	3	0.097	0.389	a1/cout<3>1 (temp)
LUT5:I3->O	3	0.097	0.521	a2/temp_c<1><1>1 (a2/temp_c<1>)
LUT3:I0->O	1	0.097	0.279	a2/Mxor_sum<2>_xo<0>1 (sum_6_OBUF)
OBUF:I->O		0.000		sum_6_OBUF (sum<6>)

Total 2.571ns (0.389ns logic, 2.182ns route)
(15.1% logic, 84.9% route)

3. Bit Serial Adder (Delay for single clock cycle)

Timing constraint: Default period analysis for Clock 'clk'
Clock period: 1.027ns (frequency: 974.184MHz)
Total number of paths / destination ports: 33 / 24

Delay: 1.027ns (Levels of Logic = 1)
Source: b1/out_0 (FF)
Destination: X/sum_7 (FF)
Source Clock: clk rising
Destination Clock: clk rising

Data Path: b1/out_0 to X/sum_7

Cell:in->out	Gate fanout	Net Delay	Delay	Logical Name (Net Name)
FDC:C->Q	2	0.361	0.561	b1/out_0 (b1/out_0)
LUT5:I1->O	1	0.097	0.000	temp_s1 (temp_s)
FDC:D		0.008		X/sum_7
Total		1.027ns (0.466ns logic, 0.561ns route) (45.4% logic, 54.6% route)		

Total Delay = 8 * 1.027ns = 8.21 ns

HARDWARE REQUIREMENTS

1. Ripple Carry Adder

Device utilization summary:

Selected Device : 7a100tcsg324-3

Slice Logic Utilization:
Number of Slice LUTs: 12 out of 63400 0%
Number used as Logic: 12 out of 63400 0%

Slice Logic Distribution:
Number of LUT Flip Flop pairs used: 12
Number with an unused Flip Flop: 12 out of 12 100%
Number with an unused LUT: 0 out of 12 0%
Number of fully used LUT-FF pairs: 0 out of 12 0%
Number of unique control sets: 0

IO Utilization:
Number of IOs: 26
Number of bonded IOBs: 26 out of 210 12%

2. Hybrid Adder

Device utilization summary:

Selected Device : 7a100tcsg324-3

Slice Logic Utilization:
 Number of Slice LUTs: 18 out of 63400 0%
  Number used as Logic: 18 out of 63400 0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used: 18
  Number with an unused Flip Flop: 18 out of 18 100%
  Number with an unused LUT: 0 out of 18 0%
  Number of fully used LUT-FF pairs: 0 out of 18 0%
  Number of unique control sets: 0

IO Utilization:
 Number of IOs: 26
 Number of bonded IOBs: 26 out of 210 12%

3. Bit Serial Adder

Device utilization summary:

Selected Device : 7a100tcsg324-3

Slice Logic Utilization:
 Number of Slice Registers: 27 out of 126800 0%
 Number of Slice LUTs: 20 out of 63400 0%
  Number used as Logic: 20 out of 63400 0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used: 29
  Number with an unused Flip Flop: 2 out of 29 6%
  Number with an unused LUT: 9 out of 29 31%
  Number of fully used LUT-FF pairs: 18 out of 29 62%
  Number of unique control sets: 4

IO Utilization:
 Number of IOs: 29
 Number of bonded IOBs: 28 out of 210 13%

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs: 1 out of 32 3%