Hybrid-Phase Metal Oxide Thin-Film Transistors and their Applications

by

Sunbin DENG

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The Hong Kong University of Science and Technology
in Partial Fulfillment of the Requirements for
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This is to certify that I have examined the above PhD thesis
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Hybrid-Phase Metal Oxide Thin-Film Transistors and their Applications

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Abstract

Metal-oxide (MO) semiconductors are expected to be one of the most promising candidates as thin-film transistor (TFT) channels. With the advancement of next-generation flat panel display technologies, technical standards of MO TFTs in active-matrix display backplanes are becoming increasingly higher. This thesis focuses on material modification and device processing to further improve the performance of MO TFTs.

Initially, a new type of hybrid-phase ITZO (hp-ITZO) thin films is proposed as TFT channels by modifying not only the element composition but also the crystal morphology. The thin films own a boosted electron Hall mobility of >30 cm^2/Vs, which is verified to surpass both the measured result and calculated upper mobility limit of their counterparts in the amorphous phase. Additionally, they also exhibit many other merits such as suppressed sub-gap states, smooth surface, wide band gap, etc. These are prerequisites to achieve high-performance and reliable MO TFTs.

Next, the feasibility as TFT channels is further confirmed by examining TFTs with a bottom-gate top-contact (BG-TC) architecture. By tuning the oxygen partial pressure and direct-current power during co-sputtering, optimal deposition conditions for the channels with reasonable electrical properties are obtained. The devices without passivation can exhibit high electrical performance, excellent spatial uniformity and long shelf-life. Even though their source/drain (S/D) electrodes are then patterned using a wet etch instead of a lift-off technique to fulfill industrial requirements, the resulted back-channel-etched (BCE) TFTs can still be fabricated successfully

via extra over-etch ratio control and prior thermal annealing treatment.

Afterwards, related top-gate TFTs are implemented as building blocks for practical applications. To deposit high-quality gate insulators (GIs), we develop a type of SiO_2 stacks containing a silane-sourced PECVD SiO_2 (SiH_4-SiO_2) layer with a tetraethyl-orthosilicate-sourced PECVD SiO_2 (TEOS-SiO_2) layer underneath. The stacks exhibit strengthened electrical quality compared with their single-layer counterparts, and fabricated top-gate bottom-contact (TG-BC) TFTs are shown to be free of hysteresis with lower off-state current and steeper subthreshold swing thanks to GI engineering. To operate high-mobility MO TFTs in enhancement mode, gate electrode (GE) engineering is introduced by replacing metallic aluminum GEs with conductive indium-tin oxide GEs. Together with the work function, GE permeability for hydrogen diffusion out of and oxygen diffusion into MO channels during post-annealing is also involved to modulate the threshold voltage of devices without degradation. Moreover, by delicately employing two different PECVD SiO_2 layers together with differentiated oxygen annealing strategies, we can further realize top-gate self-aligned (TG-SA) TFTs with good electrical characteristics as well as robust stability against gate-bias stress and thermal processing. This relies on a unique property of the hp-ITZO thin films. The S/D regions capped by the SiH_4-SiO_2 can maintain a low-resistivity state after a long-duration oxygen annealing, whereas the channel regions capped by the TEOS-SiO_2 will return to a high-resistivity state. Thus, it can save not only one photolithography step for S/D electrode patterning but also extra processes for conductive S/D region formation, leading to more cost-effective manufacturing.

Finally, a 2.2-inch monochromatic active-matrix organic-light-emitting-diode display panel using the hp-ITZO TFT technology is demonstrated from layout design, through backplane processing, to system testing. In addition, some of integrated circuits for fully transparent electronics are also implemented with preliminary but promising results.

Chapter 1 Introduction

1.1 Flat Panel Display Technology

1.1.1 Industry Overview

In today's information-driven society, visual display is an effective and powerful approach to convey complex information, and electronic displays have been a major focus of the electronics industry for the last half century [1, 2]. The common embodiments of electronic displays range from small- or medium-size mobile phones, tablets, laptops, monitors, and augmented reality/virtual reality (AR/VR) apparatus to large-area televisions, advertising boards, and signage systems. Compared with obsolete cathode-ray tube (CRT) technology, flat panel display (FPD) technology holds many advantages, such as thinner thickness, lighter weight, smaller volume and lower power consumption. Therefore, it occupies the dominant position among electronic displays for human-machine interactions. As shown in Fig. 1-1 [3], the worldwide FPD market boomed from the year 2002, and has stepped into its mature stage, with a global annual demand of over US$100 billion since 2007. With the anticipated development of flexible and transparent displays, the FPD industry is expected to enjoy a new round of rapid growth in the near future.

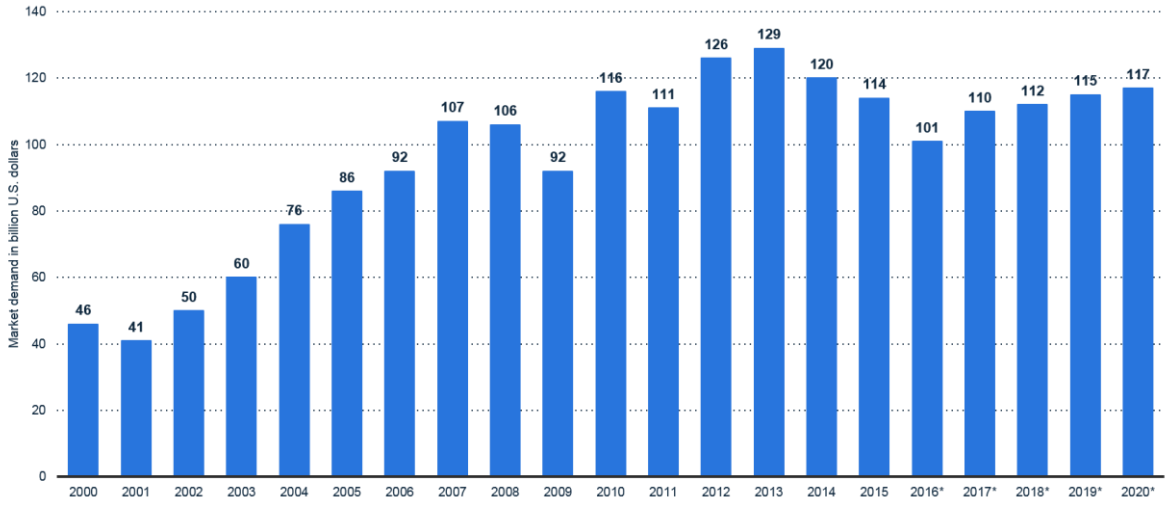

Figure 1-1: Global market demand for FPDs from 2000 to 2020 (in billion U.S. dollars).

1.1.2 Technology Classification

According to the signal addressing scheme, FPD technology can be classified as direct addressing, passive-matrix (PM) addressing and active-matrix (AM) addressing [4].

In direct addressing displays, there is no matrix formed. Each display segment in the

backplanes shares a common electrode, and also has a patterned segment electrode to directly control whether light emission is needed or not (Fig. 1-2(a)). This kind of FPD technology is generally adopted in low-resolution and inexpensive applications like timers and calculators.

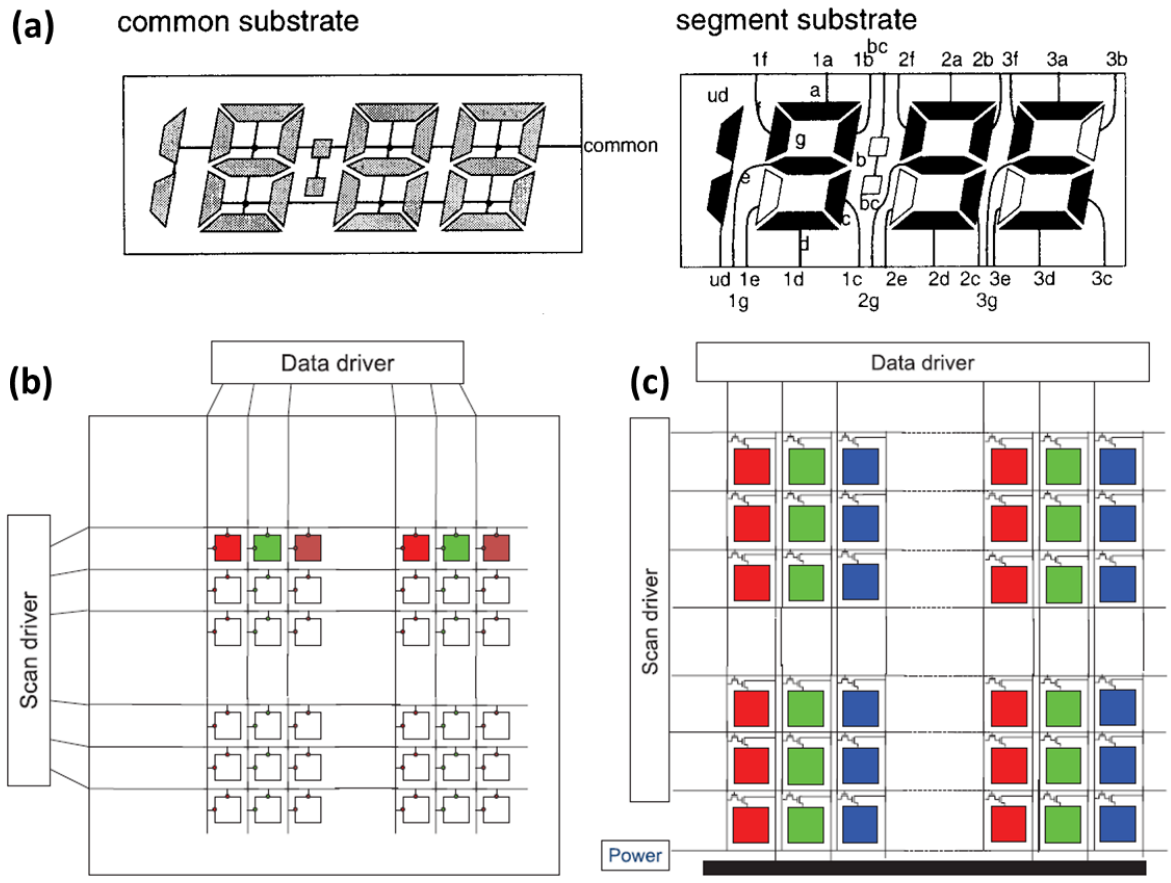

Figure 1-2: Schematic diagrams of (a) direct addressing FPDs, (b) PM-FPDs, and (c) AM-FPDs [4].

In PM addressing FPDs (PM-FPDs), each pixel is sandwiched between vertically oriented data lines and horizontally oriented scan lines, as shown in Fig. 1-2(b). These pixels are selected by a row-column scheme. When electric signals are input along the data and scan lines, only the pixels at their intersections can be addressed. Due to a lack of thin-film transistors (TFTs) and storage capacitors (C_s) in pixel circuits, the selected pixel is incapable of holding its state after signal removal. Considering the brightness averaging effect within the whole frame period, it is required to adopt a higher scanning frequency and boosted lighting intensity, resulting in increased power consumption due to ohmic loss. In addition, the crosstalk issue caused by unintended charging/discharging of neighboring pixels is also very severe in the PM-FPDs. Therefore, their applications are always limited to low-end displays.

In AM addressing FPDs (AM-FPDs), extra circuits apart from the data and scan lines are introduced in the pixels, as shown in Fig. 1-2(c). The circuit is originally composed of transistors and capacitors to control each pixel independently. The storage capacitors, with low leakage, are able to hold the voltage across pixels until they are refreshed in the following frame. Then, the selected pixels can maintain their states for the entire frame period. Since the pixels are isolated from each other once their switching TFTs are turned off, there is no serious crosstalk issue either. The AM addressing scheme can overcome the major drawbacks of PM-FPDs, and it has been widely used in high-quality and low-cost FPDs.

1.1.3 Mainstream Active-Matrix Flat Panel Displays

Nowadays, mainstream AM-FPDs employ either active-matrix liquid-crystal display (AMLCD) technology or active-matrix organic light-emitting diode (AMOLED) technology. Regardless of technology type, a full-color AM-FPD panel generally consists of millions of pixels, each of which should be further divided into three addressable subpixels. They are individually responsible for red (R), green (G) and blue (B) color primaries. Then, the color gamut of the panel will be determined by the formed triangle, which is anchored by the RGB primaries in color space [4]. However, the colors emitted from the pixels at a certain frame period are actually dependent on the input electric signals, the execution of which requires precise addressing and driving using TFT-based pixel circuits (Fig. 1-3).

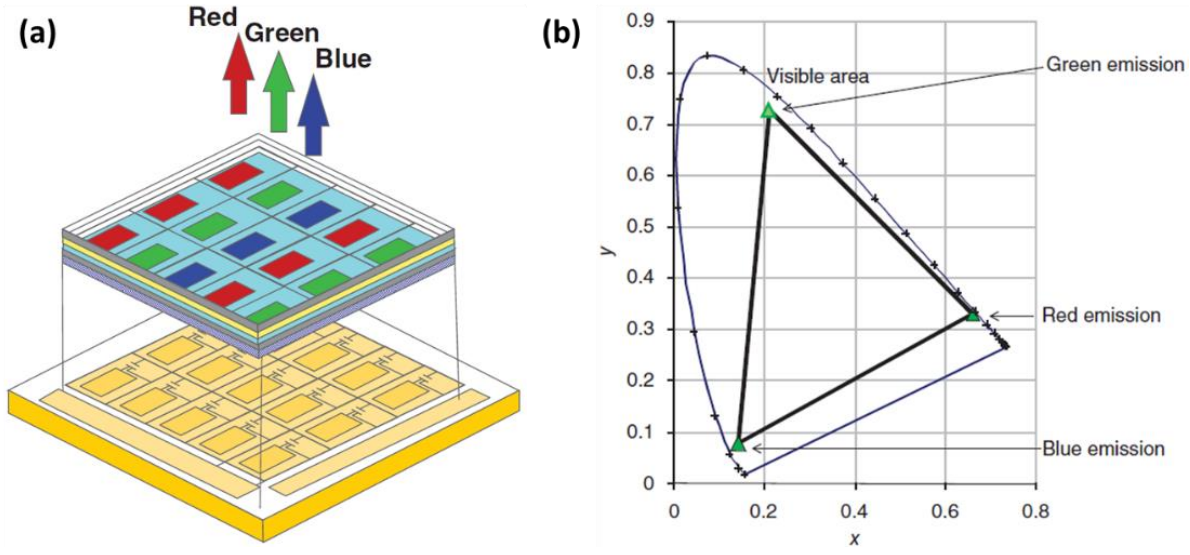

Figure 1-3: Illustration of (a) RGB subpixels and (b) a color triangle of a full-color AM-FPD panel in CIE 1931 color space for determining color gamut.

Since the dynamic scattering effect of liquid crystals (LCs) was first reported in 1968, liquid-crystal displays (LCDs) have been thought of as a promising successor to CRT

technology [5]. In the early 1990s, owing to significant demand growth of the personal computer (PC) market, the research and development (R&D) of amorphous-silicon (a-Si) TFT-LCDs was accelerated, and later this technology successfully stepped into its mass production stage. During the last twenty years, AMLCDs have clearly dominated the AM-FPD market. In an AMLCD panel, as shown in Fig. 1-4(a), an LC layer is sandwiched by two glass substrates that are coated with transparent electrodes. The voltage-driven LC shutter can act as an optical modulator, and it bridges optical transmittance and applied voltage (or electric field intensity) across the pixels. Fig. 1-4(b) shows the typical pixel circuit with one TFT and one C_s (1T1C) in AMLCD backplanes. The switching TFT in each pixel can be addressed precisely and managed independently via the scan and data lines. When this TFT is turned on, its corresponding C_s will be charged immediately, while components in other pixels will not be affected at all. Once the switching TFT is turned off, the charged C_s will then be isolated from its data line. Since the C_s and liquid crystal capacitor (C_{LC}) are connected in parallel, the voltage across C_s with grayscale information will be equally applied to the LC layer, and will be held for the whole frame period until the next refresh cycle. Then, output light beams that transmit through the RGB subpixels individually will mix together to present the colors as designed. Thus, it is clearly seen that TFTs as pixel switches are essential in the implementation of AMLCD panels.

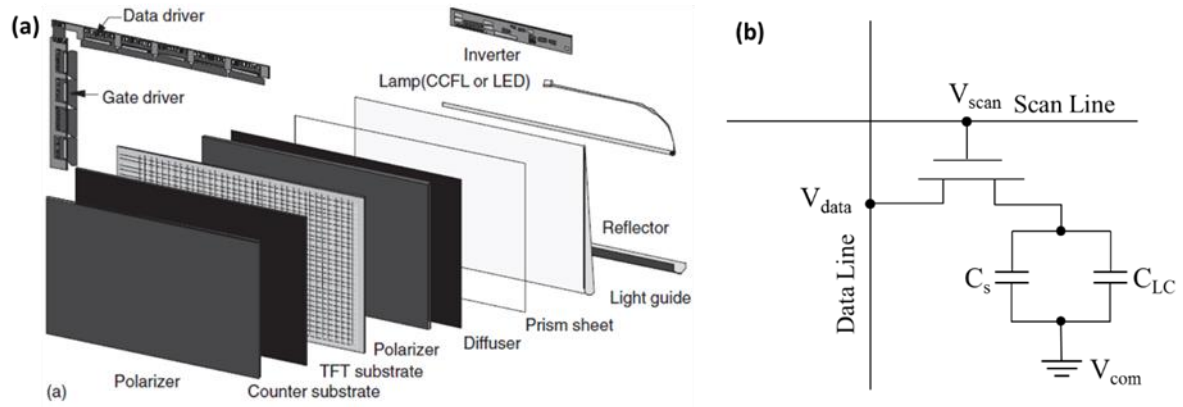

Figure 1-4: (a) Example of system components and (b) a typical 1T1C pixel circuit diagram in the AMLCD backplanes.

These days, AMOLED technology has drawn intensive attention as a very promising candidate for next-generation FPDs. It is a self-emitting display technology with fewer components, and the light beams can be directly emitted from OLED devices that are fabricated on the top of TFT backplanes (Fig. 1-5(a)). Compared with AMLCDs, AMOLED technology is endowed with many advantages such as a wider color gamut, higher contrast ratio, shorter

response time, wider viewing angle, lower power consumptions, etc. Meanwhile, it also eliminates the cell gap dilemma in the AMLCD panels and underlies the feasibility of flexible displays. Since OLEDs are driven by their inputted current, there should be at least two TFTs and one C_s (2T1C) in each pixel of the AMOLED backplanes (Fig. 1-5(b)). Among them, two TFTs herein serve not only as a switch but also as a current supplier. The driving TFT is required to provide a sufficiently high and relatively stable driving current to light the OLED device for the whole frame period. However, due to device reliability issues, the threshold voltage of TFTs often shifts, resulting in non-uniform luminescence across the AMOLED panels. Thus, extra TFTs and capacitors (such as 4T2C, 5T2C, etc.) are always employed in commercial AMOLED products in order to build more complicated circuits for brightness compensation. Thus, TFTs are thought to be one of compulsory elements in the AMOLED panels as well.

Above all, the studies on TFTs are of high value because they are essentially associated with the benign and sustainable development of the FPD industry.

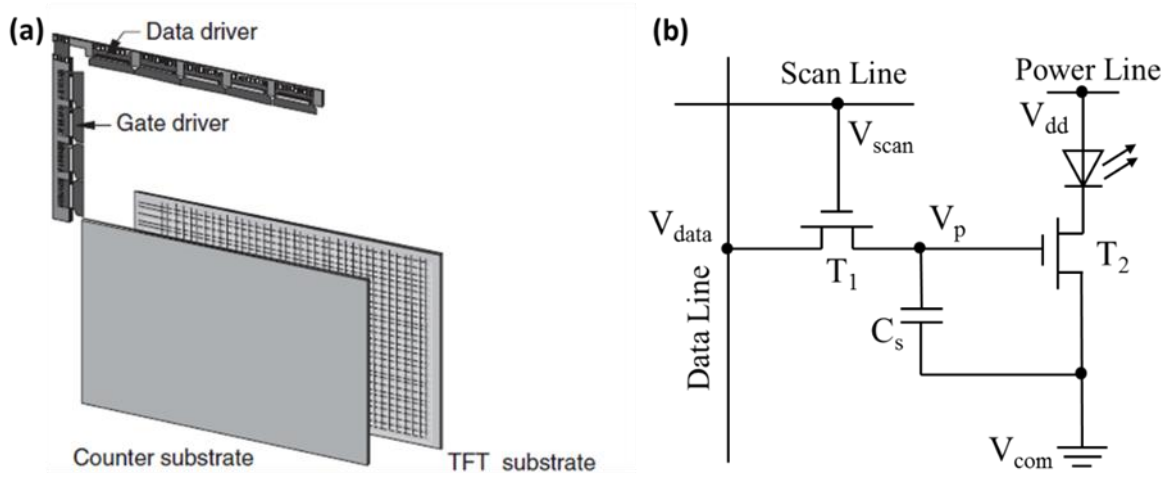

Figure 1-5: (a) Example of system components and (b) a typical 2T1C pixel circuit diagram in the AMOLED backplanes.

1.2 Thin-Film Transistor Technology

1.2.1 History and Classification

Since the field effect phenomenon was discovered in the 1930s and the first CdS TFT was demonstrated in the 1960s, TFT technology has been developing for more than half a century, and the milestones during its evolution are summarized in Fig. 1-6. So far, there are four common technology embodiments, which are hydrogenated amorphous silicon (a-Si:H) TFTs, low-temperature polysilicon (LTPS) TFTs, metal oxide (MO) TFTs and organic TFTs. The

classification strategy is primarily based on the material attributes and processing techniques of channel layers. Each technology has its own pros and cons, and their overall comparisons are presented in Table 1-1 [6, 7].

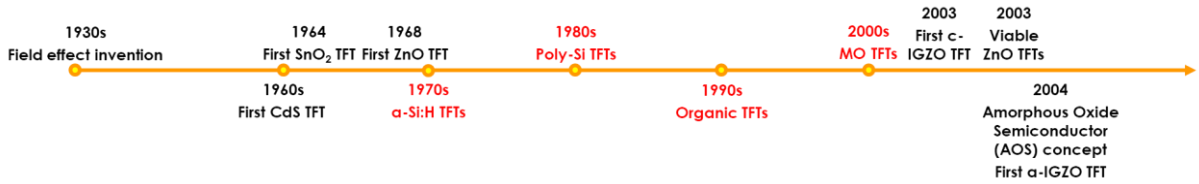

Figure 1-6: Milestones in TFT technology history.

Although traditional a-Si:H TFT technology exhibits insufficient mobility, a large leakage current and poor stability, it is still widely used in the current FPD industry owing to its low manufacturing cost and high yield after long-term development and investments. LTPS TFTs can upgrade device performance and reliability, which is particularly beneficial for current-driven OLED devices, so they have become prevalent in recent years. However, the luminescence non-uniformity issue as a result of grain boundaries limits their promotion to large-scale AMOLED panels. Compared with their inorganic competitors, organic TFT technology is more popularly used to achieve flexible displays. Unfortunately, its ambient reliability needs to be further improved in the future. As another emerging solution nowadays, the MO TFT owns many merits such as reasonable electrical properties, high transparency in the visible light band, low-temperature and low-cost manufacturing, etc. Therein, amorphous indium gallium zinc oxide (a-IGZO) is one of the most popular channel materials [6-10]. Compared with the conventional a-Si:H TFTs, the superiorities of a-IGZO TFTs mainly lie in its relatively high mobility (5-10 cm^2/Vs) and extremely low off-state current ($<10^{-13}$ A). These properties are necessary in high-definition and low-power-consumption applications, especially for small- or medium-size mobile devices. Although LTPS TFT technology can provide higher mobility, its spatial non-uniformity of electrical performance hinders its infiltration in the large-area FPD market [11, 12]. In contrast, MO TFTs can be adopted by AM-FPD products with a wider backplane size range, and they are well compatible with the production line even beyond Gen 8. These advantages ensure a bright future for MO TFT technology, particularly in the transparent and flexible displays, but the demands for strengthened reliability (though they perform more robustly than organic TFTs) and boosted electrical properties need to be fulfilled first.

Table 1-1: Overall comparison of a-Si:H, LTPS, MO and organic TFTs

TFT Type	a-Si:H	LTPS	MO	Organic
Polarity	NMOS	CMOS	NMOS	PMOS
Process temperature (ºC)	~250	250~550	RT~350	RT~100
Mobility (cm^2/Vs)	0.5~1	50~100	1~30 (target: ~100)	0.5~5 (target: 10~20)
Subthreshold slope (V/dec) (variation)	0.4~0.5 (~0.2)	0.2~0.3 (~0.1)	0.1~0.3 (~0.02)	0.1~1 (0.01~0.2)
Leakage current (A)	$\sim 10^{-12}$	$\sim 10^{-11}$	$< 10^{-13}$	$\sim 10^{-12}$
Reliability (threshold voltage shift for 10^5 hours)	Poor (> 5 V)	Good (< 0.5 V)	Fair (< 1 V)	Poor (no data)
Threshold voltage uniformity	Fair (0.5 V @ G4.5)	Poor (~1 V @G4.5)	Good (~0.2 V @G4.5)	Good (no data)
Flexibility (bending radius)	Poor (no data)	Poor (> 4 mm)	Fair (< 1 mm)	Good (<< 1 mm)
Transparency	Low	Low	High	Low
Printability	Poor	Poor	Fair	Good
Mask counts	4~5	5~11	4~7	4~5
Cost/Yield	Low/High	High/Medium	Low/Medium	Low/High

1.2.2 Device Structures

Theoretically, a TFT is a three-terminal field-effect transistor (FET). It consists of a gate electrode (GE), gate insulator (GI), active channel (AC) and source/drain (S/D) electrode compulsorily, and also normally contains an interlayer dielectric (ILD), passivation (PV) layer, etc. As a field-effect device, its gate can manipulate the capacitive injection of carriers near the GI/AC interface. Then, channel resistivity and hence current flow between the S/D electrodes can be modulated indirectly. As a part of large-area electronics, TFTs share similar design tools and layouts with metal-oxide-semiconductor field-effect transistors (MOSFETs). However, as shown in Fig. 1-7 [6], there still exist several intrinsic differences compared with the common MOSFETs that are used in high-performance applications such as microprocessors. First, the formation of interfacial conducting channels is realized by carrier accumulation in TFTs, whereas it relies on carrier inversion in MOSFETs. Thus, TFTs have no p-n junctions in their S/D regions like MOSFETs do. Second, TFTs are always fabricated on large-scale glass

substrates and require extra semiconductors as their channels, while MOSFETs are directly implemented on silicon wafers by employing their own single-crystal silicon as channels. Thus, TFTs outweigh MOSFETs in terms of substrate scalability and manufacturing cost. Though the overall electrical characteristics of TFTs are inferior, they are capable of being used in the application of FPDs. Third, MOSFETs need to be processed with a temperature of over 1000 °C, which exceeds the melting point of glass substrates. This is not applicable for TFT fabrication.

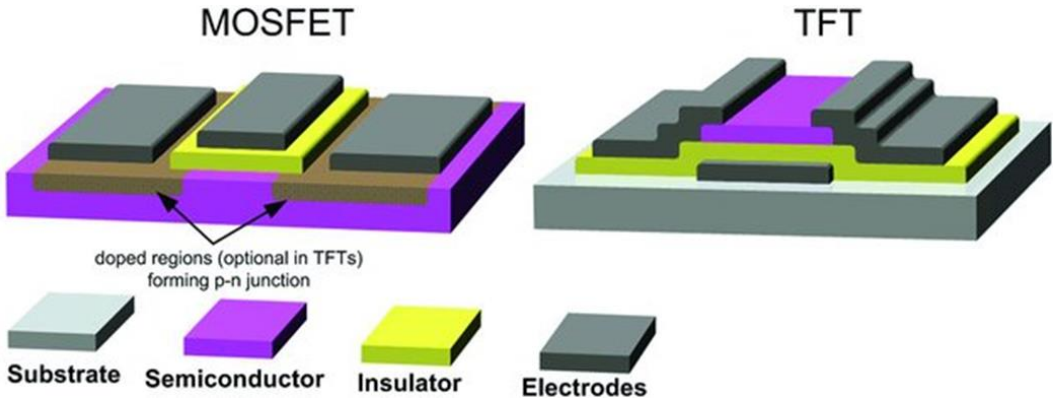

Figure 1-7: Schematic comparison between a MOSFET and a TFT.

In general, a TFT structure can be mainly defined as staggered or coplanar, referring to Weimer's definition [13]. Moreover, according to the stacking sequence, they can be further divided into a normal architecture or inverted architecture, as shown in Fig. 1-8.

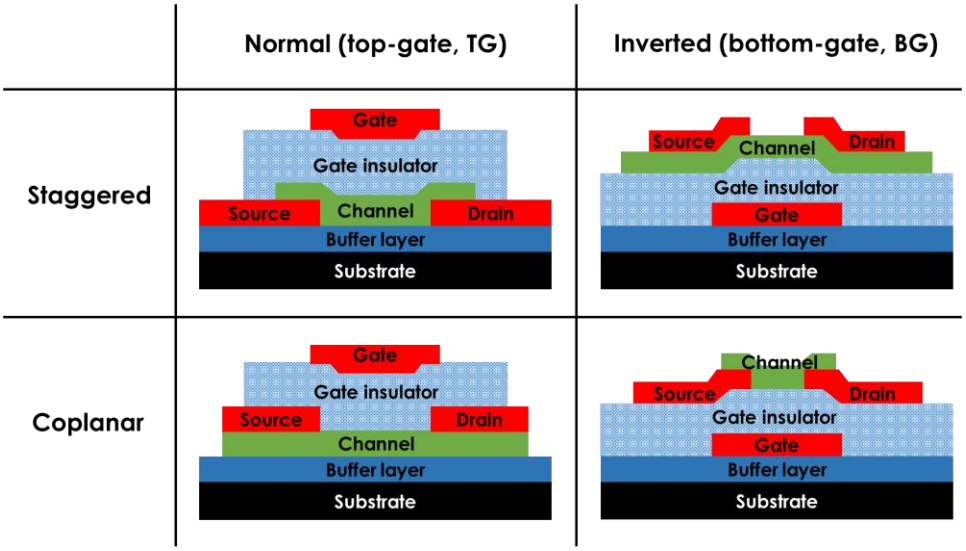

Figure 1-8: Schematic diagrams of main TFT structures.

The inverted staggered structure can be also named as a bottom-gate top-contact (BG-TC) structure, which is popularly used in a-Si:H TFTs due to their easier processing and less degraded electrical performance. Since the a-Si:H channel is light sensitive, its underlying

metallic gate can act as a light shielding layer and prevent the channel layer from backlight exposure. Considering the better process compatibility, the BG-TC configuration was also adopted by MO TFTs in their early-stage AM-FPD products. As shown in Fig. 1-9(a) and (b) [14], such a structure can be further divided into back-channel-etched (BCE) type and etch-stopper (ES) type. In the ES MO devices, an extra etch-stop layer is inserted on the top of the channel layer before S/D deposition, then the back-channel surface will be isolated from the following S/D electrode patterning process. In contrast, BCE TFT technology eliminates the etch-stop layer. This can intrinsically reduce photolithography mask counts for more cost-effective manufacturing. Meanwhile, it also miniaturizes parasitic capacitance and device footprint for the FPDs with higher definitions [14, 15]. Fig. 1-10(a) and (b) shows the layout of the ES TFT and the BCE TFT, respectively, in the 1T1C pixel circuit for AMLCD panels. Herein, the design rule is defined as 2 μm. Then, the minimum allowed channel length for the ES MO TFT should be 6 μm if a safe alignment margin is taken into consideration, whereas the result is only 2 μm for the BCE MO TFT. In order to maintain an equivalent driving current, the ratio of the channel width over the channel length should remain the same. Therefore, the BCE MO TFT will occupy a smaller area, and the AMLCD panel will own a higher aperture ratio (AR) at the same time. However, the BCE MO TFT also has some drawbacks. For example, its S/D electrode patterning is not perfect at present because most of etch processes will introduce residues or cause damage to the channels, giving rise to performance degradation and instability issues.

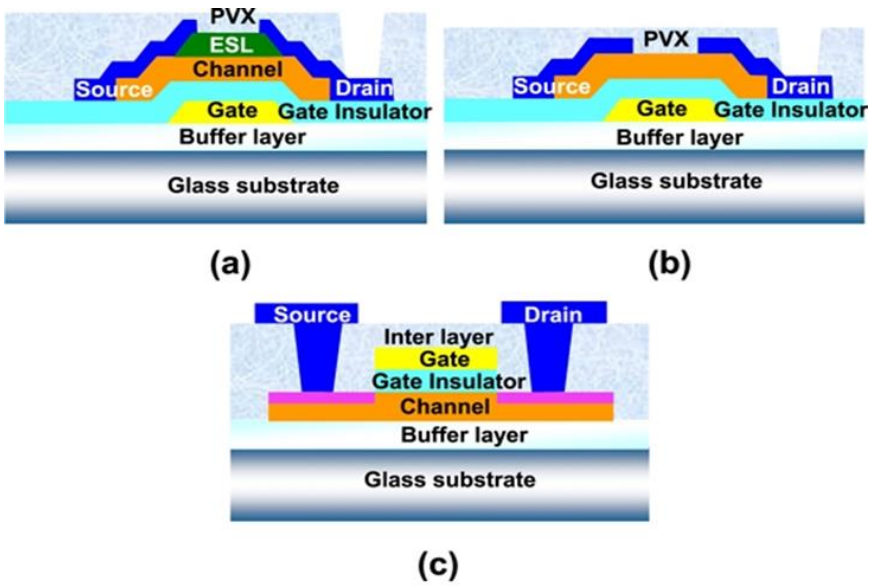

Figure 1-9: Schematic diagrams of (a) an ES-type BG-TC, (b) BCE-type BG-TC and (c) TG-SA MO TFT.

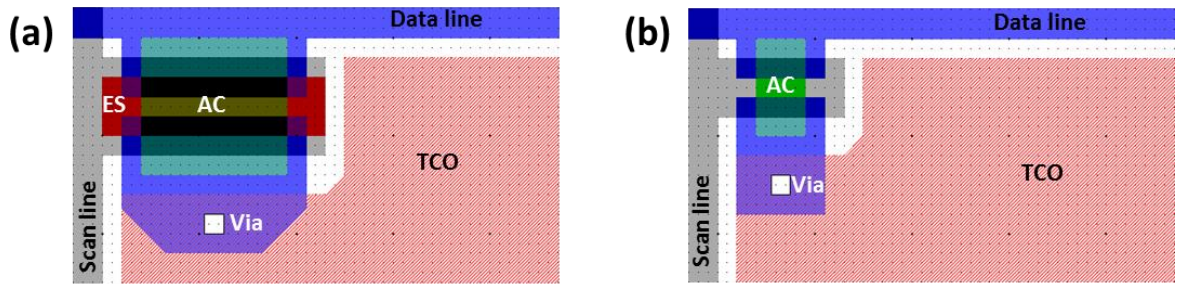

Figure 1-10: Layouts of (a) an ES-type BG-TC TFT and (b) a BCE-type BG-TC or TG-SA MO TFT in a 1T1C pixel circuit for AMLCD panels.

The normal coplanar structure is often founded in LTPS TFTs, where their channel layers are deposited first. This is because the crystallization of polysilicon channels involves high-temperature or laser annealing treatments, which may have negative impacts on other existing layers. In addition, by employing their gates as hard masks and heavily doping the exposed polysilicon regions, a special type of top-gate (TG) TFT can be achieved with self-aligned (SA) conductive S/D regions, as shown in Fig. 1-9(c). The TG-SA devices can exhibit advantages from at least three aspects. Firstly, the underlying substrates and the upper gate insulators can act as *in-situ* protection layers for the sandwiched channel. Secondly, an extra photolithography step for the S/D electrode patterning is no longer required, enabling more cost-effective manufacturing. Finally, the parasitic capacitance between the gate electrodes and the S/D electrodes can be eliminated. This provides strong device scalability. Meanwhile, it is also helpful to increase the operation speed and reduce signal RC delay TFT-based circuits. Additionally, the luminescence non-uniformity issue, especially in the AMOLED panels, can be eliminated by suppressing the pixel voltage shift (ΔV_p, also called kickback/feedthrough voltage).

According to Fig. 1-11, ΔV_p is originally induced by the gate-to-drain parasitic capacitor (C_{gd}) in the switching TFT. When the scan signal converts from high level (V_{scan_H}) to low level (V_{scan_L}), the pixel voltage (V_p) across C_s will suffer a potential variation due to capacitive coupling, and the value of ΔV_p in the AMLCDs and in the AMOLEDs are accordingly equal to

$$\Delta V_p = \frac{C_{gd}\Delta V_{scan} + C_{sd}\Delta V_{data}}{C_{gd} + C_s + C_{LC} + C_{sd}} \cong \frac{C_{gd}\Delta V_{scan}}{C_{gd} + C_s + C_{LC} + C_{sd}}, \tag{1-1}$$

$$\Delta V_p = \frac{C_{gd1}\Delta V_{scan} + C_{sd1}\Delta V_{data} + C_{gs2}\Delta V_{OLED}}{C_{gd1} + C_{sd1} + C_s + C_{gs2} + C_{gd2}} \cong \frac{C_{gd1}\Delta V_{scan} + C_{gs2}\Delta V_{OLED}}{C_{gd1} + C_{sd1} + C_s + C_{gs2} + C_{gd2}}, \tag{1-2}$$

where ΔV_{scan} is the voltage difference of the scan signal at high and low electric levels. It is noted that ΔV_p will be affected by ΔV_{scan} together with C_{gd}. However, if C_{gd} is missing, ΔV_p on the LC cell or the current through the OLED device will become neglectable. Therefore, the TG-SA architecture is of high value and necessity, but its implementation in the MO TFTs is not as easy as expected. The difficulties lie in many aspects, such as formation of the conductive and thermally stable S/D regions, growth of high-quality gate insulators, threshold voltage control for enhancement-mode devices, etc. More efforts are required to deal with these issues.

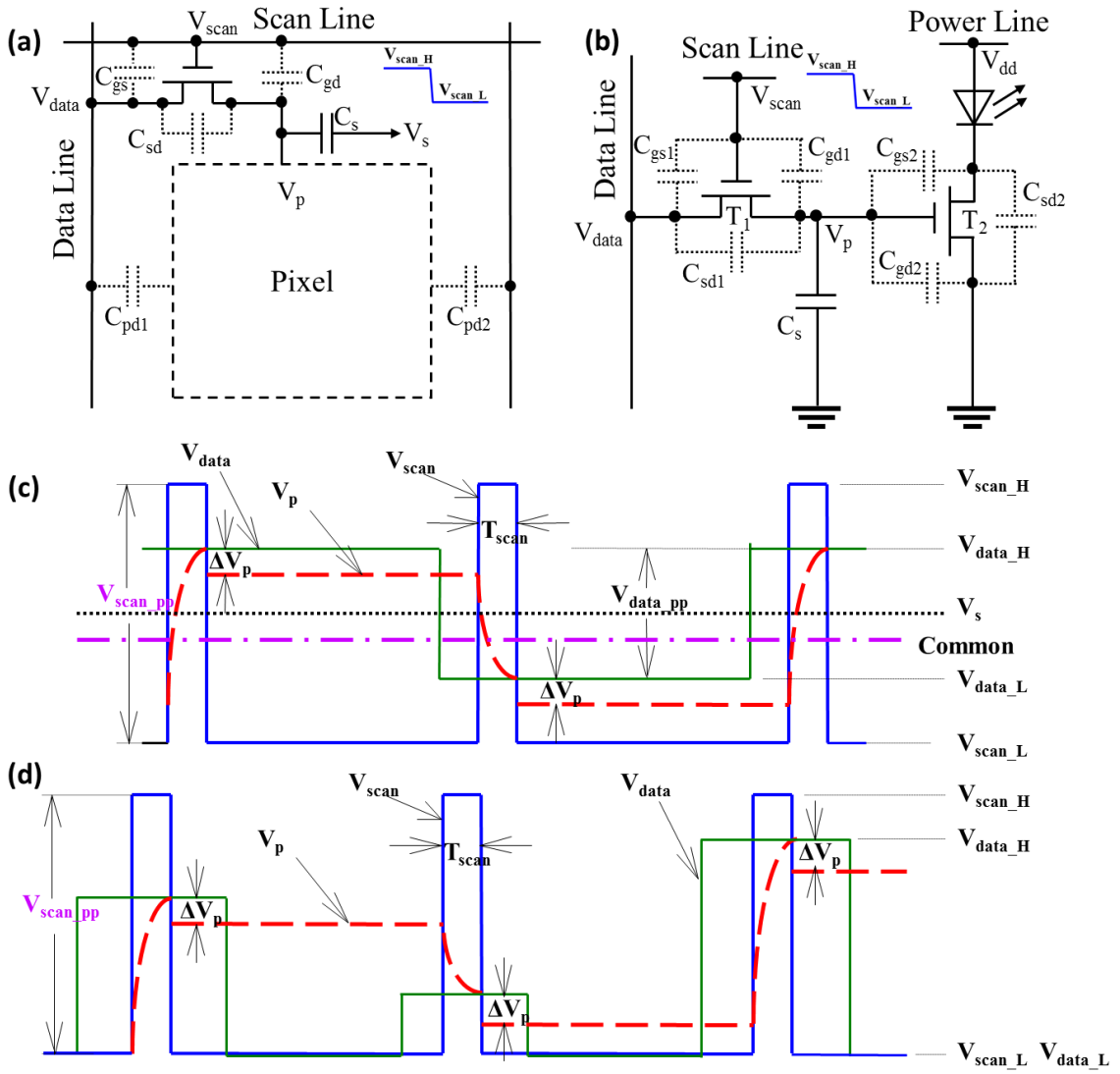

Figure 1-11: (a) a 1T1C pixel circuit diagram in an AMLCD, and (b) a 2T1C pixel circuit diagram in an AMOLED with parasitic capacitor labels. Signal waveforms with kickback/feedthrough voltage information in (c) an AMLCD and (d) an AMOLED.

Ahead of implementing the TG-SA devices, top-gate bottom-gate (TG-BC) TFTs with real S/D electrode entities (i.e., the normal staggered TFTs) are always fabricated as model devices

to investigate the impacts of the other layers except the S/D regions. The obtained results are valuable not only for the TG-SA MO TFTs but also for the TG-BC TFTs themselves. In terms of mask count and device footprint, the TG-BC devices are in fact comparable to their BCE-type BG-TC counterparts (Fig 1-10(b)). Meanwhile, the top-gate structure is more appropriate for circuit layout design. Therefore, developing the TG-BC MO TFTs is very necessary as well.

1.2.3 Key Static Parameters

The static electrical performance of TFTs can be evaluated by several parameters including field-effect mobility (μ), threshold voltage (V_{th}), subthreshold swing (SS) and on-off ratio. They can be extracted from the output (I_{ds}-V_{ds}) and transfer (I_{ds}-V_{gs}) characteristics of TFTs, as shown in Fig. 1-12.

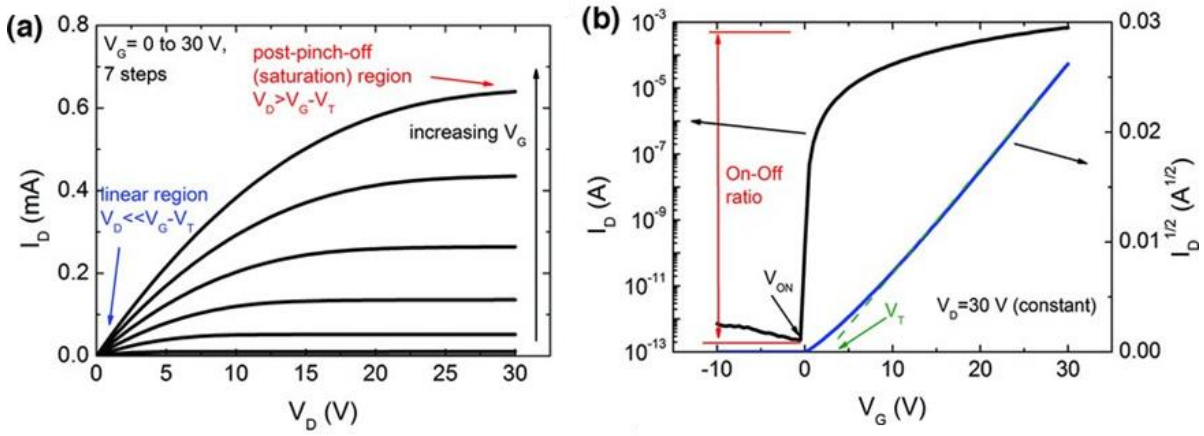

Figure 1-12: Typical (a) output and (b) transfer curves of n-type TFTs [6].

Mobility (μ) is one of key parameters to describe carrier transport in TFTs. It can directly determine drain current (I_{ds}) and transit time (t_{sd}) (or operation frequency) of devices. In theory, these two parameters can be accordingly expressed as

$$I_{ds}=\begin{cases}0,\ \text{for } V_{gs}-V_{th}<0<V_{ds}\ \text{(cutoff region)}\\ \dfrac{W}{L}\mu_{fe}C_{ox}\left[(V_{gs}-V_{th}-\dfrac{1}{2}V_{ds})V_{ds}\right],\ \text{for } V_{gs}-V_{th}>V_{ds}\ \text{(linear region)},\\ \dfrac{1}{2}\dfrac{W}{L}\mu_{sat}C_{ox}(V_{gs}-V_{th})^2,\ \text{for } V_{gs}-V_{th}<V_{ds}\ \text{(saturation region)}\end{cases} \quad (1\text{-}3)$$

and

$$t_{sd}=\frac{L^2}{\mu V_{ds}}, \quad (1\text{-}4)$$

where W, L, and C_{ox} is the channel width, channel length, and gate insulator capacitance per unit area, respectively. In the linear region, μ is specifically defined as the linear field-effect mobility (μ_{fe}), which can be obtained from the TFT transconductance (g_m) and expressed as

$$\mu_{fe} = \frac{g_m}{C_{ox}\frac{W}{L}V_{ds}}. \tag{1-5}$$

In the saturation region, μ can be further represented by the saturation mobility (μ_{sat}), which can be derived from the following equation:

$$\mu_{sat} = \frac{(\frac{d\sqrt{I_{ds}}}{dV_{gs}})^2}{\frac{1}{2}\frac{W}{L}C_{ox}}. \tag{1-6}$$

Theoretically, V_{th} corresponds to the gate bias (V_{gs}) for which a conductive source-to-drain channel is formed at the GI/AC interface by carrier accumulation. In practice, there are many different methods to extract V_{th}. For example, V_{th} can be determined by extrapolating a straight line in the I_{ds}-V_{gs} plot at a low V_{ds} (the linear region) or in the $(I_{ds})^{1/2}$-V_{gs} plot at a high V_{ds} (the saturation region). For simplicity, sometimes it is defined as the V_{gs} corresponding to a specific I_{ds} (e.g., $\frac{W}{L}\times10^{-8}$ A). V_{th} is an essential indicator of device operation mode. For n-type TFTs, enhancement- and depletion-mode devices own a positive V_{th} and negative V_{th}, respectively. Apart from V_{th}, turn-on voltage (V_{on}) is also commonly used. When V_{gs} is equal to V_{on}, TFTs are fully turned off and I_{ds} starts to increase in a log I_{ds}-V_{gs} plot. V_{th} is not the same as V_{on}, but their difference is not very large in the MO TFTs thanks to their steep SS.

SS is related to the amount of V_{gs} change required to increase I_{ds} by a decade. Its definition expression is shown below.

$$SS = \left(\frac{d\log(I_{ds})}{dV_{gs}}\right|_{max})^{-1}. \tag{1-7}$$

Since the relationship between I_{ds} and V_{gs} in the subthreshold region can be expressed as

$$I_{ds} = I_{ref}\exp[\frac{q(V_{gs}-V_{th})}{nk_BT}], \tag{1-8}$$

$$n = 1+\frac{C_d + C_{it}}{C_{ox}}, \tag{1-9}$$

where I_{ref}, n, q, k_B, T, C_d, C_{it} and C_{ox} is the effective subthreshold reference current at V_{th}, idealy factor, electron charge, Boltzmann's constant, absolute temperature, depletion capacitance, interfacial trap capacitance and gate insulator capacitance, respectively. Then, SS can be further expressed as

$$SS = \ln(10)\frac{k_B T}{q}\left(1+\frac{C_d + C_{it}}{C_{ox}}\right) = 2.3\frac{k_B T}{q}\left(1+\frac{C_d + C_{it}}{C_{ox}}\right). \quad (1\text{-}10)$$

It means that SS is an indicator of the total trap density in the channel bulk and at the GI/AC interface. For classical TFTs, there exists a fundamental lower limit for the value of SS, which is ($2.3k_BT$) mV/decade or ~60 mV/decade at room temperature (300 K). This is famous for the Boltzmann tyranny [16].

On-off ratio refers to the ratio of on-state I_{ds} over off-state I_{ds}. The on-state I_{ds} is decided by many aspects like channel materials, device dimensions, etc. The off-state I_{ds} is primarily limited by the dark current of channels, gate leakage current, or even noise level of the measurement systems. As eligible pixel switches in the AMLCD panels, the on-off ratio of TFTs should be no less than 5×10^5.

1.3 Metal Oxide Thin Film Transistors

1.3.1 From Binary to Multicomponent Metal Oxide Semiconductors

Owing to merits such as low manufacturing cost and temperature, excellent optical transparency, and reasonable electrical properties, MO TFT technology has drawn great attention in recent years, and some manufacturers have already introduced it to their released AM-FPD products. In fact, the history of the study of MO TFTs is not short, with half a century passing since the first report on single crystalline ZnO TFTs in 1968 [17], but rapid development of this technology only took place after the proposal of a-IGZO and other amorphous oxide semiconductor (AOS) materials in 2004 [9].

At the early stage, most research work focused on binary MO semiconductors. Among them, ZnO was intensively investigated for its unique properties and versatile applications in transparent electronics, ultraviolet (UV) detectors, piezoelectric devices, chemical sensors, etc. Theoretically, wurtzite ZnO is a type of semiconductor with a wide and direct band gap (E_g=3.4 eV at 300 K), so it is highly transparent in the visible light band. Meanwhile, it was found that the intrinsic electrical properties of ZnO are at a medium level. For example, the ideal electron Hall mobility (μ_{hall}) in single crystalline ZnO can reach as high as 200 cm^2/Vs, while its intrinsic carrier concentration is less than 10^6 cm^{-3} [18]. Additionally, zinc is quite abundant in

the earth's upper continental crust, leading to an extremely cheap raw material price. This is beneficial for low-cost electronics. Therefore, the implementation of ZnO TFTs was always highly expected.

After a long incubation period, remarkable progress was indeed made in 2003. Hoffman *et al.* [19], Masuda *et al.* [20], and Carcia *et al.* [21] individually reported their own well-performing ZnO TFTs. Notably, the ZnO channel layer in Carcia's work was deposited using a radio-frequency magnetron sputtering technique at room temperature, and the following processes were also free of high temperature. This was valuable for the development and promotion of ZnO TFTs. Afterwards, research in the field of MO TFTs became attractive once again. Only one year later, fully transparent ZnO TFTs with room-temperature processes were demonstrated by Fortunato *et al.* [22], and their mobility could reach near 20 cm^2/Vs.

Despite many advantages, ZnO TFTs also have many inevitable drawbacks that hinder their further development. Firstly, there are many native point defects such as oxygen vacancies (V_o) and zinc interstitials (I_{Zn}) in the ZnO channels, as shown in Fig. 1-13(a). They will release free electrons and make the ZnO channels unintentionally n-type doped. If there is no effective control of native defects, it will be hard to switch off the devices with a low off-state current. Meanwhile, these native point defects, especially V_o, are usually associated with device instability. This is why there are no ZnO TFTs with excellent reliability so far. Secondly, the sputtered ZnO films are typically polycrystalline (pc) with a preferential grain growth along the *c*-axis, even on amorphous substrates (Fig. 1-13(b)). Like LTPS TFT technology, the high density of grain boundaries will deteriorate the device electrical uniformity and limit their large-size applications. Particularly, due to atomic disorder, many native defects will be generated at the grain boundaries. This will aggravate the degradation of the pc-ZnO TFTs in both electrical performance and reliability.

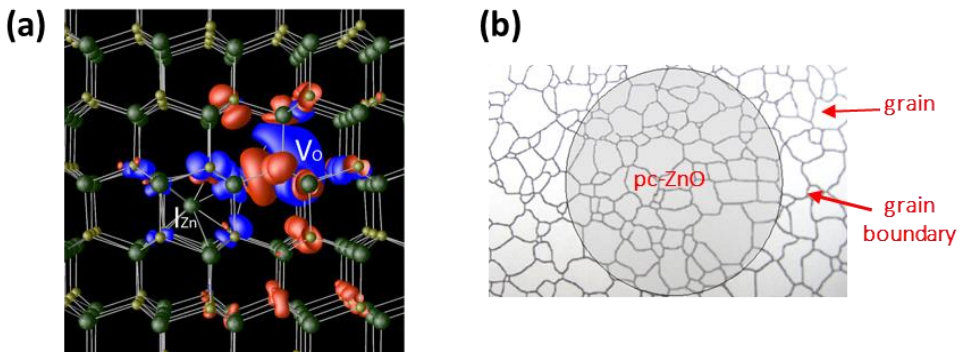

Figure 1-13: Illustration of (a) atomic arrangements and native defects, and (b) grain boundaries in pc-ZnO films.

The aforementioned drawbacks in the binary MO semiconductors can be addressed by their multicomponent variants to some extent. Since the proposal of a-IGZO by Hosono *et al.* in 2004 [9], it has drawn intensive attention and become the mainstream MO TFT technology. The related AOS concept is verified to be of extremely high value. To systhesise AOS materials, a common method is to include at least one type of post-transition-metal cation with an $(n-1)d^{10}ns^0$ ($n\geq4$) electronic configuration first [23]. For a-IGZO, this refers to indium cations, the sphere 5s orbital radius of which is as large as 180 pm [24]. Contrastively, the 4s orbital radius of zinc cations is only about 137 pm. The overlapped ns orbitals among post-transition-metal cations will then support the framework of electron conduction, and show less sensitivity to structural randomness, as shown in Fig. 1-14. Apart from the post-transition-metal cations, other types of cations with different ionic radii and oxygen coordinates need to be further incorperated. Then, the mixtures will exhibit a reduced degree of crystallization, and most can present the amorphous phase when deposited, even at room temperature.

The method above also provides more freedom to researchers in tailoring material properties. Regarding a-IGZO, it has been reported that the addition of gallium cations can not only help to amorphize, but also enlarge the material band gap and act as carrier stabilizers becasue Ga_2O_3 owns a wider band gap (~4 eV) [6] and a stronger metal-oxygen bond (~2 eV) [25] compared to In_2O_3 and ZnO. However, the modulation effect is limited in fact. The photo-stability of a-IGZO TFTs is not as good as expected [26], and their carrier concentration can be managed by other means [27]. Nevertheless, the prevalence of a-IGZO has initiated intensive studies on AOS materials, including, but not limit to a-IZO [28-30], a-ZTO [31-33], a-ITZO [34-36], a-HIZO [37-39], a-ATIZO [40-42], etc.

However, increasingly more researchers have failed to differentiate the group of AOS materials and the group of multicomponent MO semiconcutors. Herein, we would like to clarify that they are not identical concepts. One of the typical examples is c-axis-aligned crystalline indium-gallium-zinc oxide (CAAC-IGZO), which is quite different from a-IGZO, especially in their leakage current [43-45]. The CAAC-IGZO is a kind of multicomponent MO semiconcutor, but it does not belong to any AOS. Strictly speaking, the AOS materials should be a part of the multicomponent MO semiconductor family with an amorphous phase as a prerequisite.

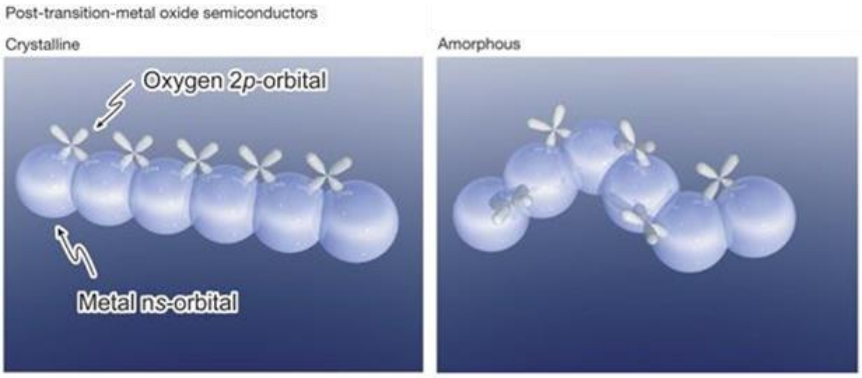

Figure 1-14: Schematic orbital drawing for carrier transport path in AOS materials composed of post-heavy-metal cations.

1.3.2 Demands for High Carrier Mobility

Compared with the popular LTPS TFT technology, MO TFT technology has electrical characteristics that, in many respects, are not inferior. They can easily escape from the electrical non-uniformity dilemma and achieve all-size FPD applications. With the advancement of next-generation FPD panels towards higher definitions, lower power consumption, narrow bezel and multifunctional ingetration, TFT backplanes are demanded to be equipped with increasingly higher switching/driving capabilities. Regardless of parasitic factors, the output drain current and the operation frequency of TFTs need to be improved. For AM-FPD panels, especially those with high pixel density, it is difficult to modify the TFT structure and dimensions vastly. Thus, boosting channel carrier mobility is the most direct and effective solution according to Eqs. (1-3) and (1-4).

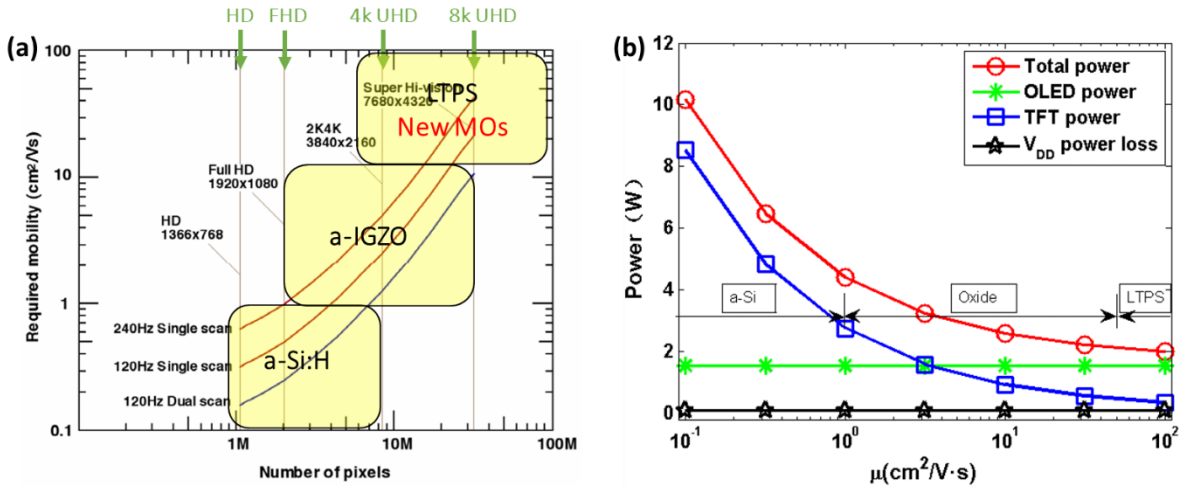

Figure 1-15: (a) Graphic summary of the demanded TFT mobility for next-generation FPD technology with different definitions. (b) Estimated power consumption as a function of TFT mobility in a 4.8-inch AMOLED panel.

However, the prevalently used a-IGZO TFTs only show a typical mobility of 5~10 cm^2/Vs, which seems insufficiently high. Accroding to Fig. 1-15(a), for ultra-high-definition (UHD) displays with an 8k×4k resolution and a frame rate of 120 Hz, the demanded mobility should exceed 16 cm^2/Vs if no advanced signal addressing scheme is introduced in the panels [10]. Additionally, for narrow-bezel panels with system-on-chip (SOP) technology, a-IGZO TFTs can successfully integrate gate drivers but struggle to implement demultiplexers. Moreover, the mobility of TFTs is also closely associated with the power consumption of panels [46]. As illustrated in Fig. 1-15(b), the power consumption of a 4.8-inch AMOLED panel is estimated to keep decreasing with the rise of mobility. In order to save energy and extend battery life in mobile devices, it is necessary to pursue MO TFTs with higher carrier mobility. Therefore, many investigations have been conducted to design new MO channel materials and boost their mobility beyond the value of that offered by a-IGZO with a common atomic ratio (In: Ga: Zn = 1:1:1 at%).

1.3.3 Carrier Mobility Boost in Multicomponent Metal Oxide Semiconductors

For AOS materials, the general solution to boost their carrier mobility is to modify the element composition. For example, metal cation ratio has been intensively studied and well optimized in the a-IGZO system [6, 47, 48]. It was reported that the field-effect mobility of a-IGZO TFTs could exceed 60 cm^2/Vs when the channels adopted a composition of In:Ga:Zn=71.2:21.3:7.5 and the SiO_2 gate insulators were deposited using the atomic layer deposition (ALD) technique at the same time [49]. Fig. 1-16 systematically presents the influence of element composition on electron transport properties in the amorphous In_2O_3-Ga_2O_3-ZnO ternary system [27, 50]. Although the films formed using the pulse laser deposition (PLD) technique can achieve a maximum Hall mobility of 39 cm^2/Vs, the occupied fraction of In_2O_3 compounds exceeds 60%. It has been found that electron Hall mobility is mainly determined by In_2O_3 content. Thus, many groups have even employed amorphous IZO (a-IZO) [28-30] or its analogues [51-54] as TFT channels or one stack among multi-layered channels directly [14, 55-57].

The incorporation of as many as possible indium cations is indeed effective to boost electron mobility. However, it will bring about the rise of the free carrier population and lead to depletion-mode devices, which are less popular in the low-power-consumption applications. Meanwhile, it is well-known that indium is very expensive and its price has maintained a high level over the past 20 years (Fig. 1-17) [58]. Therefore, excess involvement of In_2O_3 will raise material cost and lose one of the core competences of MO TFTs. More importantly, it is found

that no matter how the material compositon is adjusted, there exists an upper carrier mobility limit for amorphous semicondutors in essence.

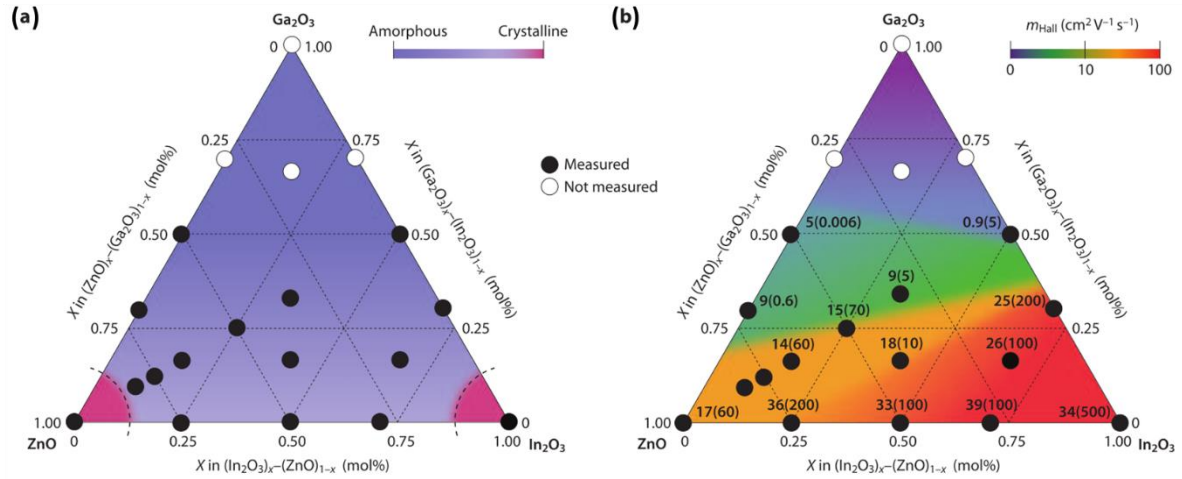

Figure 1-16: (a) Crystal morphology distribution and (b) electron transport properties in an In_2O_3-Ga_2O_3-ZnO ternary system. In (b), the values outside parentheses denote the electron Hall mobility (cm^2/Vs) density, and the values inside parentheses denote the electron concentration ($\times 10^{18}$ cm^{-3}).

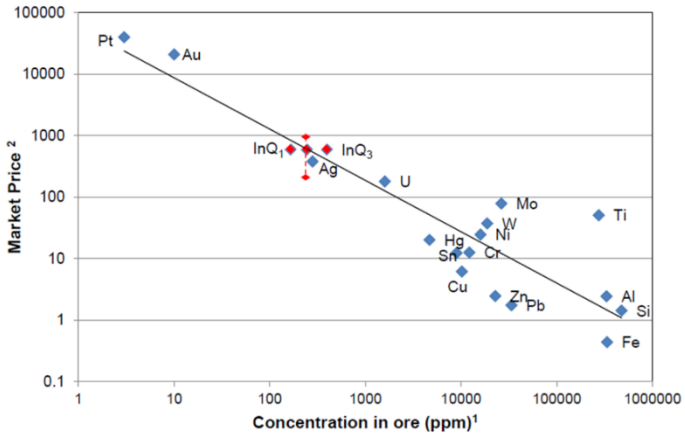

Figure 1-17: Market price versus concentration of metal in typical ore. The first and third quartile data points of indium market price are labeled by InQ_1 and InQ_3, and the fluctuation range of the indium price over the past 20 years is connected by the red dashed line.

According to Steward *et al.* [59-61], they built a physics-based carrier transport model, which involved a band tail state trapping of a diffusive mobility and considered both drift- and diffusion-induced transport. It was found that the carrier mobility of amorphous semiconductors is strongly dependent on the carrier effective mass (m^*) and band tail states at a fixed temperature. Basically, m^* is related to the energy band diagram (or band bending), and it directly determines the intrinsic (or trap-free) drift mobility of materials, while Urbach

energy (E_u) is an indicator of the band tail states, which are associated with the nature of the atomic disorder. If E_u is very large, the carrier trapping sites at the band edges will significantly deteriorate the actual drift mobility from the intrinsic value. Fig. 1-18 plots the electron and hole mobility as a function of Fermi level position and gate bias (V_{gs}) in the amorphous semiconductors. The gate bias was applied across a 100-nm-thick SiO_2 gate insulator layer (C_{OX}=34.5 nF/cm^2). The results revealed that even though the amorphous semiconductor was in the best case, with minimum variables, its upper electron and hole mobility limits could only be at 70.7 cm^2/Vs and 15.9 cm^2/Vs, respectively. For a-IGZO, its estimated mobility for electrons (holes) failed to surpass 14.7 (8.8×10^{-6}) cm^2/Vs. In terms of extraordinarily high mobility reported elsewhere [62-64], Steward *et al.* attributed it to gate insulator leakage, fringing current or the underestimation of gate insulator capacitance. Although they thought it was the nature of the atomic disorder rather than the s-orbital overlapping theory that is responsible for mobility enhancement in the AOS TFTs, their work was still very meaningful. It reminds us of the existence of the upper mobility limit in the AOS materials. Therefore, we should also consider other possible solutions apart from element composition modification to acquire higher mobility for more general multicomponent MO semiconductors.

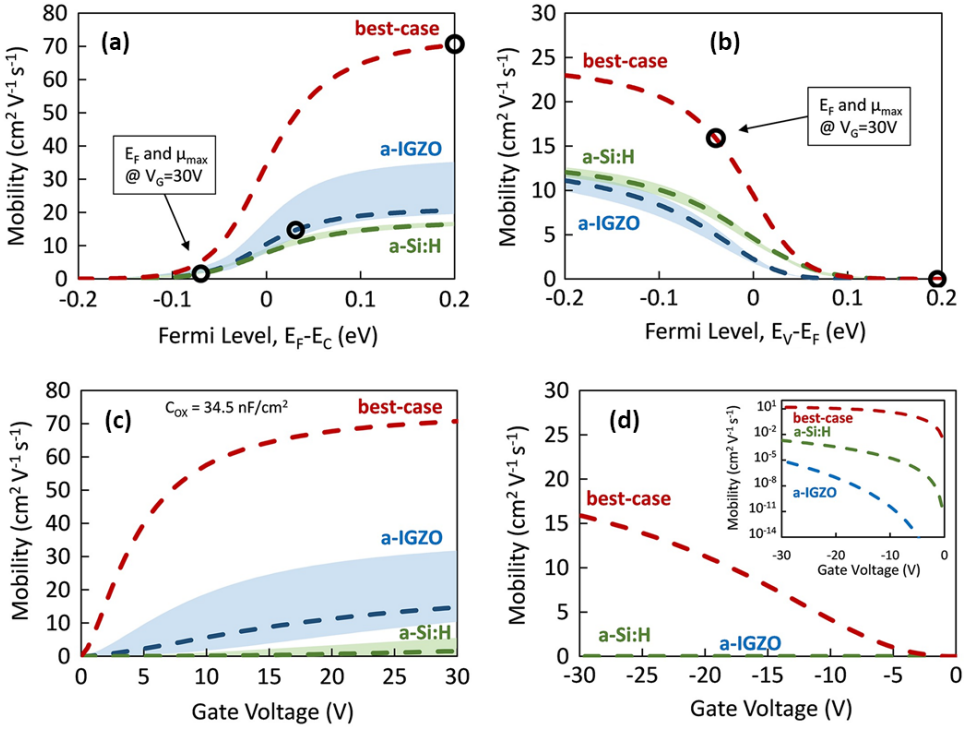

Figure 1-18: (a) Electron and (b) hole mobility as a function of Fermi level position. (c) Electron and (d) hole mobility as a function of gate voltage in amorphous semiconductors. Inset: hole mobility on a logarithmic scale.

According to the Drude model, the electron mobility of multicomponent MO semiconducotors theoretically follows the equation.

$$\frac{1}{\mu} = \frac{m_e^*}{q}\left(\frac{1}{\tau_{composition}} + \frac{1}{\tau_{crystallinity}} + \frac{1}{\tau_{defect}} + \frac{1}{\tau_{vibron}} + \frac{1}{\tau_{strain}} + K\right), \quad (1\text{-}11)$$

where q is the electron charge and m_e^* denotes the electron effective mass. $\tau_{composition}$, $\tau_{crystallinity}$, τ_{defect}, τ_{vibron}, and τ_{strain} represents the average momentum relaxation time related to the spatial distribution of incorporated cations, crystal size and density, defect form and density, thermal vibrations, and piezoelectric effects induced by internal lattice strain, respectively [65]. Thus, the electron mobility can be boosted not only by modifying the element composition but also through manipulating other aspects such as crystal morphology, defects, thermal vibration, lattice strain, etc. Rather than trapped in the upper mobility limit of AOS materials, we had better consider other aspects beyond element composition to boost mobility in general MO semiconductors.

1.3.4 Hall Mobility Evolution in Indium Oxide

In addition to element composition, crystal morphology can also participate in boosting the carrier mobility of multicomponent MO semiconductors. For example, the field-effect mobility can be improved from 5.6 cm^2/Vs to ~80 cm^2/Vs when the TFT channel evolves from a-IGZO [9] to single-crystalline IGZO (c-IGZO) [66]. However, the single-crystalline thin films need to be deposited or annealed at high temperature, which is not friendly to massive production. Although the polycrystalline thin films avoid less thermal budget and their highly ordered atomic arrangements can still offer acceptable mobility, a large amount of grain boundaries will introduce the extra issue of electrical non-uniformity like in LTPS TFTs. Thus, crystal morphology seems like not a good point. However, when we notice the intriguing Hall mobility variation in binary In_2O_3 thin films with different crystallinities, it is believed that there still exists a niche for crystal morphology manipulation to realize TFT channels, which can be easily deposited with boosted mobility, good spatial uniformity and low material cost.

As is known, an indium-indium skeleton in bixbyite In_2O_3 is formed by a network of InO polyhedra. According to the oxygen atom number that is shared between central indium atoms and their six indium neighbors, the InO polyhedra can exist in non-, corner-, edge- or face-shared form. As shown in Fig. 1-19(a), their indium-indium distance is about 3.8 Å, 3.5 Å, 3.3 Å and 3.1 Å, respectively, while the 5s-orbital radius of the indium atom is in the vicinity of 1.8 Å. This means that the central indium atoms in the corner-, edge- and face-shared InO

polyhedra can share electrons with their own neighboring indium atoms by overlapping their second and third shells, and the orbital interactions become increasingly stronger. Among these connected InO polyhedra, the corner-shared type shows the best spatial extension ability due to its longest indium-indium distance with small angle (~115°). Therefore, the long-distance chaining of the corner-shared InO polyhedra can offer the most efficient percolation conduction path. For the non-shared InO polyhedra without orbital interactions among indium atoms, electron localization will become the major factor to hinder carrier conduction. But these non-shared InO polyhedra are allowed to further evolve into their corner-, edge- and then face-shared forms in sequence. As a result, the electron mobility of XRD amorphous In_2O_3 thin films with a non-shared InO polyhedral framework can be boosted after thermal processing, but the increase trend is not simply unidirectional.

In 2014, Chang *et al.* reported their study on Hall mobility variation of In_2O_3 thin films that are deposited at different temperatures [67]. As plotted in Fig. 1-19(b), with the rise of deposition temperature from -100 °C to 600 °C, the In_2O_3 thin films gradually shifted from the XRD amorphous phase to the traditional polycrystalline phase, and their crystallinity kept increasing. However, it was not noted that their Hall mobility increased monotonically. There emerged an unexpected peak in Zone B (-50 °C ~ 100 °C), and the local extremum value at 0 °C was surprisingly comparable to the results at >400 °C, where highly crystalline In_2O_3 thin films were deposited. Referring to the X-ray diffraction (XRD) spectra in Fig. 1-19(c), the In_2O_3 films deposited at 0 °C showed a relatively broad and weak XRD peak. This reflected the existence of nanocrystals, but their occupied fraction was not so large that their XRD signal was manifested from the signal of the amorphous matrix. Therefore, the crystal morphology in the In_2O_3 films deposited at 0 °C was a transitional state between the amorphous phase (Zone A, <-50 °C) and the polycrystalline phase (Zone C, 100 °C ~ 600 °C). Herein, we describe such crystal morphology as hybrid phase (hp), where both crystal grains and an amorphous matrix exist together.

Via extended X-ray absorption fine structure (EXAFS) measurements and *ab initio* molecular dynamics (MD) liquid-quench simulations, the corner-shared InO polyhedra were found to reach a maximum fraction of >80% at 0 °C (Fig. 1-19(d)) [65]. In other words, the hybrid phase contained a sufficiently large amount of corner-shared InO polyhedra. This is beneficial to form long-distance directional chains for electron conduction, leading to a high Hall mobility. On the other hand, no very high density of grain boundaries is observed since the crystals inside are not the majority. Therefore, such a hybrid phase in the In_2O_3 thin films

is the ideal crystal morphology that we are searching for. It can surpass the upper mobility limit in AOS materials and eliminate the non-uniformity issue in polycrystalline semiconductors.

Explanations for the Hall mobility variation of binary In_2O_3 thin films are summarized in Table 1-2. Not only are the forms of the InO polyhedra but also many other factors, like grain boundaries, are found to significantly affect the Hall mobility. For example, within the narrow temperature range from 50 °C to 100 °C, Hall mobility is reduced dramatically. At the same time, the crystallinity of binary In_2O_3 thin films as well as the density of scattering centers at the grain boundaries increases rapidly. Thus, it is necessary to remove negative impacts brought by grain boundaries. The binary In_2O_3 thin films inevitably present a crystalline microstructure when deposited at or above room temperature. Though the deposition system allows the substrate temperature to cool down to 0 °C or even lower, the relatively high price of indium will hinder the application of binary In_2O_3 TFTs in FPDs. In order to gain amorphization and reduce raw material cost, it has been suggested to blend binary the In_2O_3 with other inexpensive MO materials to create multicomponent MO semiconductors. Provided that the synthesized thin films still contain enough corner-shared InO polyhedra for long-distance directional chaining, it is certain that the resulted carrier mobility will maintain a reasonably high level. But unlike the binary In_2O_3 thin films, there are many new areas that need to be investigated in the multicomponent MO semiconductors. We must carefully and sufficiently consider, for example, what kind of MO additives are appropriate for amorphization, how to easily form the hybrid phase, and what the critical indium content is for continuous chaining.

Table 1-2: Summary of Hall mobility variation in binary In_2O_3 thin films deposited at different temperatures

Temp. range	**Crystal morphology**	**μ_{hall} variation**	**Explanation**
<-50 °C	Amorphous	~	μ_{hall} is limited by electron localization (disconnection of non-shared InO polyhedra).
-50~0 °C	Amorphous → Hybrid phase	↑	μ_{hall} is enhanced by electron percolation (disconnection of non-shared InO polyhedra → long-distance chaining of corner-shared InO polyhedra).
0~100 °C	Hybrid phase → Crystalline	↓	μ_{hall} is suppressed by multiphase scattering/electron localization (long-distance chaining of corner-shared InO polyhedra → short-distance clustering of edge-/face-shared InO polyhedra with increasingly more grain boundaries).
100~600 °C	Polycrystalline phase	↑	μ_{hall} is boosted by diminished grain boundaries and enlarged grain size in densified thin films (further clustering of InO polyhedra).

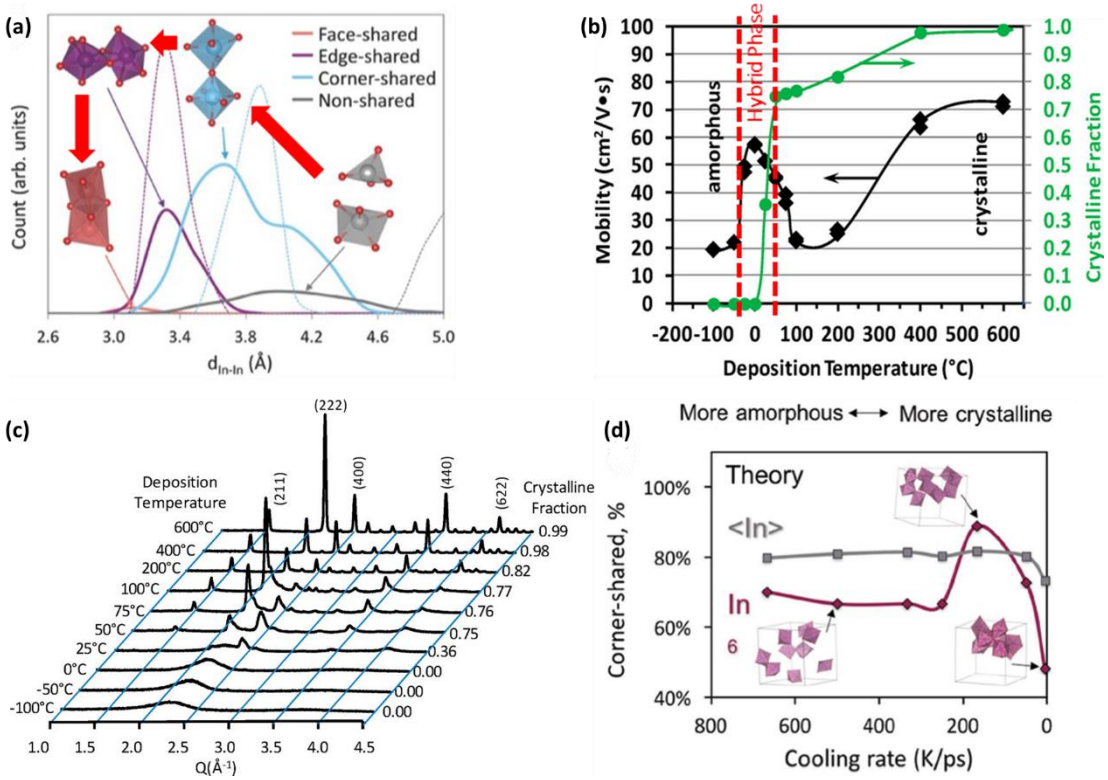

Figure 1-19: (a) Distribution of non-, corner-, edge-, and face-shared InO polyhedra as a function of indium-indium distance in amorphous (solid lines) and crystalline (dashed lines) In_2O_3 thin films. (b) Hall mobility and crystallinity of In_2O_3 thin films as a function of deposition temperature. (c) Grazing incidence XRD spectra of In_2O_3 thin films deposited at different temperatures. (d) Fraction of corner-shared InO polyhedra occupied in the total number of InO polyhedra as a function of MD quench rate.

1.4 Thesis Organization

As shown in Fig. 1-20, this thesis is divided into three major parts including hybrid-phase metal oxide thin film design, various thin-film transistor implementation, and practical technology application. These parts are organized under a bottom-up framework and are investigated in sequence.

In the first part, since display backplanes are demanded to own stronger switching/driving capability and lower power consumption, the MO TFTs inside should be equipped with increasingly higher electrical characteristics especially in carrier mobility. Considering the upper mobility limit in AOS materials and the excess employment of expensive indium cations for electron transport, a new type of hybrid-phase ITZO (hp-ITZO) thin film is proposed to boost mobility via collaboratively modifying both element composition and crystal morphology. In Chapter 2, information about their deposition conditions, (microstructural,

electrical, and optical) properties, and energy band diagrams are collected and discussed. The results indicate that such thin films are presumably promising in high-performance and reliable MO TFTs.

In the second part, by matching proper fabrication techniques, the hp-ITZO TFTs with different architectures are presented. To confirm the feasibility of hp-ITZO thin films as channel layers, the BG-TC TFTs are first fabricated using a lift-off technique in Chapter 3. By tuning the oxygen partial pressure ratio and direct-current sputtering power for an ITO target, the optimal channel deposition conditions are determined. Meanwhile, the electrical performance, spatial uniformity and shelf life of the corresponding devices are also examined. As highly demanded in industry, the BCE-type TFTs with wet-etched S/D electrodes are further fabricated and exhibit good characteristics. The core content is damage suppression at their back-channel surfaces via over-etch ratio control and prior thermal annealing enhancement.

Since the TG-SA TFTs enable miniaturized parasitic capacitance, strong device scalability and lower manufacturing cost, their implementation incorporating the hp-ITZO channels is of high value. However, for high-mobility TG MO TFTs, the deposition of high-quality gate insulators and the efficient control of threshold voltage are always not satisfactory. Thus, TG-BC TFTs with real S/D electrode entities are employed to deal with these two issues in Chapter 4. Through gate insulator engineering and gate electrode engineering, enhancement-mode devices with robust gate insulator stacks are achieved. Afterwards, the desirable TG-SA TFTs are successfully demonstrated as well. Their conductive and thermally stable S/D regions are delicately formed by employing two different PECVD SiO_2 layers together with differentiated O_2 annealing strategies.

In the third part, a 2.2-inch monochromatic AMOLED panel is fabricated using our hp-ITZO TFT technology. Other possible applications to integrated circuits (ICs) and sensors are also implemented, with some preliminary but promising results in Chapter 6.

Finally, a conclusion is drawn and suggested further work ranging from material simulation to device optimization and application exploration is proposed in Chapter 7.

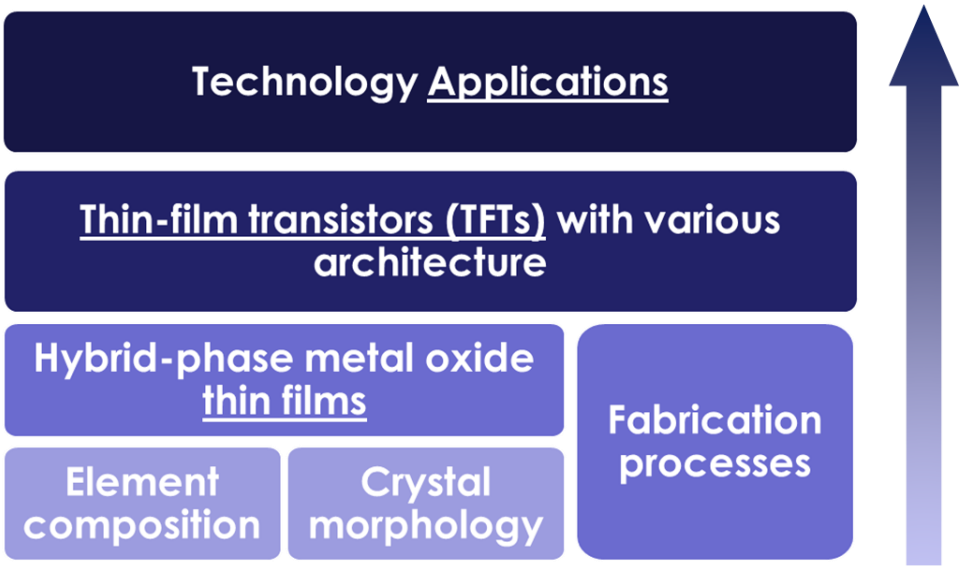

Figure 1-20: Bottom-up organization of this thesis.

Chapter 2 Hybrid-Phase Indium-Tin-Zinc Oxide Thin Films

Since FPD technology is developing towards ultra-high definitions (UHDs) (e.g., over 7680×4320 resolution and >120 Hz frame rate), narrow bezels and lower power consumption, MO TFTs are demanded to have higher switching/driving capability and faster operation frequency [10, 46, 68]. Thus, much effort has been made to boost carrier mobility in multicomponent MO semiconductors, and most of them only focused on element composition modification in AOS materials. However, Steward *et al.* [59, 60] predicted the existence of an upper carrier mobility limit in amorphous semiconductors. This was closely associated with atomic disorder. Therefore, both element composition and crystal morphology ought to be well taken into consideration for mobility boost. In this chapter, we propose a new type of hp-ITZO thin film, which is an example of collaborative modification.

2.1 Thin Film Deposition

As mentioned in Chapter 1, the binary In_2O_3 thin films can reach a Hall mobility peak in their hybrid phase. In order to achieve such crystal morphology in multicomponent MO semiconductors, there are several common approaches like deposition at precisely controlled temperature [65, 67] or post-annealing treatment [66]. However, they will involve an extra thermal budget and increase the experiment/fabrication complexity. In this thesis, we adopt a co-sputtering method, as illustrated in Fig. 2-1. The thin films can be deposited with the hybrid phase at room temperature without any further post-annealing treatment. When at least two polycrystalline targets are sputtered in a chamber simultaneously, nanocrystalline pellets from each target will have sufficiently high momentum on their way towards the substrates or at the beginning of their arrival on the substrates. Then, a large portion of pellets may interact with each other, while the rest may survive fierce collisions. The reacted pellets will lose their crystalline feature to form an amorphous matrix, or fortunately generate new crystal grains. Thus, the deposited thin films may present the hybrid-phase microstructure, which is between the XRD amorphous phase and the conventional nano-/poly-crystalline phase. For example, by co-sputtering polycrystalline ZnO (pc-ZnO) and polycrystalline ITO (pc-ITO) targets, we can obtain hp-ITZO thin films.

Specifically, the hp-ITZO thin films were deposited at room temperature through magnetron co-sputtering 2-inch circular pc-ITO (90 wt% In_2O_3 and 10 wt% SnO_2) and pc-ZnO targets. The pc-ITO target was connected to a direct-current (DC) power source, whereas the pc-ZnO

target was sputtered using a radio-frequency (RF) power source. The base pressure in the chamber was pumped to 5×10^{-6} Torr. During deposition, the gas flow rate of Ar/O_2, working pressure, DC power (P_{DC}) and RF power (P_{RF}) was set to 12/8 sccm, 3 mTorr, 120 W and 150 W, respectively. The substrates used for thin film deposition were silicon wafers coated by 500-nm-thick thermally grown SiO_2. The distance between the substrates and targets was 10 cm, and the deposition time was 20 min.

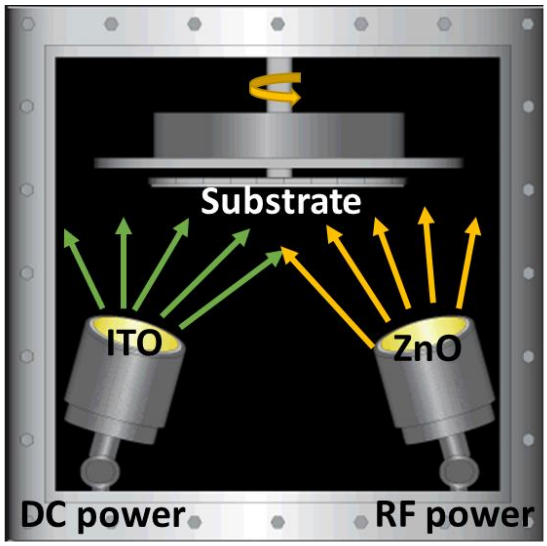

Figure 2-1: Schematic diagram of the magnetron co-sputtering system used for hp-ITZO thin film deposition.

2.2 Thin Film Characterization

2.2.1 Microstructural Properties

Firstly, the hp-ITZO thin films were analyzed using an X-ray diffractometer (XRD, PANalytical Empyrean) with Cu Ka radiation in grazing incidence geometry. As shown in Fig. 2-2(a), there is a relatively weak and broad peak centered at around 33.5° in the hp-ITZO thin films. This is consistent with the XRD spectrum of the binary In_2O_3 thin films in their hybrid phase, as plotted in Fig. 1-19(c). According to Scherrer's equation,

$$D = \frac{k\lambda}{\beta\cos\theta}, \tag{2-1}$$

where k, λ, β and θ denote a constant (0.98), incident X-ray wavelength (1.540598 Å), full width at half maximum (FWHM) of the peak and diffraction angle, respectively [69]. Therefore, the estimated average grain size is ~2 nm, indicating the existence of nanocrystals. As shown in Fig. 2-2(b), with the increase of thin film thickness from 25 nm to 100 nm, there is no doubt

that the intensity of broad diffraction peaks become gradually stronger. However, these peaks are all centered at the same diffraction angle without obvious FHWH difference regardless of annealing treatments. It implies that the obtained hp-ITZO thin films have the relatively stable microstructure, which can be immune to thickness variation and stand more thermal budget from the following processes. Since the diffraction peak herein positions between the pc-ITO (222) peak and the pc-ZnO (002) peak, the nanocrystals must be composed of more complex compounds rather than the segregated pc-ZnO or pc-ITO pellets.

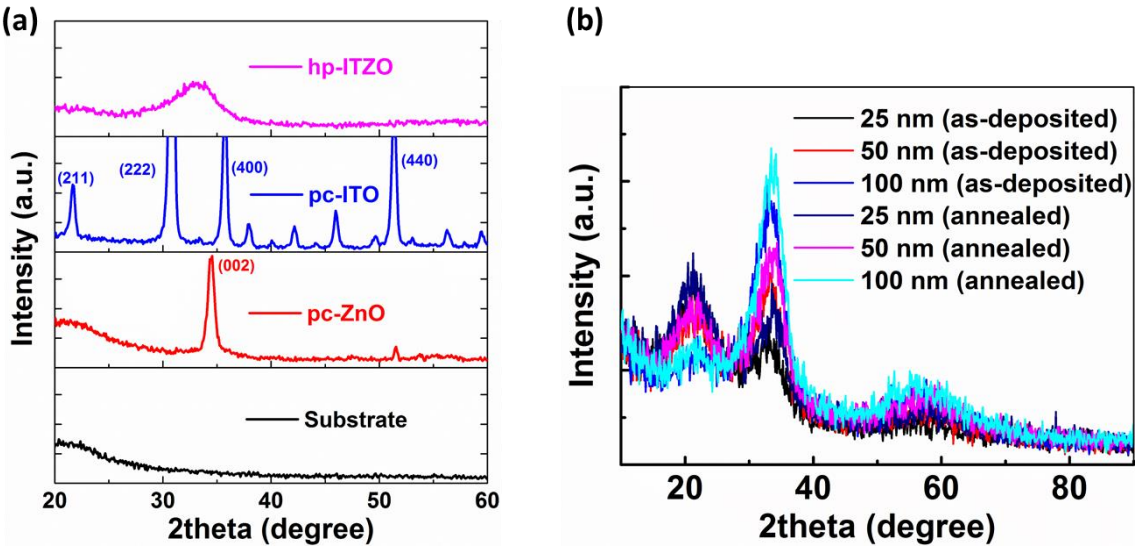

Figure 2-2: (a) XRD spectra of pc-ITO thin film, pc-ZnO thin film, hp-ITZO thin film and silicon wafer coated with thermally grown SiO_2. The thickness of thin films is 50 nm. (b) XRD spectra of hp-ITZO thin films with different thicknesses before and after annealing treatments (300 °C, 12 h, in the atmospheric environment).

Then, the thin films were further investigated using a high-resolution field emission transmission electron microscope (HRTEM, JEOL JEM-2010HR), and their cross-sectional HRTEM image is shown in Fig. 2-3(a). The lattice fringes with a measured interplanar crystal spacing of around 0.29 nm are highlighted by red dashed lines, and the grain size is consistent with the XRD-derived result. Based on the XRD diffraction peak position and the interplanar crystal spacing value, it can be inferred that the above nanocrystals are likely to consist of homologous $Zn_kIn_2O_{(k+3)}$ (where k=3, 4), ilmenite $ZnSnO_3$ and spinel Zn_2SnO_4 compounds [70]. By accumulating these nanocrystalline region areas together (Fig. 2-3(b)), we could calculate the total areal ratio of the nanocrystalline regions occupied in the whole cross-sectional field via image processing software (ImageJ). This represents the cross-sectional areal crystallinity r_{area} of the hp-ITZO thin films, and the result is ~17.9%. On the other hand, XRD

data processing software (MDI Jade 6) was also employed to analyze the thin film crystallinity. The method is to decompose the wide and weak peak into several narrow and sharp subpeaks corresponding to specific compounds (e.g., ZnO, $Zn_3In_2O_6$, $Zn_4In_2O_7$, etc.). The obtained volumetric crystallinity r_{vol} is 21.2%, which is higher than the derived result ($r_{area}^{3/2}$) from the cross-sectional areal crystallinity. The difference is because the nanocrystals are columnar rather than cubic. Above all, the hybrid phase herein actually refers to an amorphous matrix where a number of columnar nanocrystals with blurry grain boundaries are embedded. Such microstructural character is different from the XRD amorphous phase and the conventional polycrystalline phase.

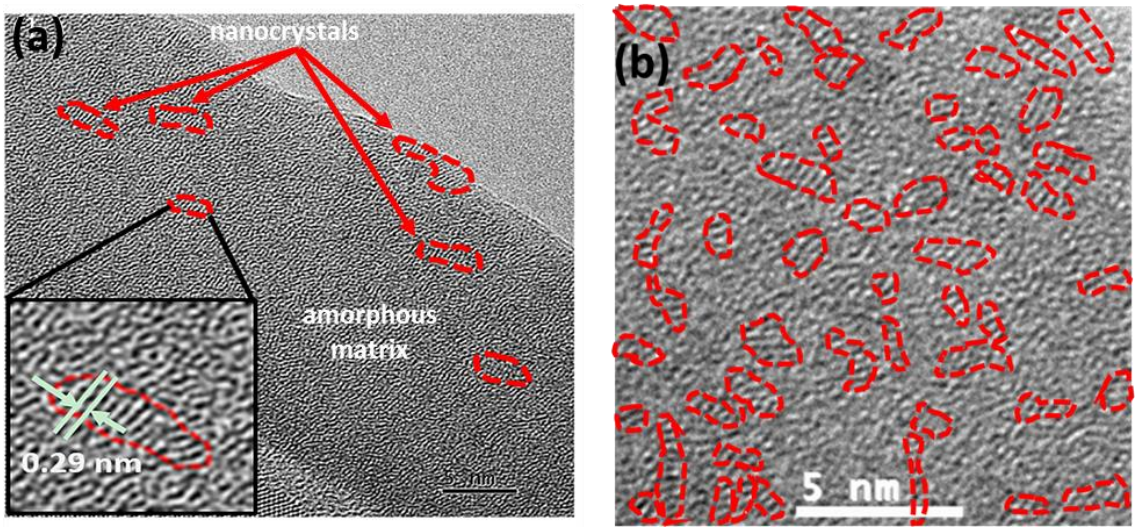

Figure 2-3: (a) Cross-sectional HRTEM image of hp-ITZO thin films. (b) Magnified HRTEM image with nanocrystalline regions, which are surrounded by red dashed lines.

As mentioned in Chapter 1, the corner-shared InO polyhedra in the hybrid phase In_2O_3 thin films occupies the maximum fraction. Therefore, it is thought that the hp-ITZO thin films also enjoy more corner-shared InO polyhedra compared to their counterparts in other crystal morphologies. Then, the internal long-distance chaining process can dominate the formation of directional carrier percolation paths for boosted Hall mobility. On the other hand, the short-distance clustering degree of the edge- and face-shared InO polyhedra and the density of the grain boundary in the hp-ITZO thin films are expected to be low, and hence their Hall mobility is less deteriorated due to suppressed scattering centers. In addition, since the grain size is in nanoscale and much smaller than TFT channel dimensions, the hp-ITZO TFTs can maintain a relatively good spatial uniformity in terms of their electrical characteristics.

To better understand the hybrid phase, an atomic force microscope (AFM, Park XE150S)

was used, and the silicon wafer coated with thermally grown SiO_2 was firstly scanned as a background reference. The substrate is shown to be extremely flat with a surface root mean square (rms) roughness of 0.221 nm (Fig. 2-4(a)), which has little effect on the following deposited thin films. Fig. 2-4(b)-(d) present the AFM images describing the surface morphology of the hp-ITZO, pc-ZnO and a-IGZO thin films, and their respective rms roughness value within a 1 μm ×1 μm region is measured to be 0.420 nm, 0.729 nm and 0.387 nm. This means that the hp-ITZO thin films with discrete nanocrystals and the a-IGZO thin films are more uniform and smoother than the pc-ZnO thin films. This shows potential to reduce roughness-related interfacial scattering and suppress mobility degradation, particularly for top-gate TFTs.

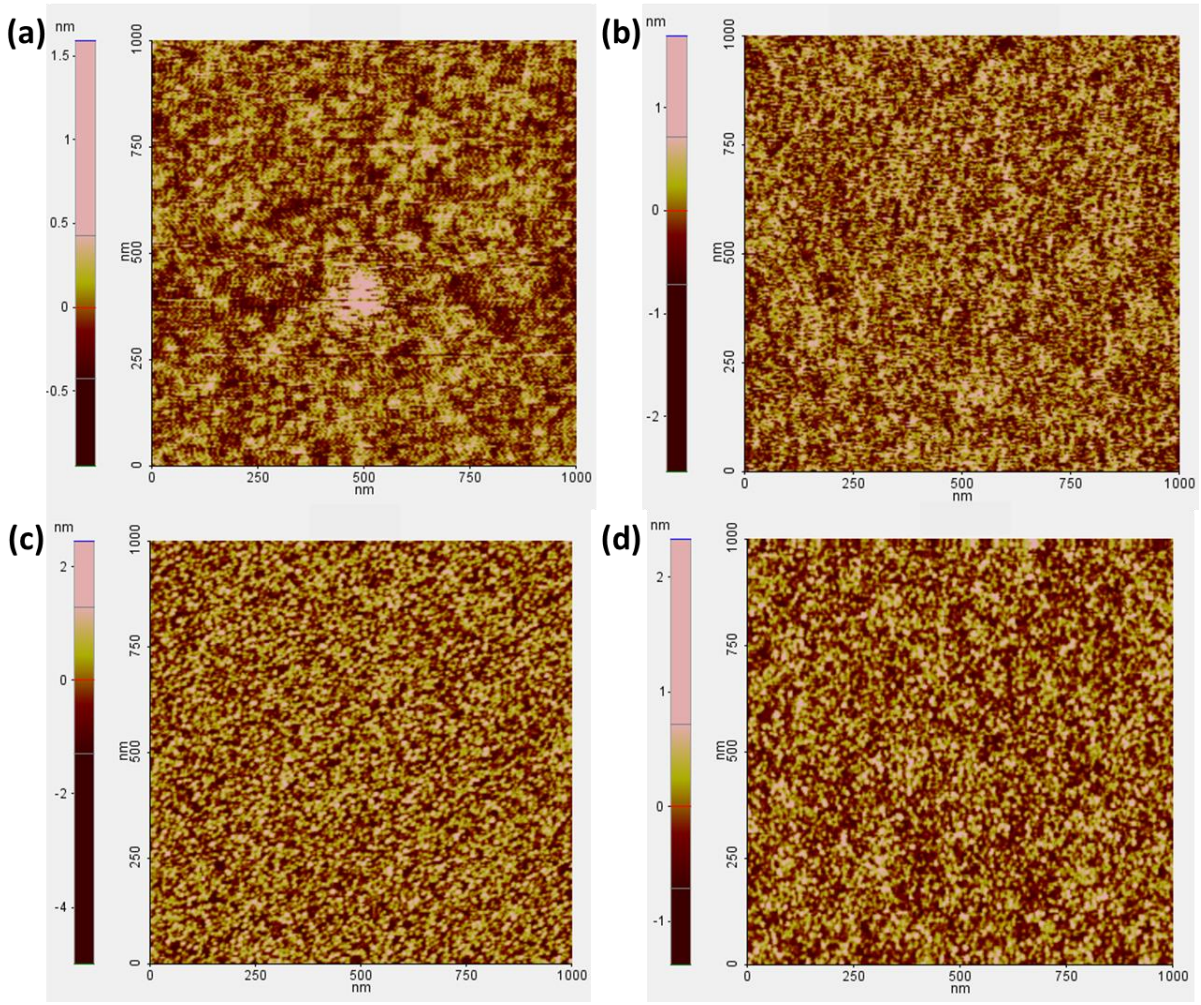

Figure 2-4: AFM images of (a) bare substrate, (b) hp-ITZO, (c) pc-ZnO and (d) a-IGZO thin film.

2.2.2 Electrical Properties

Among various electrical parameters of the hp-ITZO thin films, we mainly focus on their

Hall mobility. As shown in Fig. 2-5(a), a square Van der Pauw structure was applied to the thin films, which were deposited on 1.5 cm*1.5 cm silicon substrates with 500-nm-thick thermally grown SiO_2. Four sufficiently small contacts were deposited at the corners by sputtering 200-nm-thick Al, and they were patterned using a shallow-mask technique. Then, the results were obtained using a Hall effect measurement system (Ecopia HMS-5500). In order to study the Hall mobility variation in the ITZO thin films with different crystallinity, the samples were prepared by co-sputtering the pc-ZnO target and the pc-ITO target at room temperature (Sample B), 150 °C (Sample C), 300 °C (Sample D) and 450 °C (Sample E). Since the thin films deposited at room temperature happen to present the hybrid-phase morphology, Ar implantation was employed to form the XRD amorphous thin films (Sample A). To analyze sample composition, an X-ray photoelectron spectroscopy (XPS) measurement was further conducted on a Physical Electronics 5600 multi-technique system.

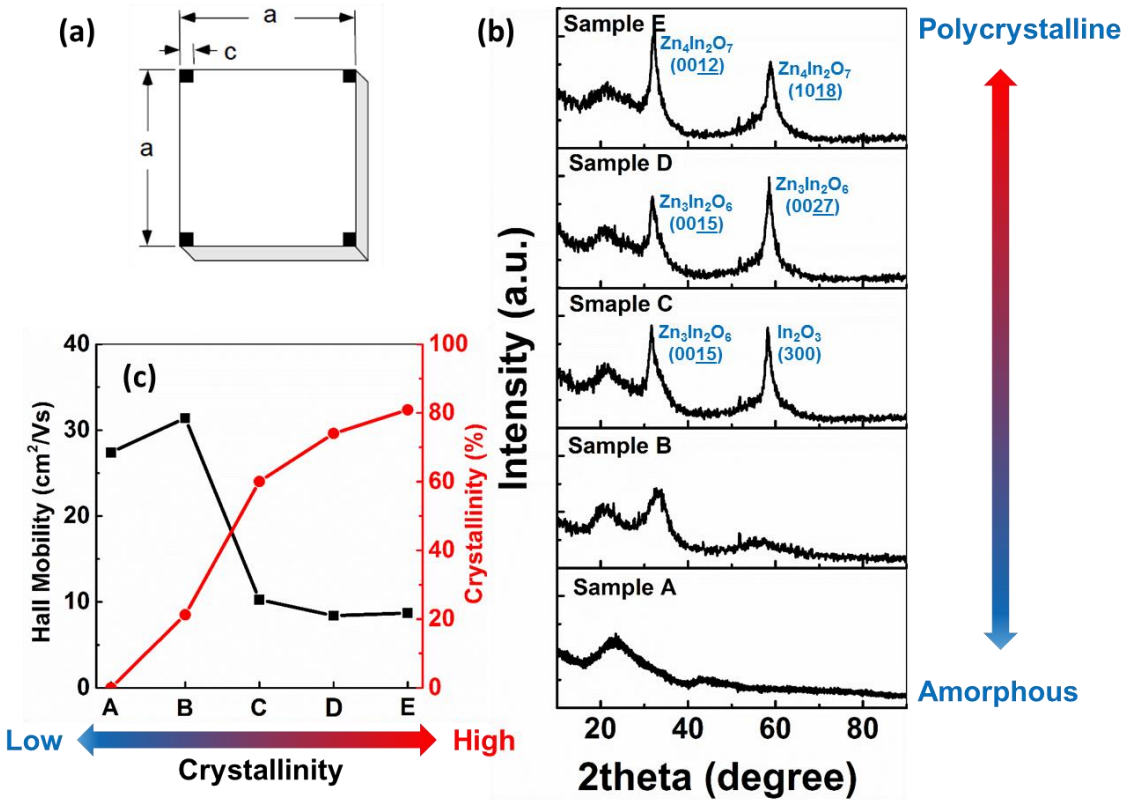

Figure 2-5: (a) Illustration of square Van der Pauw geometry for Hall effect measurement. (b) XRD spectra of ITZO thin films with different crystallinity. (c) Plot of Hall mobility variation versus ITZO thin film crystallinity.

According to the XRD spectra in Fig. 2-5(b), the crystallinity of ITZO thin films keeps increasing with the rise of deposition temperature. However, their Hall mobility does not vary monotonically. Sample B, which corresponds to the hybrid phase, presents a Hall mobility peak

of 31.6 cm^2/Vs, and this is about 15.3% higher than that in its amorphous counterparts. When the thin films possess higher crystallinity, their Hall mobility will decrease sharply and stay in the vicinity of 10 cm^2/Vs. Table 2-1 lists the atomic concentration of each sample, and their element composition is almost the same. It is found that their Hall mobility variation trend follows that of the binary In_2O_3 thin films in Chapter 1. This is due to the corner-shared InO polyhedra, which occupy the highest fraction in the hybrid phase (Sample B) [65, 67]. Although there must exist the other types (non-, edge- and face-shared) of InO polyhedra at the same time, the long-distance chaining of the corner-shared InO polyhedra is primarily responsible for the formation of carrier percolation conduction paths, as shown in Fig. 2-6. In terms of Sample A, its Hall mobility is mainly limited by the non-shared InO polyhedra, among which the 5s orbitals of indium cations are separated to form the disconnected conduction paths. In terms of Sample C, D and E, the fraction of edge- and face-shared InO polyhedra increases. Their short-distance clustering can lead to InO polyhedra with shorter indium-indium distance but also make a part of originally overlapped orbitals disconnected if the element composition remains the same. Thus, the broken conduction paths together with the increasingly higher grain boundary density hinder electron drift under a certain electric field. Above all, the hybrid phase in ITZO thin films is believed to be an effective crystal morphology, which can suppress Hall mobility degradation from the ideal value in their single crystalline counterparts.

Table 2-1: Atomic concentration in the ITZO thin films with different crystallinities

	In (at%)	**Sn (at%)**	**Zn (at%)**	**O (at%)**
Sample A	20.98	1.59	29.94	47.58
Sample B	19.41	1.38	31.98	47.23
Sample C	16.84	1.21	35.13	46.82
Sample D	16.47	1.18	36.14	46.21
Sample E	16.47	1.14	37.07	45.31

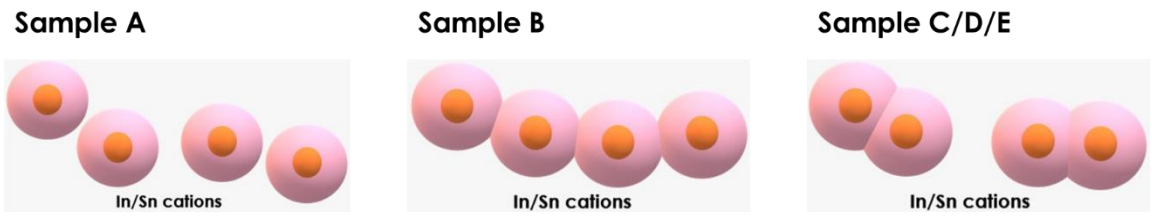

Figure 2-6: Illustration of major InO/SnO polyhedral form in Sample A~E.

Furthermore, the upper electron mobility limit of amorphous ITZO (a-ITZO) thin films was

estimated. Theoretically, the mobility of a semiconductor is equal to [59, 60]

$$\mu^{-1} = \mu_{drift}^{-1} + \mu_{diff}^{-1}, \tag{2-2}$$

where μ_{drift} and μ_{diff} is the drift mobility and diffusion mobility, respectively. Herein, μ_{diff} is introduced to appropriately describe electron conduction in the subthreshold region, where the channel current is dominated by diffusion. On the other hand, the drift mobility can be further expressed as follows [71-74]:

$$\mu_{drift} = \frac{n}{n + n_T}\mu_0 = \frac{n}{n + n_T} \cdot \frac{qh}{6m_e^* k_B T}, \tag{2-3}$$

where n, n_T , μ_0, q, m_e^*, $\hbar$, k_B, and T denotes the free carrier concentration, trapped carrier concentration, trap-free mobility, electron charge, electron effective mass, reduced Planck constant, Boltzmann's constant, and absolute temperature (300 K), respectively. Herein, the approximate value of m_e^* is 0.27 m_0 when the total atomic ratio of indium and tin cations is about 43%, referring to [75], and m_0 is the electron rest mass. n and n_T should fulfill the following equations:

$$n = \int_{E_C}^{\infty} g_C(E) f(E) dE = \int_{E_C}^{\infty} [n_{TA} + \frac{1}{2\pi^2}(\frac{2m_e^*}{h^2})^{\frac{3}{2}} \sqrt{E - E_C}] f(E) dE, \tag{2-4}$$

$$n_T = \int_{E_V}^{E_C} g_{TA}(E) f(E) dE = \int_{E_V}^{E_C} n_{TA} \exp(\frac{E - E_C}{E_U}) f(E) dE, \tag{2-5}$$

where E_C and E_V is the conduction band minimum (CBM) and the valence band maximum (VBM), respectively, $g_c(E)$ is the conduction band density of states, $g_{TA}(E)$ represents the density of conduction band tail states, n_{TA} denotes the peak density of acceptor-like band tail states, f(E) is the Fermi-Dirac occupancy function, and E_U corresponds to the conduction band Urbach energy, which is associated with the exponential decay rate of tail states below the conduction band mobility edge. In order to estimate the upper electron mobility limit of the a-ITZO thin films, we define its E_U as 10 meV, which is the best case among amorphous semiconductors and close to the value of a-IGZO (~13 meV) [10].

On the other hand, the diffusion mobility can be converted from the drift mobility according to the following relationship:

$$\mu_{diff} = \mu_{drift} \frac{n}{N_C} = \mu_{drift} \frac{n}{2(\frac{2\pi m_e^* k_B T}{h^2})^{\frac{3}{2}}}, \quad (2\text{-}6)$$

where N_C is the conduction band effective density of states, and h is the Planck constant. After Eqs. (2-3) ~ (2-6) are substituted into Eq. (2-2), we can simulate the electron mobility as a function of the Fermi level position (E_F - E_C), and the related curve is plotted in Fig. 2-7 (a). The calculated upper limit of the electron mobility in the a-ITZO thin films is 26.23 cm^2/Vs, which corresponds to the value when E_F enters E_C above 0.2 eV. This result approaches the previously measured results in the a-ITZO and is also lower than that in their hybrid-phase counterparts. In addition, the electron mobility as a function of gate bias is also simulated and the results are shown in Fig. 2-7(b). Herein, we adopt 100-nm-thick SiO_2 as gate insulators. The result is even lower. Therefore, it is concluded that the hybrid-phase crystal morphology is a promising solution to break through the upper mobility limit in amorphous semiconductors.

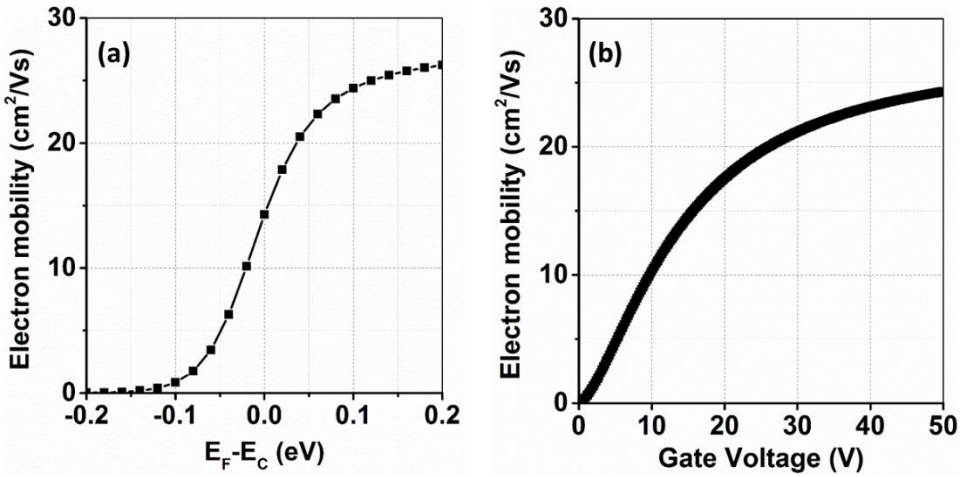

Figure 2-7: Simulated electron mobility versus (a) Fermi level position and (b) gate bias in the a-ITZO thin films.

The upper mobility limit simulation can be also carried out by accessing an amorphous semiconductor transport simulator, which is available online (https://nanohub.org/tools/asts/session?sess=1369376).

2.2.3 Optical Properties

In order to define the energy band diagram of the hp-ITZO thin films, we conducted several optical measurements to extract the related information. Their optical transmittance (T) was measured by UV-VIS spectroscopy (Perkin Elmer Lambda 20). To avoid light extinction, the thickness (d) of the thin films was fixed at ~110 nm. Fig. 2-8(a) shows the optical transmittance spectrum of the hp-ITZO thin films on quartz substrates. It is observed that such thin films are

highly transparent in the visible range with an average transmittance exceeding 80%. Then, the optical absorption coefficient (α) can be extracted from T according to the Beer-Lambert law [76],

$$I = I_0 e^{-\alpha d}, \tag{2-7}$$

$$\alpha = \left(\frac{1}{d}\right) \ln\left(\frac{I_0}{I}\right) = \left(\frac{1}{d}\right) \ln\left(\frac{1}{T}\right), \tag{2-8}$$

where I_0 and I denote the input and output light intensity, respectively. In theory, the relationship between α and incident photon energy (hν) follows the Tauc model, which is given by

$$\alpha h\nu = \alpha_0 (h\nu - E_g)^n, \tag{2-9}$$

where α_0 is an energy independent constant, and n is the power factor of the transition mode [77]. Herein, n is chosen as 0.5 for the hp-ITZO thin films. Thus, the band gap (E_g) can be determined by extrapolating a straight line in the linear region of the $(\alpha h\nu)^2$ versus hν plot (Fig. 2-8(b)), and the result is 3.40 eV.

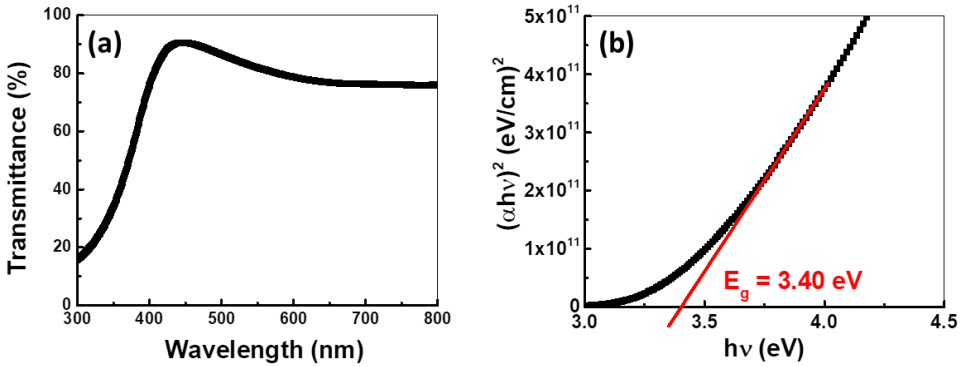

Figure 2-8: (a) Optical transmittance spectrum of the hp-ITZO thin films. (b) Plot of $(\alpha h\nu)^2$ versus hν.

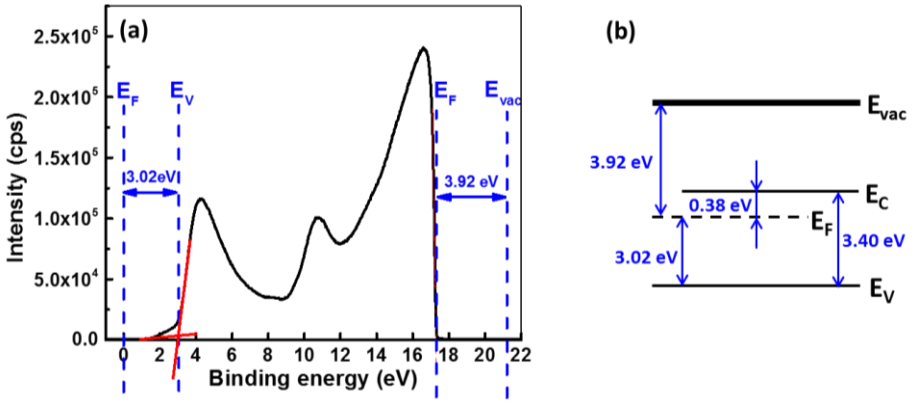

Figure 2-9: (a) UPS spectrum and (b) energy band diagram of hp-ITZO thin films.

The information regarding the energy band diagram was further explored using ultraviolet photoelectron spectroscopy (UPS, Physical Electronics 5600 multitechnique system). Before the UPS data collection, top 5-nm-thick thin films were pre-sputtered and removed to clean the sample surface. During the UPS measurement, a He I ($h\nu$ = 21.22 eV) gas discharge lamp was used as an excitation source, and a bias of -10V was applied on the samples to enhance the signals with kinetic energy near zero (i.e., the cutoff region of the secondary electrons). When the UPS test was finished, the UPS spectrum was plotted, as shown in Fig. 2-9(a). From the spectrum, we could extract the potential difference between E_F and the vacuum level (E_{vac}) as well as between E_F and E_V, and the corresponding value is 3.92 eV and 3.02 eV, respectively. Then, the energy band diagram can be comprehensively determined and plotted in Fig. 2-9(b).

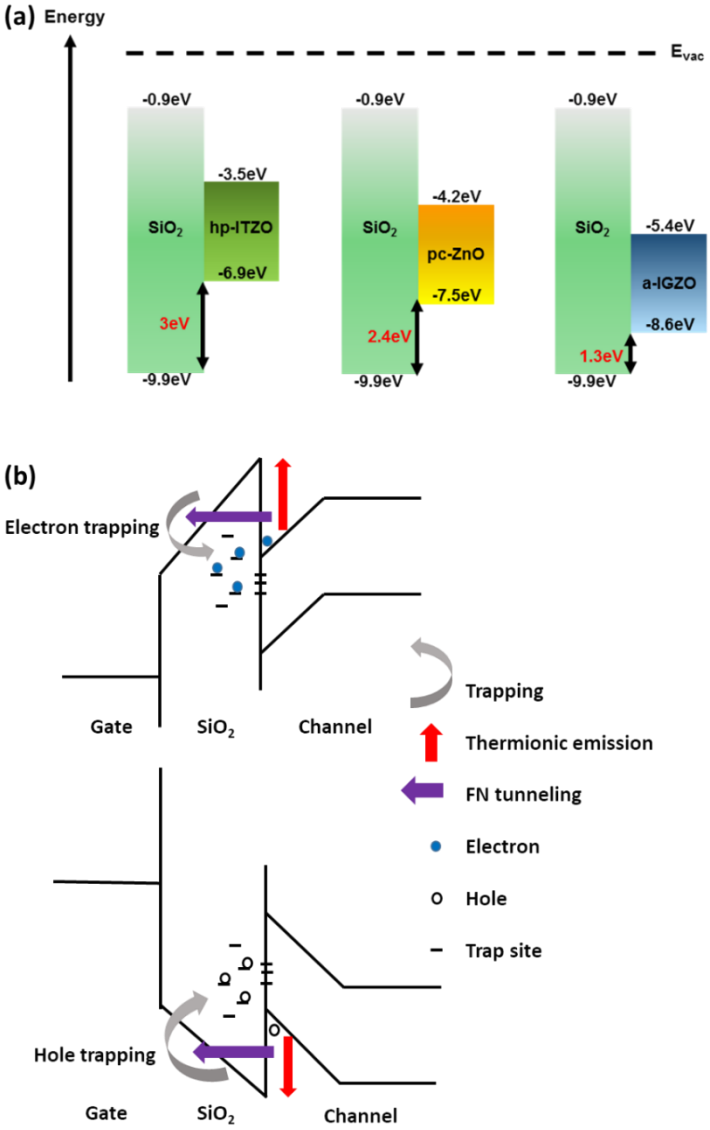

Figure 2-10: (a) Energy band diagrams of hp-ITZO, pc-ZnO and a-IGZO thin films aligned with SiO_2. (b) Schematic diagram of electron and hole trapping processes.

Compared with pc-ZnO and a-IGZO, the hp-ITZO thin films present more symmetric band offsets when aligned with SiO_2 (Fig. 2-10(a)). Their barrier height near the valence band is the largest (~3 eV) and is more than twice that of a-IGZO. As illustrated in Fig. 2-10(b), such a large barrier can significantly reduce thermionic emission and Fowler-Nordheim (FN) tunneling possibilities of holes. Then, issues related to hole trapping at the SiO_2/AC interfaces and even inside the SiO_2 bulks can be effectively addressed. The corresponding TFTs are believed to suffer less from hole-trapping-related instabilities such as negative gate-bias stress (NBS) [78]. Although the barrier height near the conduction band will have to decrease accordingly, 2.6 eV is still quite a large barrier height to block electrons. Therefore, electron trapping induced instabilities of devices will not be severely exacerbated. The robust reliability of TFTs with the hp-ITZO channels can be guaranteed in principle.

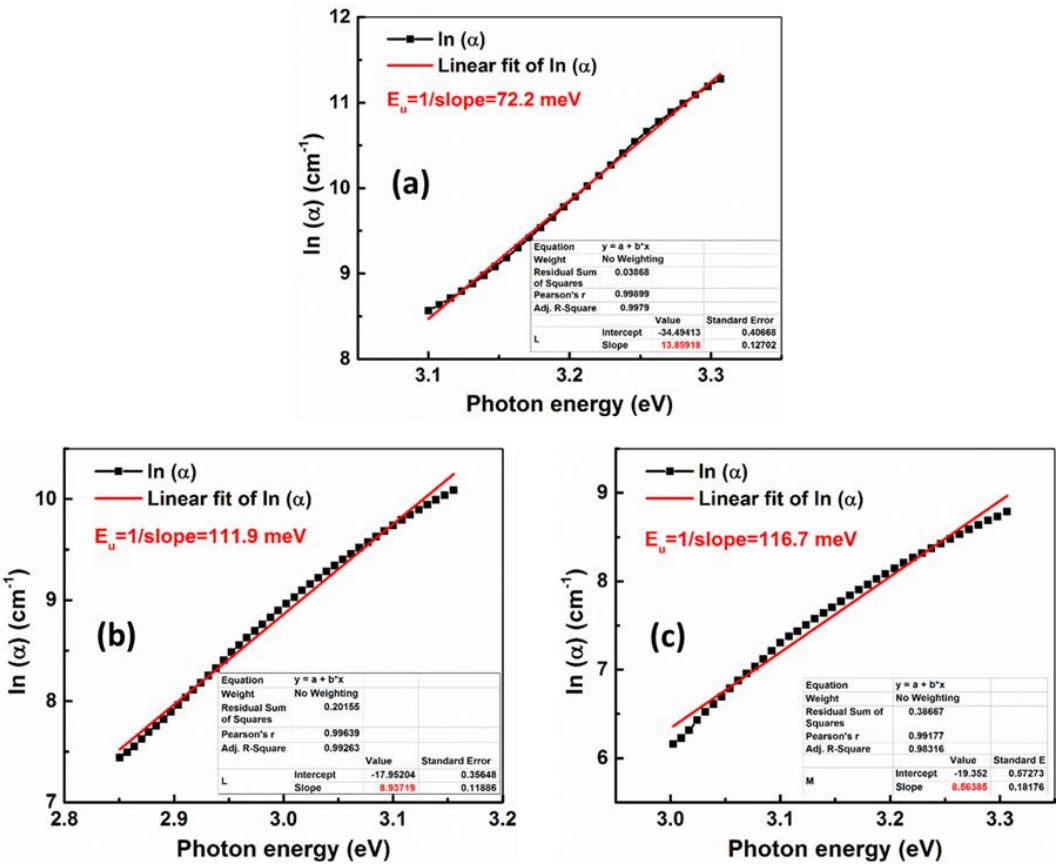

Figure 2-11: Plot of ln(α) versus incident photon energy near the fundamental absorption edge of (a) pc-ZnO, (b) hp-ITZO and (c) a-IGZO thin films. The Urbach energy is extracted from the reciprocal of the fitted straight line's slope.

Apart from the energy band diagram, both shallow and deep sub-gap states could be further figured out as well. The shallow sub-gap states in multicomponent MO semiconductors mainly belongs to tail states near the VBM and the CBM. They are related to the disordered

arrangement of atoms. To identify the degree of atomic disorder in the hp-ITZO thin films, the Urbach energy (E_U), as an indicator of tail states, was optically extracted from the absorption spectrum according to the empirical Urbach relation,

$$\alpha = \alpha_0 \exp(\frac{h\nu - E_I}{E_U}), \tag{2-10}$$

where α_0 and E_I are constant. Fig. 2-11 describes ln(α) as a function of hν near the fundamental absorption edge of the MO thin films, where E_U is equal to the reciprocal of the fitted straight line's slope. For the hp-ITZO thin films, the extracted E_U is 111.9 meV, which is well situated between the value of pc-ZnO (experiment: 72.2 meV; reference [79, 80]: 75~120 meV) and the value of a-IGZO (experiment: 116.7 meV; reference [81, 82]: 124~240 meV). It is suggested that the atoms in the hp-ITZO thin films are better organized compared to those in their amorphous counterparts. This indicates fewer shallow sub-gap states (band tail states) and contributes to less n_T. Referring to Eq. (2-3), it is possible to result in less deviation from μ_0 and obtain higher theoretical μ_{drift}. This phenomenon is certainly not as pronounced as that in silicon-based materials because the large s-orbitals of post-transition-metal cations are intrinsically helpful to generate fewer electron traps and relieve mobility degradation as a result of atomic disorder [9, 27, 59].

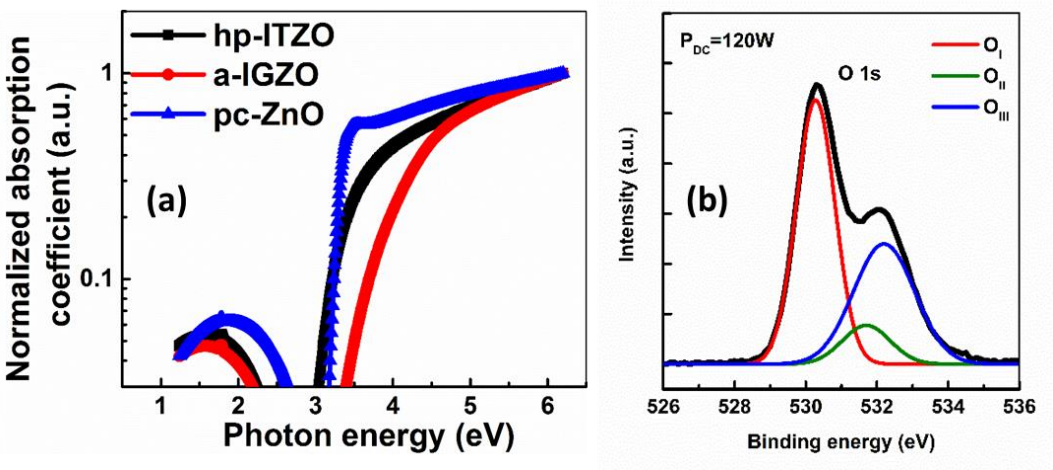

Figure 2-12: (a) Normalized optical absorption spectra of the hp-ITZO, pc-ZnO and a-IGZO thin films. (b) XPS O 1s spectra of the hp-ITZO thin films.

The deep sub-gap states mainly originate from oxygen deficiencies (oxygen vacancy (V_O) [83], weakly-bonded O^{n-} [84], and under-coordinated oxygen), M-OH bonds [85, 86], M-H bonds [87], etc. In order to identify them, the normalized optical absorption spectra of hp-ITZO, pc-ZnO and a-IGZO thin films are plotted together in Fig. 2-12(a). There exists an absorption

peak in the vicinity of 2 eV, which is related to the deep sub-gap defects in MO semiconductors [88, 89]. The deep sub-gap states in the hp-ITZO thin films are observed to be comparable to those in the a-IGZO thin films, and obviously less than those in the pc-ZnO thin films. The XPS result in Fig. 2-12(b) further confirms our analysis, because the area ratio of the oxygen-deficiency-related O_{II} peak is as small as 11.22%. It encourages the hp-ITZO thin films to achieve reliable TFTs with steep subthreshold, like a-IGZO TFTs.

Above all, it can be qualitatively concluded that the overall sub-gap states in the hp-ITZO thin films are maintained at a low level. This is very promising to realize high-performance and reliable MO TFTs.

2.3 Chapter Summary

In this chapter, hp-ITZO thin films have been successfully deposited by co-sputtering the pc-ZnO target and the pc-ITO target simultaneously at room temperature without any post-annealing treatment. In fact, the hybrid phase refers to an amorphous matrix including a number of columnar nanocrystals with blurry grain boundaries. Then, the ITZO thin films are found to reach a convincing Hall mobility peak in their hybrid phase. This is presumably attributed to the highest fraction of corner-shared InO polyhedra inside, and their long-distance chaining is helpful to form directional paths for electron percolation conduction. Afterwards, according to the simulation results, it is verified that the hybrid phase is indeed a possible solution to break through the upper mobility limit in the a-ITZO thin films. Moreover, the energy band diagram of the hp-ITZO thin films is then identified through the optical characterizations. When aligned with SiO_2, the hp-ITZO thin films can form the balanced and high potential barriers at the CBM and the VBM, and hence block electron and hole trapping. In addition, the overall (including both shallow and deep) sub-gap state density of the hp-ITZO thin films is found to maintain a low level, which is comparable to that in the a-IGZO thin films. Therefore, the hp-ITZO thin films should be very promising as TFT channels to realize high-performance and reliable devices.

Chapter 3 Bottom-Gate Top-Contact Thin-Film Transistors with Hybrid-Phase Indium-Tin-Zinc Oxide Channel Layers

Apart from merits such as high mobility, low off-state current, excellent optical transparency, and low manufacturing temperature, a-Si:H TFT process compatibility is another attractive advantage of the MO TFTs. Current FPD manufacturers can save a large amount of extra investment when their a-Si TFT-based production lines switch to MO TFT technology. Bottom-gate top-contact (BG-TC, or inverted staggered) structures, which have been employed for the mass production of a-Si:H TFTs, are also widely used for the MO TFTs.

To evaluate whether designed MO semiconductors are appropriate for TFT channels, it is compulsory to examine their performance in practical devices because other TFT components and fabrication processes may significantly affect the MO channels. From the perspective of researchers, successful implementation of TFTs with reasonable device parameters is a prerequisite. For rapid examination, the BG-TC devices commonly choose a lift-off or even shallow-mask technique to pattern their S/D electrodes. Then, the vulnerable amphoteric MO channels can be well protected. In this chapter, we first follow this approach to confirm the feasibility of hp-ITZO thin films as TFT channels and to determine their optimal deposition conditions.

The lift-off technique is, however, inapplicable to mass production. The mainstream BG-TC MO TFTs in industry are based on either etch-stopper (ES) type or back-channel-etched (BCE) type, where their S/D electrodes are patterned via direct wet or dry etch. Due to one photolithography step removal and a smaller device footprint, the BCE-type TFTs should have been more popular than the ES-type counterparts. However, they often suffer from severe characteristic and reliability deterioration because currently most of the S/D electrode patterning processes are harmful to the MO channels. Therefore, it is of high value to further optimize this step for the BCE-type MO TFTs. In the rest of this chapter, we focus on the implementation of the BCE-type hp-ITZO TFTs with high and reliable performance.

3.1 Bottom-Gate Top-Contact Thin-Film Transistors Using a Lift-Off Technique

3.1.1 Fabrication Process

The basic process flow is shown in Fig. 3-1. Herein, thermally grown SiO_2 is employed as

the gate insulator with fewer defects. This could help us to ignore negative impact from gate insulators as much as possible, and exclusively investigate the influence of different channels on device electrical performance. The whole fabrication process started on 4-inch heavily doped n-type silicon (n++) wafers, which were coated by 120-nm-thick thermally grown SiO_2. After back-side oxide removal in a buffered oxide etchant (BOE) solution, the exposed n++ silicon would serve as the gate electrodes. Then, 50-nm-thick channel layers were deposited on the substrates through magnetron co-sputtering the pc-ITO target and the pc-ZnO target at room temperature. The pc-ITO target was connected to a DC power supplier, whereas the pc-ZnO target was sputtered using an RF power supplier. The distance between substrates and targets was 10 cm. The base pressure and working pressure in the chamber were pumped to 5×10^{-6} Torr and 3×10^{-3} Torr, respectively. During deposition, the total gas flow rate was 20 sccm, and the RF power (P_{RF}) was fixed at 150 W. To investigate the influence of oxygen partial pressure ratio (P_{O2}) ($P_{O2}=O_2/(Ar+O_2)$) on the devices, the DC power (P_{DC}) was set to 120 W, and the O_2 flow rate was tuned from 2 sccm to 12 sccm. Accordingly, P_{O2} would vary from 10% to 60%. To study the influence of P_{DC} on the devices, P_{O2} was kept at 40%, and P_{DC} was configured from 60 W to 90 W, 120 W and 150 W. Next, the channels were patterned into active islands using conventional photolithography and etched in diluted hydrofluoric acid. The channel width and length were defined as 90 μm and 45 μm, respectively. After photoresist stripping, a lift-off method was performed to form 150-nm-thick sputtered aluminum S/D electrodes. Finally, the devices were subjected to thermal annealing at 300 °C in air.

The electrical characteristics of the TFTs were measured in a dark probe station using a semiconductor parameter analyzer (Agilent 4156C). In addition, an XRD system (PANalytical Empyrean) with Cu Kα radiation was used to detect the crystal morphology of the channels. It was operated in thin-film mode, and the angle between the X-ray and thin film surface was set to 0.5°. To analyze the element composition and chemical states of oxygen, an XPS measurement was conducted on a Physical Electronics 5600 multi-technique system. For precise detection, the surface 5-nm-thick thin films were etched using Ar ions before XPS characterization. The channel resistivity was measured using a four-point-probe system (Lucas Pro4-640R).

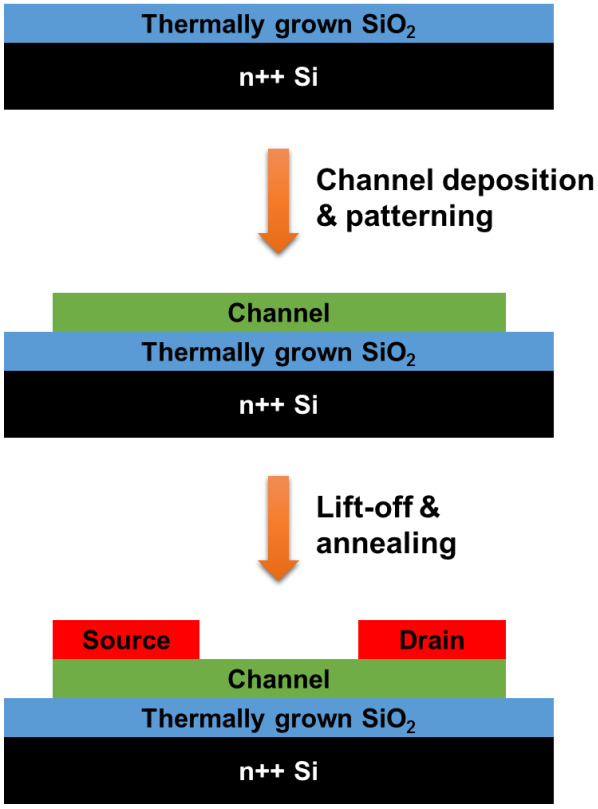

Figure 3-1: Process flow of the BG-TC hp-ITZO TFTs using the lift-off technique.

3.1.2 Impact of Oxygen Partial Pressure Ratio

It is known that V_O is closely associated with carrier capture/release, and hence electrical conductivity of MO thin films. It is believed that the concentration of V_O can be effectively controlled by modulating P_{O2} during the sputtering process [90]. To make the relationship between P_{O2} and V_O in the hp-ITZO channels clearer, XPS characterization was employed to analyze the chemical states of oxygen in the deposited thin films. As plotted in Fig. 3-2(a)-(d), the XPS spectra of the O 1s peak are divided into three peaks, O_I, O_{II}, and O_{III}, and further fitted by Gaussian Lorentzian deconvolution. Theoretically, the O_I, O_{II}, and O_{III} peak is relevant to oxygen atoms bonded in lattices (In-O, Sn-O and Zn-O), oxygen deficiencies in lattices (such as V_O), and chemisorbed oxygen atoms (such as the bonded oxygen atoms in hydroxyl groups) or excess oxygen atoms (such as oxygen interstitials), respectively [91-93]. These peaks are centered at 530.2 ± 0.1 eV, 531.5 ± 0.2 eV, and 532.2 ± 0.1 eV, respectively.

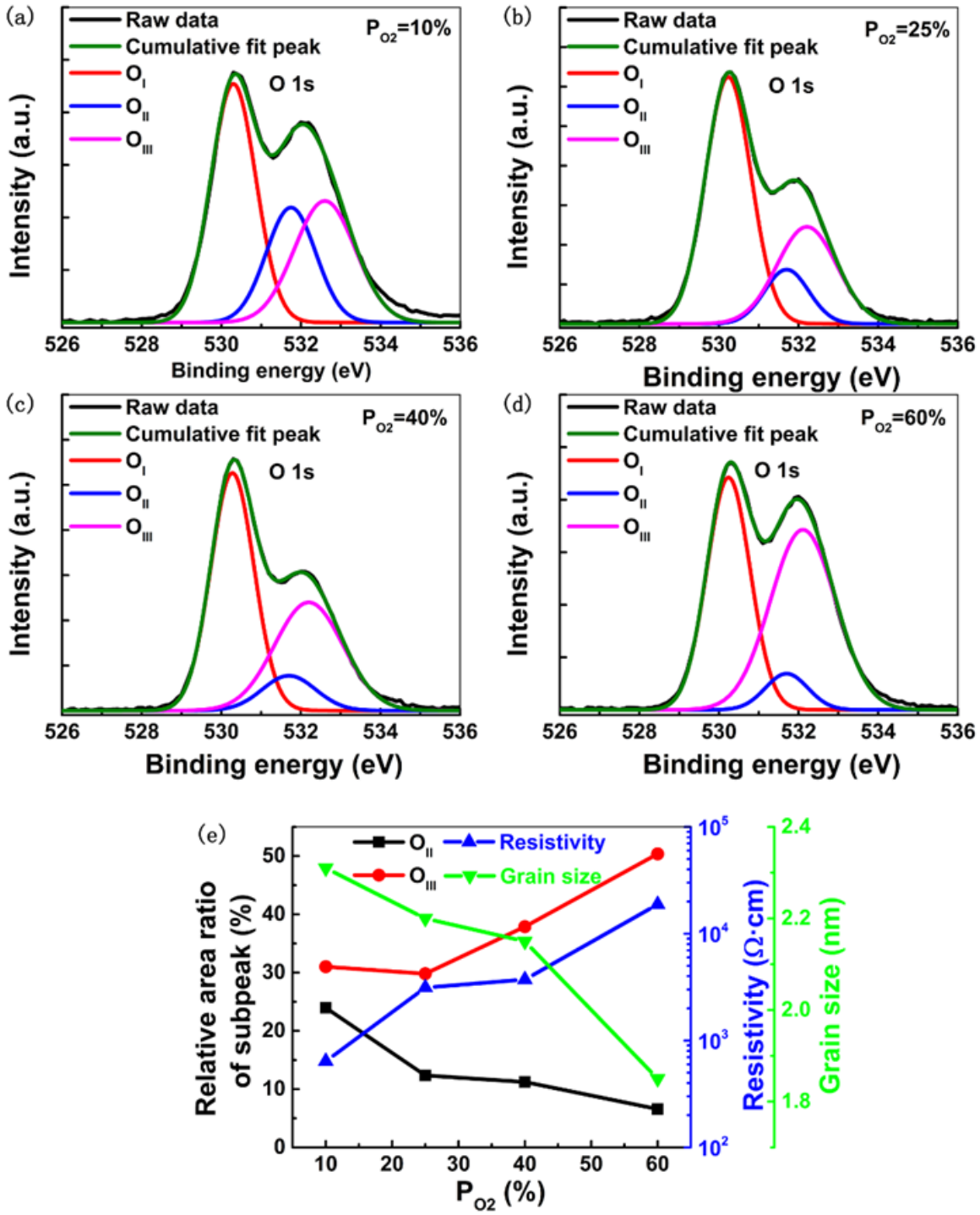

Figure 3-2: XPS O 1s spectra of the hp-ITZO channels deposited with a P_{O2} of (a) 10%, (b) 25%, (c) 40%, and (d) 60%. (e) Plot of the relative area ratio of subpeaks, thin film resistivity and grain size as a function of P_{O2}.

Fig. 3-2(e) exhibits that the relative area ratio occupied by the O_{II} peak gradually reduces with the rise of P_{O2} from 10% to 60%, while the ratio occupied by the O_{III} peak increases monotonically. It reveals that P_{O2} and V_O concentration maintains a negative correlation.

Meanwhile, the thin film resistivity is found to climb by nearly two orders of magnitude. This is because V_O acts as a donor-like defect and contributes to electron release. A higher P_{O2} can compensate a greater portion of V_O and regulate the free carrier concentration in the thin films towards a lower level [90, 94]. This is beneficial to suppress more V_O-related traps and build enhancement-mode TFTs with a lower off-state current. Fig. 3-2(e) also shows that the average XRD-derived grain size shrinks by about 20% (from 2.31 nm to 1.85 nm) when P_{O2} rises from 10% to 60%. Some plausible explanations for this phenomenon are provided as follows. 1) When P_{O2} keeps rising, it will introduce increasingly higher oxygen ion density during the sputtering process and cause severe bombardment on the as-deposited thin films. Then, the internal nanocrystals may be deteriorated, or at least their growth process may be restrained [95-97]. 2) The originally sputtered crystal nuclei from the pc-ZnO and the pc-ITO targets are complex and contain different species with diverse orientations. Although more oxygen involvement is helpful for crystal nucleus expansion, their mutual growth competitions also intensify at the same time, so a phenomenon of grain size shrinkage can be observed instead. Then, the atomic arrangement in the hp-ITZO thin films will become more disordered, resulting in more band tail trap states. Above all, P_{O2} should be carefully adjusted to well manage both deep V_O-related traps and shallow band tail traps in the sub-gap region.

The electrical performance of the hp-ITZO TFTs under different P_{O2} was further examined. As shown in Fig. 3-3, their electrical characteristics are dramatically improved when P_{O2} grows from 10% to 25%. Notably, V_{th} remarkably shifts from -35.85 V to -0.75 V, reflecting that a large amount of V_o are compensated and the free carrier concentration drops dramatically. This is consistent with the significant decrease of the relative area ratio of the O_{II} peak [94]. When P_{O2} further climbs from 25% to 60%, the relative area ratio will decrease more slowly, and the positive shift of V_{th} will become very slight. This indicates that the oxygen compensation effect approaches its saturation leading to a persistently low free carrier concentration. This offers quite a wide process window (P_{O2} from 25% to 60% or above), which is of high value in industry. Then, the field-effect mobility (μ_{fe}) with different P_{O2} is derived according to the equation as follows:

$$\mu_{fe} = \frac{Lg_m}{WC_{OX}V_{ds}}, \tag{3-1}$$

where L, W, g_m, C_{ox}, and V_{ds} denotes the channel length, channel width, transconductance, gate insulator capacitance per unit area, and drain voltage (0.1 V), respectively. It is found that μ_{fe} can reach the maximum at P_{O2}=10%, where the channels also have the highest free carrier

concentration considering the extremely negative V_{th}. This is well consistent with the theory of percolation conduction. With the further rise of P_{O2}, μ_{fe} will drop but will remain high. This is probably attributed to the well-defined electron percolation conduction paths, which are formed by the long-distance chaining of InO (and SnO) polyhedra in the channels. As a result, lower n_T and higher μ_0 in Eq. (2-3) can be provided. Additionally, a higher P_{O2} is also found to be accompanied with steeper SS. This is reasonable because the internal oxygen vacancies are gradually anhilated and this contributes to less trap states in the channel bulks. Over all, we would like to fix the optimal P_{O2} at 40%.

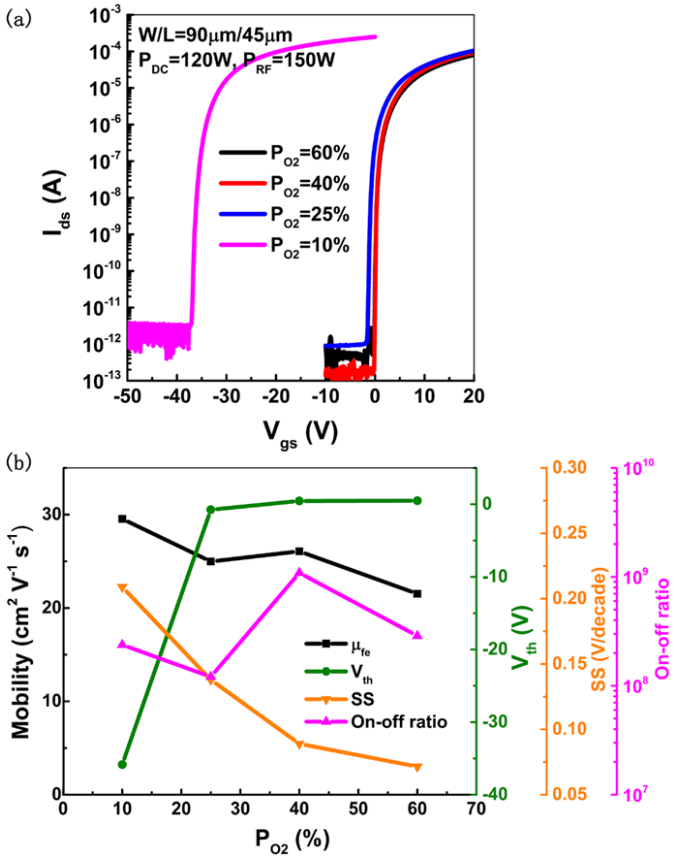

Figure 3-3: (a) Transfer curves and (b) key electrical parameters of the BG-TC hp-ITZO TFTs using the lift-off technique versus P_{O2} during channel sputtering.

3.1.3 Impact of Direct-Current Sputtering Power

Table 3-1 lists several typical parameters of the channel layers under different P_{DC} for pc-ITO sputtering. These parameters are directly related to the element composition and the crystal morphology of the channels. In this subsection, P_{RF} is always fixed at 150 W, while P_{DC} will vary from 60 W to 150 W. With the rise of P_{DC}, it is found that the grain size as well as the total ratio of post-transition-metal cations (In+Sn)/(In+Sn+Zn) keep increasing. However, the

latter shows much more drastic variation compared with the former one. It is believed that P_{DC} may affect the element composition more than the crystal morphology. In principle, the electron conduction band of a-IGZO is composed of the delocalized 5s orbitals of indium cations [27]. Similarly, both indium and tin cations with large 5s orbitals can also contribute to electron transport in the hp-ITZO channels. Therefore, P_{DC} should be one of key sputtering parameters to significantly affect device electrical characteristics.

Table 3-1: Element composition and crystal-morphology-related parameters of the hp-ITZO thin films under different P_{DC}

P_{DC} (W)	60	90	120	150
Grain size (nm)	1.97	2.15	2.26	2.38
In/(In+Sn+Zn) (%)	18.9	33.4	38.6	46.7
Sn/(In+Sn+Zn) (%)	1.3	2.3	2.7	3.3
Zn/(In+Sn+Zn) (%)	79.8	64.3	58.7	50.0
(In+Sn)/(In+Sn+Zn) (%)	20.2	35.7	41.3	50.0
ITO deposition rate (nm/min)	2.03	3.6	4.4	5.1
ZnO deposition rate (nm/min)		3		

Fig. 3-4 present the electrical performance of TFTs under different P_{DC}. It is found that all the key electrical parameters of the devices are improved qualitatively when P_{DC} is boosted from 60 W to 90 W. Within the same range, the pc-ITO deposition rate (from 2.0 nm/min to 3.6 nm/min) begins to surpass the pc-ZnO deposition rate (3.0 nm/min), as shown in Fig. 3-5. Such consistency indicates that the content of pc-ITO can significantly affect electron transport properties in the channels [51, 75]. If the total fraction of indium and tin cations is insufficient, the electron percolation conduction paths built by their 5s orbital overlaps will remain disconnected (Fig. 3-6(a)). Only if the fraction surpasses a critical ratio, the basic framework for electron transport can be well defined. One of the advantages brought by the corner-shared InO polyhedra is that the required critical ratio of post-transition-metal cations should be lower (Fig. 3-6(b) and (c)). Herein, the critical ratio is found to be between 20.2% and 35.7%. When P_{DC} climbs from 90 W to 150 W, the further rise of indium and tin cation ratio will still bring mild improvement to the devices. However, it does not mean that over high P_{DC} is acceptable. Firstly, indium cations can substitute zinc cation sites and then release electrons, resulting in

more negative V_{th} [98, 99]. This is indeed observed in Fig. 3-4(b) when P_{DC} climbs from 90 W to 150 W. On the other hand, higher P_{DC} will reduce the utilization efficiency of indium cations and increase raw material cost. This is not friendly to low-cost electronics. According to Table 3-1, it should be ZnO that occupies the majority in the hp-ITZO channels. Nevertheless, P_{DC} needs to be well modulated together with other deposition parameters such as P_{O2} and P_{RF}. Herein, the P_{DC} is set in the vicinity of 120 W.

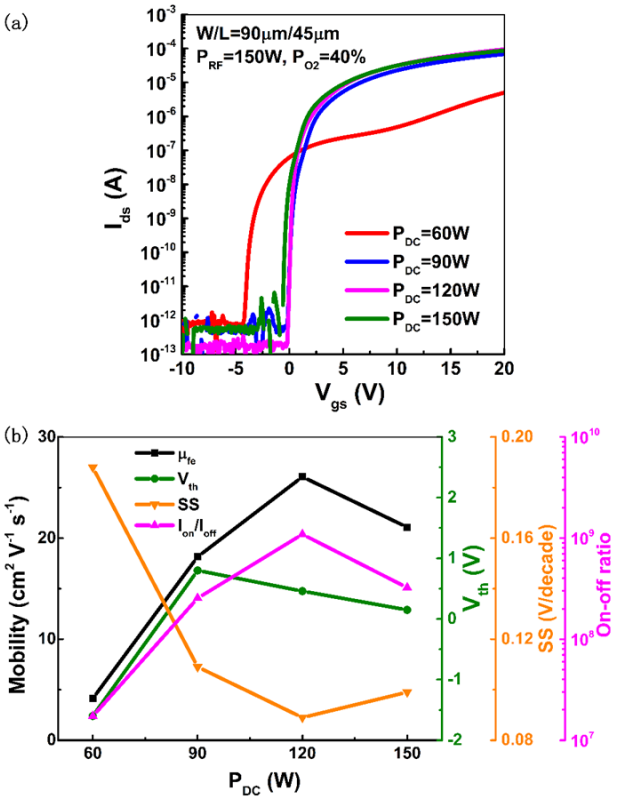

Figure 3-4: (a) Transfer curves and (b) key electrical parameters of the BG-TC hp-ITZO TFTs using the lift-off technique versus P_{DC} during channel sputtering.

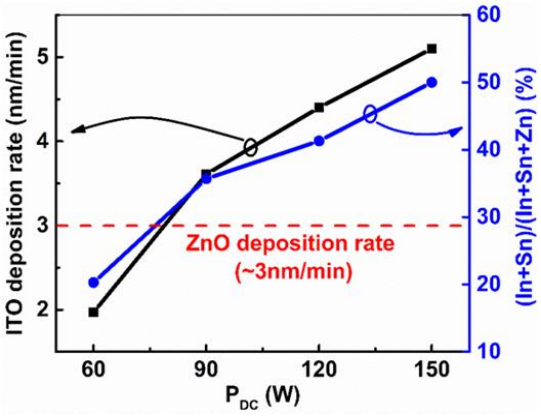

Figure 3-5: Deposition rate of pc-ITO and post-transition-metal cation ratio as a function of P_{DC}. As a reference, pc-ZnO deposition rate at P_{RF}=150 W is plotted.

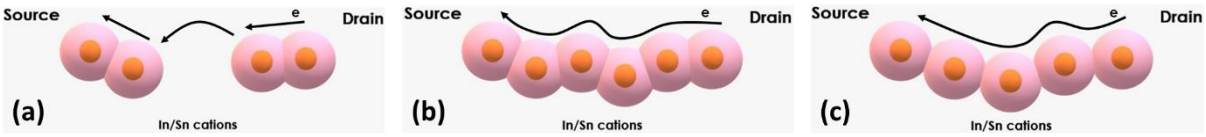

Figure 3-6: Illustration of electron percolation conduction path that is formed by 5s orbitals of indium and tin cations. (a) Disconnected path with insufficient cations, (b) well-defined path mainly formed by edge-/face-shared polyhedra with sufficient cations, and (c) well-defined path mainly formed by corner-shared polyhedra with sufficient cations.

3.1.4 Optimal Device Characterizations

Referring to the co-sputtering conditions above, the optimal BG-TC TFTs using the lift-off technique can be fabricated by setting P_{O2} at 40% and P_{DC} at 120 W. The XRD spectrum in Fig. 3-7 confirms the existence of the hybrid-phase in the ITZO channels, and the derived grain size is around 2.15 nm on average. The XPS results show that the fraction of indium, tin, and zinc cations in the channels is 38.6%, 2.7%, and 58.7%, respectively. The transfer and output curves of the optimal devices are plotted in Fig. 3-8(a) and (b). Their extracted μ_{fe}, V_{th} and on/off ratio can typically reach 27.3 cm^2/Vs, 0.5 V and over 10^9, respectively. In addition, the value of SS is as low as 89 mV/decade. This means that the total trap density (n_{total}) in the channel bulks and at the GI/AC interfaces is maintained at a relatively low level, which is only 2.67×10^{11} cm^{-2} eV^{-1}. The relationship between N_{total} and SS fulfills the following equation:

$$SS = \frac{qk_BTn_{total}}{C_{OX}\log(e)}, \tag{3-2}$$

where q, k_B, T and C_{ox} is the electron charge, Boltzmann's constant, absolute temperature and gate insulator capacitance per unit area, respectively [41, 100].

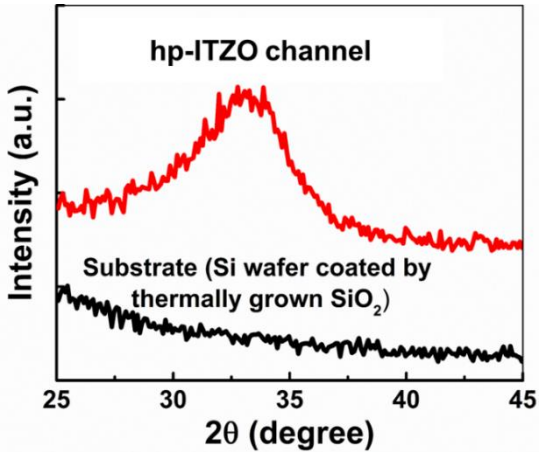

Figure 3-7: XPD spectrum of the hp-ITZO channel in practical TFTs.

Fig. 3-9 plots μ_{fe} as a function of V_{gs}. The trend is quite similar to the case of a-IGZO [6]. At low gate bias, the trap-limited conduction prevails. The abrupt increase of μ_{fe} reflects a low level of carrier traps, which can be filled rapidly [101]. At medium gate bias, the percolation conduction becomes dominant. The average potential barrier height and variance will be weakened with the increase of gate bias, and more induced carriers can lead to a higher μ_{fe}, but the rising rate becomes mild. At high gate bias, μ_{fe} starts to drop off, and this is related to the intensive carrier scattering. From the output curves, a current crowding effect at low drain voltage is still observed, indicating imperfect contacts in the S/D regions. Thus, future work is needed to further promote the S/D contacts.

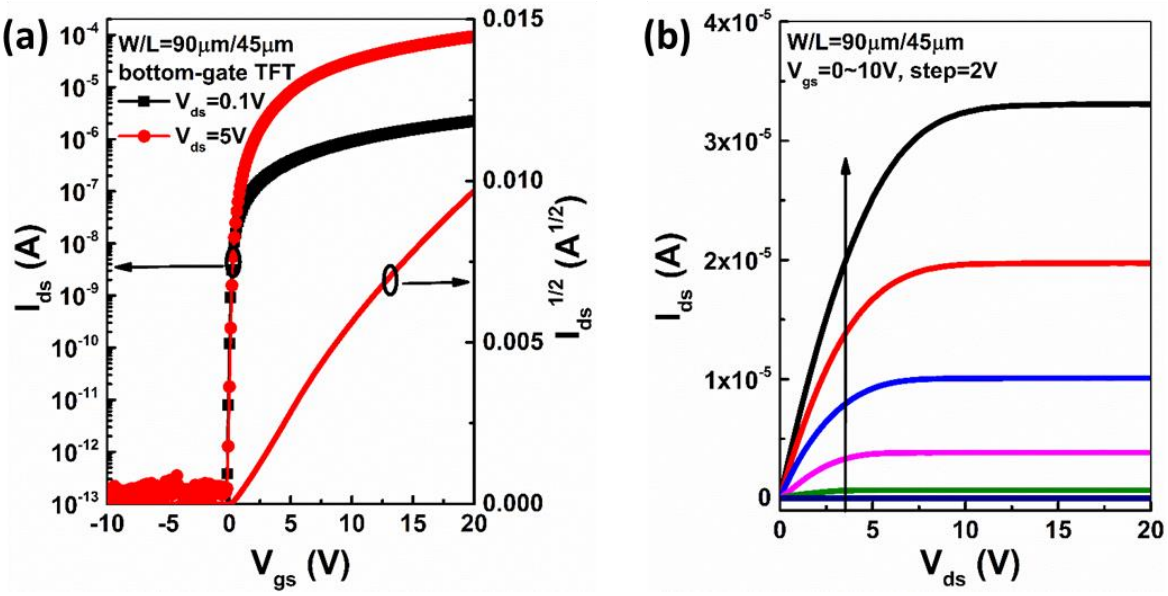

Figure 3-8: (a) Transfer curves and (b) output curves of the optimal BG-TC hp-ITZO TFTs using the lift-off technique.

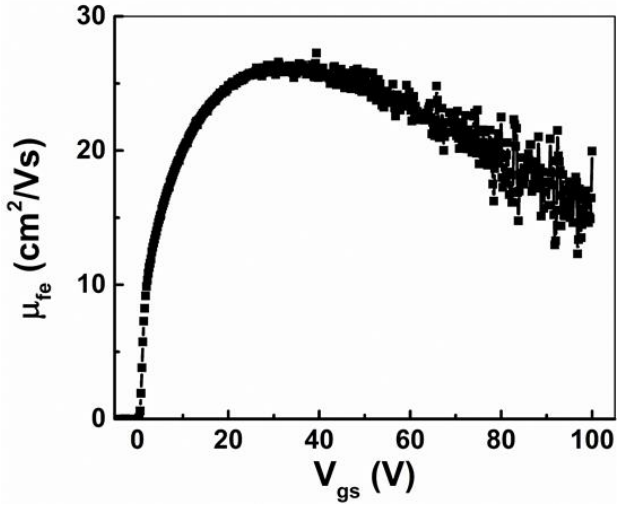

Figure 3-9: Plot of μ_{fe} as a function of gate bias.

The devices were also measured at different temperature, and the Arrhenius plot of μ_{fe} versus the reciprocal of the temperature is plotted in Fig. 3-10. With a simple Arrhenius analysis

$$\mu_{fe} = \mu_{fe0} \exp(-\frac{E_{act}}{kT}), \tag{3-3}$$

we can extract the intrinsic mobility μ_{fe0} and activation energy E_{act} of the mobility, and the results is 33.9 cm^2/Vs and 3.59 meV, respectively. Compared with a-IGZO (5 meV) [102] and a-ITZO (3.8 meV) [103] thin films, the hp-ITZO thin films show lower activation energy. It indicates a steeper tail-state distribution near the CBM as well as a lower average potential barrier height and variance above the CBM [101]. As mentioned in Chapter 2, the presumable explanation is that there is a larger portion of corner-shared InO (and SnO) polyhedra in the hp-ITZO thin films, and then they will participate in the long-distance chaining for directional electron percolation conduction paths.

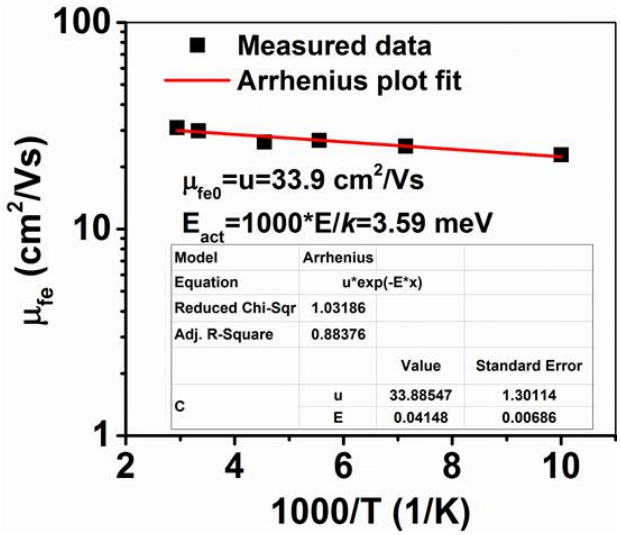

Figure 3-10: Arrhenius plot of μ_{fe} versus the reciprocal of the temperature.

Table 3-2: Comparison of our hp-ITZO TFTs with some MO TFTs published in recent years

Channel composition	Crystal morphology	(In+Sn)/(In +Sn+Zn)	Gate insulator	μ_{fe} (cm^2/Vs)	V_{th} (V)	SS (decade/V)	On-off ratio	Reference
ITZO	hybrid-phase	41.3%	SiO_2	27.3	0.5	0.089	$>10^9$	This work
ITZO	amorphous	>66.7%	Yb_2TiO_5	27.9	0.52	0.203	1.1×10^8	[104]
ITZO	amorphous	N/A	SiO_2	27.59	-0.93	0.153	$\sim10^9$	[105]
ITZO	amorphous	>65%	$Al_2O_3/SiO_x/SiO_2$	31.08	0.28	0.096	$\sim10^7$	[106]
ITZO	amorphous	>65%	SiO_2	21.67	2.46	0.568	—	[107]

IGZO	amorphous	>33.4%	SiO_2	10.1	-2.2	0.171	$>10^9$	[108]
IGZO	amorphous	>40%	SiO_2	11.5	0.2	0.27	$>10^9$	[109]
IGZO	c-axis aligned crystalline	>33.4%	—	7.7	0.79	0.109	$>10^{19}$	[110]
IZO	amorphous	~40%	SiO_2	26.5	2	0.24	10^{10}	[29]
IZO	amorphous	>67%	P-doped SiO_2	~18	-0.12	0.13	1.5×10^6	[111]
ZnO	polycrystalline	0	HfO_2	1.4	0.9	0.089	7.1×10^8	[112]
ZnO	polycrystalline	0	Al_2O_3	21.9	4.1	0.244	4×10^8	[113]
ZnO	polycrystalline	0	Al_2O_3	12	-1.2	0.3	$\sim10^8$	[114]
ITO	amorphous	100%	Ta_2O_5	29.0±1.2	1.05±0.28	0.2	$>10^8$	[115]
ITO	amorphous	100%	Al_2O_3	56.1	0.7	0.14	$\sim10^9$	[54]

Table 3-2 lists the key electrical parameters of our hp-ITZO TFTs as well as some MO TFTs, which have been reported in recent years. It should be noted that the listed atomic ratios of post-transition-metal cations in a-ITZO channels are based on those in their sputtering targets. According to ref. [116, 117], the sputtering yield of Zn is generally lower than that of In and Sn, so the total atomic ratio of In and Sn cations in the a-ITZO channels should be higher. Compared with the a-ITZO TFTs, our hp-ITZO devices have competitive mobility but with a lower atomic ratio of post-transition-metal cations thanks to a greater proportion of corner-shared InO polyhedra. It enables higher utilization efficiency of indium cations for lower material cost. In addition, the value of SS and the on-off ratio are among the best that have ever been reported. This is because the overall sub-gap states in the hp-ITZO channels are maintained at a relatively low level as mentioned in Chapter 2. When compared to the IGZO TFTs, no matter whether their channels are amorphous or crystalline, our hp-ITZO TFTs can present obviously higher mobility and hence more efficient utilization of post-transition-metal cations for lower material cost. Moreover, in comparison to the pc-ZnO and pc-ITO TFTs, the electrical performance of our devices in this work are also very attractive.

Next, the spatial uniformity of the hp-ITZO TFTs was examined. Fig. 3-11 describes the key electrical parameters of 30 devices, which are uniformly distributed over a 4-inch circular substrate. Apart from enhanced device behaviors, it is clearly seen that all the parameters can fluctuate within a narrow range. Particularly, the relative standard deviation (RSD) of μ_{fe} and SS is only 3.1% and 8.2%, respectively. It can be concluded that the hybrid phase is able to well maintain the spatial electrical uniformity of devices. This is because the sparse nanocrystals inside the thin films are ignorable, especially when they are compared with the

micrometer-scaled TFT channels. Therefore, it is certain that the hp-ITZO TFTs are compatible with large-area applications.

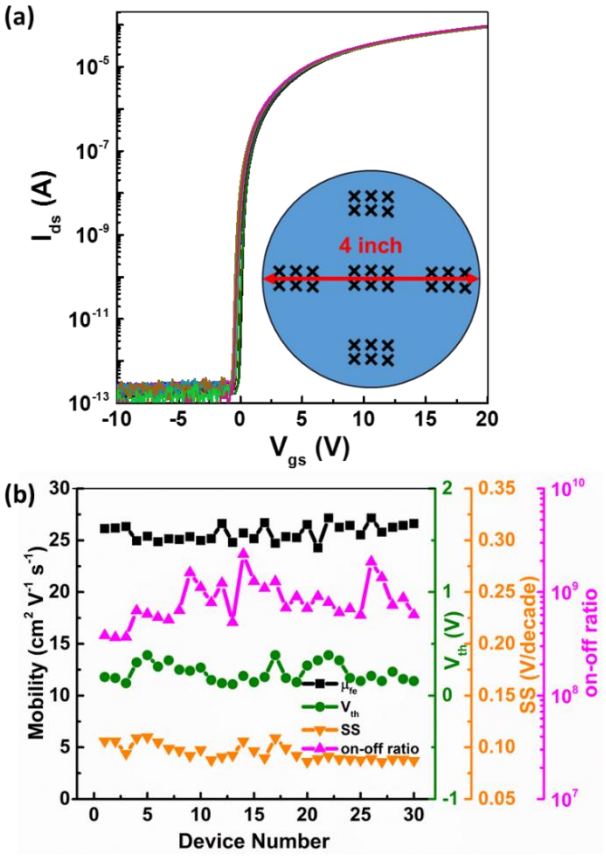

Figure 3-11: (a) Transfer curves of 30 devices that are uniformly distributed over a 4-inch circular wafer. (b) Statistical diagram of key electrical parameters of the devices.

Furthermore, the BG-TC hp-ITZO TFTs exhibit their robustness to ambient air. For many ZnO-based devices, there generally exists strong interactions with the ambient oxygen and moisture molecules at their exposed surface, especially at the grain boundaries of pc-ZnO. The ambient chemisorption effects are always accompanied by electron capture/release and trap state generation/annihilation, resulting in severe ambient instability and a very short shelf life [93, 118, 119]. However, Fig. 3-12 illustrates that the hp-ITZO TFTs without any passivation can operate normally, with only a small V_{th} fluctuation even after storage in the atmospheric environment (relative humidity is 50% and temperature is 25 °C) for 10 weeks. It is observed that the V_{th} of the as-fabricated devices drops sharply from about 0.5 V to below zero after half a day, and then its value fluctuates within a narrow range. The ambient interactions seem to achieve a dynamic equilibrium eventually. In addition, there is no stretch-out phenomenon observed in the subthreshold region of the transfer curves, and the extracted SS always stays around 0.1 V/decade. This means few defects are created during this period. Compared with

other pc-ZnO [120, 121] and a-IGZO TFTs [122], which deteriorate significantly in the long term, our TFTs have robust atmospheric stability. One plausible explanation is described as follows: the polarity structure and grain boundaries where severe chemisorption effects take place in the pc-ZnO almost no longer exist in the hp-ITZO thin films. Meanwhile, a large proportion of the originally exposed zinc sites at the back-surface are screened by indium and tin cations, which are less sensitive to the adsorption/desorption of oxygen and water molecules. Then, the ambient interactions can be well suppressed, enabling *in-situ* passivation for the channels. Since the hp-ITZO thin films contain nearly 60% zinc cations, our hp-ITZO is also often called as hp ITO-stability ZnO. In this thesis, we would like to exclusively use the name "hp-ITZO" for simplicity.

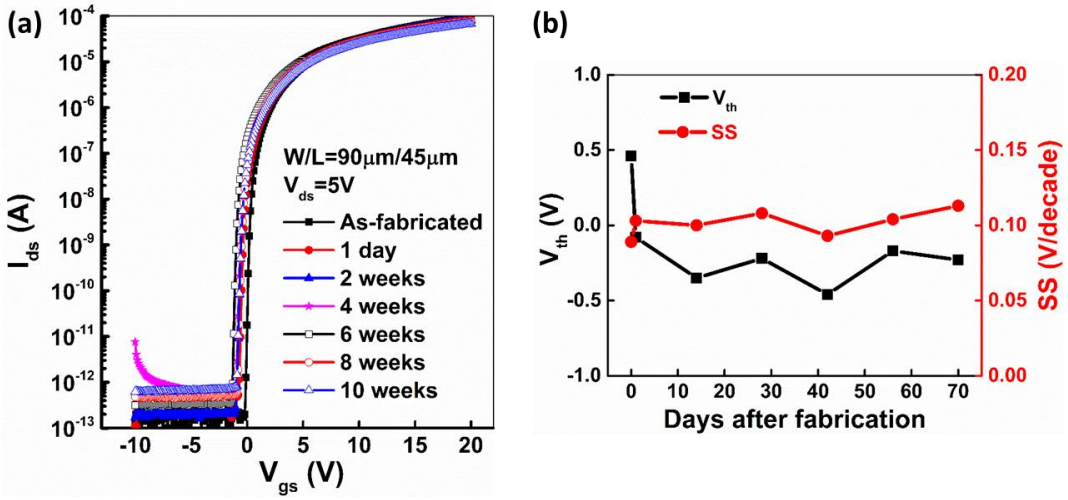

Figure 3-12: (a) Transfer curve evolution and (b) V_{th} and SS variation of devices without any passivation which are aged in ambient air for 10 weeks.

Finally, the transfer curve evolution of the BG-TC hp-ITZO TFTs using the lift-off technique under repeated cycling tests is shown in Fig. 3-13. It is found that apart from the long shelf life, such devices also exhibit reliable repeated switching behavior, with a slight V_{th} shift of 0.8 V after 3001 sweeping cycles. This is essential in practical applications.

Above all, by adjusting P_{O2} and P_{DC}, the optimal deposition conditions for the hp-ITZO channels were able to be obtained. The corresponding TFTs exhibited high electrical performance with a typical μ_{fe} of 27.3 cm^2/Vs, V_{th} of 0.5 V, on-off ratio of over 10^9 and extremely low SS of 89 mV/decade. Meanwhile, the devices also demonstrated excellent spatial uniformity, long shelf life and satisfying repeated switching behavior. The hp-ITZO thin films are thought to be an appropriate type of TFT channel via collaborative modification in element composition and crystal morphology. In fact, the fabricated hp-ITZO TFTs present

much better performance than the pristine pc-ZnO TFTs especially in their shelf life [120, 121]. Now that the hp-ITZO channels show excellent ambient stability, it is suggested they may be also robust to fabrication processes of TFTs (e.g., BCE-type TFTs).

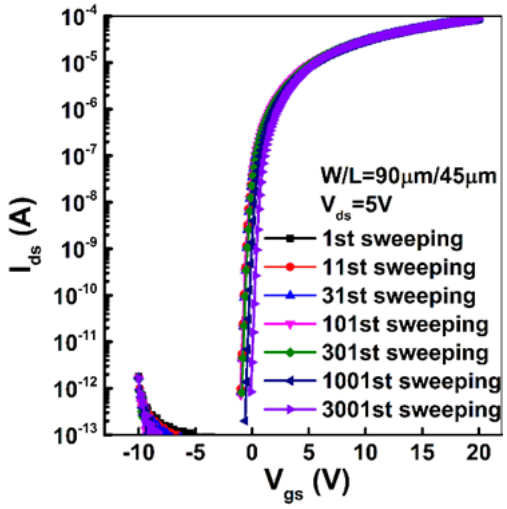

Figure 3-13: Transfer curve evolution of the devices under repeated cycling tests.

3.2 Back-Channel-Etched Thin-Film Transistors

Compared with their ES-type counterpart, BCE-type TFT technology is intrinsically able to save photolithography mask counts for more cost-effective manufacturing, and also reduce parasitic capacitance and device footprint for higher-definition displays [14, 15]. However, they are also troubled by some urgent performance and reliability issues, most of which are induced by etching residues or damage during their S/D electrode etching processes [123-125].

Currently, the S/D electrodes of the BCE-type MO TFTs often employ molybdenum or molybdenum-based metal stacks (Mo/Al, Mo/Cu, etc.), which are patterned through dry etch, wet etch, or their combination. The anisotropic dry etch techniques, such as reactive ion etch (RIE), can well control the sidewall profile of S/D electrodes, but they always involve Cl- or F-based reactive gases. The residual Cl or F ions in the channels, together with back-surface plasma bombardment, will severely degrade the device performance [126, 127]. The isotropic wet etch technique is simple and low-cost, but the lateral etching of S/D patterns is inevitable. So far, there are two main types of wet etchants. One is based on HNO_3 (e.g., HNO_3 + H_3PO_4 + CH_3COOH, namely PAN). Its selectivity between the MO channels and the S/D electrodes is low, so the MO channels will be destroyed without precise process control [128, 129]. The other is based on H_2O_2 (e.g., H_2O_2 + H_2O + PH-adjustment additives, or H_2O_2 + H_2O + ammonium + azole + NH_4F, etc.). This type of etchant often introduces Mo-related residues

and surface hydroxyl groups on the back side of channels, and the tapered S/D electrode sidewall profile is poor. Despite all this, its overall etching effects are better than those of the HNO_3-based etchants [125, 129-131].

By combining wet etch and dry etch, it is possible to reduce etching residues and even repair oxygen vacancies on the back-side of channels via introducing an extra dry etch treatment after the wet etch in the H_2O_2-based etchant [124, 132]. However, this approach increases process complexity at the same time. Herein, we still adopt the wet etch method to pattern the S/D electrodes in the H_2O_2-based etchant. Via over-etch ratio control and annealing sequence adjustment, the high-performance and reliable BCE-type TFTs with the hp-ITZO channels can then be successfully fabricated.

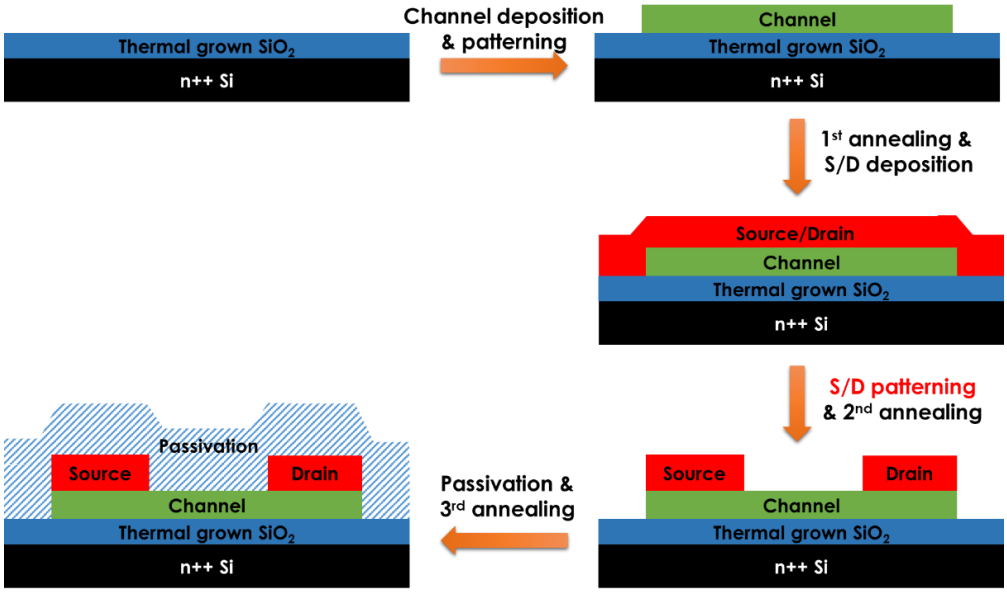

Figure 3-14: Process flow of the BCE-type hp-ITZO TFTs.

3.2.1 Fabrication Process

The entire fabrication process (Fig. 3-14) was initiated on 4-inch Si/SiO_2 wafers. The heavily n-type doped (n++) silicon substrates and the coated 100-nm-thick thermally grown silicon dioxide were regarded as the gate electrodes and the gate insulators, respectively. Next, 50-nm-thick hp-ITZO channel layers were deposited through magnetron co-sputtering the pc-ITO target and the pc-ZnO target at room temperature. The base pressure in the sputtering chamber was pumped to 5×10^{-6} Torr. During the sputtering process, the gas flow rate of Ar/O_2, working pressure, P_{DC} and P_{RF} was set to 12/8 sccm, 3 mTorr, 120 W and 150 W, respectively. After channel etching in diluted hydrofluoric (HF) acid, a portion of the samples were annealed in air at 300 °C for 2 h (1^{st} annealing), and the rest were not. Then, all the samples were covered

by 40-nm-thick Mo layers. After photolithography and hard baking, the sputtered Mo layers were patterned into the S/D electrodes in the H_2O_2-based etchant (KANTO-PPC, MAE 295 series, <10% H_2O_2 + <30% amino additive) at 35 °C. The over-etch ratio was controlled from 20% to 80%. To repair the back-channel damage caused by the wet etch process, all the devices were then annealed in air at 300 °C for 2 h (2nd annealing). Afterwards, 300-nm-thick PECVD-SiO_2 layers were deposited as passivation layers. Finally, a 3rd annealing was conducted to do dehydrogenation and electrically activate the devices. The electrical characteristics of the TFTs were measured in a dark probe station using a semiconductor parameter analyzer (Agilent 4156C).

3.2.2 Impact of Over-Etch Ratio

Theoretically, the Mo wet etch using the H_2O_2-based etchants contains at least two steps, which follow the reaction formulas as follows [129]:

$$Mo + 2H_2O_2 \rightarrow MoO_2 + 2H_2O \quad (3\text{-}3)$$

$$MoO_2 + H_2O_2 \rightarrow MoO_4^{2-} + 2H^+ \quad (3\text{-}4)$$

Herein, we define as-etched time corresponding to the consumed time when the metal luster becomes completely invisible. However, this moment does not represent the end of the wet etch, and Eq. (3-3) reveals that there are still metal oxide residues remaining on the back channels. These acceptor-like residues will severely degrade the electrical characteristics and reliability of devices [124, 132]. Therefore, over-etch treatment is compulsory for residue removal. On the other hand, too long over-etch process is unacceptable either. This is because the generated protons (H^+) will erode the amphoteric channels according to Eq. (3-4). Above all, to investigate the influence of over-etch ratio on device performance is worthwhile. If the channels are less robust to the etchants, it will be rather difficult to find a balance between two reactions and achieve the BCE-type TFTs with high and uniform performance across large area.

Table 3-3: Equivalent thickness of the etching residues with different over-etch ratios in the S/D electrode wet etch process

	Sample A	**Sample B**	**Sample C**	**Sample D**
Over-etch time (s)	30	60	90	120
Over-etch ratio (%)	20	40	60	80
Equivalent SiO_2 thickness (nm)	3.9	1.2	0.8	0.7

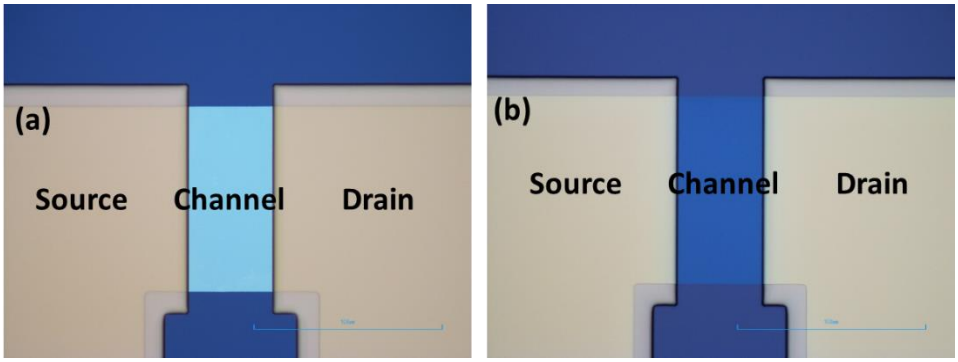

Figure 3-15: Micrographs of the channels with an over-etch ratio of (a) 60% and (b) 80%.

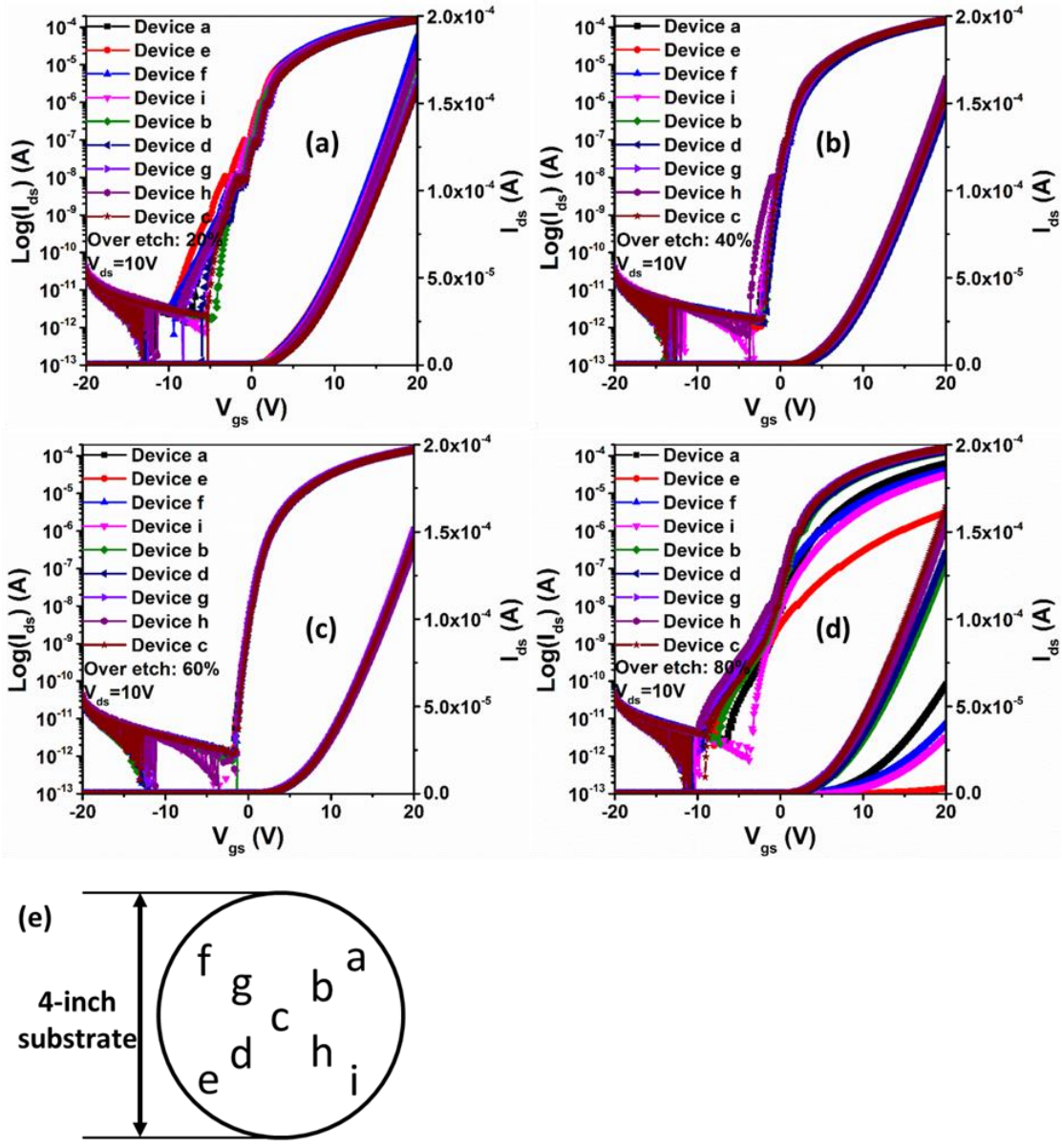

Figure 3-16: Transfer curves of the BCE-type TFTs with an over-etch ratio of (a) 20%, (b) 40%, (c) 60% and (d) 80%. (e) Illustration of tested positions across 4-inch circular substrates.

In this work, the as-etched time for the 40-nm-thick Mo layer in the 35°C H_2O_2-based

etchant is around 150 s. The over-etch time varies from 30 s, 60 s and 90 s to 120 s; thus, the corresponding over-etch ratio is 20%, 40%, 60% and 80%, respectively. Prior to the wet etch, all the samples were treated by the 1st annealing process. A Nanospec reflectometer (Nanometrics) was used to measure the etching residue thickness, which can be approximately indicated by the equivalent thickness of SiO_2. The results are listed in Table 3-3. It is found that the etching residues can be almost eliminated with a slight thickness decrease when the over-etch ratio rises from 40% to 60%. This is quite a wide process window, indicating the excellent process robustness of the hp-ITZO channels. But it does not mean that the over-etch time should be very long. Fig. 3-15 shows micrographs of the channels with an over-etch ratio of 60% and 80%. There exists obvious corrosion in the latter channel regions. This is because the reaction (Eq. 3-4) to dissolve MoO_x residues will also release H^+ ions at the same time. The more exposure to the wet etchant, the higher the portion of the back channels that will be eroded, despite the existence of pH-value stabilizers inside.

Fig. 3-16 shows the transfer curves of the BCE-type hp-ITZO devices with different over-etch ratios. The tested TFTs are distributed across the 4-inch substrates from the edge to the center, so their spatial uniformity can be examined as well. As observed, the devices become gradually uniform in terms of their electrical characteristics when the over-etch ratio increases from 20% to 60%. In particular, the transfer curves of the TFTs with an over-etch ratio of 60% are almost overlapped, and the jitter phenomenon in the subthreshold region also disappears. This is thanks to the nearly complete removal of etching residues, so that the back-channel quality can be the same from device to device. In addition, a slight reduction is observed in terms of the on-state current. This is presumably attributed to the extension of the actual channel length caused by lateral etching. Furthermore, when the over-etch ratio climbs to 80%, the devices are found to be deteriorated significantly. This is consistent with the observed channel corrosion in Figure 3-15(b). Above all, the optimal over-etch ratio should be between 40% and 60%, so that high-performance BCE-type hp-ITZO TFTs can be guaranteed with good spatial uniformity across a large area.

3.2.3 Impact of Annealing Treatment

As mentioned above, excess over-etch treatment is harmful to the TFTs due to the channel corrosion by H^+ ions in the wet etchants. However, in order to eliminate these etching residues, the back-side of channels will inevitably encounter the wet etchants. In such circumstances, it is necessary to remove the accompanying adversities as much as possible. One effective solution is to strengthen the channels before depositing the molybdenum S/D layers. After the

1st annealing treatment shown in Fig. 3-14, the channel quality can be significantly improved, and the chemical resistivity to the following wet etchant is also enhanced. According to our measurement, the etching rate for the as-deposited channels is as fast as ~17.3 nm/min, which is comparable to that of molybdenum (~16 nm/min). In contrast, the etching rate for the annealed channels decreases by more than four times (<4 nm/min). Fig. 3-17(a) is a micrograph of the unannealed channel region with an over-etch ratio of 60%. Compared with Fig. 3-15(a), this channel region has already been damaged severely, and the electrical performance of the corresponding device is also very inferior (Fig. 3-17(b)). Therefore, it is evident that the 1st annealing treatment prior to the S/D electrode patterning is highly essential as it can provide more robust channels and enlarge the process window of the wet etch process.

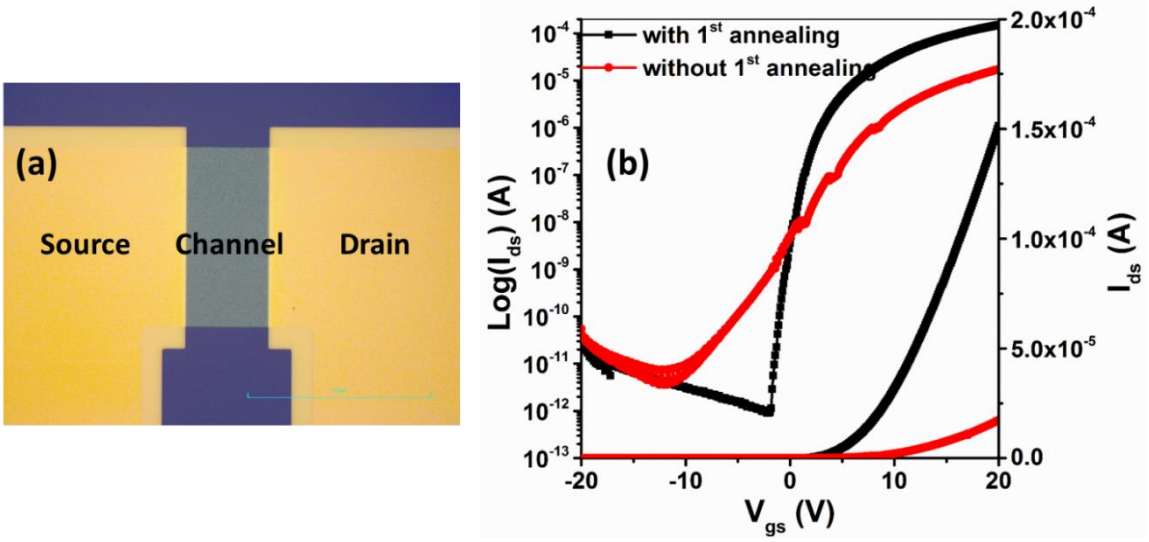

Figure 3-17: (a) Micrograph of the unannealed channel region in the BCE-type TFTs with an over-etch ratio of 60%. (b) Transfer curves of the BCE-type TFTs with and without annealing treatment prior to the S/D electrode patterning.

3.2.4 Optimal Device Characterizations

Through optimizing the over-etch ratio for the molybdenum S/D electrode patterning, and carrying out thermal annealing treatment prior to that, the BCE-type hp-ITZO TFTs can be fabricated with good electrical performance. The corresponding transfer and output curves are plotted in Fig. 3-18. The devices exhibit a typical μ_{fe} of 23.4 $cm^2/V \cdot s$, V_{th} of 0.7 V, on-off ratio of over 10^8, and SS of 0.289 V/decade. Compared with the previous BG-TC TFTs using the lift-off technique, the BCE-type devices herein show worse SS and on-off ratio (or higher off-state current). Since the main difference between these two kinds of devices is the technique used for their S/D electrode patterning, it is believed that performance degradation originates

from the etching residues and damage, as reported by [124, 132]. Therefore, more optimization work in this respect needs to be carried out in the future. From the output curves, there is little current crowding effect observed at low drain voltage. This indicates the good ohmic contact between the S/D electrodes and the hp-ITZO channels.

Fig. 3-19 shows the reliability of devices against gate-bias stress. The V_{ds} for sweeping is 5 V, and the applied V_{gs} for positive gate-bias stress (PBS) and negative gate-bias stress (NBS) is set to (V_{th}+20) V and (V_{th}-20) V, respectively, for 10 000 s. In the subthreshold region, there is no stretch-out phenomenon for either cases, indicating few defects are generated during the stress tests. However, the contacts between the S/D electrodes and the channels deteriorate, resulting in on-state current reduction. The threshold voltage shift in the PBS test is found to be slight, while the threshold voltage negatively shifts about 1 V in the NBS test. This reveals that there may exist electron (acceptor-like) traps at the back-channel interface between the channel and the passivation layer. These acceptor-like traps are mainly offered by the etching residues. When negative gate-bias stress is applied, electrons will move towards the back-channel interface and get trapped. These trapped electrons can build a negative potential at the back-channel interface and repel the remaining electrons towards the front-channel interface, leading to a negative threshold voltage shift. Therefore, improvement work is required to eliminate the etching residues and cancel as many electron traps as possible in the future.

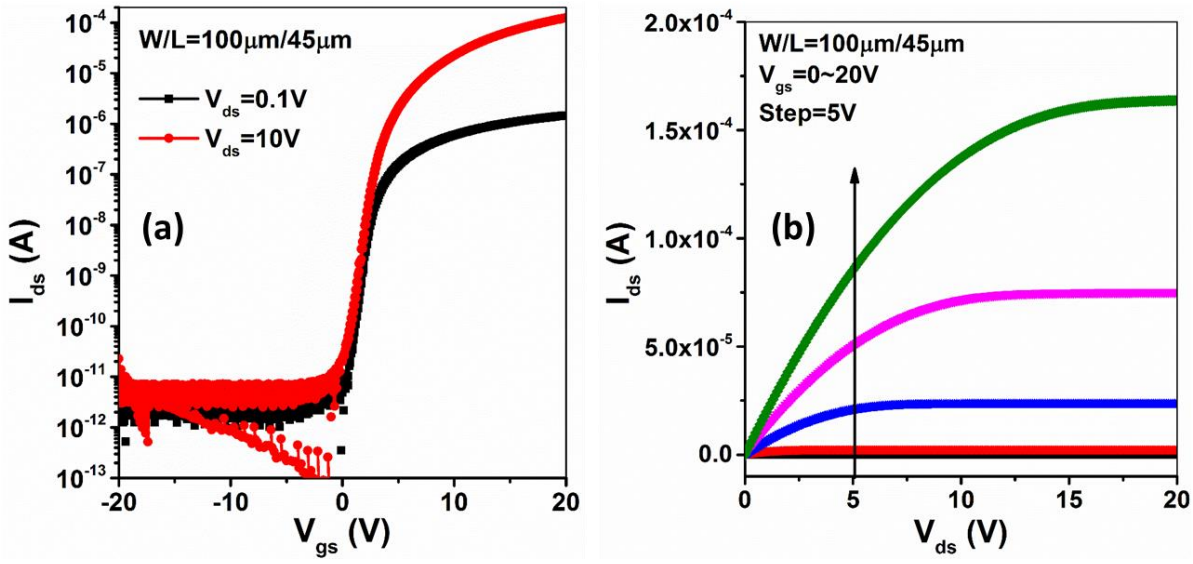

Figure 3-18: (a) Transfer and (b) output curves of the optimal BCE-type hp-ITZO TFTs.

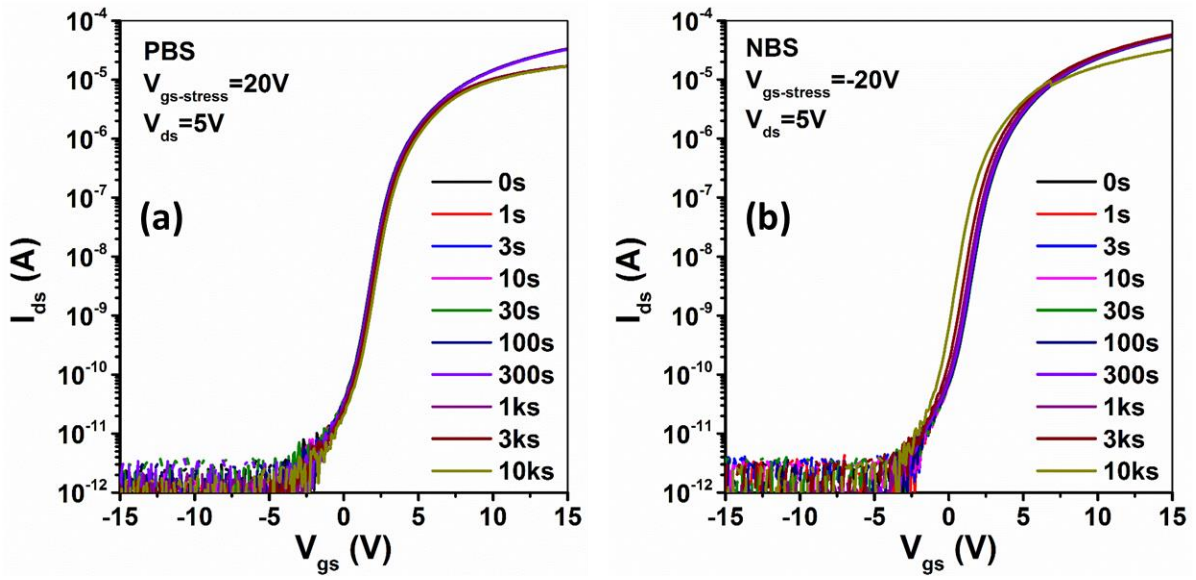

Figure 3-19: Transfer curve variation of the optimal BCE-type hp-ITZO TFTs under (a) PBS and (b) NBS tests.

Compared with the ES-type TFTs, the BCE devices can save photolithography steps and reduce the parasitic capacitance and device footprint. Through annealing the hp-ITZO channels before the molybdenum S/D layer deposition, the channels are significantly strengthened and show enhanced resistivity to the H_2O_2-based etchants. Meanwhile, by controlling the over-etch ratio within 40% ~ 60%, the etching residues can be almost removed without severe channel corrosion. The relatively process window exhibits the excellent process robustness of the hp-ITZO channels. Then, the corresponding BCE-type TFTs have been successfully fabricated with high performance and robust stability against gate-bias stress. The results are promising for the next-generation FPDs with higher definitions and more cost-effective manufacturing.

3.3 Chapter Summary

In this chapter, the previously proposed hp-ITZO thin films have been verified as high-performance TFT channels by implementing BG-TC with the lift-off S/D electrodes. The devices exhibit fairly high and spatially uniform electrical characteristics, long shelf-life and excellent repeated switching behavior. Then, the hp-ITZO channels have been further applied to the BCE-type TFTs, which are highly demanded in industry. Via the over-etch control for S/D electrode patterning and the prior annealing reinforcement, the BCE-type TFTs can be also demonstrated with high electrical performance and robust stability against gate-bias stress. The relative wide over-etch range implies the excellent process robustness of the hp-ITZO channels.

Chapter 4 Top-Gate Bottom-Contact Thin-Film Transistors with Hybrid-Phase Indium-Tin-Zinc Oxide Channel Layers

In Chapter 3, the hp-ITZO thin films have been verified as one of the most promising TFT channels, and the corresponding BG-TC TFTs have been demonstrated with high performance and robust stability. Considering merits such as miniaturized parasitic capacitance, stronger device scalability and fewer photolithography mask counts, the top-gate self-aligned (TG-SA) TFTs should be more appropriate for AM-FPDs and ICs. Currently, they are indeed highly demanded in industry. However, their practical implementation encounters many technical challenges, including but not limited to conductive and reliable S/D region formation, which is one of the core issues. We will discuss this and provide our own solution in Chapter 5. Additionally, for many top-gate MO TFTs, especially with high mobility in enhancement mode, their high-quality gate insulator deposition and efficient threshold voltage control are another two common issues, and they should be well solved first. Otherwise, it is hard to achieve high and reliable performance in the TG-SA hp-ITZO TFTs, even though our solution to dope the S/D regions is very effective. Therefore, gate insulator engineering and gate electrode engineering are employed to deal with the latter two issues in this chapter. To avoid the interference from S/D regions on our studies, the TG-BC (i.e., normal staggered) TFTs with real ITO S/D electrode entities are adopted as models herein.

4.1 Gate Insulator Engineering

For TFTs especially with the process-sensitive MO channels, their gate insulators (GIs) are one of the core device components. The choice of appropriate gate insulator materials [133, 134] and their deposition processes [135, 136] will directly affect the quality of gate insulators and GI/AC interfaces, which are further relevant to device performance and reliability [134, 137, 138]. Proven successful in complementary metal-oxide-semiconductor (CMOS) and hydronated amorphous silicon (a-Si:H) TFT technology, silicon dioxide created using the PECVD technique is often selected as the gate insulators or one layer of gate insulator stacks in MO TFTs. In general, PECVD SiO_2 has two popular and mature embodiments. One is based on a gaseous silane (SiH_4) source (SiH_4-SiO_2), and the other uses a liquid tetraethyl-orthosilicate (TEOS) precursor (TEOS-SiO_2). However, there always exist some undesirable issues when they are separately employed as the MO TFT gate insulators. It is known that the hydrogen (H) content in the SiH_4-SiO_2 is quite high, which can easily diffuse into the channels

[139-141]. These H atoms can donate electrons by forming M-OH bonds with metal cations [86], or generate sub-gap states near the VBM by forming M-H bonds and hence degrade the negative bias illumination stress stability [87]. TEOS-SiO_2, on the other hand, is very rich in hydroxyl (OH) groups and water [141]. It is reported that the OH groups are able to induce electric dipoles at the GI/AC interfaces, resulting in remarkable hysteresis [142]. Meanwhile, water molecules can serve as either electron donors or acceptor-like trap sites with regard to the thickness of the MO channels [143].

To obtain gate insulators with enhanced quality, many researchers have looked beyond PECVD SiO_2 to develop other dielectrics using various deposition techniques [112, 144-146], but these require extra investment for process adjustment and facility replacement. In this work, we will demonstrate that the issues of PECVD SiO_2 can be simply addressed via stacking a SiH_4-SiO_2 layer and a TEOS-SiO_2 layer together. To validate our solution, the content of H and OH groups in the single-layer, and the stacked PECVD SiO_2 gate insulators will be characterized first. Next, we will compare the electrical properties of the stacked PECVD SiO_2 with those of the single-layer counterparts. Finally, after optimizing the thickness of each PECVD SiO_2 layer and its deposition order, we can successfully fabricate the TG-BC hp-ITZO TFTs incorporating the stacked gate insulators, and they are shown to exhibit good electrical performance.

4.1.1 Fabrication Process

The cross-sectional schematic of the TG-BC TFTs in this work is shown in Fig. 4-1(a). Initially, 50-nm-thick indium tin oxide (ITO) source/drain electrodes were sputtered and patterned on 4-inch circular substrates. Then, the hp-ITZO thin films were deposited at room temperature, with a thickness of 50 nm. The detailed sputtering conditions have been described in Chapter 3. Next, a 1/2000 molar aqueous hydrofluoric acid solution was used as the hp-ITZO channel wet etchant after photolithography. Afterwards, 150-nm-thick single-layer gate insulators based on the single-layer TEOS-SiO_2 or the single-layer SiH_4-SiO_2, and the stacked gate insulators, including both the TEOS-SiO_2 layer and the SiH_4-SiO_2 layer, were deposited at 300 °C. To optimize the device performance, we tested various combinations of the gate insulator stacks, where the TEOS-SiO_2 thickness increased from 25 nm to 50 nm, 75 nm, 100 nm and 125 nm, and the SiH_4-SiO_2 thickness was adjusted accordingly to keep the total gate insulator thickness at 150 nm. (Note that, except where otherwise stated in this work, the TEOS-SiO_2 layer thickness and the SiH_4-SiO_2 layer thickness in the gate insulator stacks refer to 100 nm and 50 nm, respectively.) It is noted that the TEOS-SiO_2 layer must be used to form

the GI/AC interfaces in our TG-BC TFTs with the stacked gate insulators. For the TEOS-SiO_2 deposition, the TEOS cylinder was kept at 40 °C, and the source was carried into the chamber using Ar gas. The gas flow rate of N_2O/O_2/Ar, pressure, and RF power were 200/200/30 sccm, 220 mTorr and 30 W, respectively. For the SiH_4-SiO_2 deposition, the gas flow rate of $SiH_4/N_2/N_2O$, pressure and RF power were 8/400/1425 sccm, 900 mTorr and 60 W, respectively. Then, 300-nm-thick aluminum layers were sputtered and dry-etched to form the gate electrodes. Finally, the SiO_2 regions above the S/D electrodes were exposed for testing using the RIE technique in CHF_3 plasma, followed by post-annealing at 300 °C in air. Above all, the fabrication of devices can be completed at a temperature of no more than 300 °C.

The electrical characteristics of the TFTs were measured in a dark probe station using a semiconductor parameter analyzer (B1500, Keysight) and an LCR meter (E4980, Agilent). The content of the H and OH groups in the PECVD SiO_2 gate insulators was characterized using Fourier transform infrared spectroscopy (FTIR, Vertex 70 Hyperion 1000, Bruker) and secondary ion mass spectrometry (SIMS, PHI 7200, Physical Electronics), respectively.

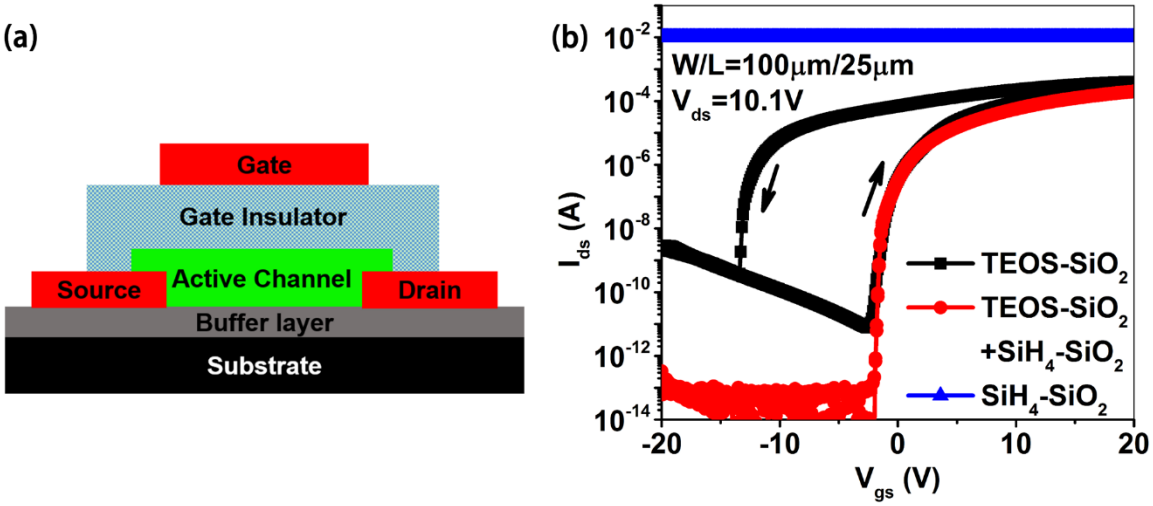

Figure 4-1: (a) Schematic and (b) transfer curves of the TG-BC hp-ITZO TFTs with different types of gate insulators.

4.1.2 Comparison of Different Gate Insulators

Fig. 4-1(b) plots the typical transfer curves of the TG-BC hp-ITZO TFTs with different types of gate insulators. The devices with the single-layer SiH_4-SiO_2 gate insulators are short-circuited, even though the post-annealing time has been extended to >10 h (not shown here). The SIMS spectra in Fig. 4-2(a) describes the level of H content in different SiO_2 gate insulators. The spectra have been calibrated using the relatively stable SiO_2^- signal as a reference. The significant intensity decline of the H-/SiO_2^- signal before 50 s is caused by an extra ~16-nm-

thick gold conducting layer together with an inevitable contamination layer on the surface of the PECVD SiO_2 gate insulators. The former conducting layer was deposited to improve measurement accuracy. Even though the latter contamination layer was not removed prior to gold sputtering, the SIMS spectra after 50 s could still faithfully reflect the relative level of H content in the PECVD SiO_2 gate insulator bulks as well as at the GI/AC interfaces. Obviously, the H content in the single-layer SiH_4-SiO_2 is much higher than that in the single-layer TEOS-SiO_2 and the TEOS-SiO_2 plus SiH_4-SiO_2 stacks. This means that more H dopants can diffuse into the channels and donate a larger amount of electrons [86, 139-141]. Moreover, there also exists an unexpected silicon-doping phenomenon in our channels during the SiH_4-SiO_2 deposition process [144]. Thus, the devices with the single-layer SiH_4-SiO_2 gate insulators can be found to lose their switching behavior without doubt.

Fig. 4-1(b) also reveals that the on-state current of the TFTs with the single-layer TEOS-SiO_2 gate insulators is higher than that of the devices with the stacked gate insulators. This is because plenty of OH groups (in the form of Si-OH^+-Si) in the TEOS-SiO_2 can drift towards the GI/AC interfaces under a positive gate bias. Then, they will induce extra image electrons and form an ultrathin electric-double-layer (EDL) at the interfaces [147, 148]. Together with the gate potential bias, the EDL effect enables stronger capacitive coupling for mobility and on-state current boost. However, an undesired anti-clockwise hysteresis phenomenon is also clearly observed after a cyclic sweep, and the threshold voltage shift (ΔV_{th}) reaches as high as -12.2 V. This is attributed to the large number of electric dipoles induced by the OH groups at the GI/AC interfaces [142]. The FTIR spectra in Fig. 4-2(b) can verify our inference. The IR absorption signal of the single-layer TEOS-SiO_2 is much more intensive than that of the other PECVD SiO_2 gate insulators within the OH-related band (2500~3645 cm^{-1}) [149].

Unlike TFTs employing single-layer gate insulators, those with stacked PECVD SiO_2 gate insulators have substantially different behaviors. Although the SiH_4-SiO_2 layer is involved, these TFTs can maintain normal operation (Fig. 4-1(b)). This means that the negative impacts of H and Si doping on the channels during the SiH_4-SiO_2 deposition can be effectively buffered by the underlying TEOS-SiO_2 layer. On the other hand, the existence of TEOS-SiO_2 does not bring any severe hysteresis issues. This is because the OH group content in the TEOS-SiO_2 plus SiH_4-SiO_2 stacks, which is comparable to that in the single-layer SiH_4-SiO_2 gate insulators, is far lower than that in the single-layer TEOS-SiO_2 gate insulators (Fig. 4-2(b)). But the decrease of OH groups is hard to simply explain by the thinner TEOS-SiO_2 layer in the stacks. There must be other underlying reasons.

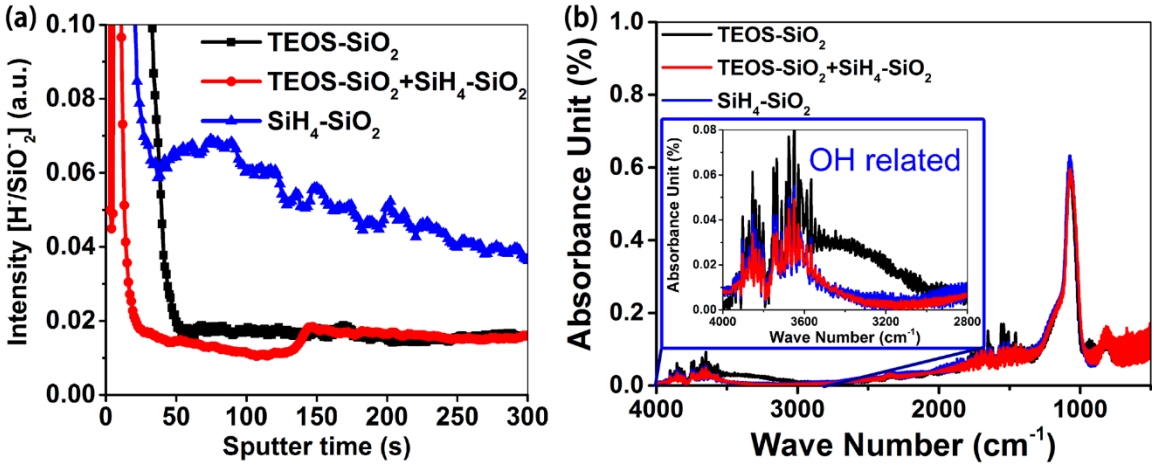

Figure 4-2: (a) SIMS spectra related to H^- species and (b) FTIR spectra in different types of gate insulators. Inset: the specific IR absorption information within the OH-related band.

In Fig. 4-2(a), the H^-/SiO_2^- signal before 150 s is associated with the H content in the upper SiH_4-SiO_2 layer of the stacks. Despite the conducting layer and the contamination layer on the surface, its intensity is obviously weaker than that in the single-layer SiH_4-SiO_2. Therefore, both H and OH traps in the stacks are reduced in fact compared with those in their single-layer counterparts. One plausible explanation for the reduction is that the H groups in the SiH_4-SiO_2 layer and the OH groups in the TEOS-SiO_2 layer can mutually diffuse. They may interact and even annihilate each other, forming by-products that can be removed during the PECVD and the following post-annealing processes (Fig. 4-3(a)). Thus, the quality of PECVD SiO_2 can be automatically improved by themselves. This is further verified by sandwiching the dielectrics between the heavily doped n-type (n++) silicon substrates and the aluminum electrodes. As shown in Fig. 4-3(b), the leakage current of the stacked gate insulators is remarkably decreased compared with the single-layer TEOS-SiO_2 gate insulators, even though the TEOS-SiO_2 layer occupies the majority of the stacks. Moreover, the stacked gate insulators are found to have the highest critical electric field intensity for soft breakdown, indicating they have the fewest traps and the most robust dielectric strength among the three types of gate insulators. Therefore, the TG-BC hp-ITZO TFTs with the stacked PECVD SiO_2 gate insulators can reasonably present the sharpest SS and the lowest gate leakage current (I_{gs}) (Fig. 4-3(c)).

The single-layer and stacked PECVD SiO_2 gate insulators were further investigated via C-V characterizations at 100 kHz, where the TFT S/D electrodes were grounded and a gate bias was applied. As shown in Fig. 4-3(d), due to short circuit, the TFTs with the single-layer SiH_4-SiO_2 gate insulators behave like parallel plate capacitors. For the other two types of devices, their transition from channel depletion mode to charge accumulation mode in metal-oxide-

semiconductor (MOS) capacitors can be clearly observed from their C-V curves. The capacitance density of the TFTs with the single-layer TEOS-SiO_2 gate insulators in the electron accumulation mode is nearly 15 nF/cm^2 larger than that of the devices with the stacked gate insulators. This presumably originates from the EDL effect, as mentioned above.

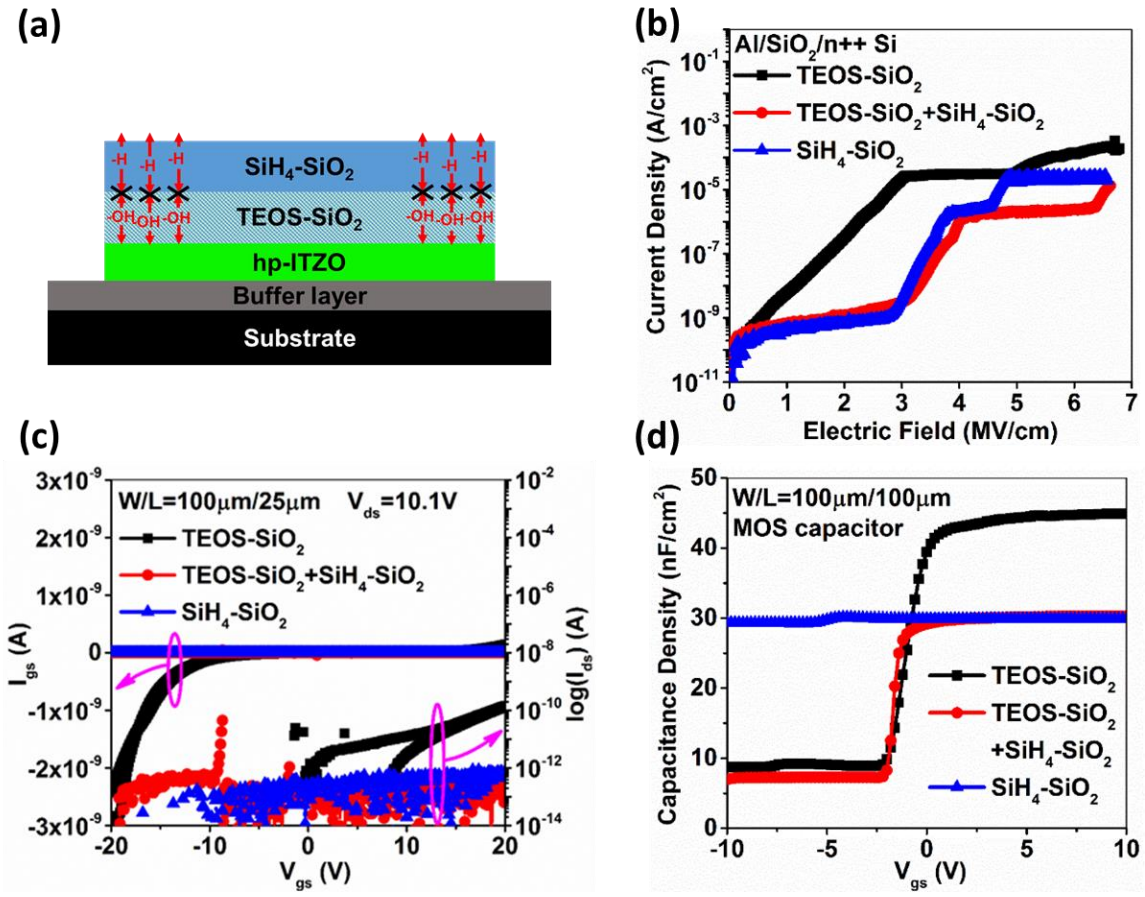

Figure 4-3: (a) Illustration of mutual interactions between H groups and OH groups in the gate insulator stacks. (b) Leakage current density of different types of gate insulators. (c) Gate leakage current and (d) C-V curves of the TFTs with different types of gate insulators.

Table 4-1: Key electrical parameters of the TG-BC hp-ITZO TFTs with different gate insulator combinations

TEOS-SiO_2 +SiH_4-SiO_2	**C_{ox} (pF)**	**μ_{fe} (cm^2/Vs)**	**SS (V/dec)**	**On-off ratio**	**V_{th} (V)**	**ΔV_{th} (V)**
150 nm+0 nm	0.753	112.7	0.287	5.1×10^7	-0.9	-12.2
125 nm+25 nm	0.674	11.5	0.079	5.5×10^9	0.1	~0.1
100 nm+50 nm	0.665	15.1	0.097	1.6×10^{10}	-0.9	<0.1
75 nm+75 nm	0.671	16.8	0.102	2.4×10^9	-1.2	<0.1
50 nm+100 nm	0.659	18.9	0.169	2.2×10^9	-2	<0.1
25 nm+125 nm	0.627	23.6	0.306	1.6×10^9	-12.5	<0.1

0 nm+150 nm	0.648	70.6	-	-	-	-

To optimize the device performance, TG-BC hp-ITZO TFTs with different TEOS-SiO_2 and SiH_4-SiO_2 thickness combinations were further fabricated. Their transfer curves are plotted together in Fig. 4-4(a), and the corresponding key electrical parameters are summarized in Table 4-1. Faithfully, the H doping from the upper SiH_4-SiO_2 layer enables the devices to own higher μ_{fe} with the thickness increase of the SiH_4-SiO_2 layer. Meanwhile, it also leads to more negative V_{th} and worse SS. Overall, the optimal device performance can be obtained when the thickness ratio of the TEOS-SiO_2 layer over the SiH_4-SiO_2 layer varies within the range of 1:1 and 2:1.

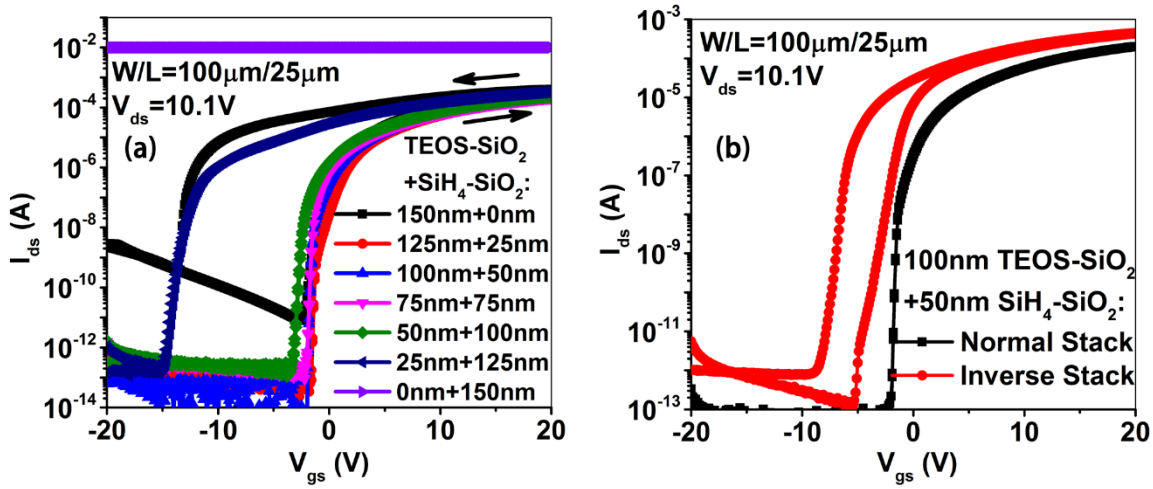

Figure 4-4: Transfer curves of the TG-BC hp-ITZO TFTs (a) with different TEOS-SiO_2 and SiH_4-SiO_2 thickness combinations and (b) with normally or inversely stacked gate insulators.

4.1.3 Optimal Device Characterizations

Fig. 4-5 plots the typical transfer and output curves of the optimal TFTs with the stacked gate insulators containing 50-nm-thick SiH_4-SiO_2 on the top and 100-nm-thick TEOS-SiO_2 underneath. Thanks to the system-noise-level leakage current of the stacked gate insulators and the low free carrier concentration in the channels, the off-state current is low enough to approach the measurement limit. Thus, the devices can be operated with a fairly high on-off ratio of over 1.6×10^{10}. In addition, their SS reaches as low as 96.9 mV/decade. Then, the total trap density (n_{total}) in the channel bulks and at the stacked GI/AC interfaces can be calculated as 3.5×10^{11} cm^{-2} eV^{-1} according to Eq. 3-2. In contrast, the TFTs with the single-layer TEOS-SiO_2 gate insulators own an SS of 287 mV/decade and hence an n_{total} of 9.7×10^{11} cm^{-2} eV^{-1}. This indicates that the stacked gate insulators can contribute to the channel bulks and the GI/AC

interfaces with higher quality. However, Fig. 4-4(b) illustrates that such an improvement relies on the stacked gate insulators in a normal deposition order, where the TEOS-SiO_2 layer should be under the SiH_4-SiO_2 layer and participates in the formation of GI/AC interfaces. Otherwise, the devices with inversely stacked gate insulators will behave disappointingly as a result of the H and Si doping effects from the direct SiH_4-SiO_2 deposition (we will discuss this in the next chapter). According to Fig. 4-6, it is clearly seen that the optimal devices are also free of hysteresis and short-channel effects.

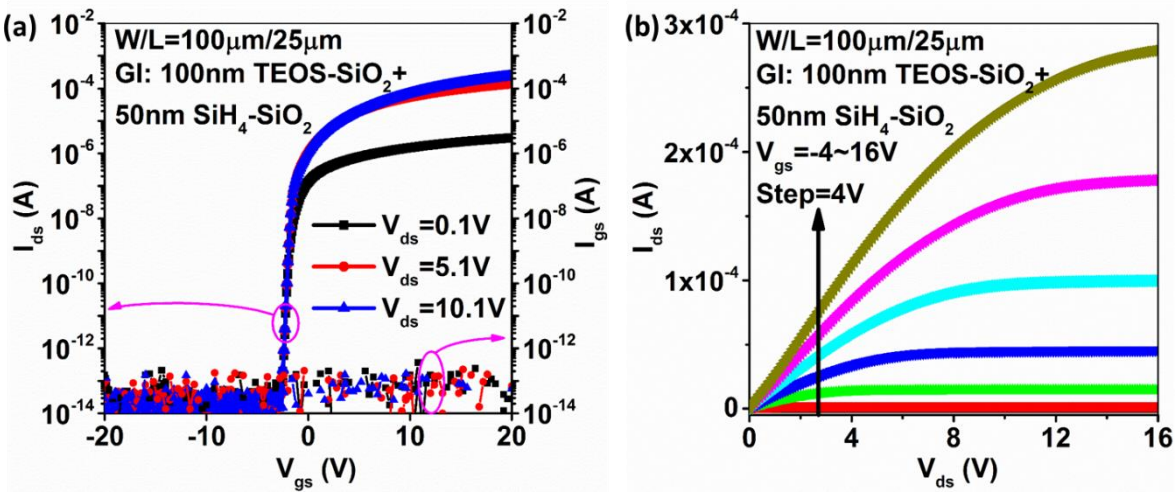

Figure 4-5: Typical (a) transfer and (b) output curves of the TG-BC hp-ITZO TFTs with the optimal stacked gate insulators containing 50-nm-thick SiH_4-SiO_2 on the top and 100-nm-thick TEOS-SiO_2 underneath.

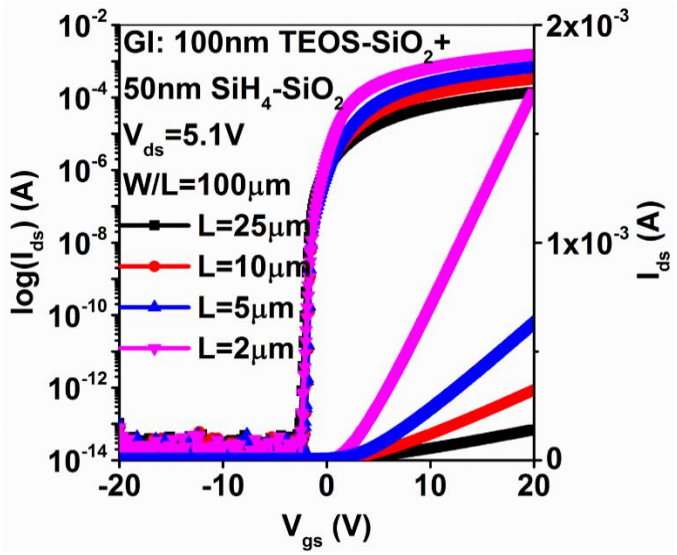

Figure 4-6: Transfer curves of the TG-BC hp-ITZO TFTs with the optimal stacked gate insulators. The channel length varies from 25 μm to 2 μm, and the channel width is fixed at 100 μm.

The reliability of the optimal TFTs against PBS/NBS was also examined. During the PBS and NBS tests, their S/D electrodes were connected to the ground, while a (V_{th}+20) V or (V_{th}-20) V bias was applied on the top gate electrodes of the devices for 10 000 s each. As presented in Fig. 4-7, there is no transfer curve shift after either type of test, confirming the extremely high quality of the stacked PECVD SiO_2 gate insulators and the corresponding GI/AC interfaces. Moreover, the original slight hump phenomenon in the subthreshold region disappears after 10 000 s of the NBS tests. This is beyond our expectation and presumably related to the S/D contact improvement.

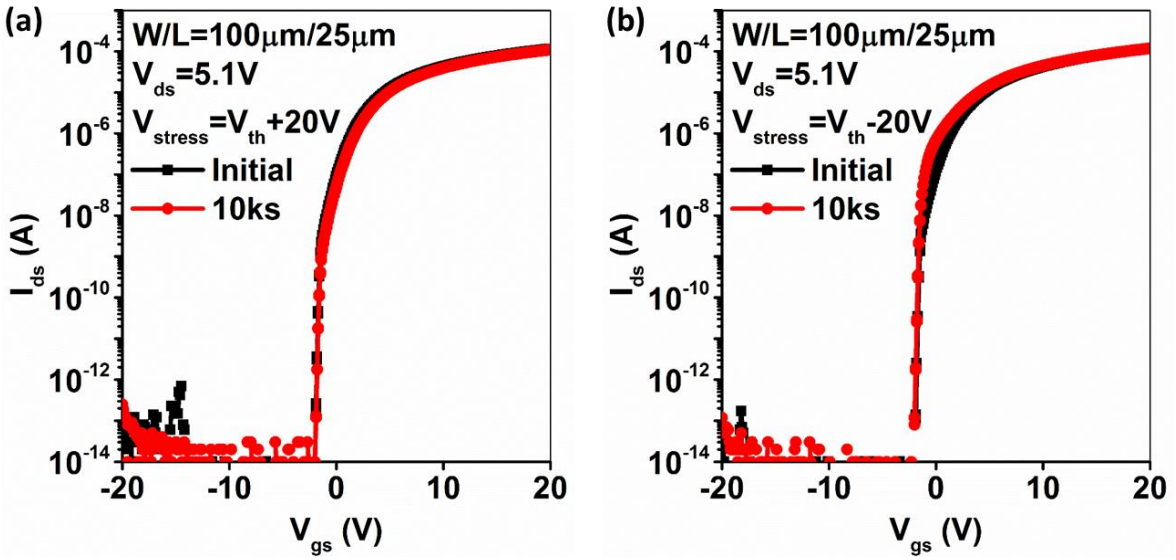

Figure 4-7: Transfer curve evolution of the TG-BC hp-ITZO TFTs with the optimal stacked gate insulators under (a) NBS and (b) PBS tests for 10 000 s.

Above all, a high-quality type of PECVD SiO_2 stacks for the top-gate MO TFTs has been proposed. It consists of a SiH_4-SiO_2 layer with a TEOS-SiO_2 layer underneath. The issues of high H content in the SiH_4-SiO_2 and rich OH groups in the TEOS-SiO_2 were found to be well addressed when the TEOS-SiO_2 was capped by the SiH_4-SiO_2. The Al/SiO_2/n++ Si capacitors revealed that the electrical quality of the PECVD SiO_2 stacks could be strengthened compared with their single-layer counterparts. This is owing to the mutual interactions between the H atoms in the SiH_4-SiO_2 and the OH groups in the TEOS-SiO_2. The TG-BC hp-ITZO TFTs with optimal stacked gate insulators were shown to be free of hysteresis with a fairly high on-off ratio of over 1.6×10^{10} and extremely sharp subthreshold swing of 96.9 mV/decade. The combination of TEOS-SiO_2 and SiH_4-SiO_2 initiates a strategy to achieve high-quality PECVD SiO_2 gate insulators for TG MO TFTs. This is also helpful to realize TG-SA hp-ITZO TFTs with high and reliable electrical performance.

4.2 Gate Electrode Engineering

Via gate insulator engineering, TG-BC hp-ITZO TFTs with aluminum gate electrodes can exhibit good electrical performance and robust stability, but their threshold voltage is always negative. This means that they have to be operated in the depletion operation mode. However, for most of AM-FPDs with low power consumption, the TFTs in the enhancement mode are more preferred [140]. In theory, the threshold voltage is closely associated with the carrier concentration in the MO channels. For ZnO-based TFTs, the primary sources to generate free carriers come from H atoms [150-152] and V_O [22, 153, 154], which unintentionally act as shallow donors in the channels. Thus, their population variation will directly affect the value of the threshold voltage. This relationship is also effective when the binary ZnO thin films are extended to the multicomponent MO semiconductors that are composed of post-transition-metal cations with $(n-1)d^{10}ns^0$ ($n>4$) electronic configurations. Particularly for materials with high carrier mobility (e.g., InZnO), their mobility boost is always accompanied by the formation of more oxygen vacancies and hence the rise of free carrier concentration, apart from the increased fraction of post-transition-metal cations (e.g., In^{3+}) and the following optimization of electron conduction bands [14]. Then, more negative gate bias needs to be applied to switch off these MO TFTs considering the inversely proportional relationship between the free carrier concentration and the threshold voltage [6, 155, 156]. Although solutions such as adopting a dual-active-layer structure [157], employing dual-gate design [158], and chemical doping in channels [69] are capable of tuning the threshold voltage, they will also increase the fabrication complexity or sacrifice the device mobility at the same time [38, 69, 159].

To more efficiently shift the threshold voltage and modulate the operation mode of our top-gate hp-ITZO TFTs, the top gates in this work start to adopt the conductive indium-tin oxide electrodes to replace the original metallic aluminum electrodes. The resultant devices can successfully exhibit good electrical characteristics in the enhancement mode, as well as robust reliability against gate-bias stress. The extra impacts on threshold voltage shift will be investigated from the aspect of gate electrode permeability for hydrogen diffusion out of the MO channels, and oxygen diffusion into the MO channels during the post-annealing process. Apart from the work function of the gate electrodes, a new perspective is provided to tune the threshold voltage in the top-gate hp-ITZO TFTs via gate electrode engineering. This has the potential to enable monolithic integration of high-performance MO TFTs in both the

enhancement and depletion mode. This is beneficial for the design of low-power-consumption circuits using unipolar MO TFT technology [160].

4.2.1 Fabrication Process

Fig. 4-8 shows the schematic diagram of our TG-BC hp-ITZO TFTs with the stacked gate insulators but with different gate electrodes. The entire fabrication process started from the formation of ITO S/D electrodes on 4-inch circular substrates. Afterwards, 50-nm-thick hp-ITZO channels were deposited by magnetron co-sputtering the pc-ITO target and the pc-ZnO target at room temperature. The detailed deposition conditions have been described in Chapter 3. Afterwards, the active islands were defined using photolithography, followed by wet etch in diluted hydrofluoric acid. Next, the stacked PECVD SiO_2 gate insulators, composed of 50-nm-thick SiH_4-SiO_2 with 100-nm-thick TEOS-SiO_2 underneath, were deposited at 300 °C. Then, 100-nm-thick metallic aluminum or conductive indium-tin oxide gate electrodes were sputtered at room temperature. By four-point probe measurement, the conductivity of Al and ITO was 1.05×10^7 S/m and 1.33×10^5 S/m, respectively. To avoid any impact caused by different etch processes, both types of gate electrodes were patterned using the lift-off technique. After contact hole opening using the RIE technique in CHF_3 plasma, a post-annealing treatment was conducted at 300 °C in O_2 for 2 h. Overall, the entire fabrication processes could be completed at a temperature of no more than 300 °C. The electrical characteristics of the TFTs were measured in a dark probe station using a semiconductor parameter analyzer (Agilent 4156C).

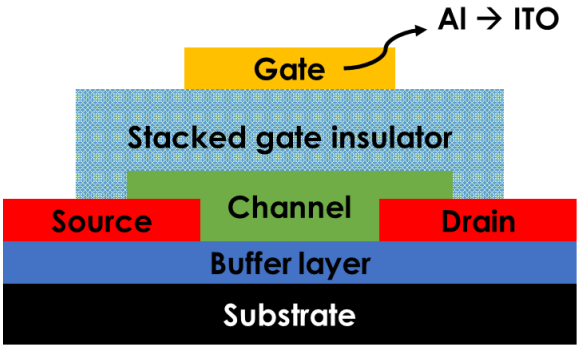

Figure 4-8: Schematic diagram of the TG-BC hp-ITZO TFTs with different gate electrodes.

To monitor the variation of H and V_O inside the MO TFTs with different gate electrodes, samples for testing were also prepared by stacking the thermally grown SiO_2 layer, the hp-ITZO channel layer, the gate insulator layer and the gate electrode layer (Al or ITO or neither) on the silicon wafers in sequence with no extra patterning (Fig. 4-9). Some samples were then annealed at 300 °C in O_2 for 2 h, and the rest were not. The depth profile of the H species was

detected using a secondary ion mass spectrometer (SIMS, PHI 7200, Physical Electronics). The information about V_O was indirectly obtained via analyzing the XPS O 1s spectra, and the work function of the gate electrodes was extracted from each of their UPS spectra. Both XPS and UPS characterizations were carried out on a Physical Electronics 5600 multi-technique system.

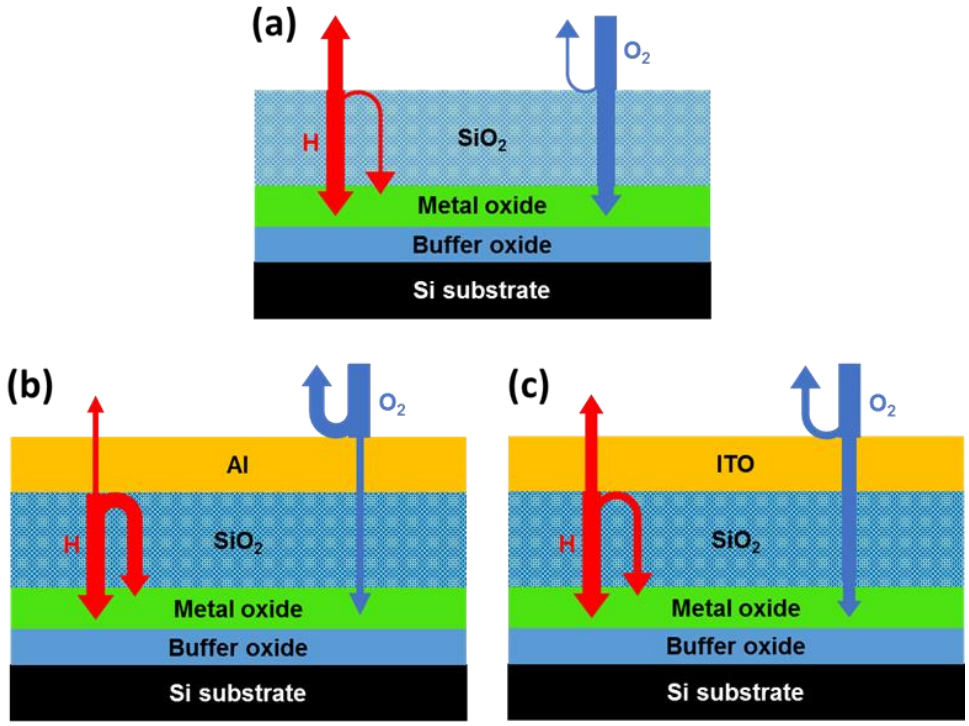

Figure 4-9: Schematic diagrams of thin-film-stacked samples (a) without gate electrodes, (b) with Al gate electrodes, and (c) with ITO gate electrodes. The arrow width indicates the degree of hydrogen diffusion out of or oxygen diffusion into the hp-ITZO channels.

4.2.2 Device Characterizations

Fig. 4-10 plots the typical transfer curves of Al-gated and ITO-gated hp-ITZO TFTs. Their key electrical parameters are listed in Table 4-2. It can be clearly seen that there are two main differences between these two types of devices. Firstly, the on-off ratio of the ITO-gated TFTs is nearly two orders of magnitude larger than that of the Al-gated devices, which is primarily attributed to their lower off-state current. Secondly, in comparison with the Al-gated TFTs in the depletion mode, the positive threshold voltage shift (ΔV_{th}) of the ITO-gated TFTs reaches as much as ~1.7 V (from -1.2 V to 0.5 V). Such devices can then enter the enhancement operation mode.

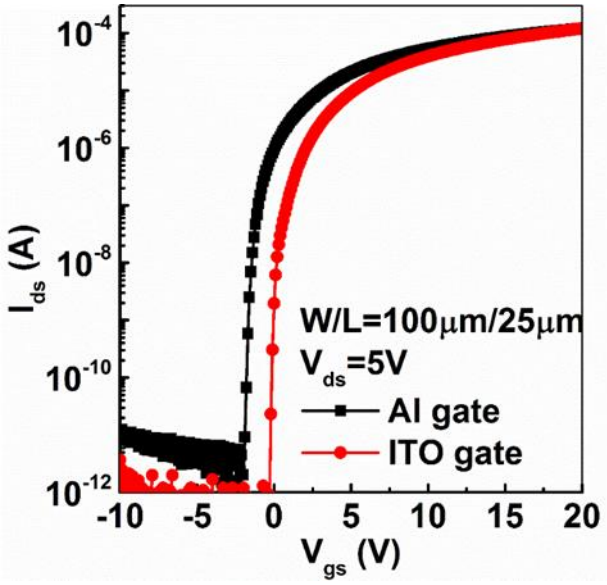

Figure 4-10: Typical transfer curves of the TG-BC hp-ITZO TFTs with Al and ITO gate electrodes.

Table 4-2: Key electrical parameters of the TG-BC hp-ITZO TFTs with Al and ITO gate electrodes

	μ_{fe} (cm^2/Vs)	V_{th} (V)	SS (V/decade)	On-off ratio
Al GE	18.5	-1.2	0.115	$>10^8$
ITO GE	17.4	0.5	0.109	$>10^{10}$

Fig. 4-11 shows the UPS spectra of the Al and ITO gate electrodes. Then, their work function can be extracted according to the following equation [161]:

$$\Phi_m = 21.22 + E_{cutoff} - E_{Fermi}, \tag{4-1}$$

where Φ_m, E_{Fermi}, and E_{cutoff} is the gate electrode's work function, Fermi energy, and onset energy of the secondary electron cut-off region, respectively. E_{Fermi} corresponds to the energy that meets the largest gradient in intensity, while E_{cutoff} is determined by extrapolating the fitting straight line for the step at the secondary electron cutoff region. Herein, the results of the Al and ITO gate electrodes are extracted as 3.63 eV and 4.03 eV, respectively. Thus, the work function of the ITO is only about 0.4 eV higher than that of the Al. Theoretically, the threshold voltage in a field-effect transistor is given by [162]

$$V_{gs} = \Phi_{ms} - \frac{Q_i}{C_{ox}} + \Psi_s + \frac{\varepsilon_s}{C_{ox}} E(\Psi_s), \tag{4-2}$$

where $\Phi_{ms}=\Phi_m-\Phi_s$, Q_i, C_{ox}, ε_s, Ψ_s, and $E(\Psi_s)$ is the work function difference between the gate electrodes and the channels, effective positive charges in the gate insulator bulks and at the GI/AC interfaces, gate insulator capacitance per unit area, dielectric constant of the channels, surface potential, and its corresponding electric field, respectively. V_{th} corresponds to the gate bias at which the accumulated carriers can start to form the conductive channels. Among the variables above, the impacts of Q_i on V_{th} can be very slight via strict process control, while Φ_{ms} is able to act as an important role. However, when Al is replaced by ITO as the GE, the actual ΔV_{th} (~1.7 V) is found to be much larger than the ΔV_{th} (~0.4 V) caused by the work function difference. Thus, apart from the work function, there should exist other factors to determine V_{th}.

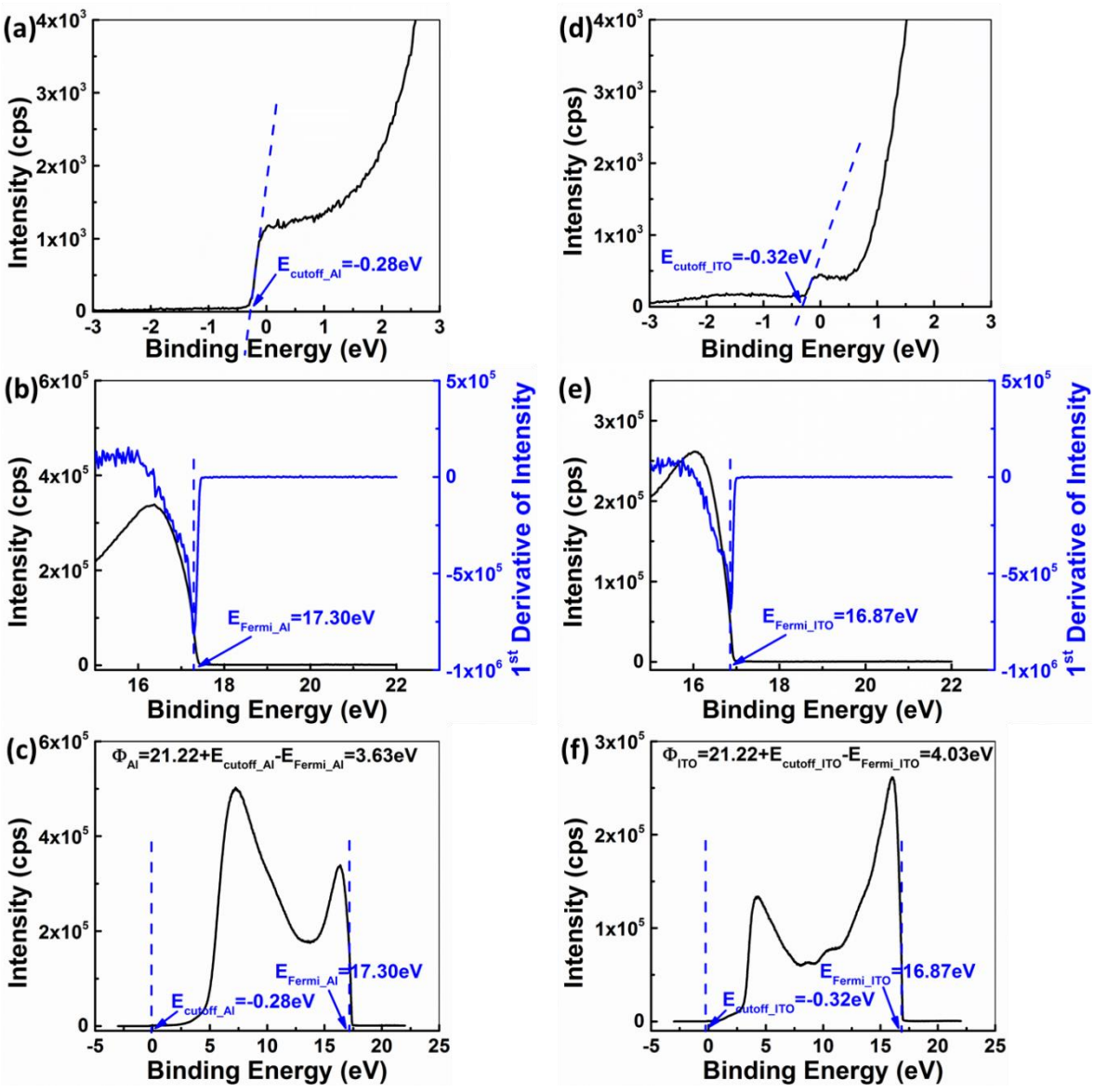

Figure 4-11: UPS spectra of (a)-(c) Al and (d)-(f) ITO gate electrodes.

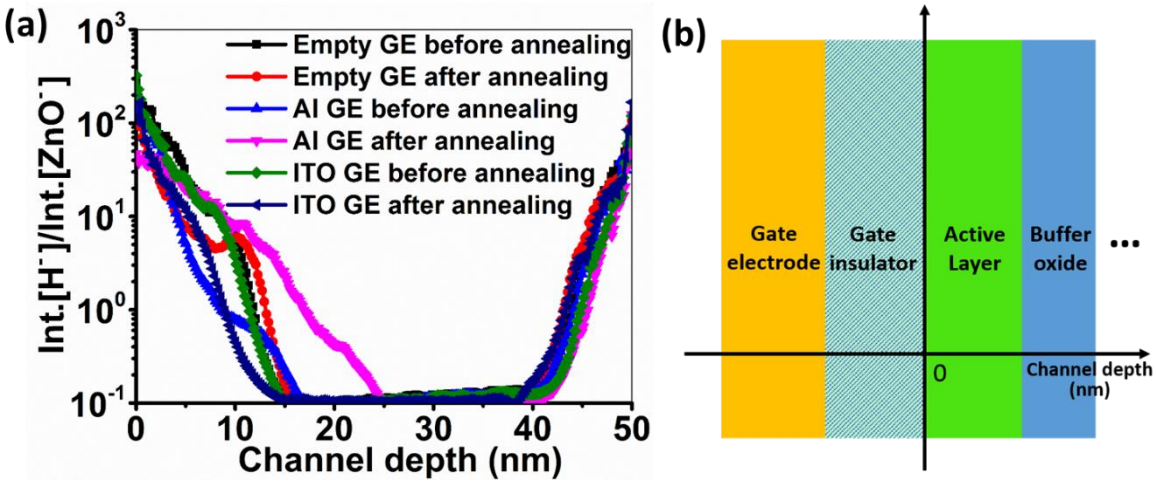

Figure 4-12: (a) Depth profile of the H species along the hp-ITZO channels in the thin-film-stacked samples with different gate electrodes before and after post-annealing. (b) Illustration of the original position in terms of channel depth.

It is known that both H and V_O serve as shallow donors in the MO channels, and their population are related to free carrier concentration and hence V_{th}. H atoms mainly originate from the MO channel deposition and the subsequent processes such as PECVD. Fig. 4-12 presents the depth profile of the H species along the direction that is perpendicular to the MO channels, and the H^- signal has been calibrated by employing the relatively stable ZnO^- signal as a reference. Herein, we regard the channel depth where the signal intensity ratio of H^- over ZnO^- reaches 0.1 as the diffusion length (L_{diff}) of the H species. The diffusion coefficient D_H of the H species in the channels can be approximately figured out referring to Fick's second law. Suppose the total dose of the H species that has accumulated at the GI/AC interfaces is constant and the reaction/exchange rate at the interface is very fast, then, the diffusion profile should follow the Gaussian function, which is given by

$$n(d,t) = \frac{Q}{\sqrt{\pi D_H t}} \exp\left[-\left(\frac{d}{2\sqrt{D_H t}} \right)^2 \right], \qquad (4\text{-}3)$$

where n(d, t) corresponds to the H species concentration in the channels at a depth of d after t-second annealing at a temperature of 300 °C, and Q is the initial total dose of H species at the GI/AC interfaces. The calculated diffusion coefficient D_H of the H species in the channels at 300 °C is about 3.6×10^{-17} cm^2/s, which is dramatically smaller than the value of D_H (~1.2×10^{-11} cm^2/s) in the SiO_2 gate insulators at 300 °C. It implies that if the H species in the SiO_2 are blocked by the upper gate electrodes, they are able to respond rapidly by diffusing towards the opposite direction and affecting the initial total dose Q at the GI/AC interfaces due to their fast

movement in the SiO_2 gate insulators, as shown in Fig. 4-9(b). It can be further reflected through the ultimate diffusion profile of H species in the hp-TIZO channels. In Fig. 4-12(a), the H species in the samples with Al gate electrodes are observed to diffuse 10 nm deeper after the post-annealing process. However, the samples with ITO gate electrodes or without gate electrodes exhibit a similar L_{diff} (~15 nm) regardless of post-annealing. For constant dose diffusion, a deeper L_{diff} means a larger Q. This reveals a higher proportion of the H species are blocked by the Al gate electrodes. In other words, the Al gate electrodes are less permeable for the H species diffusion out of the samples in comparison with the ITO gate electrodes.

The diffusion coefficient D_O of oxygen in the SiO_2 gate insulators is reported at the level of 10^{-16} cm^2/s [163], which is far less than D_H in the SiO_2 gate insulators. However, the diffusion of oxygen atoms into the MO channels during the post-annealing process is still significant. To verify this, the TG-BC hp-ITZO devices were further post-annealed in a vacuum rather than an O_2 atmosphere. The test results are shown in Fig. 4-13 and Table 4-3. Firstly, there is no doubt that the ITO-gated devices possess less negative V_{th} than the Al-gated devices after the vacuum annealing, and the difference of V_{th} is larger than 0.4 V. This is because the ITO gate electrodes are more permeable for H species diffusion out of the devices, regardless of the annealing atmosphere. Secondly, the devices that are annealed in oxygen are found to present more positive V_{th} in comparison with their counterparts that are annealed in a vacuum. Also, when the Al gate electrodes are replaced by the ITO gate insulators, the value of ΔV_{th} in the oxygen annealing case (1.7 V) is larger than that in the vacuum annealing case (1.1 V). It is confirmed that oxygen diffusion can also make a remarkable contribution during the post-annealing process. Owing to a lack of oxygen supply, the vacuum annealing will prevent oxygen diffusion into the devices from annihilating V_O in the channels. Therefore, both Al-gated and ITO-gated TFTs after the vacuum annealing exhibit worse SS.

Table 4-3: Key electrical parameters of Al-gated and ITO-gated TFTs after post-annealing in an oxygen or a vacuum atmosphere

	Al-gated + O_2 annealing	**ITO-gated + O_2 annealing**	**Al-gated + vacuum annealing**	**ITO-gated + vacuum annealing**
V_{th} (V)	-1.2	0.5	-1.6	-0.5
SS (V/decade)	0.115	0.109	0.328	0.271

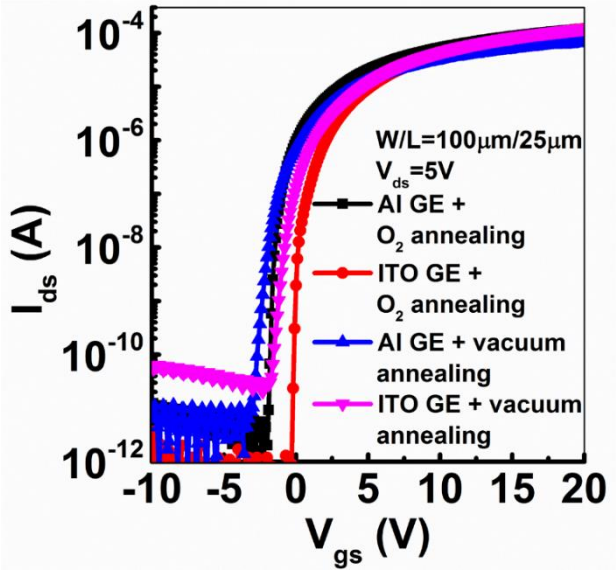

Figure 4-13: Transfer curves of Al-gated and ITO-gated TFTs after post-annealing in an oxygen or a vacuum atmosphere.

The content of V_O was further characterized using the XPS technique. Fig. 4-14 plots the XPS O 1s spectra of the MO channels in the samples with different gate electrodes. The data were collected when the Zn 2p signal intensity began to climb and the Si 2p signal intensity was found to decline in the XPS depth profile measurement. Through Gaussian-Lorentzian deconvolution, the XPS spectra of the O 1s peak can be theoretically decomposed into three subpeaks that are separately centered at 530.2 ± 0.1 eV (O_I), 531.5 ± 0.1 eV (O_{II}) and 532.7 ± 0.1 eV (O_{III}). Among them, the O_{II} peak is associated with the oxygen deficiencies in lattices (such as V_O) [91, 92]. The relative area ratio of the O_{II} peak in the un-annealed samples without gate electrodes is 23.15%, but after oxygen post-annealing, it decreases to 14.33%. This is because of oxygen diffusion into the MO channels for V_O compensation. For the ITO-gated samples, the derived ratio is 14.77%, which is lower than the result of the Al-gated samples (16.84%), and approaches that of the samples without gate electrodes. This reveals that the ITO gate electrodes are also more permeable for oxygen diffusion into the hp-ITZO channels and they can compensate more V_O than the Al gate electrodes. Above all, it can be concluded that the ITO gate electrodes are equipped with better hydrogen/oxygen permeability for their diffusion during the post-annealing process compared with the Al gate electrodes (Fig. 4-9). Thus, they can further enlarge the V_{th} shift in the top-gate MO devices.

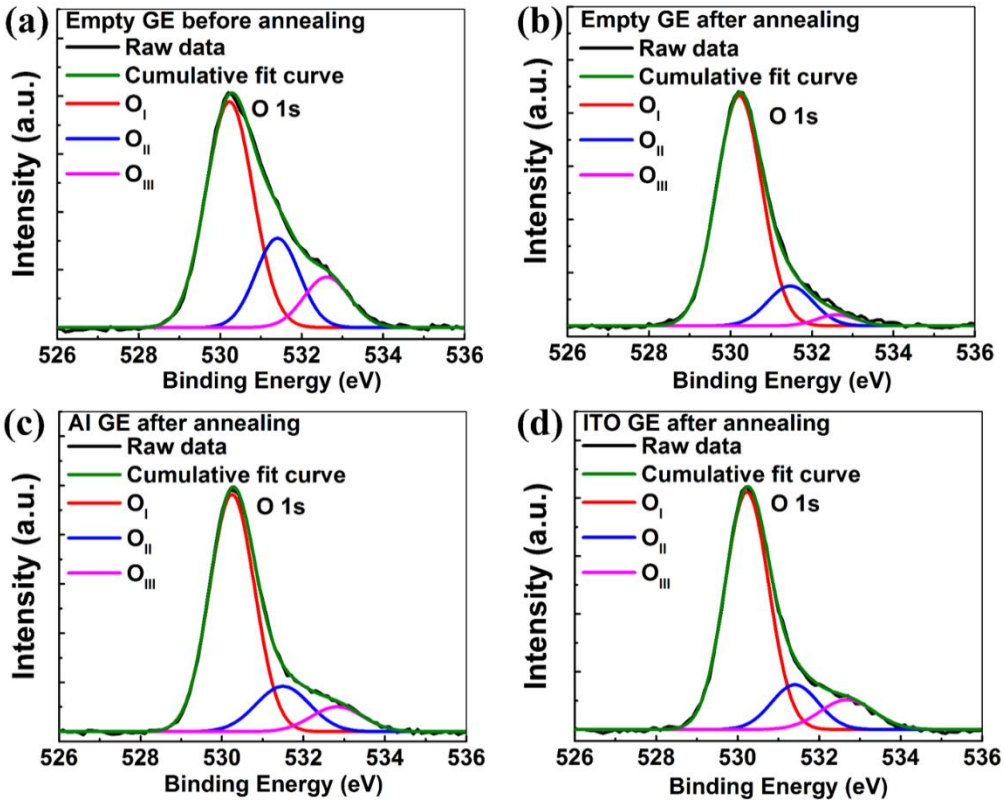

Figure 4-14: (a) XPS O 1s spectra of the channels in the samples without gate electrodes before post-annealing. XPS O 1s spectra of the channels in the samples (b) without gate electrodes, (c) with Al gate electrodes, and (d) with ITO gate electrodes after post-annealing.

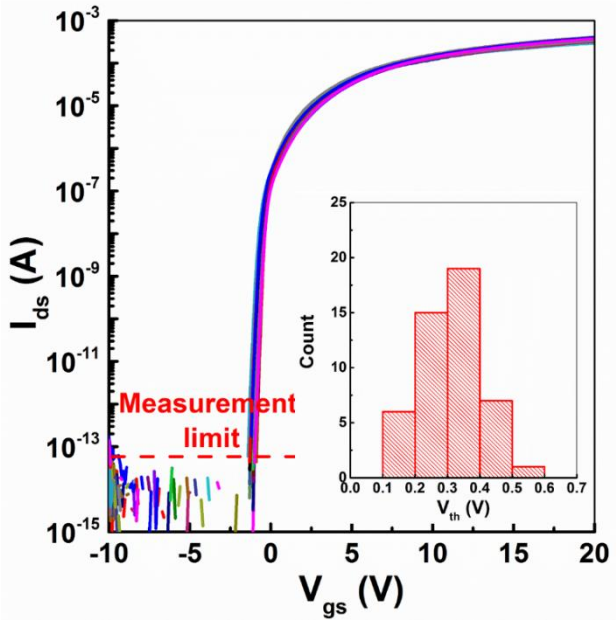

Figure 4-15: Spatial uniformity of the ITO-gated TFTs, which are uniformly distributed across 4-inch circular substrates. Inset: V_{th} distribution of the devices.

Fig. 4-15 groups the transfer curves of the ITO-gated hp-ITZO TFTs. There are 48 TFTs in total, which are uniformly distributed across 4-inch circular substrates. The devices have an average V_{th} of 0.31 V with a standard deviation of 0.085 V, and the difference between the maximum and minimum V_{th} is only 0.38 V. Compared with the TFTs with amorphous MO channels, these hp-ITZO devices herein are confirmed to exhibit excellent spatial uniformity in terms of their electrical characteristics because the nanoscale crystals in the channels are sparse and tiny in comparison with the TFT channel dimensions.

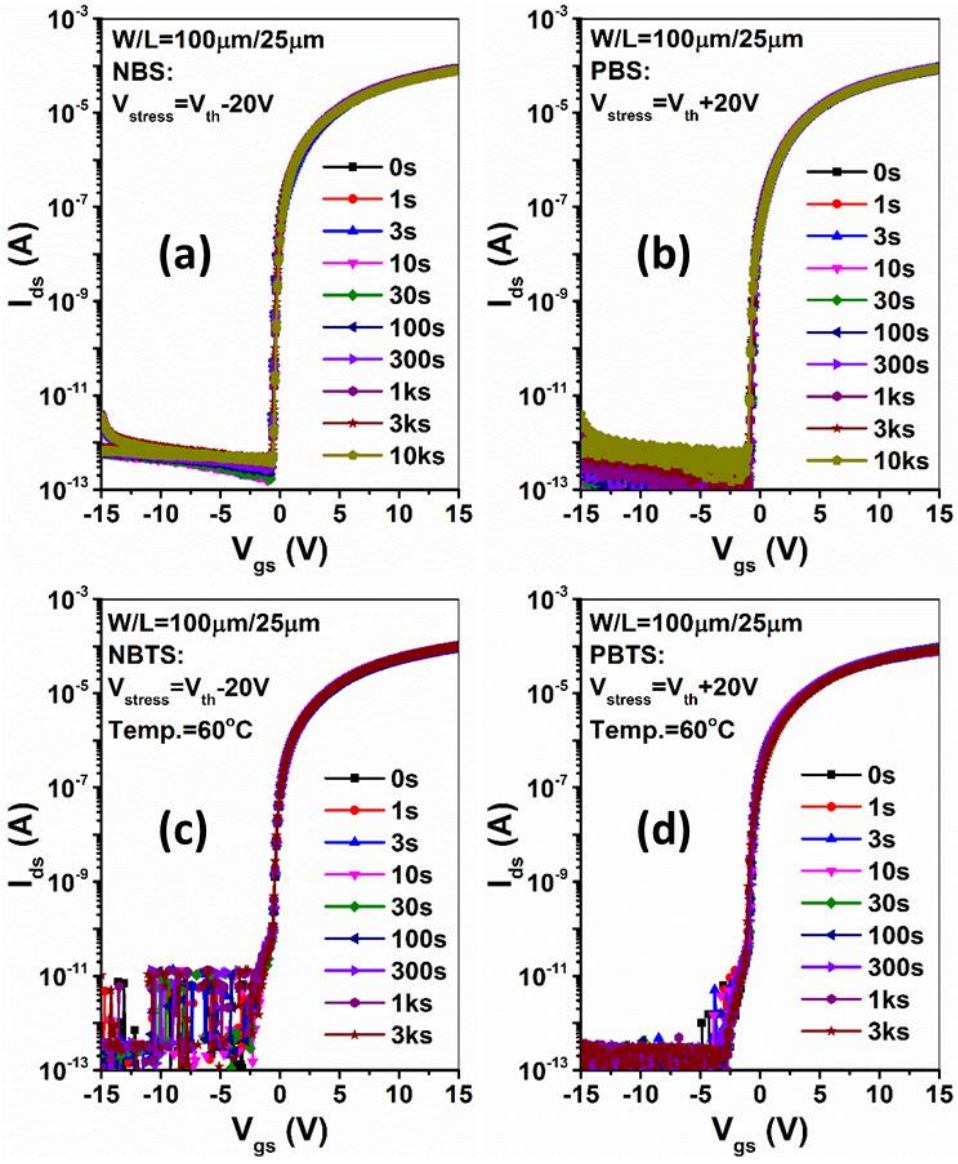

Figure 4-16: Transfer curve evolution of the ITO-gated TFTs under (a) NBS, (b) PBS, (c) NBTS and (d) PBTS tests.

The reliability of our enhancement-mode TG-BC hp-ITZO TFTs was further tested. Fig. 4-16 shows the transfer curve evolution of the ITO-gated devices that were subjected to the

NBS/PBS tests at room temperature and the NBTS/PBTS tests at 60 °C. During the gate-bias stress, their S/D electrodes were grounded, and the applied gate bias in the NB(T)S and PB(T)S cases was set to (V_{th}-20) V and (V_{th}+20) V, respectively. In the NBS and PBS tests, all the transfer curves were overlapped very well. This is attributed to the high quality of the GI/AC interfaces and the stacked gate insulators themselves. In the NBTS and PBTS tests, a slight hump phenomenon emerges in the subthreshold region and remains with the extension of stress time. This is presumably related to the parasitic TFTs that formed at the channel edges, where the gate insulators are thinner. Apart from the hump phenomenon, there is no other degradation observed. This indicates that the main channel regions across the devices retain quite high quality and most of the traps exist at the parasitic channel regions locally.

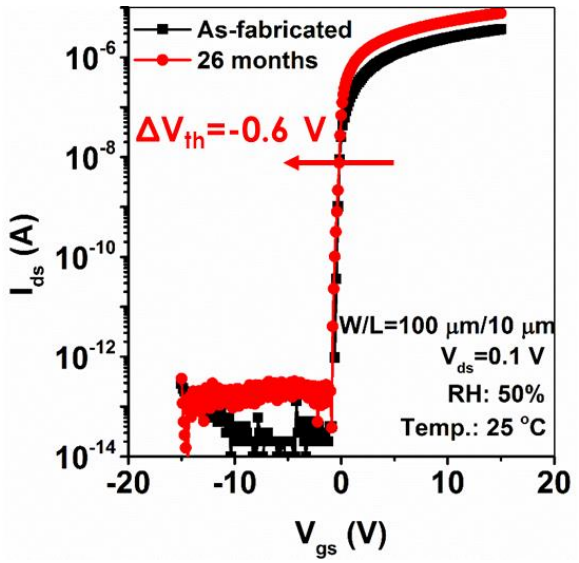

Figure 4-17: Transfer curve evolution of the enhancement-mode TG-BC hp-ITZO TFTs which are aged in ambient air for over 26 months.

Apart from the electrical stability, the ambient stability of the enhancement-mode TG-BC hp-ITZO TFTs was also tested. As shown in Fig. 4-17, the devices could be normally operated after storage in the atmospheric environment (relative humidity is 50% and temperature is 25 °C) for over 26 months. The ΔV_{th} was measured as small as -0.6 V without SS deterioration, and the on-state and off-state current were increased a little bit. This is consistent to the ambient chemisorption of oxygen and moisture molecules on the devices. The excellent ambient stability may be attributed to the high-quality gate insulator stacks with good oxygen/water impermeability as well as the intrinsic insensitively of the hp-ITZO channels to the ambient.

Above all, it has been found that not only the work function of the gate electrodes but also their permeability for hydrogen diffusion out of and oxygen diffusion into the MO channels

during post-annealing can efficiently modulate V_{th} in the top-gate MO TFTs. When the original Al gate electrodes were replaced by the ITO gate electrodes, the TG-BC hp-ITZO TFTs could evolve from the depletion mode to the enhancement mode with good electrical characteristics and robust reliability against gate-bias stress. The results in this section have improved the understanding regarding V_{th} adjustment and provided another potential solution to monolithically integrate enhancement-mode and the depletion-mode TFTs with high-performance n-type MO channels.

4.3 Chapter Summary

In this chapter, two common issues, high-quality gate insulator deposition and efficient threshold voltage control in top-gate MO TFTs, have been well addressed via gate insulator engineering and gate electrode engineering, respectively. Firstly, the PECVD SiO_2 stacks containing the SiH_4-SiO_2 layer with the TEOS-SiO_2 layer underneath has been demonstrated as a type of gate insulator with high quality. The high H content in the single-layer SiH_4-SiO_2 and the rich OH groups in the single-layer TEOS-SiO_2 no longer exist. The fabricated TG-BC hp-ITZO TFTs with the corresponding gate insulator stacks are shown to be free of hysteresis with a fairly low leakage current and extremely sharp SS. Secondly, the enhancement-mode TFTs can be further implemented without significant performance degradation by replacing the metallic Al gate electrodes with the conductive ITO electrodes. It has been found that not only the work function of gate electrodes but also their permeability for hydrogen diffusion out of and oxygen diffusion into the channels during post-annealing can efficiently modulate V_{th}. This initiates a new perspective to adjust V_{th} in the TG MO TFTs and provides a feasible solution to monolithically integrate the enhancement-mode and the depletion-mode MO TFTs together. The efforts in this chapter are of high value to achieve high and reliable performance in the TG-SA hp-ITZO TFTs that are presented in the next chapter.

Chapter 5 Top-Gate Self-Aligned Thin-Film Transistors with Hybrid-Phase Indium-Tin-Zinc Oxide Channel Layers

In Chapter 4, two common issues in top-gate MO TFTs, especially with high mobility and the enhancement mode, have been well addressed via gate insulator engineering and gate electrodes engineering. The fabricated TG-BC hp-ITZO TFTs present high and reliable electrical performance. However, there are intrinsic overlaps between the gate electrodes and the S/D electrodes in this type of devices, leading to undesirable parasitic capacitance and hence signal delay in circuits. For AMOLED displays, capacitive coupling will also create a kickback/feedthrough voltage and then deteriorate the luminescence uniformity of panels [164]. To minimize the parasitic capacitance and save manufacturing cost, TG-SA MO devices are highly demanded in industry. Since the S/D regions are defined by serving their gate electrodes as hard masks, there will be no gate-to-source/drain overlaps in principle. But extra processes such as ion doping [165, 166] or plasma treatment [164, 167, 168] are required to gain conductivity of the MO S/D regions, and the effects are not very satisfactory as well.

When the hp-ITZO thin films are capped by the SiH_4-SiO_2 layer or the TEOS-SiO_2 layer, their resistivity are found to evolve towards two different directions after oxygen annealing. In this chapter, we will seize this unique behavior of the hp-ITZO thin films and try to implement the TG-SA hp-ITZO TFTs, where their conductive and thermally stable S/D regions can be automatically formed during the SiH_4-SiO_2 interlayer dielectric deposition. Thus, additional treatments for the S/D regions can be further eliminated to enable more cost-effective manufacturing.

5.1 Formation of Conductive Source/Drain Regions

As mentioned in Chapter 4, TG-BC hp-ITZO TFTs with single-layer TEOS-SiO_2 gate insulators can exhibit switching behavior, while those with the single-layer SiH_4-SiO_2 gate insulators are found to be short-circuited even after long-period annealing treatment. Since the short-circuit current keeps several orders of magnitude higher than the gate leakage current regardless of switching state, it is thought that the hp-ITZO channels in the latter devices are too conductive to turn off. This is an attractive and meaningful phenomenon, which may have potential to form the conductive S/D regions in the TG-SA hp-ITZO TFTs.

In order to make this phenomenon and its underlying mechanism clear, the resistivity of the

hp-ITZO thin films that are capped by the TEOS-SiO_2 layers or the SiH_4-SiO_2 layers were investigated systematically. The results were obtained by sweeping the I-V curves of Van der Pauw structures that were integrated in cross-bridge structures. Fig. 5-1 shows the cross-sectional and plan-view schematic diagrams of the cross-bridge structure. The fabrication process was initiated from the hp-ITZO thin film deposition. The optimal co-sputtering conditions have been described in Chapter 3. The thickness was 50 nm, and the substrates were silicon wafers coated with 500-nm-thick thermally grown SiO_2. After patterning in a 1/2000 molar aqueous hydrofluoric acid solution, the thin films were capped by the 150-nm-thick TEOS-SiO_2 or SiH_4-SiO_2 layers at 300 °C. Then, contact hole opening and contact pad definition were carried out in sequence. The contact pads were made of 300-nm-thick aluminum. Finally, the thin-film stacks were annealed in an oxygen atmosphere at 300 °C, and the annealing durations were separately 0 h, 2 h, 4 h and 6 h. The resistivity of the hp-ITZO thin films was characterized in a dark probe station using a semiconductor parameter analyzer (Agilent 4156C). As illustrated in Fig. 5-1(b), a proper current I_{12} was applied between Pad 1 and 2, and the other two probes that were connected to Pad 3 and 4 were responsible for meansuring their voltage difference V_{34}. The thin film resistivity (ρ) was then calculated according to the following equations:

$$R_s = \frac{\pi}{\ln 2} \times \frac{V_{34}}{I_{12}}, \tag{5-1}$$

$$\rho = R_s \times d, \tag{5-2}$$

where R_s and d denotes the sheet resistance and the thin film thickness, respectively.

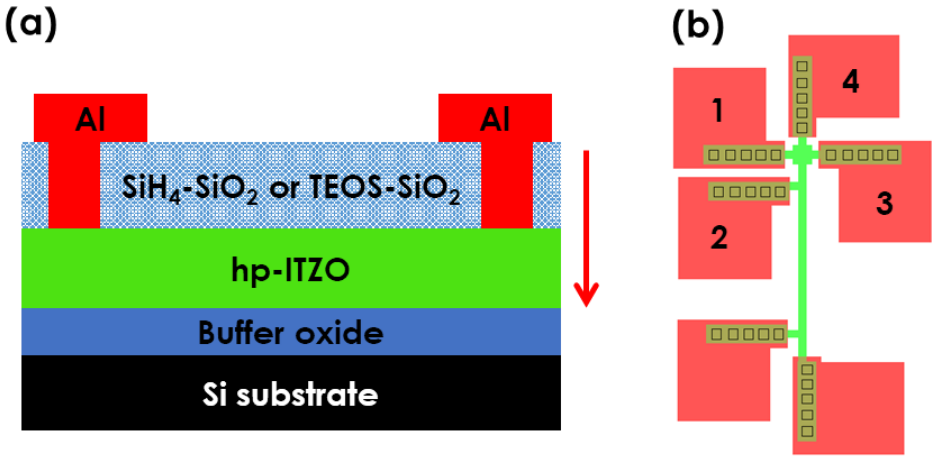

Figure 5-1: (a) Cross-sectional and (b) plan-view schematic diagram of the cross-bridge structure, where the hp-ITZO thin films are capped by SiH_4-SiO_2 layers or TEOS-SiO_2 layers.

Fig. 5-2 and Table 5-1 present the hp-ITZO thin film resistivity (ρ) as a function of oxygen

annealing duration at a temperature of 300 °C. It is clearly seen that the SiH_4-SiO_2- and the TEOS-SiO_2-capped hp-ITZO thin films own an initial resistivity of 1.45×10^{-3} Ω·cm and 1.09×10^{-2} Ω·cm, respectively, with the former thin films having a lower value. Assume that the hp-ITZO thin films in both types of samples hold a mobility μ of ~30 cm^2/Vs (Fig. 2-5(c)), then we can estimate the free electron concentration (n) inside referring to the equation below:

$$\rho = \frac{1}{qn\mu}, \tag{5-3}$$

where q is electron charge. The derived free carrier concentration in the hp-ITZO thin films before oxygen annealing is about 1.43×10^{20} cm^{-3} and 1.91×10^{19} cm^{-3}, respectively. Since the hp-ITZO thin films are 50 nm thick, the total dose of free electrons that is released by the dopants can be further approximated as 7.65×10^{14} cm^{-2} and 9.55×10^{13} cm^{-2}, respectively.

When annealed in the oxygen atmosphere, both types of the hp-ITZO thin films will present an increasingly higher resistivity without doubt. The TEOS-SiO_2-capped hp-ITZO thin films return to a high-resistivity state after 4-hour oxygen annealing, whereas the resistivity of the SiH_4-SiO_2-capped hp-ITZO thin films is nearly three orders of magnitude lower. The increase is presumably related to the oxygen deficiency compensation in the thin films [169, 170] and the hydrogen diffusion out of the thin films, as observed in other TG-SA MO TFTs with hydrogen-doped S/D regions [164]. However, the resistivity variation difference between these two types of samples after long-duration oxygen annealing is hard to explain by only the reason above.

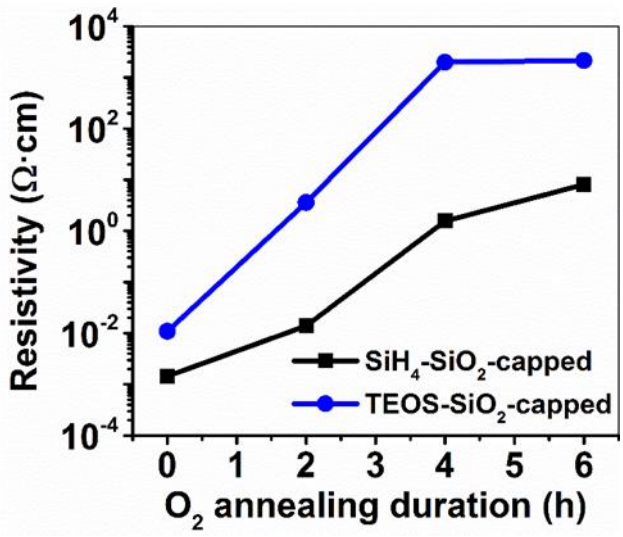

Figure 5-2: Resistivity of the SiH_4-SiO_2-capped or the TEOS-SiO_2-capped hp-ITZO thin films as a function of oxygen annealing duration at 300 °C.

Table 5-1: Resistivity of the SiH_4-SiO_2-capped or the TEOS-SiO_2-capped hp-ITZO thin films after different oxygen annealing durations at a temperature of 300 °C

Annealing duration (h)	**0**	**2**	**4**	**6**
Resistivity of SiH_4-SiO_2-capped thin films (Ω·cm)	1.45×10^{-3}	1.39×10^{-2}	1.56	8.08
Resistivity of TEOS-SiO_2-capped thin films (Ω·cm)	1.09×10^{-2}	3.56	1.98×10^{3}	2.14×10^{3}

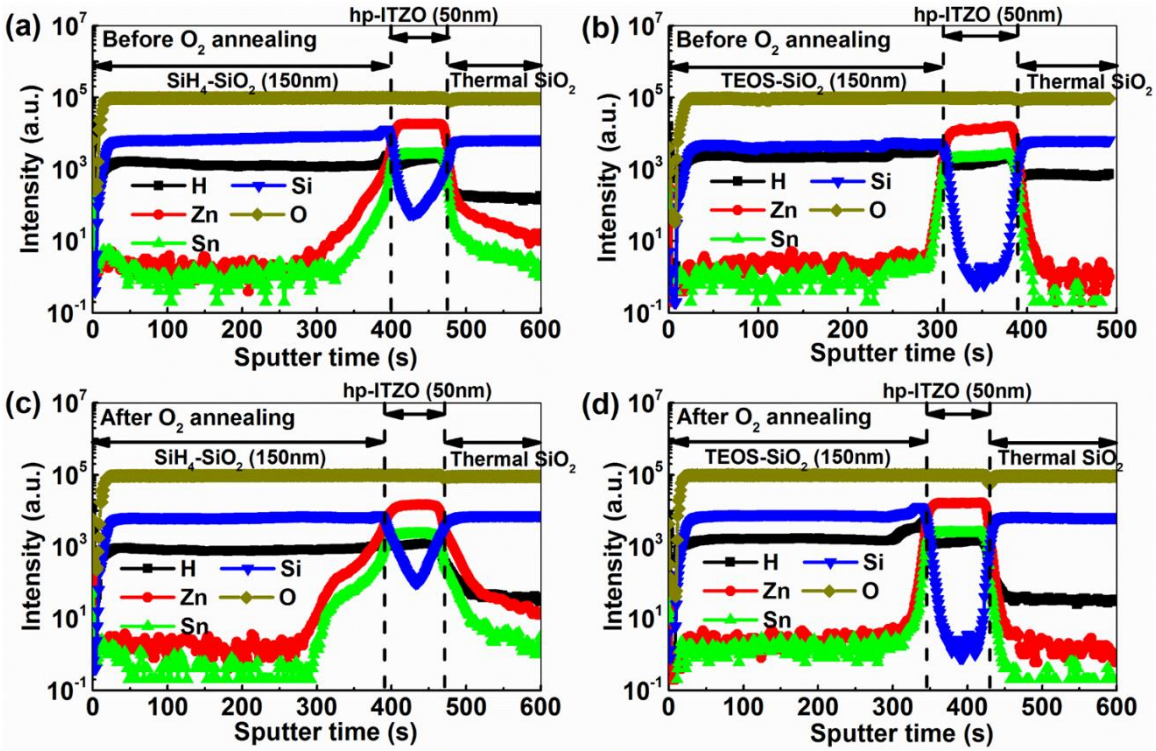

Figure 5-3: Depth profiles of major species in the hp-ITZO thin films capped by SiH_4-SiO_2 layers (a) before and (c) after 6-hour oxygen annealing at 300 °C, and by the TEOS-SiO_2 layers (b) before and (d) after 6-hour oxygen annealing at 300 °C.

The depth profiles of species along the thin-film stacks were then analyzed using the SIMS characterization (PHI 7200, Physical Electronics). Fig. 5-3(a) and (b) plot the depth profiles of several major species (along the arrow direction in Fig. 5-1(a)) in the samples before oxygen annealing. The hydrogen species are found to pile up at the interfaces between both the PECVD SiO_2 layers and the hp-ITZO layers. However, according to the reactions that occurred in each PECVD process, most hydrogen species in the SiH_4-SiO_2 exist as SiH_x radicals, while they are H_2O and Si-OH forms in the TEOS-SiO_2 [141]. Therefore, the SiH_4-SiO_2 deposition can result in more shallow donors and contribute to the hp-ITZO thin films with higher conductivity [171, 172].

From Fig. 5-3(a) and (c), it is also clearly seen that there is a mutual penetration phenomenon between the SiH_4-SiO_2 layers and the hp-ITZO layers, causing ambiguous interfaces. After 6-hour oxygen annealing at 300 °C, the detected penetration degree becomes more significant compared with that in the as-deposited thin film stacks. The acceleration is consistent with the increase of thermal budget. In contrast, regardless of whether oxygen annealing is conducted or not, the penetration in the TEOS-SiO_2-capped samples is always slight according to Fig. 5-3(b) and (d). As known, silicon ions are capable of substituting zinc cation sites and release free carriers in ZnO [173-176]. Therefore, though the following oxygen annealing will raise the resistivity of both the SiH_4-SiO_2-capped and the TEOS-SiO_2-capped hp-ITZO thin films, the existence of silicon dopants weakens the effect of oxygen annealing and slows down the resistivity increase of the SiH_4-SiO_2-capped hp-ITZO thin films. Then, the resistivity variation difference between these two types of thin film stacks can be reasonably explained. In terms of the dose of silicon dopants, it can be estimated according to Eq. (5-3). The resistivity ρ of the SiH_4-SiO_2-capped hp-ITZO thin films for approximation is chosen as 8.08 Ω·cm. It corresponds to the result of 6-hour oxygen annealing, because most of the hydrogen dopants will diffuse to elsewhere after long-term annealing, while most of the silicon dopants with lower diffusion coefficient will remain in the hp-ITZO thin films to realize the long-standing low-resistivity state. Herein, the mobility μ is still assumed as ~30 cm^2/Vs. Then, the electron concentration and its total dose in 50-nm-thick thin films can be derived as 2.6×10^{16} cm^{-3} and 1.37×10^{11} cm^{-2}, respectively. If every silicon dopant releases two electron by substitute a zinc cation site, the total dose of silicon dopants should be about 6.85×10^{10} cm^{-2}.

In Fig. 5-2, it is noted that the resistivity of the SiH_4-SiO_2-capped hp-ITZO thin films after oxygen annealing treatment for ≤2 h (≤1.39×10^{-2} Ω·cm) is much lower than that of the TEOS-SiO_2-capped hp-ITZO thin films after O_2 annealing treatment for ≥4 h (≥1.98×10^{3} Ω·cm). Their resistivity difference can reach as high as five orders of magnitude. Therefore, it is possible to adopt the thin films in these two conditions as the intrinsic channels and the highly conductive S/D regions of the TG-SA hp-ITZO TFTs, separately.

5.2 Contact Resistance

To employ SiH_4-SiO_2-capped hp-ITZO thin films as the highly conductive S/D regions of TG-SA TFTs seems to be promising but still requires further verification. As shown in Fig. 5-4(a), the total resistance in the S/D regions consists of parasitic resistance (R_p) along the conductive MO S/D regions and contact resistance (R_c) between the MO semiconductors and the contact pads. Although the value of R_p herein is shown to be small, the information about

R_c is still unknown. Therefore, the contact resistance between the conductive hp-ITZO regions and the Al contact pads was then characterized through a Kelvin resistor structure, the schematic diagram of which is illustrated in Fig. 5-4(b). The fabrication process is the same as that of the cross-bridge structure. The contact resistance was measured by applying a proper current I_{13} between Pad 1 and 3 and meanwhile detecting the voltage difference V_{24} between Pad 2 and 4. Then, the contact resistance (R_{kelvin}) in the Kelvin resistor and specific contact resistance (ρ_c) between the conductive hp-ITZO regions and the Al contact pads were equal to

$$R_{kelvin} = \frac{V_{24}}{I_{13}}, \tag{5-4}$$

and

$$\rho_c = R_{kelvin} \times A_{kelvin}, \tag{5-5}$$

where A_{kelvin} is the contact size (10 μm × 10 μm). Then, ρ_c is divided by the contact size A_c (180 μm × 180 μm) in the TG-SA TFTs, and the actual contact resistance R_c can be obtained. The results of ρ_c and R_c with different oxygen annealing durations at 300 °C are presented in Fig. 5-5 and Table 5-2. It is clearly seen that the contact resistance in the TG-SA hp-ITZO devices is low enough so that the on-state current of the TFTs will not be clamped. With the extension of thermal annealing duration, the variation is also slight. Therefore, it is believed the implementation of TG-SA hp-ITZO TFTs is highly possible via our own proposed solution.

Table 5-2: Contact resistance between the conductive hp-ITZO regions and the Al contact pads after different oxygen annealing durations at 300 °C

Annealing duration (h)	**0**	**2**	**4**	**6**
Contact resistance in Kelvin resistor structure R_{kelvin} (Ω)	277.7	357.5	1073.9	1023.6
Specific contact resistance ρ_c (Ω·cm^2)	2.78×10^{-4}	3.58×10^{-4}	1.07×10^{-3}	1.02×10^{-3}
Contact resistance in TG-SA TFTs R_c (Ω)	0.86	1.10	3.31	3.16

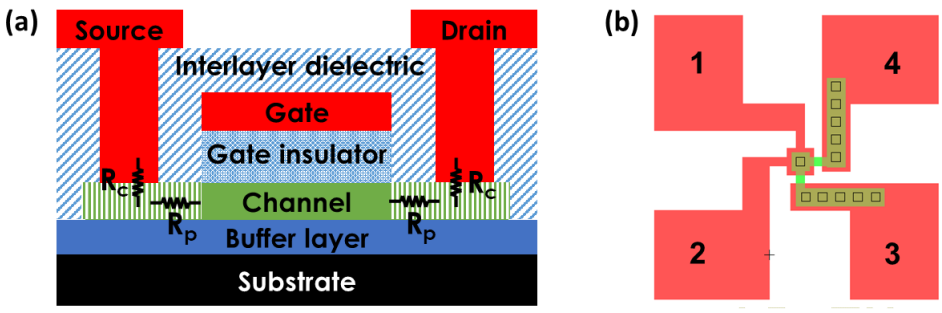

Figure 5-4: Schematic diagrams of (a) contact and parasitic resistances in the TG-SA MO TFTs, and (b) the Kelvin resistor structure.

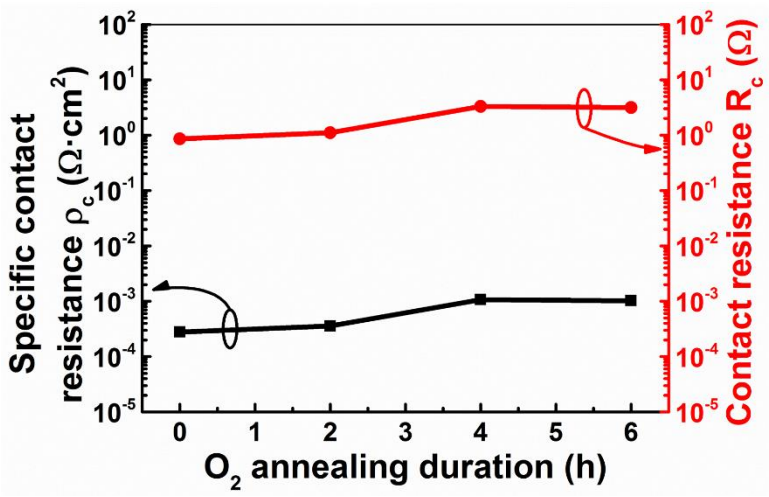

Figure 5-5: Specific contact resistance and actual contact resistance between the conductive hp-ITZO S/D regions and the Al contact pads in the TG-SA TFTs as a function of oxygen annealing duration at 300 °C.

5.3 Fabrication Process

As shown in Fig. 5-6, the entire process of the TG-SA hp-ITZO TFTs started from 4-inch p-type silicon wafers coated with 500-nm-thick thermally grown SiO_2. 50-nm-thick hp-ITZO channel layers were then deposited by co-sputtering the pc-ITO target and the pc-ZnO target. The detailed deposition conditions have been described in Chapter 3. Next, the channel layers were patterned into active islands by wet etch in diluted hydrofluoric acid, followed by 150-nm-thick stacked PECVD SiO_2 gate insulator deposition. The stacked gate insulators consisted of 50-nm-thick SiH_4-SiO_2 with 100-nm-thick TEOS-SiO_2 underneath. Afterwards, 200-nm-thick aluminum was sputtered and patterned as the gate electrodes. After photoresist removal, the aluminum gate electrodes served as hard masks for the definition of S/D regions, which were then exposed via dry etching the stacked gate insulators above. After the 1st oxygen annealing treatment at 300 °C for 2 h to improve the stacked gate insulator island quality and gain the channel resistivity, 150-nm-thick SiH_4-SiO_2 was deposited as the interlayer dielectrics (ILDs). At this moment, the exposed S/D regions were highly conductive. Next, the contact holes were opened using the RIE technique in CHF_3 plasma, followed by 300-nm-thick aluminum test pad deposition and patterning. Last, the 2nd oxygen post-annealing treatment was carried out at 300 °C. The annealing durations lasted from 0 h to 2 h, 4 h and 6 h. Over all, the whole fabrication process could be completed at a temperature of no more than 300 °C. The electrical characteristics of the TFTs were measured with a dark probe station using a semiconductor parameter analyzer (Agilent 4156C).

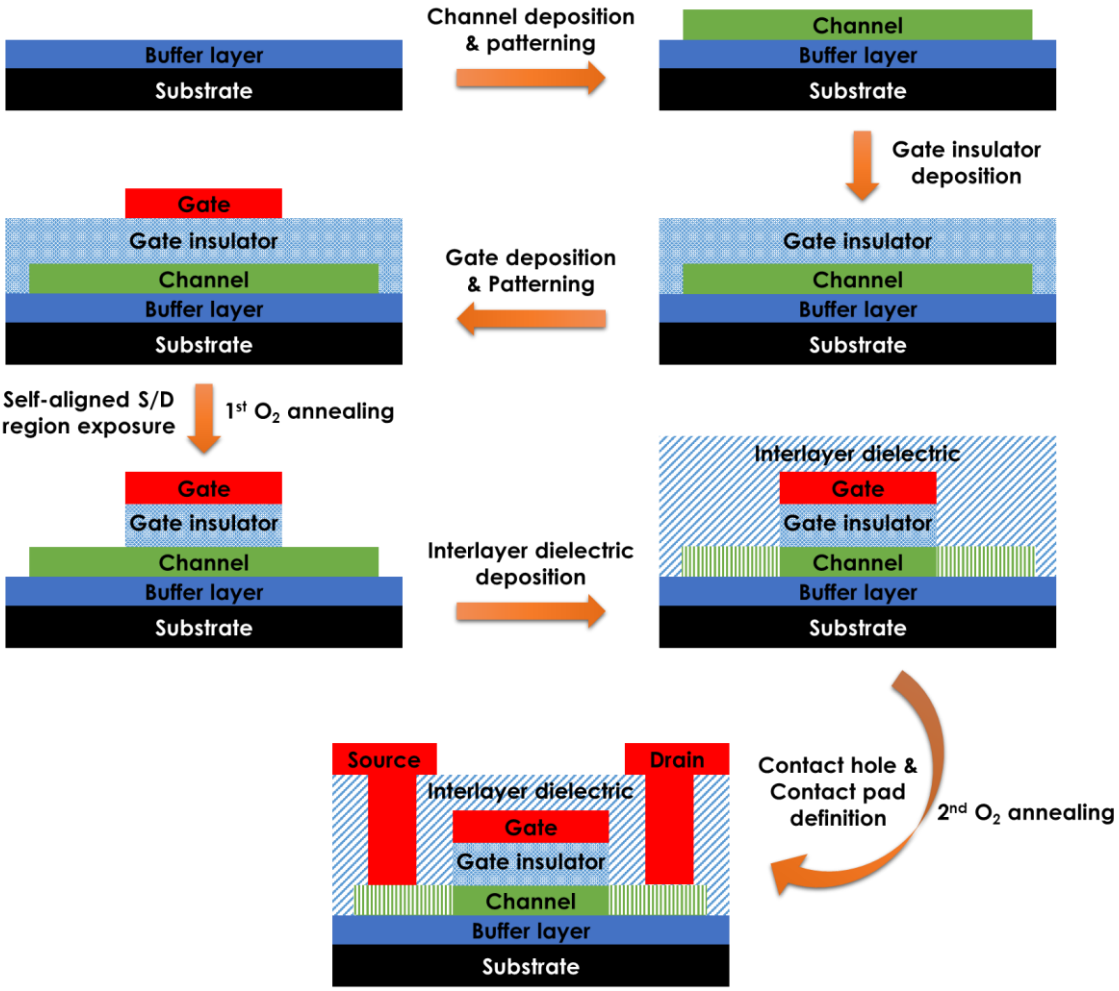

Figure 5-6: Process flow of the TG-SA hp-ITZO TFTs.

5.4 Device Characterizations

The transfer curves of the TG-SA hp-ITZO TFTs are shown in Fig. 5-7. Herein, the 1st oxygen annealing duration is fixed at 2 h, while the 2nd oxygen annealing duration varies from 0 h to 6 h. It is clearly seen that the device performance is sensitive to the oxygen annealing duration, so the differentiated O_2 annealing strategy should be feasible. If the devices are tested without the 2nd oxygen post-annealing treatment, it will be hard to observe their switching behavior. This is because the TEOS-SiO_2-capped channels still perform with low resistivity after 2-hour oxygen annealing (Table 5-1). On the other hand, if the 2nd oxygen post-annealing duration exceeds 2 h, the on-state current of the devices will be deteriorated owing to the continuous growth of resistivity in the SiH_4-SiO_2-capped S/D regions. Therefore, the optimal duration for the 2nd oxygen post-annealing in this work should be around 2 h. Accordingly, the increase of contact resistance is also very slight (Table 5-2).

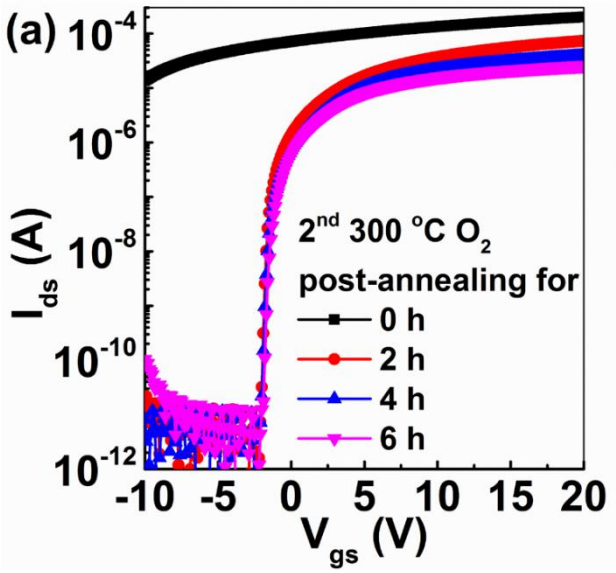

Figure 5-7: Transfer curves of the TG-SA hp-ITZO TFTs. Herein, the 1st oxygen annealing duration is fixed at 2 h, while the 2nd oxygen post-annealing lasts from 0 h to 6 h.

The transfer and output curves of the optimal TG-SA TFTs are plotted in Fig. 5-8. The devices can exhibit good electrical performance with an average μ_{fe} of 19.56 cm^2/Vs, V_{th} of -1.65 V, SS of 105 mV/decade, and on-off ratio of over 10^7. Unsatisfactorily, the TFTs are operated in the depletion mode, which is less popular for low-power-consumption applications. The depletion mode is partially caused by the diffusion of hydrogen species into the channel regions during the SiH_4-SiO_2 ILD layer deposition and the following annealing process. So, more negative gate bias is required to deplete all the free carriers. In terms of the output curves, the clear pinch-off and the saturation of drain current at high drain voltage reflect that the hp-ITZO channels can be efficiently controlled by the gate and drain electrodes. It should be noted that there is a slight current crowding effect at low drain voltage, indicating the imperfect S/D contacts. However, it is quite satisfying to observe that these devices still perform well even after the 2nd oxygen post-annealing treatment for several hours. Compared with the other MO TFTs with hydrogen-doped S/D regions [165], our devices are more robust to the following thermal treatments. This is a very attractive feature, because long-term annealing can contribute to the channel bulks and the GI/AC interfaces with higher quality. Therefore, our TG-SA hp-ITZO TFTs are shown to present the sharpest SS among the published counterparts. In addition, compared with other types of TG-SA MO TFTs in Table 5-3, not only can the photolithography step for the definition of S/D electrodes be eliminated, but also the extra processes for the formation of highly conductive and thermally stable S/D regions at the same time. This will lead to more cost-effective manufacturing.

Table 5-3 Comparison of our TG-SA hp-ITZO TFTs with other types of TG-SA MO TFTs

	[177]	[178]	[179]	[180]	[181]	This work
Channel	a-IGZO	a-IGZO	a-IGZO	a-IZO	a-ITZO	hp-ITZO
Post-transitional-metal at.%	>40%*	>40%*	>33%*	>50%*	>56%*	41.3%
Mobility (cm^2/Vs)	9.8	12.49	9.2	16.84	27.0	19.56
V_{th} (V)	-1.5	-0.57	-1.5	0.22	-1.5	-1.65
SS (V/decade)	0.22	0.39	0.3	0.14	0.40	0.105
On-off ratio	$>10^9$	$>10^7$	$>10^7$	$>10^9$	$>10^8$	$\sim10^8$
Gate-bias stress	~0.1 V (PBS, 10 ks)	0.08 V (PBS, 1 h); -0.14 V (NBS, 1 h)	~0.4 V (PBS, 10 ks); ~-1.5 V (NBS, 10 ks)	0.05 V (PBS, 1 h); -0.04 V (NBS, 1 h)	~0.5 V (PBS, 10 ks); ~-1.5 V (NBS, 10 ks)	-0.2 V (PBS, 10 ks); -0.35 V (NBS, 10 ks)
Process for S/D region formation	Thin Al layer deposition	Ar plasma treatment	H doping	Thin Al layer deposition	H plasma treatment	Si and H doping
Remarks	Low yield, non-uniformity	Poor SS, high leakage	Limited temperature (<240 °C)	Low yield, non-uniformity	Poor SS, high leakage, limited thermal budget	Thermally stable, no extra processes for S/D region formation

The excellent stability of the optimal TG-SA hp-ITZO TFTs against gate-bias stress is presented in Fig. 5-8. During the tests, the S/D pads were grounded, and the applied gate bias for PBS and NBS were set to (V_{th}+20) V and (V_{th}-20) V, respectively, for 10 000 s. There is no stretch-out phenomenon observed in the subthreshold region of the transfer curves, indicating that few defects are generated during the stress tests. Meanwhile, all the transfer curves are almost overlapped, except for a slight on-state current decrease after the NBS test due to the S/D region degradation.

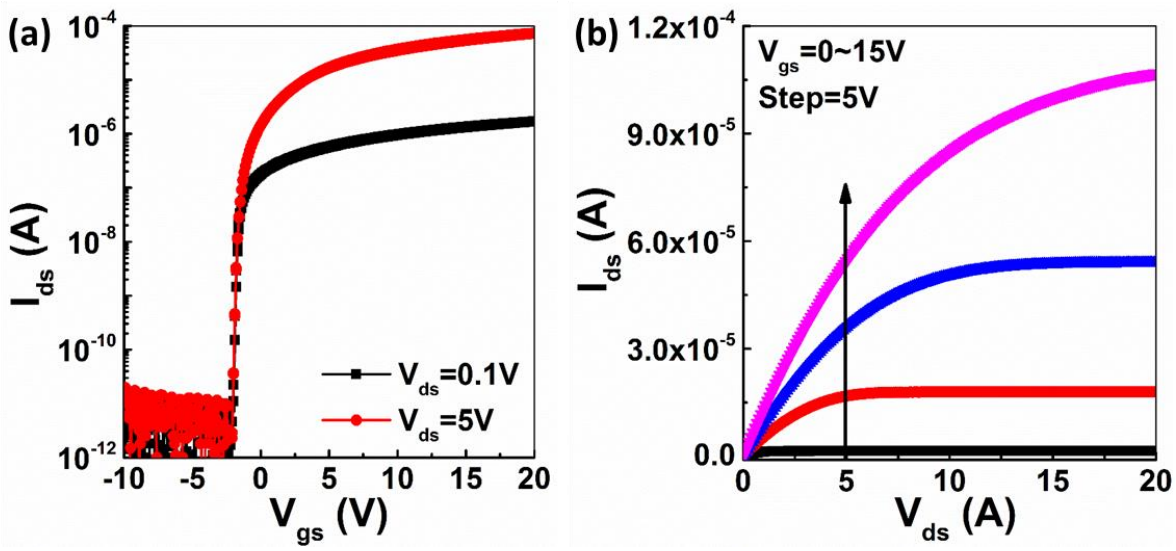

Figure 5-8: (a) Transfer and (b) output curves of the optimal TG-SA hp-ITZO TFTs.

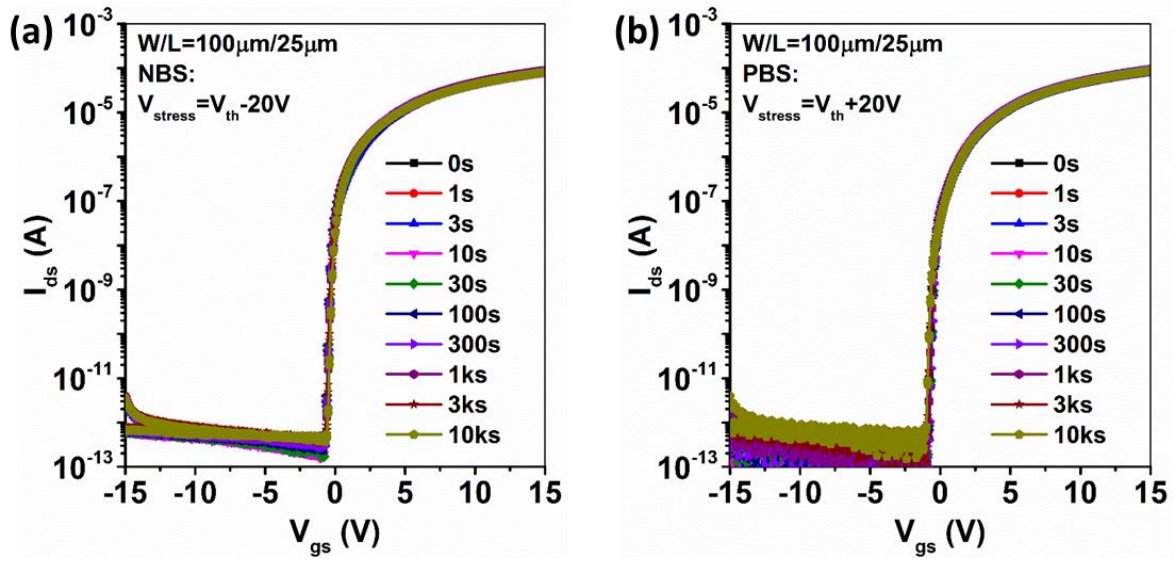

Figure 5-9: Transfer curve evolution of the optimal TG-SA hp-ITZO TFTs under (a) NBS and (b) PBS tests for 10 000 s.

So far, we have successfully fabricated the hp-ITZO TFTs at a temperature of 300 °C, whether their architecture is TG-BC or TG-SA. It is believed to touch the floor level of processing temperature for high-performance and reliable TFTs with sputtered MO channels. Referring to [182-184], ion bombardments during the sputtering process will introduce internal stresses and generate extra electron traps in the MO films. For structural relaxation and then defect reduction, the channels always require a post-deposition annealing process. If only the thermal annealing is employed, the suggested temperature should be no less than 300 °C. Otherwise, the devices will be hard to activate for improved stability and negligible hysteresis. In practice, since the high-quality dielectrics is typically deposited at 380 °C using the industrial

PECVD techniques, the thermal annealing temperature is usually set at ~400 °C. However, over high temperature is not suitable for the fabrication of MO TFTs on flexible substrates, and it demands thermal budget as low as possible. So far, there have emerged many advanced annealing technologies [185-189] for post-annealing temperature reduction, but it is found that the corresponding MO TFTs suffer from inferior electrical characteristics (e.g., higher leakage current, larger SS) and electrical stability against gate-bias stress in comparison with those devices treated by the conventional high-temperature thermal annealing. If the dielectric deposition temperature follows the post-annealing temperature, the devices will behave even worse. Above all, to guarantee both satisfied device performance and suppressed thermal budget, it is reasonably compulsory to decrease the entire processing temperature towards ~300 °C regardless of annealing methods. Perfectly, our top-gate hp-ITZO TFTs can well meet this target.

Compared with other MO TFT counterparts such as elevated-metal metal-oxide (EMMO) TFTs with a-IGZO channels processed at 300 °C [190, 191], the superiorities of hp-ITZO TFTs include the following six aspects: (1) The thermal annealing atmospheres for the hp-ITZO TFTs and the EMMO a-IGZO TFTs are atmospheric air and pure oxygen, respectively. Additionally, the former ones require much shorter annealing time (~2 h). Thus, it is possible to enable cost-effective manufacturing. (2) The field-effect mobility of top-gate hp-ITZO TFTs (~18 cm^2/Vs) is obviously higher than that of EMMO a-IGZO TFTs (~8 cm^2/Vs) owing to the collaborative modification of channels. (3) Thanks to the involvement of PECVD SiO_2 stacks, the gate insulators of hp-ITZO TFTs possess significantly enhanced quality even though they are deposited at 300 °C, rather than 380 °C. Together with the intrinsically high quality of channels and interfaces, they can contribute to the hp-ITZO TFTs with steeper subthreshold swing (~0.1 V/decade) compared with their counterparts (~0.3 V/decade). (4) For most of a-IGZO TFTs processed at 300 °C, they are often operated in the depletion mode with negative threshold voltage, while the hp-ITZO TFTs can freely choose their operation mode via gate electrode engineering. This is preferable in low-power-consumption applications. (5) The hp-ITZO TFTs are free of hysteresis and short-channel effects. There is no threshold voltage shift even though the channel length is reduced to 2 μm, while the critical channel length for the EMMO a-IGZO TFTs without fluorination treatments is 10 μm. (6) The top-gate hp-ITZO TFTs processed at 300 °C can show more robust electrical stability than the EMMO a-IGZO TFTs processed at 300 °C. For example, the former ones exhibit almost no threshold voltage shift in the PBS/NBS tests ((V_{th}+20) V / (V_{th}-20) V, 10000 s), while the latter ones under the

same stress tests show a threshold voltage shift of 0.3 V and 0.2 V, respectively.

5.5 Chapter Summary

In this chapter, it has been found that the hp-ITZO thin films that are capped by a SiH_4-SiO_2 layer can maintain a low-resistivity state after long-duration oxygen annealing, while the hp-ITZO thin films that are capped by a TEOS-SiO_2 layer will return to a high-resistivity state. Apart from hydrogen-related factors, the unexpected silicon-doping phenomenon along with the SiH_4-SiO_2 deposition process is also responsible for the durable low-resistivity state. Then, via combining two different types of PECVD SiO_2 and adopting differentiated oxygen annealing strategies, the TG-SA hp-ITZO TFTs have been successfully fabricated. The devices can exhibit good electrical characteristics as well as robust stability against gate bias stress and thermal processing. In this chapter, apart from one photolithography step for the definition of S/D electrodes, extra processes for the formation of conductive S/D regions can be omitted as well. This is very promising for more cost-effective manufacturing.

Chapter 6 Applications of Hybrid-Phase Indium-Tin-Zinc Oxide Thin-Film Transistors

As known, TFT technology is applicable in many fields, including but not limited to display backplanes, integrated circuits [192-194] and sensors [195-197]. According to the previous chapters, hp-ITZO TFTs have been available with various architectures, and all of them can exhibit relatively high electrical characteristics such as remarkably boosted field-effect mobility, substantially steep subthreshold swing, and extremely low leakage current. When they are employed in practical applications, their advantages should be of high value and can contribute to better performance. In this chapter, we will attempt to implement several types of integrated circuits for transparent electronics and demonstrate a 2.2-inch AMOLED display panel using our hp-ITZO TFT technology. Considering limited device scalability and yield in our lab, the relatively more reliable TG-BC TFTs will be chosen as building blocks to participate in these applications at the present stage. To predict circuit/system performance prior to fabrication, compact models for the related TFTs will be extracted for future simulation.

6.1 Integrated Circuits

6.1.1 Compact Thin-Film Transistor Model

Regardless of what kind of applications our hp-ITZO TFT technologies serve, it is a common practice for designers to perform circuit simulation before a successful tape-out. Therefore, a robust compact model, which precisely describes TFT electrical behaviors and accurately predicts circuit performance in simulators, is highly demanded to enable efficient design with low cost and short time. So far, there are many TFT models that have been proposed and are available in circuit simulators. For example, the HSPICE Level = 40 was customized for TFTs by Synopsys [198]; C. Perumal *et al.* modified the unlicensed MOSFET SPICE Level = 3 model template [199]; Rensselaer Polytechnic Institute developed the RPI-aTFT and RPI-pTFT model for amorphous silicon and polysilicon TFTs, respectively [200]. However, their initial targets are to serve silicon-based TFT technologies. When these models are employed for metal oxide TFT circuit simulation, the results may not be very accurate, because physical descriptions in the silicon-based TFT models sometimes cannot well match the MO TFTs.

In order to represent the electrical behaviors of our TG-BC hp-ITZO TFTs, we tried to optimize the currently available silicon-based TFT model in commercial simulators.

Considering the hybrid-phase crystal morphology in the channels, the pristine compact model adopted for empirical fitting herein is RPI-pTFT (Level = 36) rather than RPI-aTFT (Level = 35). In practice, the simulated results based on the former model show it is indeed more accurate compared to the later one. After the global extraction procedure, we can obtain the modified RPI-pTFT model parameters for the description of our TG-BC hp-ITZO TFTs. The results for the Al-gated devices are listed in Table 6-1 (the results for the ITO-gated TFTs are not shown here). In general, these parameters can be separated into five parts (i.e., leakage current parameters, subthreshold current parameters, above threshold regime parameters, temperature parameters, and capacitance parameters). Although most of the temperature parameters and the capacitance parameters are defaulted due to data insufficiency, the simulated static characteristics based on the extracted parameters can still precisely describe the measured results. Fig. 6-1 plots the simulated and the measured transfer/output curves together, and it is found that these curves overlap well with each other. The RMS error in the I_{ds}-V_{gs}, log(I_{ds})-V_{gs} and I_{ds}-V_{ds} curves is only 0.80%, 0.75% and 1.04%, respectively. Therefore, the modified RPI-pTFT model is believed to be eligible for the following highly precise circuit simulation using our TG-BC hp-ITZO TFTs.

Table 6-1: List of parameters in the modified RPI-pTFT model for the description of TG-BC TFTs with Al gate electrodes and hp-ITZO channels

Leakage Current Parameters			
Parameter	**Unit**	**Value**	**Description**
BLK	mV	1e-10	Leakage barrier lowering constant
DD	m	1.5e-7	V_{ds} field constant
DG	m	2e-7	V_{gs} field constant
EB	eV	0.68	Barrier height of diode
I0	A/m	6	Leakage scaling constant
I00	A/m	70	Reverse diode saturation
Subthreshold Current Parameters			
Parameter	**Unit**	**Value**	**Description**
AT	m/V	0	DIBL parameter 1
BT	m*V	2.1e-6	DIBL parameter 2
ETA	-	2.2	Subthreshold ideality factor

VSI	V	2	First parameter for V_{gs} dependent
VST	V	2	Second parameter for V_{gs} dependent
MUS	$cm^2/(Vs)$	1	Subthreshold mobility

Above Threshold Regime Parameters

Parameter	Unit	Value	Description
VTO	V	-1.3	Zero-bias threshold voltage
VON	V	0	On voltage
ASAT	-	1.11	Proportionality constant of V_{dsat}
LASAT	m	0	Coefficient for length dependence of ASAT
MMU	-	0.395	Low field mobility exponent
MU0	$cm^2/(Vs)$	20	High field mobility
MU1	$cm^2/(Vs)$	0.063	Low field mobility parameter
LKINK	m	2.5e-6	Kink effect constant
VKINK	V	6.5	Kind effect voltage

Temperature Parameters

Parameter	Unit	Value	Description
TNOM	^oC	25	Nominal (room) temperature
DVTO	-	0	Temperature coefficient of VTO
DASAT	-	0	Temperature coefficient of ASAT
DMU1	-	0	Temperature coefficient of MU1

Capacitance Parameters

Parameter	Unit	Value	Description
TOX	m	5e-8	Oxide thickness
CGDO	F/m	0	Gate-drain overlap
CGSO	F/m	0	Gate-source overlap
ETAC00	-	0	Capacitance subthreshold coefficient factor of drain bias
MC	-	3	Capacitance knee shape parameter

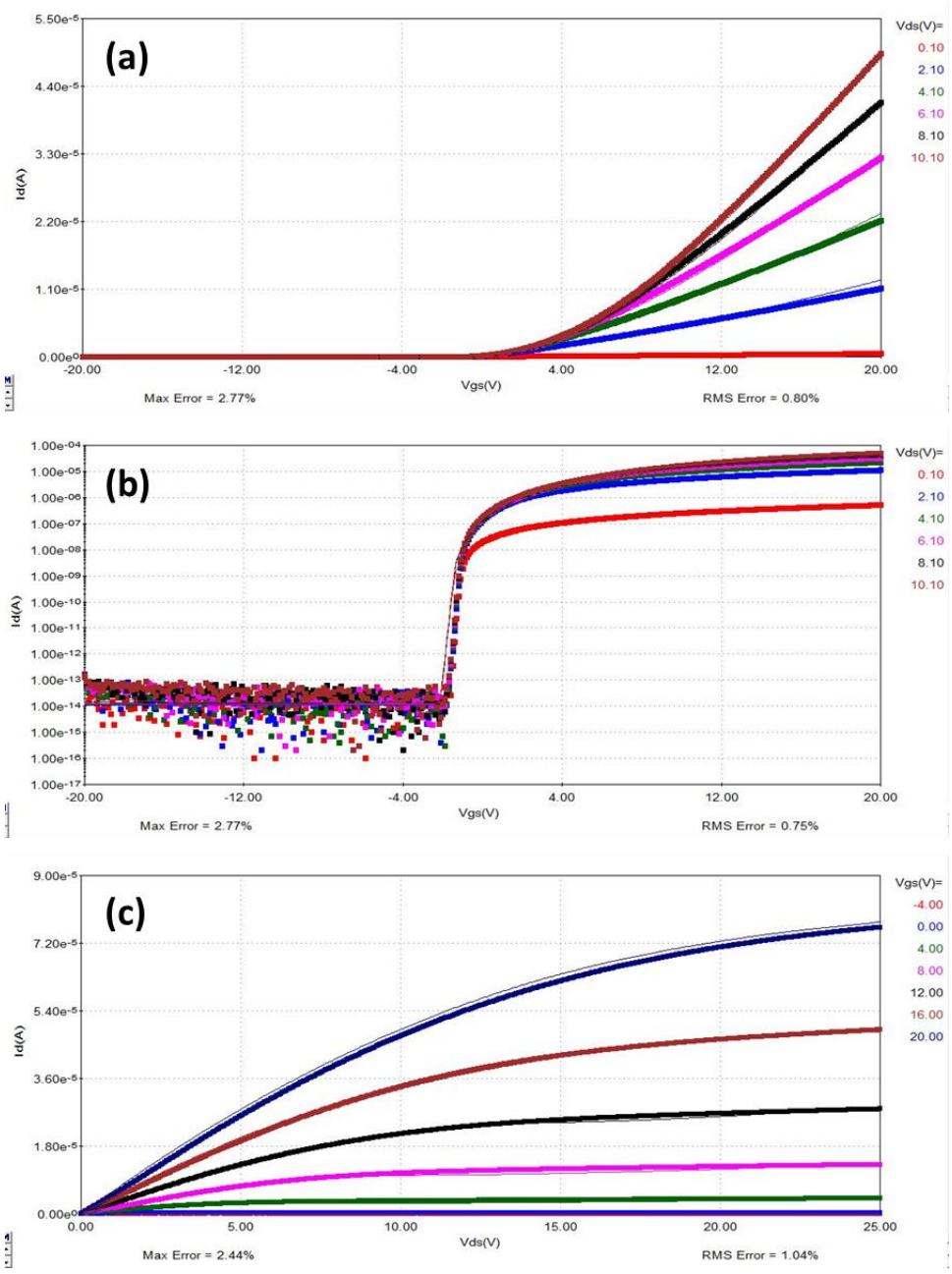

Figure 6-1: Simulated (solid) and measured (dots) (a) I_{ds}-V_{gs}, (b) log(I_{ds})-V_{gs} and (c) I_{ds}-V_{ds} curves of the TG-BC TFTs with Al gate electrodes and hp-ITZO channels. The channel width and length are both 10 μm.

6.1.2 Fundamental Digital Circuits

Transparent electronics is one of popular topics in the development roadmap of electronics technologies. In many applications such as see-through displays, smart windows and wearable electronics, transparent circuits are highly demanded. Considering our TG-BC hp-ITZO TFTs with ITO gate electrodes, all the layers in the devices are highly transparent. Meanwhile, they also present many merits such as high mobility, sharp subthreshold swing and extremely low

leakage current. Therefore, they should be promising as the building blocks of transparent circuits. In this subsection, we would like to share some of the preliminary progresses in the implementation of fundamental digital circuits for transparent electronics. Since the ITO-gated TFTs are unipolar, a pseudo-CMOS design [201, 202] is adopted to make circuit performance more comparable to their dual-V_{th} complementary-type counterparts.

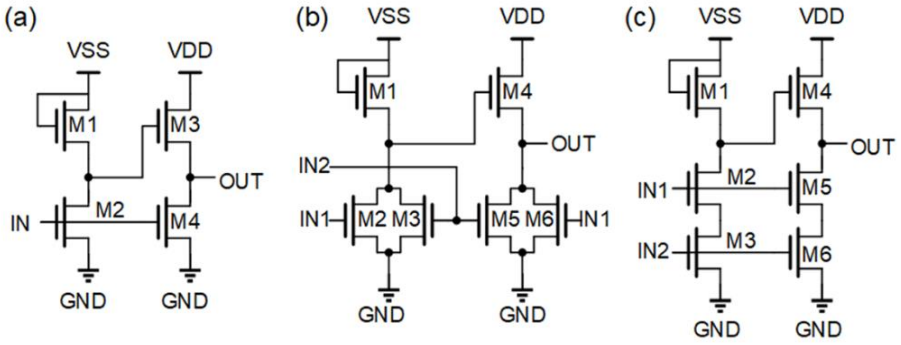

Figure 6-2: Circuit diagrams of (a) an inverter, (b) a NOR gate and (c) a NAND gate based on the pseudo-CMOS design.

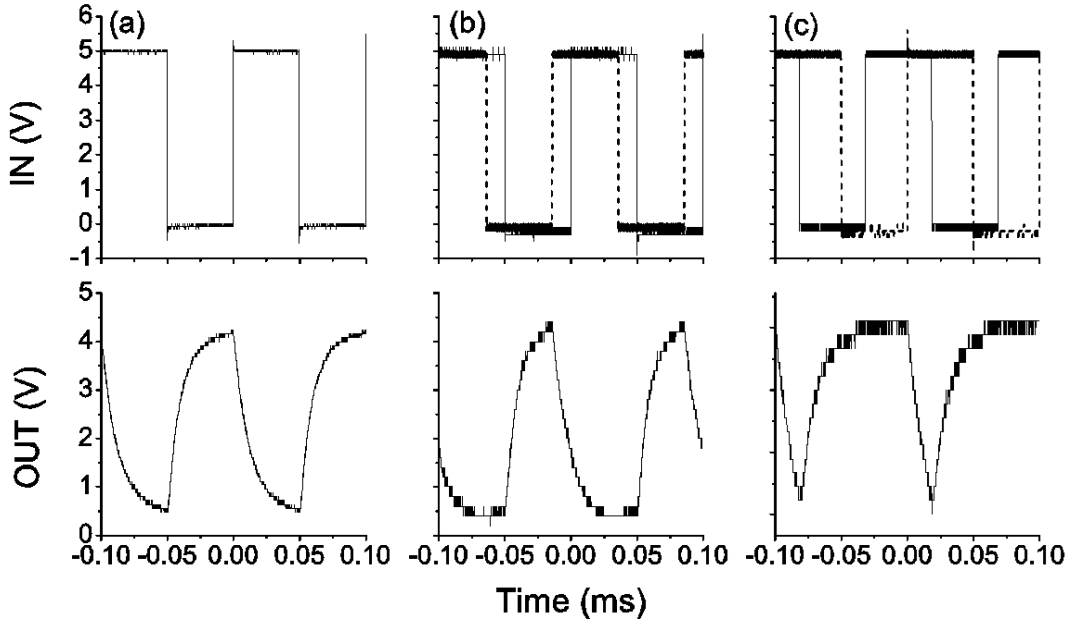

Figure 6-3: Measured waveforms of (a) the inverter, (b) the NOR gate, and (c) the NAND gate with 10 kHz inputs at V_{DD} = 5 V and V_{SS} = 10 V.

For combinational digital circuits, we mainly focus on several specific logic gates including inverters, NOR gates and NAND gates. Originating from them, any other circuits can be further implemented. Fig. 6-2 shows circuit diagrams of a pseudo-CMOS inverter, NOR gate and NAND gate. For the inverter, the channel width of M1-M4 is 20, 160, 160, and 160 μm, respectively. For the NOR gate, the channel width of M1-M6 is 20, 160, 160, 160, 160, and

160 μm, respectively. For the NAND gate, the channel width of M1-M6 is 20, 320, 320, 160, 320, and 320 μm, respectively. In theory, V_{SS} should be higher than $V_{DD}+2V_{th}$ in order to ensure that the high level of the output is equal to V_{DD} [202]. For simplicity, V_{SS} is directly set as $2V_{DD}$ herein. As shown in Fig. 6-3, the measured waveforms verify the correct Boolean functions of the logic gates with 10 kHz inputs at V_{DD} = 5 V and V_{SS} = 10 V. For the pseudo-CMOS inverter, its voltage transfer characteristics at different V_{DD} are further plotted in Fig. 6-4(a). When V_{DD} is set as 10 V, the inverter gain, switching threshold voltage (V_M), low noise margin, high noise margin, transition width and logic swing can be extracted as 2.75 V/V, 4.8 V, 2.14 V, 3.60 V, 3.77 V, 9.52 V, respectively. According to Fig. 6-4(b), its crossing current during operation is smaller than that of the pseudo-CMOS inverters based on a-IGZO TFTs [203], indicating better swing performance and potentially lower operation power consumption.

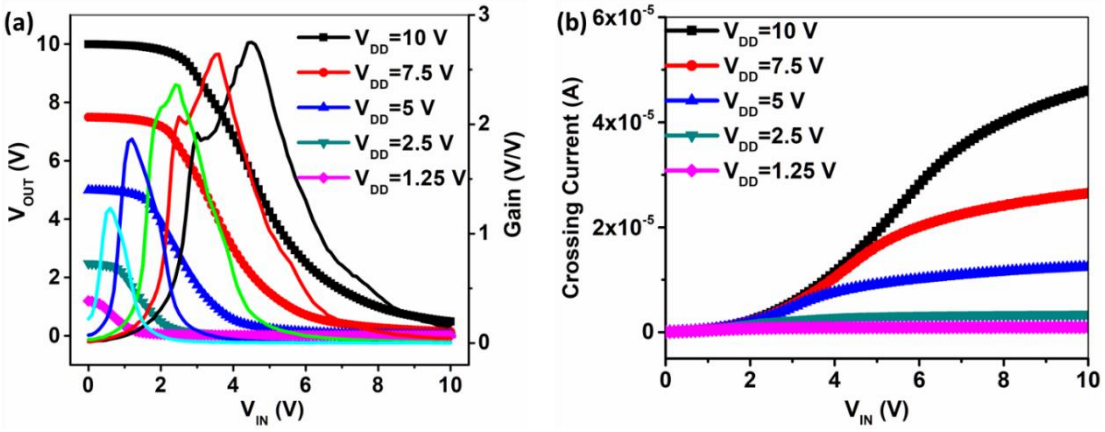

Figure 6-4: (a) Voltage transfer characteristics, internal gain, and (b) crossing current of the pseudo-COMS inverter at different V_{DD}.

For sequential digital circuits, a D latch and a falling edge triggered D flip-flop (DFF) have been built based on the NOR gates as mentioned above. Fig. 6-5 and Fig. 6-6 present their circuit diagrams and measured output waveforms. It is clearly seen that their functions are both logically correct with 10 kHz inputs. For the D latch, its output (Q) can follow the inputted data signal (D) when the clock signal (CLK) stays logic 0. When the CLK becomes logic 1, the output can hold its previous state. For the falling edge triggered DFF, its output can latch the input value at the falling edge of CLK. Typically, the measured logic 1 and logic 0 are 4.3 V and 500 mV, respectively. These are slightly different from the simulated results. The degradation of the output swing is mainly caused by the oscilloscope with a resistive load of 1 MΩ. However, the output waveform distortion is still acceptable even though the input signal frequency rises to 10 kHz. Above all, it is concluded that the operation frequency of both combinational and sequential digital circuits can exceed 10 kHz, which is higher than that of

fully transparent circuits based on a-IGZO TFTs [204, 205]. This is presumably thanks to the adoption of pseudo-CMOS design, the optimal layout design of circuits and the possibly higher mobility that is provided by the hp-ITZO channels. Currently, the channel length (10 μm) and the gate-to-source/drain overlap (5 μm) of the TFTs are still quite large. It is expected that the circuit performance can be further improved via scaling down the channel dimension and reducing parasitic capacitance from layout design. Fig. 6-7 presents a photograph of these basic digital circuits on a 4-inch circular glass substrate. The measured optical transmittance is shown to vary from 77% to 92% within the entire visible wavelength band (380-800 nm). This indicates a relatively high transparency of the circuits, which are promising building blocks for transparent electronics. Based on these fundamental digital circuits, the related implementation of completed functional modules and systems is in process. Designing and fabricating advanced analog and digital integrated circuits for transparent and flexible electronics using the hp-ITZO TFT technology will be also a part of future work.

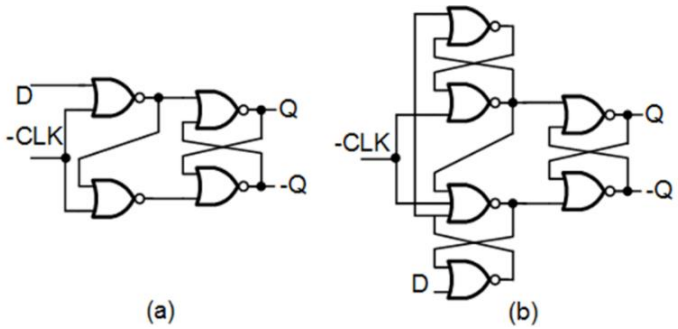

Figure 6-5: Circuit diagrams of (a) a D latch and (b) a falling edge triggered DFF based on the pseudo-CMOS NOR gates.

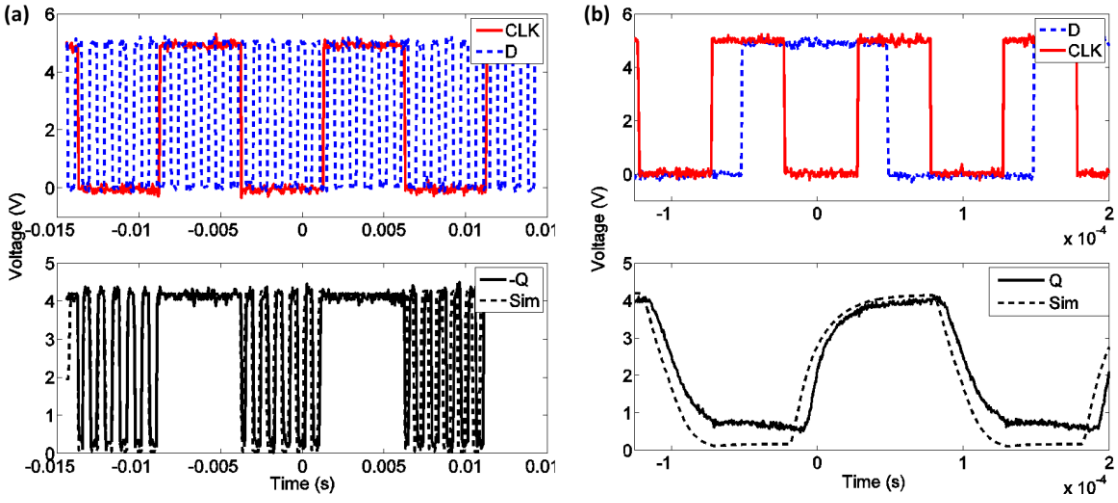

Figure 6-6: Measured waveforms of (a) the D latch and (b) the falling edge triggered DFF with 10 kHz inputs (the higher one) at V_{DD} = 5 V and V_{SS} = 10 V.

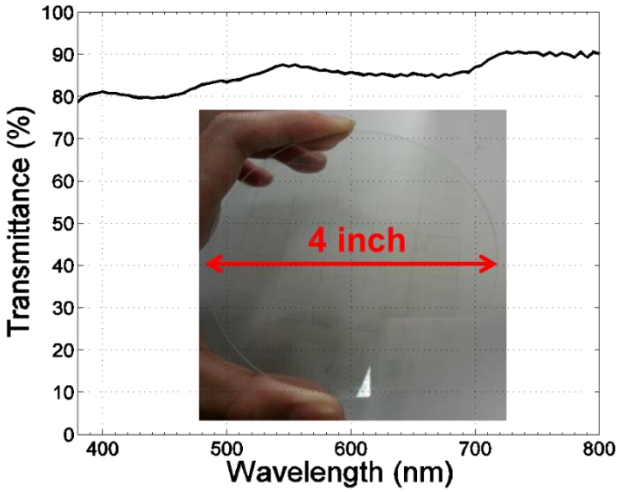

Figure 6-7: Measured optical transmittance as a function of wavelength within a visible band. Inset: photograph of the fundamental digital circuits on a 4-inch circular glass substrate.

6.2 Flat Panel Displays

A 2.2-inch monochromatic AMOLED panel has been demonstrated using TG-BC hp-ITZO TFTs. The TFT backplane including the active area and peripheral circuits was designed and fabricated in NFF-HKUST, while the OLED section and the following driver bonding were completed by Guangzhou New Vision Opto-electronic Technology Co., Ltd. The detailed specifications of the AMOLED panel are listed in Table 6-2. Since it is the TFT technology rather than other components that we are concerned about most, the requirements for the OLED section are not very high, and only one open mask was employed to evaporate the remaining layers of the green OLEDs at the current stage. Full-color AMOLED or AMQLED panels will be demonstrated in the future.

Table 6-2: Detailed specifications of the AMOLED display panel

Panel size	Pixel number	Pixel size	Resolution	Frame rate	Emission type	Aperture ratio
2.2 inch	200(H)×600(V)	90μm×30μm×3(green)	287×3 ppi	60 Hz	Top emission	40.7%

6.2.1 Layout Design

In order to be compatible with the facilities in HKUST-NFF, 4-inch circular glass is used as processing substrates in this project. As shown in Fig. 6-8(a), there are a display panel region, testing dies, leakage measurement structures, testing OLEDs, metal strips and other markers over the global glass.

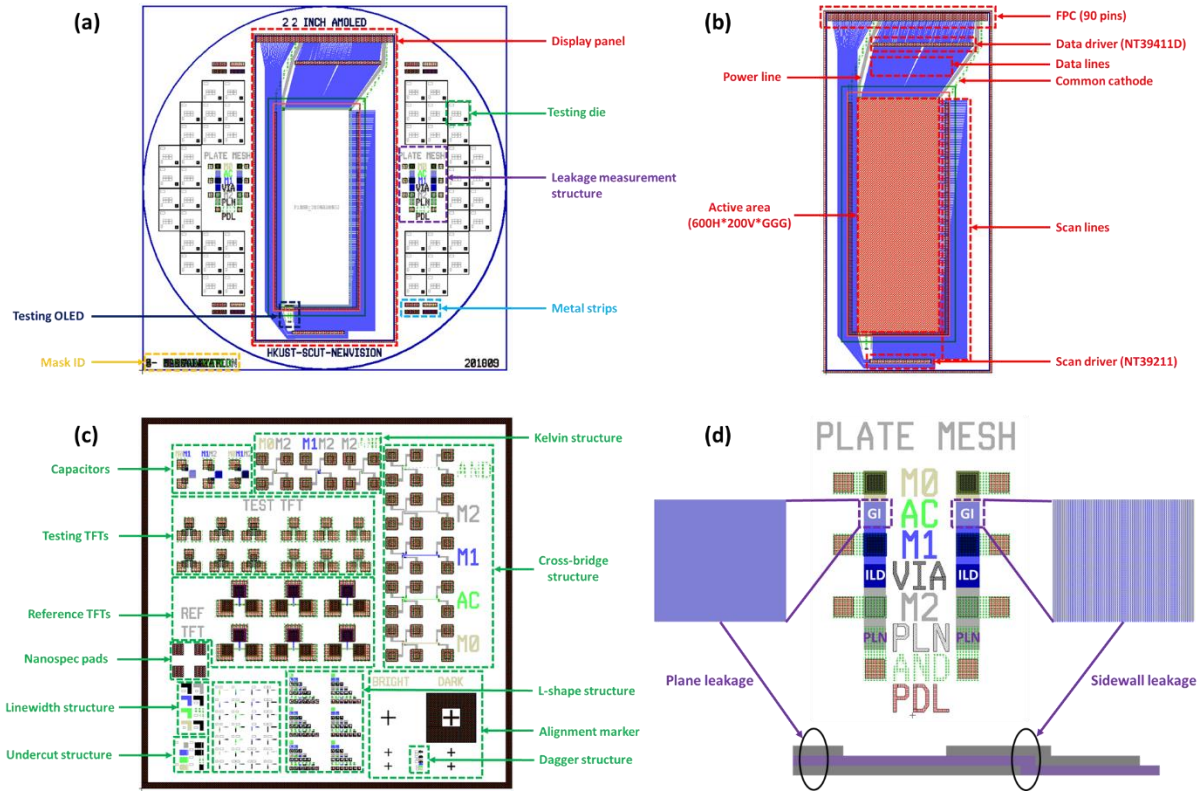

Figure 6-8: Layout illustration of (a) global design, (b) display panel region, (c) testing die region, and (d) leakage measurement structure.

This display panel region consists of an active area and peripheral circuits (Fig. 6-8(b)). Among them, the peripheral scan lines and data lines end in the form of metal pads, which are used to bond a scan driver IC (Novatek NT39211) and a data driver IC (Novatek NT39411T) via traditional chip-on-glass (COG) technology. The ICs together with power lines and OLED common cathodes are then connected to a flexible printed circuit (FPC) board for further signal communication. Since the peripheral circuits in this panel do not employ any TFTs, the resulted bezel is relatively wide (the whole panel size is 8.6 cm × 4 cm, whereas the active area size is 5.4 cm × 1.8 cm). Advanced designs such as gate-on-array (GOA) technology for narrow-bezel panels will be considered in the next version. The 2.2-inch long-strip active area contains 200 (H) × 600 (V) × 3 subpixels. The resolution of this monochromatic panel can be regarded to be as high as 861 ppi with an aperture ratio (AR) of 40.7%. In order to save space within the limited area of 90 μm × 30 μm, the arrangement of pixels follows a back-to-back layout, where every two adjacent columns form a pair and share a common power line (Fig. 6-9(a)). Herein, a basic 2T1C circuit design is adopted in every subpixel. Since the top-emitting OLEDs have a normal structure, the corresponding 2T1C circuit schematic is a little bit different from that in Fig. 1-5(b) with inverted OLEDs. As shown in Fig. 6-9(b), the switching TFT (T1) and the

driving TFT (T2) remain the same, while the storage capacitor (C_S) is placed between the gate and the drain of T2, and the OLED is placed between the source of T2 and the common. To confirm high device yield, both T1 and T2 employ the TG-BC hp-ITZO TFTs. Their channel width/length are 5 μm/5 μm and 10 μm/5 μm, respectively. Fig. 6-9(c) illustrates the cross-sectional schematic of the driving TFTs, which are formed by 9 layers on the top of glass substrates. These layers in sequence are the source/drain electrode layer (M0), active channel layer (AC), gate insulator layer (GI), gate electrode/scan line layer (M1), interlayer dielectric layer (ILD), data/power line layer (M2), planarization layer (PLN), anode/common cathode layer (AND), and pixel definition layer (PDL). The structure of the switching TFTs is similar but free of the AND layer, and there is no need to pattern the PLN layer and the PDL layer. The TFT backplane fabrication process generally follows that of the TG-BC hp-ITZO TFTs in Chapter 4, and the details are also described in Appendix I. Fig. 6-9(d) shows the cross-sectional schematic of the storage capacitors. According to our estimation, the C_S should adopt a double-dielectric-layer capacitor structure in order to achieve a sufficiently large capacitance density ($0.126\ \mathrm{pF}/369\ \mu\mathrm{m}^2 \approx 34.15\ \mathrm{nF/cm}^2$) for a voltage-holding ratio (VHR) of over 99%. In this case, the theoretical VHR value can be calculated as

$$\mathrm{VHR} = \frac{V(T_f)_{rms}}{V_0} = \sqrt{\frac{\tau}{2T_f}\left(1 - \exp\left(\frac{-2T_f}{\tau}\right)\right)} \approx 99.34\%, \tag{6-1}$$

where $V(T_f)_{rms}$ and V_0 is the root-mean-square voltage across the C_S after a frame time T_f (here it is 16.7 ms for 60 Hz) and the initial voltage across the C_S when it finishes charging, respectively. In addition, τ is the voltage decay time constant, which is equal to

$$\tau = \frac{V_0 C_s}{I_{off}} = \frac{10 \times 0.126 \times 10^{-12}}{10^{-12}} = 1.26\ \mathrm{s}, \tag{6-2}$$

where I_{off} denotes the leakage current (mainly from the TFT off-state current), and we approximate its value as 10^{-12} A. Above all, the sufficiently high VHR will prevent the fabricated AMOLED display panel from the undesirable flicker phenomenon.

In the testing dies, there are parallel plate capacitors for capacitance measurement, Kelvin resistor structures for contact resistance measurement, cross-bridge structures for sheet resistance and line width change measurement, testing and reference TFTs for TFT characterization, and other assisted structures for panel fabrication (Fig. 6-8(c)).

In terms of leakage current measurement, there are two types of structures based on metal-insulator-metal (MIM) stacks. One is a plate structure with an overlapped plane area of 2.1 mm^2 (1.4 mm × 1.5 mm), and it is used to measure the intrinsic leakage current of each insulator.

The other one is a mesh structure, which is particularly designed for the sidewall leakage current measurement of insulating layers when they are required to cover a large number of metal lines. As shown in Fig. 6-8(d), there are 75 horizontal strips and 75 vertical strips intersecting with each other. Their formed crossovers will result in 11250 sidewalls and 5625 (75 × 75) overlapped plane regions with a total area of 0.5625 mm^2 (75 × 75 × 10 μm × 10 μm).

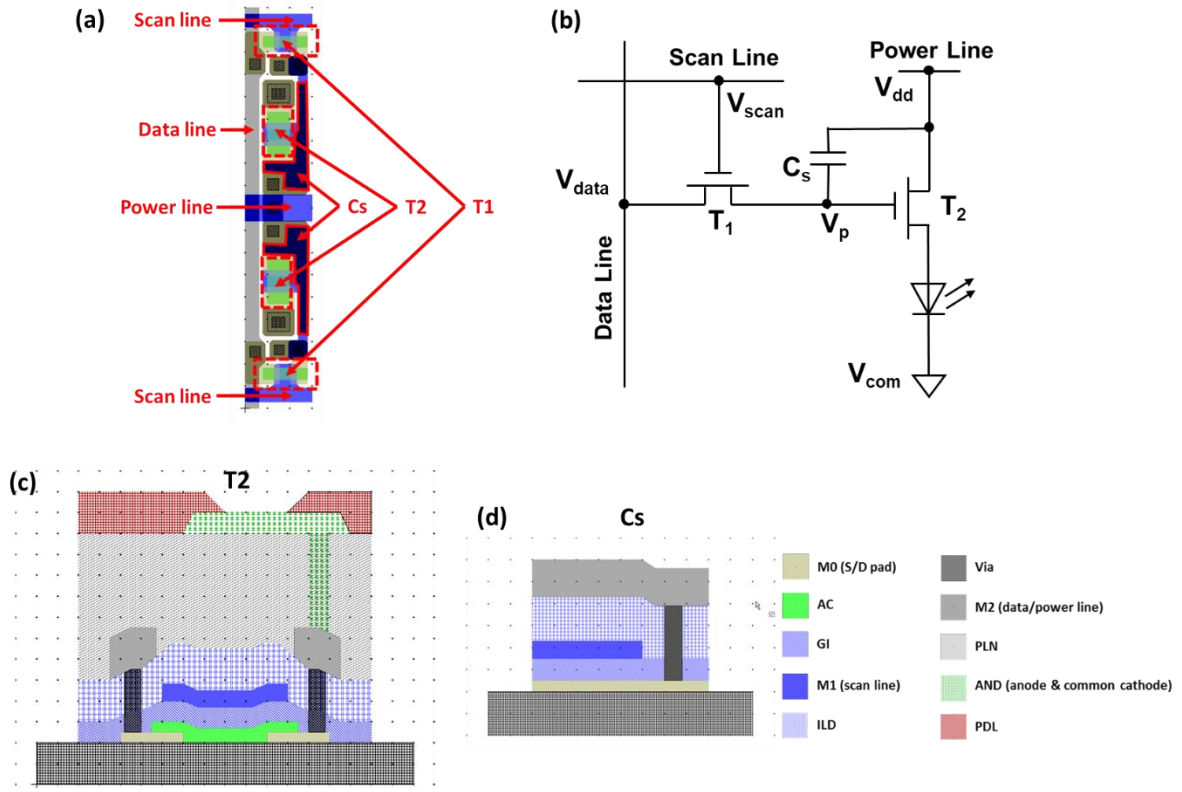

Figure 6-9: (a) Illustration of the back-to-back layout. (b) Schematic of the 2T1C circuit with two n-type TFTs and a normally structured OLED. Cross-sectional schematic of (c) driving TFT T2 and (d) double-dielectric-layer storage capacitor C_S.

6.2.2 Pixel Circuit Simulation

As basic building blocks of display panels, the behaviors of pixel circuits will directly affect the overall display effect. Thus, it is a common practice to run pixel circuit simulations both at the pixel level and in global system level prior to panel fabrication. Takeing our 2T1C pixel circuit as an example, it is simulated in this subsection to explore the relationship between brightness (L_{panel}) and reasonable power supply voltage (V_{dd}) in the AMOLED panels. Then, the simulation results can provide a reasonable V_{dd} range for reference in order to regulate L_{panel} for panel tests.

According to the scan/data driver IC manuals, when the switching TFT T1 is switched from the off state to the on state by tuning the scan voltage (V_{scan}) on its gate from -10 V to 10 V, the signal information that is conveyed by the data voltage (V_{data}) will be loaded to the C_S by charging it to a voltage between 0 V and 10 V. When the inputted V_{data} is set to the maximum 10 V, L_{panel} will be mainly determined by the value of V_{dd} if the common voltage (V_{com}) remains the same. Referring to our extracted compact TFT model and the OLED model that is provided by the cooperation partner, we can simulate the electrical behaviors of the pixel circuit (Fig. 6-3(b)) using an HSPICE simulator. The relationship between green OLED current (I_{oled}) and V_{dd} together with the relationship between its luminance (L_{oled}) and I_{oled} is presented in Fig. 6-10(a) and (b), respectively. Since the designed AR in the AMOLED panel is 40.7% and the light outcoupling efficiency (η_{out}) is about 21.9% ($= \frac{1}{2\times(1.51)^2}$), L_{panel} can be then converted from L_{oled} according to the following equation:

$$L_{pixel} = L_{oled} * AR * \eta_{out} = L_{oled} * 40.7\% * 21.9\% = 0.0891 * L_{oled}, \qquad (6\text{-}3)$$

and the obtained L_{panel}-I_{oled} curve is also plotted in Fig. 6-10(b). Together with the I_{oled}-V_{dd} curve above, we can figure out L_{panel} as a function of V_{dd}. For example, if the L_{panel} of the AMOLED panel is defined as 500 nits, the required L_{oled}, I_{oled} and V_{dd} should be about 5610 nits, 84 nA and 3.15 V, respectively. In this case, the corresponding panel current (I_{panel}), total TFT power consumption (P_{tft}) and total static panel power consumption (P_{panel}) can be derived as 30.24 mA, 19.35 mW and 95.26 mW, respectively. Although there must be deviation between the simulated and the practical results, it is full of guiding significance for the following practical applications, enabling rapid evaluation and debugging.

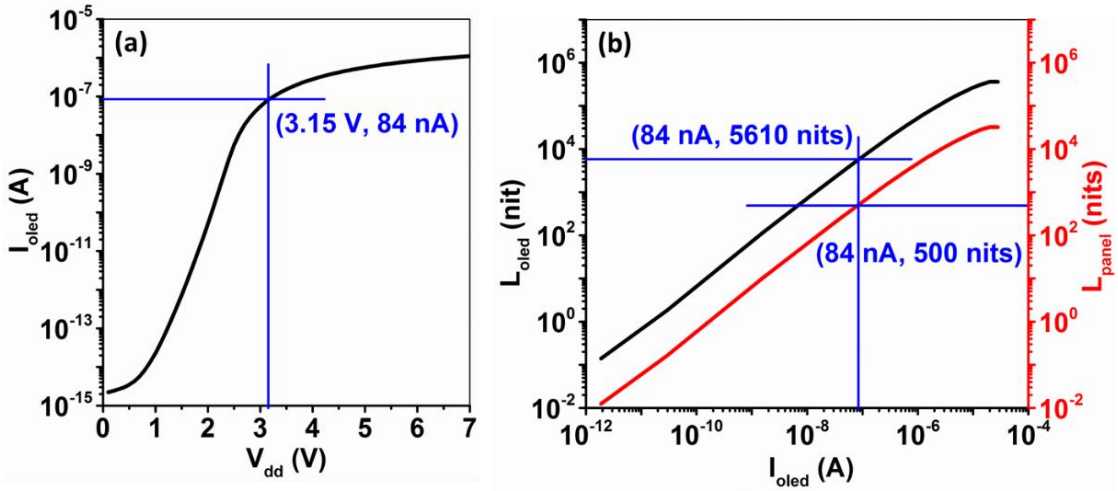

Figure 6-10: (a) Plot of I_{oled} versus V_{dd}. (b) Plot of L_{oled} and L_{panel} versus I_{oled}.

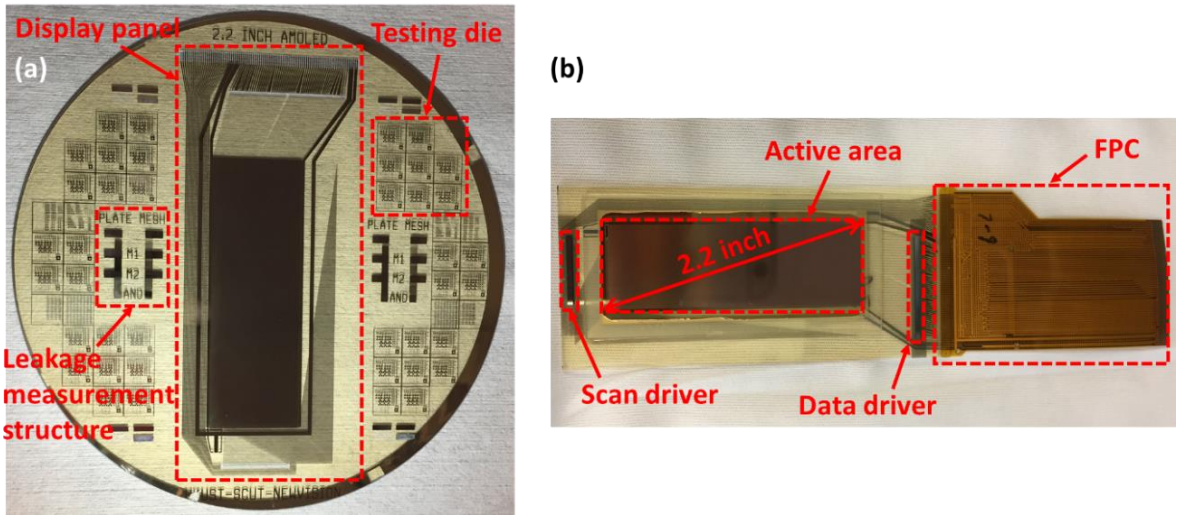

Figure 6-11: Photographs of (a) the hp-ITZO TFT backplane before OLED processing and (b) the fabricated 2.2-inch AMOLED panel.

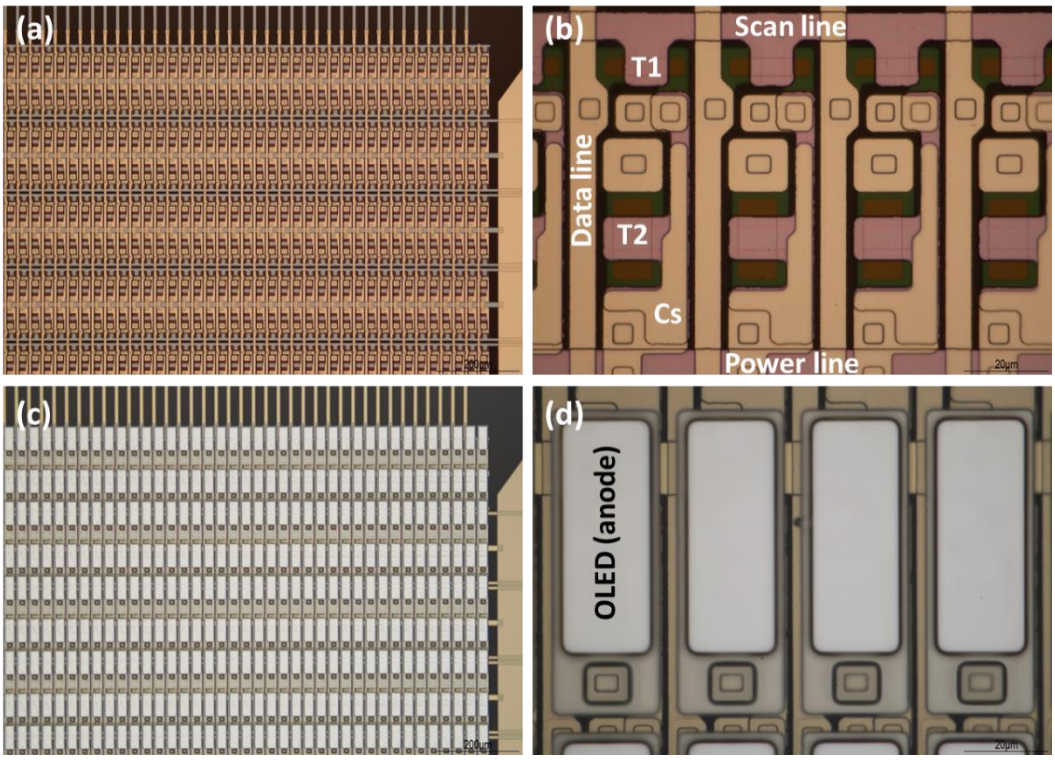

Figure 6-12: Micrographs of the pixel arrangement on the backplane (a)-(b) before the PLN layer and (c)-(d) after the PDL layer.

6.2.3 Panel Performance

Fig. 6-11 presents photographs of the hp-ITZO TFT backplane before OLED processing, and the fabricated 2.2-inch AMOLED display panel. The former circular backplane was fabricated in HKUST-NFF first, then it was sent to our partner for further processes including

glass cutting, OLED evaporation, encapsulation, IC/FPC bonding and testing. Fig. 6-12 shows micrographs of the pixel arrangement on the backplane before the PLN layer and after the PDL layer. Although no particle is observed in the micrographs, we have no way to completely avoid them on account of lab cleanliness. Their existence will cause dot defects, disconnected lines, etc. It will result in the corresponding regions being out of control, as presented later on. In this subsection, we will focus on discussing the TFT electrical characteristics and the AMOLED display panel performance.

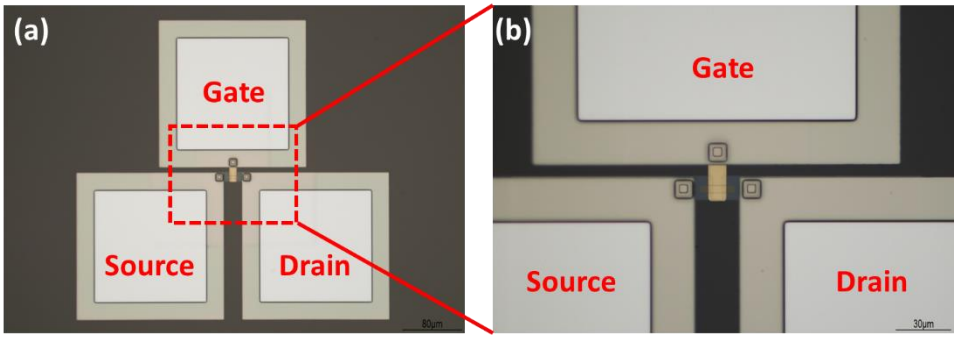

Figure 6-13: Micrographs of the testing TFT with a channel width/length ratio of 5 μm/5 μm.

Firstly, the TFTs with a channel width/length ratio of 5 μm/5 μm (Fig. 6-13) in the testing dies were characterized. The transfer curve of twelve devices that uniformly distributed across a 4-inch glass are plotted together in Fig. 6-14(a). The average μ_{sat}, V_{th}, SS and on-off ratio can be extracted as 18.36 cm^2/Vs, 0.23 V, 0.085 V/decade and 4.7×10^9, respectively. Fig. 6-14(b) presents the statistical diagram of their key electrical parameters. It can be clearly seen that all the parameters can fluctuate within a narrow range. Particularly, the relative standard deviation (RSD) of μ_{sat}, SS and on-off ratio are only 3.02%, 11.14% and 3.30%, respectively. This indicates that the hp-ITZO channel can offer excellent spatial uniformity, as verified in Chapter 3.

Compared with the TG-BC hp-ITZO devices with Al gate electrodes in Chapter 4, the devices with Al/Mo bilayer gate electrodes herein are found to exhibit a more positive V_{th}, a steeper SS and a larger on-off ratio (or lower off-state current). Meanwhile, their mobility decrease is quite slight. Although these two types of devices have different gate electrodes, it is hard to simply attribute their obvious difference in performance to this aspect. After all, the Al (200 nm)/Mo (100 nm) gate electrodes are primarily composed of the Al layers, which also contact the underneath gate insulators directly. In fact, it will be more faithful to think about the planarization process, where a kind of fluorinated polyimide is involved. It is inferred that fluorine-based species in the polyimide may diffuse into the TFTs during the polyimide cure

process at 250 °C. It is possible to introduce a fluorination treatment for the MO channels at the same time. As a result, more oxygen deficiencies can be efficiently compensated with less oxygen annealing or without extra fluorination treatment, leading to lower free carrier population in the channels [160, 206]. Nevertheless, a further comprehensive study needs to be carried out as a part of future work.

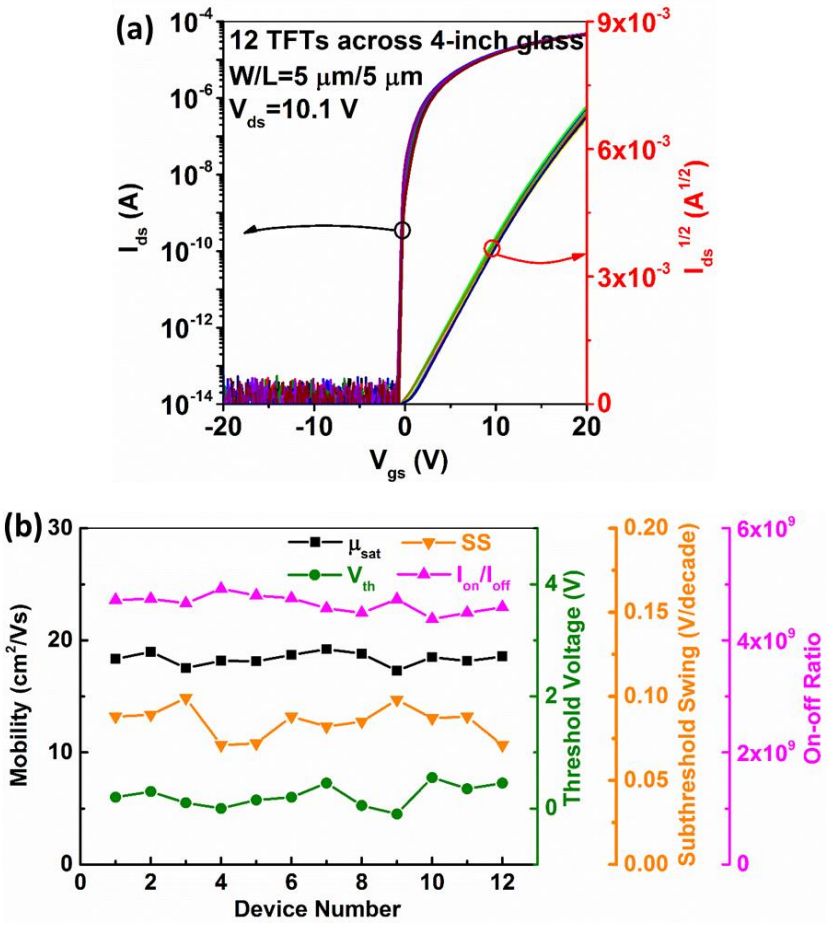

Figure 6-14: (a) Transfer curves of twelve testing TFTs that are uniformly distributed across a 4-inch glass. (b) Statistical diagram of their key electrical parameters.

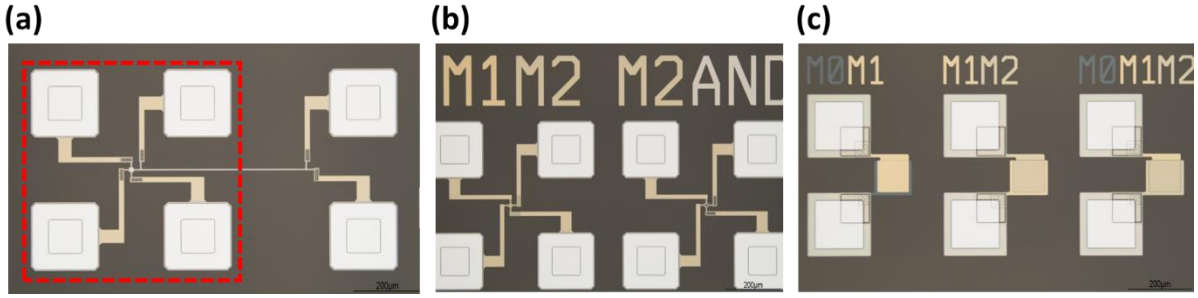

Figure 6-15: Micrographs of (a) cross-bridge structure (the Van der Pauw structure is highlighted by red dash line), (b) Kelvin resistor structures and (d) parallel plate capacitors in the testing dies (M0M1M2 denotes the double-dielectric-layer capacitor).

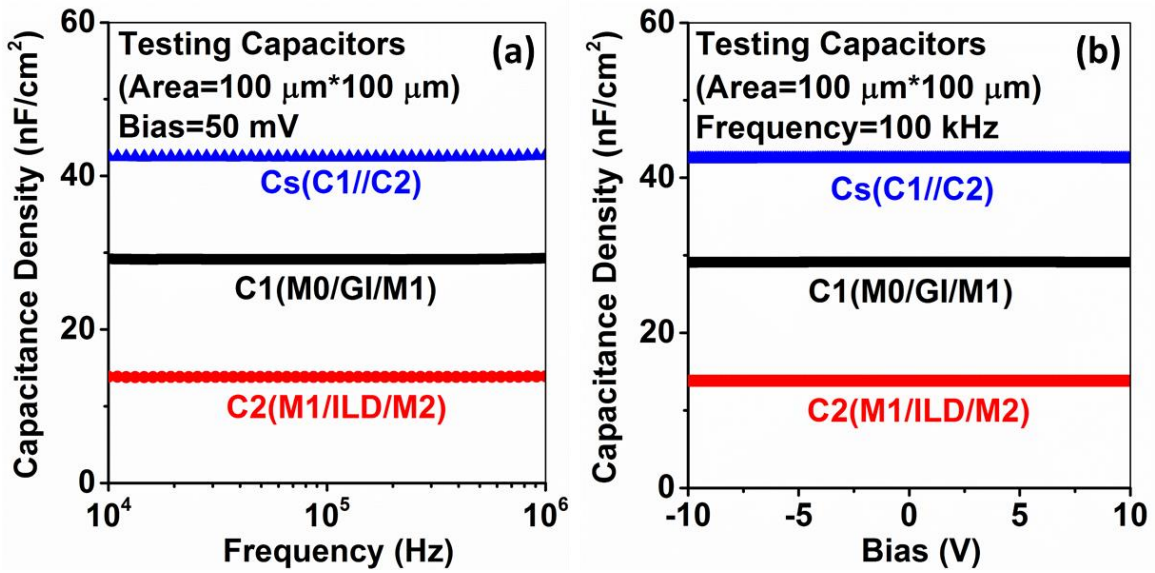

Figure 6-16: Capacitance density of parallel plate capacitors in the testing dies as a function of (a) operation frequency and (b) applied bias.

Next, other passive structures (Fig. 6-15) in the testing dies were characterized. Through the Van der Pauw structures that are integrated in the cross-bridge structures, the resistivity of the M0 layer (ITO), M1 layer (Al/Mo bilayer), M2 layer (Mo) and AND layer (Mo) were able to be measured as 1.45×10^{-2} Ω·cm, 8.55×10^{-4} Ω·cm, 7.66×10^{-3} Ω·cm and 8.06×10^{-4} Ω·cm, respectively. In terms of the AC layer, its resistivity exceeds the measurement limit of the semiconductor parameter analyzer, and should be higher than 10^5 Ω·cm. Through the Kelvin resistor structures, we measured the specific contact resistance between the M0 layer and the M2 layer, between the M1 layer and the M2 layer, and between the M2 layer and the AND layer, and the obtained result is 2.36×10^{-4} Ω·cm^2, 2.42×10^{-7} Ω·cm^2 and 5.36×10^{-7} Ω·cm^2, respectively. In addition, via transfer length method (TLM), the specific contact resistance between the AC layer and the M0 layer is also extracted as 2.2 Ω·cm^2. By using an LCR meter (E4980, Agilent), the capacitance of the parallel plate capacitors in the testing dies could be measured. When its operation frequency varies from 10 kHz to 1 MHz, the fabricated double-dielectric-layer C_S keeps an average capacitance density of 42.47 nF/cm^2 (Fig. 6-16(a)). On the other hand, when the applied bias is swept from -10 V to 10 V with an operation frequency of 100 kHz, the measured capacitance density fluctuates within a very narrow range between 42.41 nF/cm^2 and 42.45 nF/cm^2 (Fig. 6-16(b)). The results are much higher than the designed value (34.15 nF/cm^2). Therefore, sufficiently high VHR value (>99%) is guaranteed to avoid the undesirable flicker effect in the AMOLED display panels.

Afterwards, through the leakage measurement structures (Fig. 6-17), we tested the intrinsic electrical quality of insulating layers and their performance at the sidewalls of the metal lines. The results are shown in Fig. 6-18. In terms of the plate structures, the GI layer leads to the largest leakage current among the three types of insulating layers (which here are GI, ILD and PLN). This is presumably attributed to film thickness, and the GI layer is the thinnest (50 nm) among the insulators. In terms of the mesh structures, the leakage current of the ILD layer is more than one order of magnitude higher than that of the other two types of insulators. Although the ILD layer is twice as thick as the GI layer, the latter employs the TEOS-SiO_2, which is commonly recognized as a type of PECVD SiO_2 with excellent conformality and uniformity. Additionally, the PLN layer is also highly conformal. Thus, the coverage of the ILD layer at the sidewall is the worst, resulting in the largest leakage current in the mesh structures.

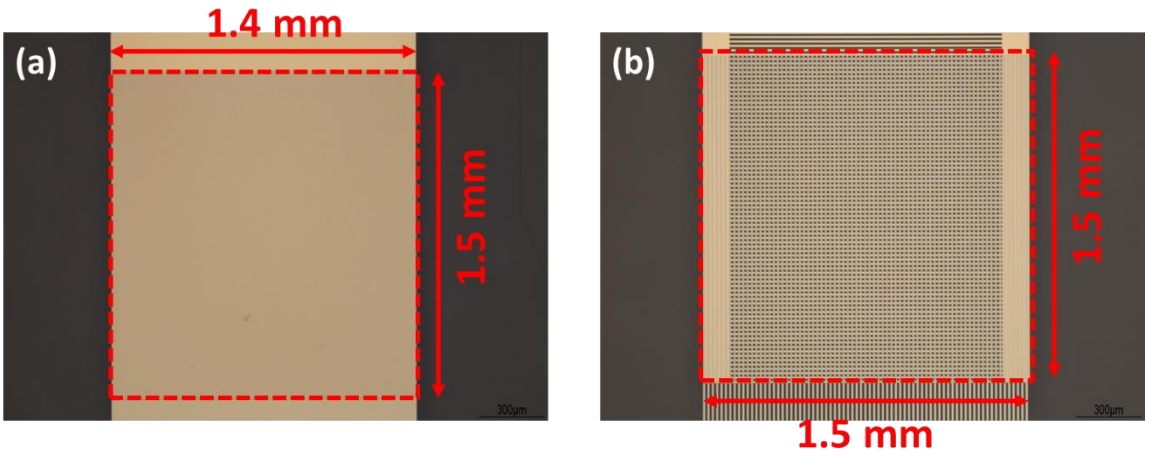

Figure 6-17: Micrographs of (a) the plate structure and (b) the mesh structure for leakage current measurement.

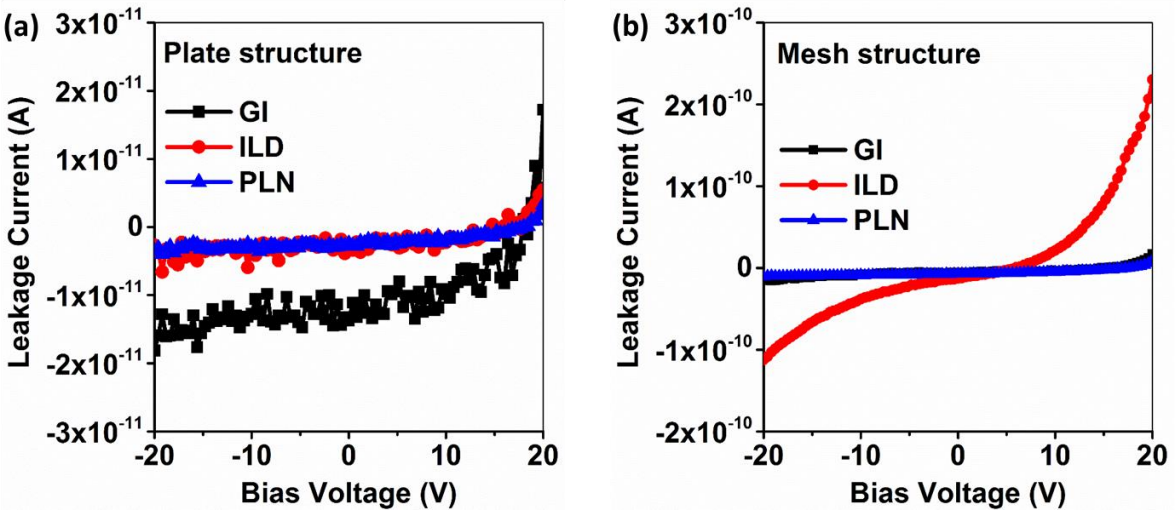

Figure 6-18: Leakage current in (a) the plate structure and (b) the mesh structure as a function of bias voltage.

Finally, a fabricated 2.2-inch AMOLED display panel was demonstrated. When V_{dd} and V_{com} are defined as 4.2 V and -1 V, respectively, the monochromatic AMOLED panel can reach a brightness of 500 nits with a color coordinate of (0.2975, 0.6511) in the CIE 1931 chromaticity diagram. Since the measured I_{panel} is 46 mA, the derived I_{oled} that passes through one OLED device is 127.8 nA. Then, the value of P_{tft} and P_{panel} across the global panel can be calculated as 35.7 mW and 239.2 mW, respectively. The detailed measurement results are listed in Table 6-3. Compared with the simulation results above, we notice a difference between the estimated and the measured V_{dd}. This is partially because of the voltage drop along the Mo power lines, which was ignored in the simulation for the individual pixel circuit. Additionally, the inaccuracy of the OLED model should be another possible reason for such a difference. The practical I_{oled} for a certain brightness is higher than the current provided in the model, which requires further optimization.

Table 6-3: Measurement results of the global AMOLED panel with different brightnesses

L_{panel} (nit)	V_{dd} (V)	V_{com} (V)	I_{panel} (mA)	I_{oled} (nA)	P_{tft} (mW)	P_{panel} (mW)
100	1.1	-0.46	31	86.2	19.8	48.36
200	2.67	-0.87	33	91.6	21.69	116.82
300	3.18	-1	37	102.8	25.79	154.66
400	3.8	-1	42	119.4	32.28	201.6
500	4.24	-1	46	127.8	35.75	241.04

Regardless of the defects in dots, and column and row lines, the display panel can well present the static and dynamic images as loaded according to Fig. 6-19. The uniform luminance in different regions confirms the excellent spatial uniformity of the TFTs and the OLEDs. In addition, there is also no flicker phenomenon observed. This indicates that the capacitance of the fabricated storage capacitors and the practical leakage current of every insulating layer can fulfill the design requirements. This is the first demonstration of an AMOLED display panel using MO TFT technology in HKUST. The updated full-color versions with less defects and higher definitions will be fabricated in the future.

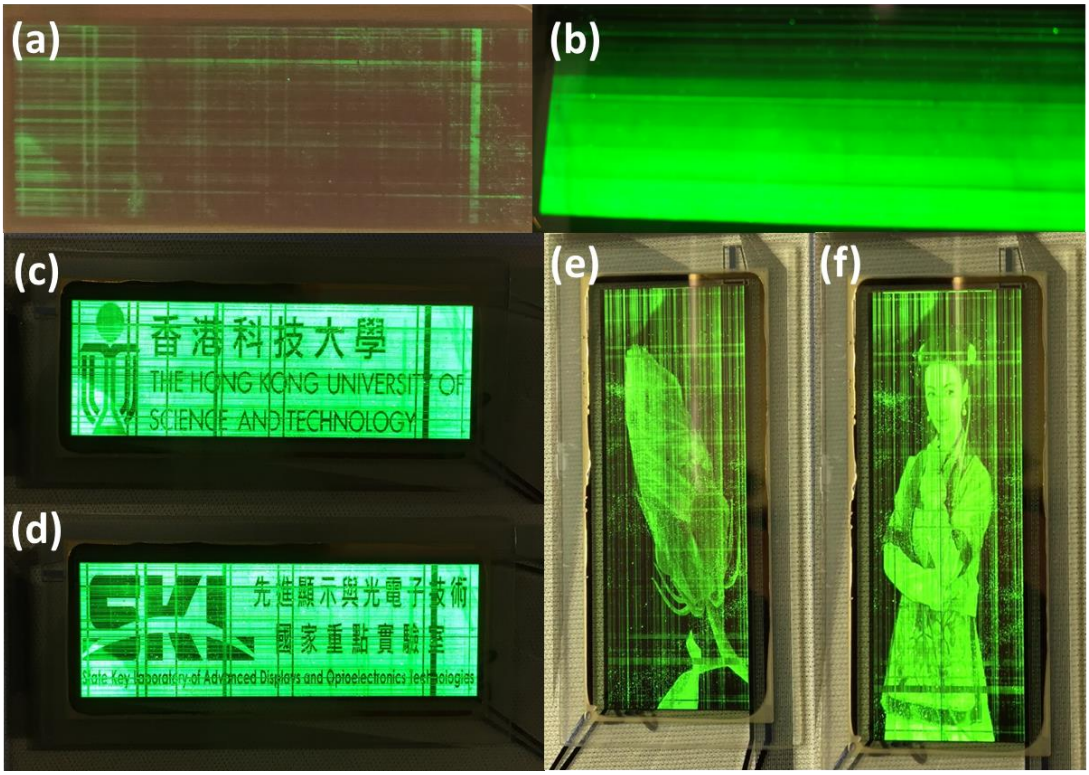

Figure 6-19: Capture of images that are displayed on the 2.2-inch monochromatic AMOLED panel: (a) black image, (b) grey scale image, (c) HKUST logos, (d) SKL-ADT logo, and (e)-(f) other loaded images.

6.3 Chapter Summary

In this chapter, some practical applications have been successfully implemented. Prior to fabrication, the compact TFT models have been faithfully extracted for circuit simulation. Then, the fundamental digital circuits including both combinational and sequential types have been implemented. As their building blocks, the TG-BC hp-ITZO TFTs with the ITO gate electrodes are fully transparent. Their high and reliable performance can guarantee a circuit operation frequency exceeding 10 kHz with a supply voltage of 10 V. This is promising for full-

transparent applications that are operated in moderate frequency, such as driving circuits in see-through displays. Moreover, a 2.2-inch monochromatic AMOLED display panel using the hp-ITZO TFTs has been successfully demonstrated from layout design, through backplane processing to system testing. The high and uniform characteristics of the devices together with the good display performance of the panel confirms that hp-ITZO TFT technology is feasible and promising for AM-FPD applications.

Chapter 7 Conclusion and Future Work

7.1 Conclusion

In this thesis, hp-ITZO thin films have been proposed to be one of the most promising MO TFT channels via collaborative modification in both their element composition and their crystal morphology. When the ITZO thin films evolve from the XRD amorphous phase to the conventional polycrystalline phase, their Hall mobility (>30 cm^2/Vs) can reach a peak in the hybrid phase, which is an amorphous matrix including a number of columnar nanocrystals with blurry grain boundaries. Additionally, the peak of Hall mobility is verified to break through the theoretical upper mobility limit in the amorphous counterparts. This is attributed to the long-distance chaining of internal corner-shared InO (and SnO) polyhedra for the formation of efficient electron percolation conduction paths. Thus, the potential of indium cations can be fully harnessed, avoiding redundancy for low-cost electronics. Apart from the boosted mobility, the hp-ITZO thin films also exhibit many other merits such as suppressed overall sub-gap states, wide band gap, a balanced band diagram, etc. These are of high value to realize high-performance and reliable MO TFTs.

The feasibility of the hp-ITZO thin films as TFT channels has been further confirmed by implementing BG-TC TFTs with the lift-off S/D electrodes. By tuning P_{O2} and P_{DC}, we can determine the optimal conditions for channel deposition. The fabricated devices exhibit high electrical performance with a typical μ_{fe} of 27.3 cm^2/Vs, V_{th} of 0.5 V, on-off ratio of over 10^9 and extremely low SS of 89 mV/decade. Their excellent spatial uniformity and long shelf life are also observed. The electrical non-uniformity concern in the hp-ITZO thin films can be ignored. To fulfill industrial demands, the TFT S/D electrodes are then patterned using the wet etch rather than the lift-off technique. Through the over-etch ratio control and the prior thermal annealing reinforcement, the BCE-type BG-TC TFTs can be successfully fabricated with high performance and good stability against gate-bias stress. The relative wide over-etch range reveals the excellent process robustness of the hp-ITZO channels.

Next, the related top-gate hp-ITZO TFTs have been developed as building blocks in practical applications. To deposit high-quality gate insulators, we have demonstrated a type of stacked PECVD SiO_2, which contains the SiH_4-SiO_2 layer with the TEOS-SiO_2 layer underneath. The issues of high H content in the SiH_4-SiO_2, and rich OH/H_2O groups in the TEOS-SiO_2 can be well addressed, and the stacks are found to exhibit strengthened electrical quality compared to their single-layer counterparts. Via gate insulator engineering, the TG-BC

hp-ITZO TFTs are shown to be free of hysteresis with a fairly high on-off ratio of over 1.6×10^{10} and extremely sharp SS of 0.097 V/decade. To efficiently control V_{th}, particularly in the top-gate MO TFTs with high mobility, gate electrode engineering is then proposed and employed in the TG-BC hp-ITZO TFTs. By replacing their original metallic Al gate electrodes with the conductive ITO gate electrodes, the devices can exhibit a ΔV_{th} as large as 1.7 V, evolving from the depletion mode to the enhancement mode. It is found that not only the gate electrode's work function but also the permeability for hydrogen diffusion out of and oxygen diffusion into the channels during post-annealing will efficiently modulate V_{th} without performance degradation in the TG MO TFTs. The results provide a potential solution to monolithically integrate enhancement- and depletion-mode n-type MO TFTs for low-power-consumption circuit design.

As discovered in the gate electrode engineering, the hp-ITZO thin films that are capped by the SiH_4-SiO_2 will maintain a low-resistivity state after long-duration oxygen annealing, whereas they can return to a high-resistivity state when capped by the TEOS-SiO_2. Based on this unique property, TG-SA hp-ITZO TFTs have been then successfully achieved by delicately adopting two different PECVD SiO_2 layers together with differentiated O_2 annealing strategies. The devices can exhibit good electrical characteristics as well as robust stability against gate-bias stress and thermal processing. Then, not only the photolithography step for the definition of S/D electrodes but also the extra processes for the formation of conductive S/D regions can be saved, enabling more cost-effective manufacturing.

Finally, a 2.2-inch monochromatic AMOLED display panel using hp-ITZO TFT technology has been demonstrated from layout design, through backplane processing to system testing. The testing TFTs over the global backplanes can exhibit high and uniform electrical performance as expected. Regardless of some defects in dots, and column and row lines, the panel is able to well present the static and dynamic images as loaded. It confirms that our hp-ITZO TFT technology is applicable to AM-FPDs. In addition, some of the integrated circuits for fully transparent electronics are also implemented with preliminary but promising results.

In conclusion, this thesis has laid a foundation for hybrid-phase metal oxide TFT technology from material design to device implementation and technology application. The entire work is beneficial for the benign and sustainable development of MO TFT technology, which can fulfill the requirements of next-generation AM-FPD technologies for higher definitions, narrower bezels, lower power consumption, more cost-effective manufacturing, etc.

7.2 Suggested Future Work

In this thesis, we mainly focused on the study of hybrid-phase metal oxide thin-film transistors ranging from material design, through device implementation to technology application. For more complete and comprehensive research, much work needs to be done in the future.

From the aspect of materials, it is found that the Hall mobility variation of ITZO thin films with different crystallinities matches the observation in stoichiometric In_2O_3 thin films. Thus, we have chosen to explain such a variation in the multicomponent ITZO thin films with reference to the evolution of InO polyhedra in the binary In_2O_3 thin films. Although it looks reasonable, other unrevealed mechanisms may also exist in the multicomponent MO materials. Therefore, it is suggested to further explore the reasons. Tools such as Vienna Ab Initio Simulation Package (VASP) and Large-scale Atomic/Molecular Massively Parallel Simulator (LAMMPS) will be required to do first-principle calculation and molecular dynamic simulation.

From the aspect of devices, the core work should continue to develop TG-SA TFTs. Although such type of devices has been successfully realized in this thesis, their yield has not yet been as satisfactory, and the channel length is hard to scale down to <10 μm. These issues will hinder their applications to both large-area and high-density electronics. Thus, process optimizations or alternative solutions need to be explored in the future.

Additionally, we have significantly improved the TG-BC hp-ITZO TFT performance via gate insulator/electrode engineering, but the devices still suffer from non-ohmic contacts (or built-in potential barriers) between the S/D electrodes and the channels. When we tried to replace the currently-used ITO S/D electrodes with other metals (e.g., Mo, Ti, Al, etc.) or ITO that is sputtered with low P_{O2}, the devices lost their switching behavior. This is an unexpected but meaningful phenomenon, which may be related to the height of the built-in potential barriers or the amount of metallic states in the S/D electrodes. Therefore, future work is required to explore the underlying mechanisms and then take advantage of them. For example, apart from the gate electrode engineering, the amount of metallic states in their ITO S/D electrodes, which corresponds to the value of P_{O2} during ITO sputtering, may also control V_{th} in the TG-BC TFTs.

Moreover, during the AMOLED panel fabrication, we noticed that the planarization process seems helpful to positively shift V_{th} and improve SS. It is suspected that the fluorine-based species from the photo-sensitive fluorinated polyimide may diffuse into the MO channels

during the polyimide cure process at 250 °C. Then, fluorination of TFT channels is possible to compensate more oxygen deficiencies and lead to a lower free carrier population [160, 206]. If this hypothesis is correct, it will reduce the required annealing time or steps required for robust MO TFTs, bringing process renovation for high efficiency. As a result, further experiments are demanded to verify this analysis.

Furthermore, the devices should be developed on flexible substrates. Now that our devices can be processed at a temperature of no more than 300 °C, it is a good opportunity for us to implement the flexible devices especially with the self-aligned structure, serving for flexible and transparent electronics.

From the aspect of applications, we will further develop full-color display panels with higher definitions (e.g., >120 Hz frame rate). Thanks to the extremely low off-state current of our devices, it is also worthy of attempting low-power-consumption displays with a lower frame rate (even to 1 Hz). On the other hand, since the compact models of our TFTs have been extracted for circuit design and simulation, we will continue to develop more advanced integrated circuits (e.g., sensor readout circuits, non-volatile memories, etc.) in cooperation with circuit experts. Particularly for sensor readout circuits, we will promote the monolithic integration of signal readout TFTs and various sensors (including conventional sensors and novel sensing TFTs). The integrated sensor units are expected to show many merits like wider dynamic range, stronger detectivity and higher signal-to-noise ratio.

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Appendix I Process Flow of Display Backplanes

1. Starting Substrates and Their Preparation

Type: Corning Eagle XG Glass Wafer

Thickness: 0.7 mm

Diameter: 100 mm +/- 0.254mm

Edges: C radius ground

1.1 RCA1 clean

(1) Wetstation G, $NH_4OH : H_2O_2 : H_2O = 1 : 1 : 5$, 70 ^oC, 30 min;

(2) Wetstation G, DI spray rinse 4 cycles, spin rinse/dry.

1.2 Buffer layer deposition

Furnace B4, 420 ^oC, 300 nm LTO.

1.3 Pre-shrinkage

(1) Wetstation D, DI spray rinse 4 cycles, spin rinse/dry;

(2) Furnace F1, N_2, 500 ^oC, 15 h.

2. Source/Drain Pad (M0 Layer) Deposition and Patterning

2.1 Photolithography

(1) Sample preparation:

Wetstation Y, DI spray rinse 4 cycles, spin rinse/dry;

Oven, 120 ^oC, 30 min;

(2) Mask preparation:

Wetstation Y, MS 2001, 70 ^oC, 5 min;

Wetstation Y, DI spin rinse 4 cycles, blowing dry;

Oven, 105 ^oC, 10 min;

(3) Photoresist coating (UTS Track 1):

HMDS prime, hot plate, 105 ^oC, 30 s (Program 1);

PR506 manual dispense, 4000 rpm, 30 s, with backside rinse only (Program 3);

Soft bake, hot plate, 110 ^oC, 60 s (Program 1);

(4) Exposure: MA6-2, hard contact, ~6.5 s * 25 mW/cm^2;

(5) Development (UTS Track 2):

Puddle develop, FHD-5, 65 s (Program 1);

Free of hard bake (Program 7);

(6) Microscope inspection.

2.2 ITO deposition (pre-sputtering time: 5 min)

Old AJA system (ITO target at righthand position), Ar : O_2 = 20 sccm : 0.3 sccm, 3 mTorr, 120 W dc power, 50 nm/3.5 min.

2.3 Lift-off

(1) Branson 3510, ultrasonic with acetone, 20 min*2;

(2) Branson 3510, ultrasonic with IPA, 5 min;

(3) Wetstation Y, DI spray rinse 4 cycles, spin rinse/dry;

(4) Microscope inspection.

2.4 1st annealing

(1) Wetstation D, DI spray rinse 4 cycles, spin rinse/dry;

(2) Furnace F1, O_2, 300 ^oC, 1 h.

3. Active Channel (AC Layer) Deposition and Patterning

3.1 Hybrid-phase ITZO thin film deposition (pre-sputtering time: 15 min)

New AJA system (pc-ZnO target at Gun 1, pc-ITO target at Gun 3), Ar : O_2 = 12 sccm : 8 sccm, 3 mTorr, 150 W rf power for Gun 1, 110 W dc power for Gun 3, 50 nm/7 min.

3.2 Photolithography

(1) Sample preparation:

Wetstation Y, DI spray rinse 4 cycles, spin rinse/dry;

Oven, 120 ^oC, 30 min;

(2) Mask preparation:

Wetstation Y, MS 2001, 70 ^oC, 5 min;

Wetstation Y, DI spin rinse 4 cycles, blowing dry;

Oven, 105 ^oC, 10 min;

(3) Photoresist coating (UTS Track 1):

HMDS prime, hot plate, 105 ^oC, 30 s (Program 1);

PR504 manual dispense, 4000 rpm, 30 s, with backside rinse only (Program 3);

Soft bake, hot plate, 110 ^oC, 60 s (Program 1);

(4) Exposure: MA6-2, hard contact, ~4 s * 25 mW/cm^2;

(5) Development (UTS Track 2):

Puddle develop, FHD-5, 65 s (Program 1);

Hard bake, hot plate, 120 ^oC, 60 s (Program 1);

(6) Microscope inspection;

(7) Hard bake (continue): Oven, 120 ^oC, 20 min.

3.3 Wet etch

(1) Wetstation E, HF : H_2O = 1 : 2000, RT, 14 s;

(2) Wetstation E, DI spin rinse 4 cycles, blowing dry;

(3) Microscope inspection.

3.4 Photoresist strip

(1) Branson 3510, ultrasonic in acetone, 20 min*2;

(2) Branson 3510, ultrasonic in IPA, 5 min;

(3) Wetstation Y, DI spray rinse 4 cycles, spin rinse/dry;

(4) Microscope inspection.

4. Gate Insulator (GI Layer) Deposition

4.1 TEOS-SiO_2 deposition

(1) Wetstation D, DI spray rinse 4 cycles, spin rinse/dry;

(2) TEOS-PECVD, recipe: 101, 300 ^oC, 50 nm*2. (pre-deposition time: 15 min + 20 min)
(Rotate 180^o after 1st 50-nm-thick TEOS-SiO_2 deposition.)

4.2 SiH_4-SiO_2 deposition

(1) O_2 annealing:
Recipe: o2ann, 300 ^oC, 5 min;

(2) SiH_4-SiO_2 deposition:
Recipe: hfsio, 300 ^oC, 50 nm;

(3) O_2 annealing:
Recipe: o2ann, 300 ^oC, 5 min.

5. Gate Electrode/Scan Line (M1 Layer) Deposition and Patterning

5.1 Mo/Al bilayer deposition

(1) Wetstation D, DI spray rinse 4 cycles, spin rinse/dry;

(2) Varian 3180 sputter, 200 nm Al + 100 nm Mo (pre-heating time: 2 min).

5.2 Photolithography

(1) Sample preparation:
Wetstation Y, DI spray rinse 4 cycles, spin rinse/dry;
Oven, 120 ^oC, 30 min;

(2) Mask preparation:
Wetstation Y, MS 2001, 70 ^oC, 5 min;
Wetstation Y, DI spin rinse 4 cycles, blowing dry;
Oven, 105 ^oC, 10 min;

(3) Photoresist coating (UTS Track 1):
HMDS prime, hot plate, 105 ^oC, 30 s (Program 1);

PR504 manual dispense, 4000 rpm, 30 s, with backside rinse only (Program 3);

Soft bake, hot plate, 110 ^{o}C, 60 s (Program 1);

(4) Exposure: MA6-2, hard contact, ~3.4 s * 25 mW/cm^2;

(5) Development (UTS Track 2):

Puddle develop, FHD-5, 65 s (Program 1);

Hard bake, hot plate, 120 ^{o}C, 60 s (Program 1);

(6) Microscope inspection;

(7) Hard bake (continue): Oven,120 ^{o}C, 1 h.

5.3 Mo layer wet etch

(1) Wetstation D, Mo/Al/Mo etchant (Huate), RT, ~65 s;

(2) Wetstation D, DI spin rinse 4 cycles, blowing dry;

(3) Microscope inspection.

(4) Oven,120 ^{o}C, 5 min;

5.4 Al layer dry etch

(1) Oxford Al etcher, recipe: Al 5000A 30deg (40W), ~80 s + 40 s;

(2) Wetstation D, DI spray rinse 4 cycles, blowing dry;

(3) Microscope inspection.

5.5 Photoresistor strip

(1) IPC 3000 asher, recipe: STRIP20, 20 min *3;

(2) Wetstation D, DI spray rinse 4 cycles, spin rinse/dry;

(3) Microscope inspection.

5.6 2nd annealing

Oven, 300 ^{o}C, in air, 1.5 h (including heating-up time: ~45 min).

6. Interlayer Dielectric (ILD Layer) Deposition and Contact Hole (VIA) Definition

6.1 SiH_4-SiO_2 deposition

(1) Wetstation D, DI spray rinse 4 cycles, spin rinse/dry;

(2) PECVD1, recipe: hfsio, 300 ^{o}C, 100 nm*3 (open chamber and move samples after every 100-nm-thick SiH_4-SiO_2 deposition);

(3) Microscope inspection.

6.2 Photolithography

(1) Sample preparation:

Wetstation Y, DI spray rinse 4 cycles, spin rinse/dry;

Oven,120 ^{o}C, 30 min;

(2) Mask preparation:

Wetstation Y, MS 2001, 70 ^{o}C, 5 min;

Wetstation Y, DI spin rinse 4 cycles, blowing dry;

Oven, 105 ^{o}C, 10 min;

(3) Photoresist coating (UTS Track 1):

HMDS prime, hot plate, 105 ^{o}C, 30 s (Program 1);

PR504 manual dispense, 4000 rpm, 30 s, with backside rinse only (Program 3);

Soft bake, hot plate, 110 ^{o}C, 60 s (Program 1);

(4) Exposure: MA6-2, hard contact, ~3.7 s * 25 mW/cm^{2};

(5) Development (UTS Track 2):

Puddle develop, FHD-5, 65 s (Program 1);

Hard bake, hot plate, 120 ^{o}C, 60 s (Program 1);

(6) Descum:

IPC 3000 asher, recipe: DES120, 2 min;

(7) Microscope inspection;

(8) Hard bake (continue): Oven, 120 ^{o}C, 20 min.

6.3 Via opening

(1) Trion RIE etcher, recipe: NFF1078 oxide, ~660 s + 120 s (= 195 s*4);

(2) Wetstation D, 777 etchant, RT, 5 s;

(3) Wetstation D, DI spin rinse 4 cycles, blowing dry;

(4) Microscope inspection and multimeter test.

6.4 Photoresist strip

(1) Branson 3510, ultrasonic in acetone, 20 min*2;

(2) Branson 3510, ultrasonic in IPA, 5 min;

(3) Wetstation Y, DI spray rinse 4 cycles, spin rinse/dry;

(4) Microscope inspection;

(5) Oven, 120 ^{o}C, 20 min.

7. Data/Power Line (M2 Layer) Deposition and Patterning

7.1 Mo Deposition

Varian 3180 sputter, Mo, 100 nm*2 (pre-heating time: 2 min) (two-step deposition without breaking vacuum).

7.2 Photolithography

(1) Sample preparation:

Wetstation Y, DI spray rinse 4 cycles, spin rinse/dry;

Oven, 120 ^{o}C, 30 min;

(2) Mask preparation:

Wetstation Y, MS 2001, 70 ^{o}C, 5 min;

Wetstation Y, DI spin rinse 4 cycles, blowing dry;

Oven, 105 ^{o}C, 10 min;

(3) Photoresist coating (UTS Track 1):

HMDS prime, hot plate, 105 ^{o}C, 30 s (Program 1);

PR504 manual dispense, 4000 rpm, 30 s, with backside rinse only (Program 3);

Soft bake, hot plate, 110 ^{o}C, 60 s (Program 1);

(4) Exposure: MA6-2, hard contact, ~3.4 s * 25 mW/cm^{2};

(5) Development (UTS Track 2):

Puddle develop, FHD-5, 65 s (Program 1);

Hard bake, hot plate, 120 ^{o}C, 60 s (Program 1);

(6) Microscope inspection;

(7) Hard bake (continue): Oven, 120 ^{o}C, 1 h.

7.3 Wet etch

(1) Wetstation D, Mo/Al/Mo etchant (Huate), RT, ~140 s;

(2) Wetstation D, DI spin rinse 4 cycles, blowing dry;

(3) Microscope inspection.

7.4 Photoresist strip

(1) Branson 3510, ultrasonic in acetone, 20 min*2;

(2) Branson 3510, ultrasonic in IPA, 5 min;

(3) Wetstation Y, DI spray rinse 4 cycles, blowing dry;

(4) Microscope inspection;

7.5 3rd annealing

Oven, 300 ^{o}C, in air, 1.5 h (including heating-up time: ~45 min).

8. Planarization (PLN Layer)

8.1 Preparation

(1) Polyimide preparation (Photoneece DL-1000-C should be taken out of refrigerator 1 hour ahead before spin coating)

(2) Sample preparation:

Wetstation Y, DI spray rinse 4 cycles, blowing dry;

Oven, 120 ^{o}C, 30 min;

(3) Mask preparation:

Wetstation Y, MS 2001, 70 ^{o}C, 5 min;

Wetstation Y, DI spin rinse 4 cycles, blowing dry;

Oven, 105 ^{o}C, 10 min.

8.2 Photolithography

(1) Spin coating:

CEE coater, manual dispense, 300 rpm, 30 s → 450 rpm, 90 s, with manual edge rinse;

(2) Soft bake:

Hot plate, 120 ^{o}C, 120 s;

(3) Exposure:

MA6-2, hard contact, ~3.8 s * 25 mW/cm^2;

(4) Development:

Wetstation Y, FHD-5, 70 s;

Wetstation Y, DI spin rinse 4 cycles, blowing dry;

Microscope check;

*Hot plate, 120 ^{o}C, 4 min;

(5) Bleaching:

MA6-2, flood, 20 s * 25 mW/cm^2 (= 500 mJ/cm^2).

8.3 Cure

Oven, 250 ^{o}C, in N2, 1 h (stable time).

9. OLED Anode and Common Cathode (AND Layer) Deposition and Patterning

9.1 Mo deposition

(1) Wetstation Y, DI spray rinse 4 cycles, blowing dry;

(2) Varian 3180 sputter, Mo, 100 nm*2 (pre-heating time: 2 min) (two-step deposition without breaking vacuum).

9.2 Photolithography

(1) Sample preparation:

Wetstation Y, DI spray rinse 4 cycles, spin rinse/dry;

Oven, 120 ^{o}C, 30 min;

(2) Mask preparation:

Wetstation Y, MS 2001, 70 ^{o}C, 5 min;

Wetstation Y, DI spin rinse 4 cycles, blowing dry;

Oven, 105 ^{o}C, 10 min;

(3) Photoresist coating (UTS Track 1):

HMDS prime, hot plate, 105 ^{o}C, 30 s (Program 1);

PR504 manual dispense, 4000 rpm, 30 s, with backside rinse only (Program 3);

Soft bake, hot plate, 110 ^{o}C, 60 s (Program 1);

(4) Exposure: MA6-2, hard contact, ~8 s * 25 mW/cm^2 (fully exposed near the sidewalls of PLN layer);

(5) Development (UTS Track 2):

Puddle develop, FHD-5, 65 s (Program 1);

Hard bake, hot plate, 120 ^{o}C, 60 s (Program 1);

(6) Microscope inspection;

(7) Hard bake (continue): Oven, 120 ^{o}C, 30 min.

9.3 Wet etch

(1) Wetstation D, Mo/Al/Mo etchant (Huate), RT, ~140 s;

(2) Wetstation D, DI spin rinse 4 cycles, blowing dry;

(3) Microscope inspection.

9.4 Photoresist strip

(1) Wetstation Y, soak in acetone, 20 min*2;

(2) Wetstation Y, soak in IPA, 5 min;

(3) Wetstation Y, DI spray rinse 4 cycles, blowing dry;

(4) Microscope inspection.

10. Pixel Definition (PDL Layer)

10.1 Preparation

(1) Polyimide preparation (Photoneece DL-1000-C should be taken out of refrigerator 1 hour ahead before spin coating)

(2) Sample preparation:

Wetstation Y, DI spray rinse 4 cycles, blowing dry;

Oven, 120 ^{o}C, 30 min;

(3) Mask preparation:

Wetstation Y, MS 2001, 70 ^{o}C, 5 min;

Wetstation Y, DI spin rinse 4 cycles, blowing dry;

Oven, 105 ^{o}C, 10 min.

10.2 Photolithography

(1) Spin coating:

CEE coater, manual dispense, 300 rpm, 30 s → 450 rpm, 90 s, with manual edge rinse;

(2) Soft bake:

Hot plate, 120 ^{o}C, 120 s;

(3) Exposure:

MA6-2, hard contact, ~3.8 s * 25 mW/cm^2;

(4) Development:

Wetstation Y, FHD-5, 70 s;

Wetstation Y, DI spin rinse 4 cycles, blowing dry;

Microscope check;

*Hot plate, 120 ^{o}C, 4 min;

(5) Bleaching:

MA6-2, flood, 20 s * 25 mW/cm^2 (= 500 mJ/cm^2).

10.3 Cure

Oven, 250 ^{o}C, in N_2, 1 h (stable time).

11. OLED Fabrication and Encapsulation (Completed by Guangzhou New Vision Opto-electronics Technology Co., Ltd.)

12. Scan/Data Driver and Flexible Printed Circuit Bonding (Completed by Guangzhou New Vision Opto-electronics Technology Co., Ltd.)

Appendix II Achievements during Ph.D. Career

Journal:

1. **S. Deng**, R. Chen, G. Li, M. Zhang, F. S. Y. Yeung M. Wong, and H. S. Kwok, "Gate Insulator Engineering in Top-Gated Indium-Tin-Oxide-Stabilized ZnO Thin-Film Transistors", *IEEE Electron Device Letters*, vol. 40, no. 7, pp. 1104-1107, July 2019.
2. **S. Deng**, R. Chen, G. Li, M. Zhang, Z. Xia, M. Wong, and H. S. Kwok, "Threshold voltage adjustment in hybrid-microstructural ITO-stabilized ZnO TFTs via gate electrode engineering", *IEEE Electron Device Letters*, vol. 39, no. 7, pp. 975-978, July 2018.
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4. **S. Deng**, R. Chen, G. Li, Z. Xia, M. Zhang, W. Zhou, M. Wong, and H. S. Kwok, "Investigation of high-performance ITO-stabilized ZnO TFTs with hybrid-phase microstructural channels", *IEEE Transactions on Electron Devices*, vol. 64, no. 8, pp. 3174-3182, Aug. 2017.
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8. Y. Xu*, **S. Deng***, Z. Wu, B. Li, Y. Qin, W. Zhong, R. Chen, G. Li, M. Wong, and H. S. Kwok, "The Implementation of Fundamental Digital Circuits With ITO-Stabilized ZnO TFTs for Transparent Electronics", *IEEE Transactions on Electron Devices*, vol. 65, no.

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9. W. Zhong*, **S. Deng***, K. Wang, G. Li, G. Li, R. Chen, and H. S. Kwok, "Feasible route for a large area few-layer MoS_2 with magnetron sputtering", *Nanomaterials*, vol. 8, no. 8, p. 590, Aug. 2018. (*Equal contribution)

10. Q. Yu, G. Li, Y. Xu, R. Chen^, **S. Deng^**, W. Zhong, Z. Wu, B. Li, G. Li, F. S. Y. Yeung, M. Wong, and H. S. Kwok, "Low-Power Design for Unipolar ITO-Stabilized ZnO TFT RFID Code Generator Using Differential Logic Decoder", *IEEE Transactions on Electron Devices*, vol. 66, no. 11, pp. 4768-4773, Oct. 2019. (^Corresponding author)

11. Y. Xu, B. Li, **S. Deng^**, Y. Qin, H. Fan, W. Zhong, Y. Liu, Z. Wu, F. S. Y. Yeung, M. Wong, H. S. Kwok, and R. Chen^, "A Novel Envelope Detector Based on Unipolar Metal-Oxide TFTs", *IEEE Transactions on Circuits and Systems II: Express Briefs*. (^Corresponding author) (Accepted)

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13. M. Zhang, Y. Yan, G. Li, **S. Deng**, W. Zhou, R. Chen, M. Wong, and H. S. Kwok, "High-Performance Polycrystalline Silicon Thin-Film Transistors without Source/Drain Doping by Utilizing Anisotropic Conductivity of Bridged-Grain Lines", *Advanced Electronic Materials*. (Accepted)

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21. Y. Liu, **S. Deng**, R. Chen, B. Li, Y. F. En, and Y. Chen, "Low-frequency noise in hybrid-phase-microstructure ITO-stabilized ZnO thin-film transistors", *IEEE Electron Device Letters*, vol. 39, no. 2, pp. 200-203, Dec. 2017.
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23. Z. Xia, L. Lu, J. Li, Z. Feng, **S. Deng**, S. Wang, H. S. Kwok, and M. Wong, "Characteristics of elevated-metal metal-oxide thin-film transistors based on indium-tin-zinc oxide", *IEEE Electron Device Letters*, vol. 38, no. 7, pp. 894-897, July 2017.
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26. Y. Xu, B. Li, **S. Deng^**, Y. Qin, H. Fan, W. Zhong, Z. Wu, L. Lu, F. S. Y. Yeung, H. S. Kwok, and R. Chen^, "Transconductance Boosting Technology for Single-Gate Unipolar Metal-Oxide TFT Amplifiers", *IEEE Transactions on Circuits and Systems II: Express*

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27. Y. Liu, Y. Huang, **S. Deng**, M. Wong, H. S. Kwok, and R. Chen, "Dimension Scaling Effects on Conduction and Low Frequency Noise Characteristics of ITO-Stabilized ZnO Thin Film Transistors", *IEEE Journal of the Electron Devices Society*. (Under review)

Conference:

1. **S. Deng**, R. Chen, G. Li, M. Zhang, F. S. Y. Yeung, M. Wong, and H. S. Kwok, "P-16: Stacked PECVD SiO_2 Gate Insulators for Top-Gate Metal Oxide Thin- Film Transistors in Enhancement Operation Mode", *SID 2019 International Symposium Digest of Technical Papers*, vol. 50, no. 1, pp. 1271-1274, San Jose, USA, May 2019.
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7. **S. Deng**, R. Chen, G. Li, Z. Xia, K. Wang, M. Zhang, W. Zhou, M. Wong, and H. S. Kwok, "Achievement of High-Performance and Environmentally Stable TFTs by Introducing Hybrid-Phase Microstructure into InSnZnO Channels", *23rd International Display*

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8. **S. Deng**, R. Chen, G. Li, Z. Xia, K. Wang, M. Zhang, W. Zhou, M. Wong, and H. S. Kwok, "Hybrid-Phase Microstructure in Indium-Tin-Zinc-Oxide Thin Films and Its Application to High-Performance Thin-film Transistors", *2018 Cross-Strait Postgraduate Workshop on Display Research*, pp. 8-10, Guangzhou, China, Sept. 2016.
9. **S. Deng**, R. Chen, W. Zhou, J. Y. L. Ho, M. Wong, and H. S. Kwok, "Fabrication of High-Performance Bridged-Grain Polycrystalline Silicon Thin-Film Transistors with Laser Interference Lithography Technology", *The International Display Manufacturing Conference & 3D Systems and Applications (IDMC/3D-SA'15)*, CP3-007, Taipei, Taiwan, Aug. 2015.
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12. M. Zhang, Y. Yan, W. Zhou, R. Chen, **S. Deng**, M. Wong, and H. S. Kwok, "Degradation Behaviors of Driving Thin-Film Transistors in Active-Matrix Organic Light-Emitting Diode Displays", *2018 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC'18)*, pp. 1-3, Shenzhen, China, June 2018.
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17. R. Chen, **S. Deng**, Z. Xia, M. Zhang, W. Zhou, M. Wong, and H. S. Kwok, "High Performance Thin-film Transistors with Hybrid-phase ITO-stabilized ZnO Active Channel Layer", *2017 International Conference on Display Technology (ICDT'17)*, 29.5, Fuzhou, China, Feb. 2017.
18. R. Chen, **S. Deng**, W. Zhou, and H. S. Kwok, "Hybrid-Phase Microstructure in InSnZnO Thin Film and Its Application to High-Performance TFT", *7th International Conference on Computer Aided Design for Thin-Film Transistors (CAD-TFT'16)*, p. 102, Beijing, China, Oct. 2016.
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Patent:

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3. R. Chen, S. Deng, and H. S. Kwok, "Hybrid-phase microstructural inorganic metal oxide thin film and method of manufacturing the same", US Patent. (Pending)
4. R. Chen, S. Deng, and H. S. Kwok, "具有复合晶型的无机金属氧化物薄膜晶体管及其制造方法", Chinese Patent No. 201711000066.0, 24 Oct. 2017. (Pending)
5. R. Chen, S. Deng, and H. S. Kwok, "一种具有复合晶型的无机金属氧化物薄膜及其制

造方法”, Chinese Patent No. 201711000109.5, 24 Oct. 2017. (Pending)

Award:

1. **Academic Award for Continuing PhD Students**, *School of Engineering, HKUST*, 2019.
2. **Best Poster Presentation Award**, *Cross-Strait Postgraduate Workshop on Display Research*, 2018.
3. **Distinguished Poster Award**, *The International Display Manufacturing Conference (IDMC’17)*, 2017.
4. **Best Oral Presentation Award**, *Cross-Strait Postgraduate Workshop on Display Research*, 2016.
5. **Distinguished Paper Award**, *The International Display Manufacturing Conference & 3D Systems and Applications (IDMC/3D-SA’15)*, 2015.