All-Oxide Thin-Film Transistors for Low-Voltage-Operation Circuits

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Abstract

This work reports fully transparent all-oxide thin-film transistors (TFTs) and circuits with high electrical performance under a one-volt operation. By configuring a high oxygen partial pressure ratio in the deposition of indium-tin oxide (ITO) source/drain (S/D) pads, non-ohmic S/D contacts were formed to regulate a noise-level off-state current and a nearly-zero turn-on voltage for the devices. Depending on different post-annealing time, the one-volt operation was realized in both normally-on and normally-off TFTs. Among various unipolar-TFT-based inverters, the one composed of the normally-off devices exhibited a record small power-delay product of ~0.35 pJ. These results are applicable to the development of energy-efficient wearable electronics.

Author Keywords

All-oxide; thin-film transistor; inverter; source/drain contact; post-annealing; low-voltage operation.

1. Introduction

Apple Watch Series 4 was equipped with a low-temperature poly-crystalline silicon and oxide (LTPO) thin-film transistor (TFT) backplane, which can be driven with a refresh rate as low as 1 Hz [1]. The extension of battery life strongly indicates a great potential of metal oxide (MO) TFT technology in energy-efficient applications. To facilitate the further development of wearable electronics, MO TFTs already having an extremely low off-state current (I_{off}) should be also compatible with a low-voltage operation mode because static power consumption (P_{static}) and dynamic power consumption ($P_{dynamic}$) of circuits are proportional to supply voltage (V_{dd}) and its square (V_{dd}^2), respectively. However, to date, only a small number of MO TFTs are possible to exhibit a sufficiently high on/off ratio (i.e., $\geq 10^5$) at a low V_{dd} (e.g., 1 volt).

To support the low-voltage operation of MO TFTs, many efforts to boost areal gate insulator capacitance (C_{ox}) have been made. The common methods are to adopt high-k gate insulators (GIs) and to decrease GI thickness. Then, an equivalent or even higher on-state current (I_{on}) can be recorded despite a reduced V_{dd}. While dielectrics like Al_2O_3 [2], ZrO_2[3] Ta_2O_5 [4] and HfO_2 [5] are effective high-k GI candidates, their high-quality deposition usually relies on an atomic layer deposition (ALD) technique, the growth rate of which is much slower than that of plasma-enhanced chemical vapor deposition (PECVD). Apparently, the reduction of GI thickness can save the deposition time, but this solution often brings about the increase of gate leakage (I_g) and I_{off} at the same time.

The on-off ratio is directly associated with not only the I_{on} but also the I_{off}. If MO TFTs exhibit an I_{off}-level drain current (I_d) (i.e., below the measurement limit of a typical semiconductor parameter analyzer [6]) at zero-volt gate bias (V_{gs}), it should not be difficult to operate these devices at a low voltage. Top-gated hybrid-phase ITO-stabilized ZnO TFTs have been reported with a high field-effect mobility (μ_{fe}, ~18 cm^2/Vs) and a steep subthreshold swing (SS, <0.1 V/decade), a noise-level I_{off} (<10 fA) after being capped by stacked PECVD SiO_2 GIs [7] and transparent ITO gates [8]. However, because of redundant carriers in the channels, their I_d@0V (i.e., I_d at V_{gs}=0 V) was still a bit large (10~100 nA), so their low-voltage operation has not been realized yet.

In this work, we introduced non-ohmic source/drain (S/D) contacts to the devices for further suppressing the I_d@0 V. Although the non-ohmic S/D contacts lead to large S/D contact resistance and restrict current flow from drain to source, they are effective to regulate a noise-level I_{off} and a nearly-zero turn-on voltage (V_{on}) for the devices even with a carrier concentration (N_e) as high as ~10^{19} cm^{-3} in the channels [9]. Depending on different post-annealing time, both normally-on and normally-off devices were fabricated. The all-oxide inverters with optical transparency were further demonstrated at a supply voltage of 1 V.

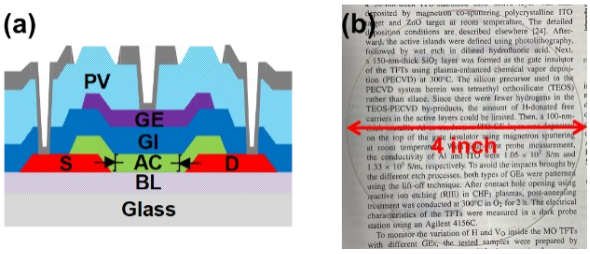

Figure 1. (a) Cross-sectional schematic diagram of the all-oxide TFT in this work. (b) Photography of the all-oxide TFTs and circuits on a 4-inch glass wafer.

2. Fabrication Processes

Fig. 1 (a) is the cross-sectional schematic of the low-voltage TFTs in this study. The devices are all composed of oxides, so they have a high optical transmittance of 77%~92% in the visible band [10], as shown in Fig. 1(b). The fabrication was performed on 4-inch circular glass wafers coated with a 300-nm-thick low temperature oxide (LTO) buffer layer. To avoid any sneak conducting paths caused by etching residues, a lift-off technique was used to pattern separated S/D pads after the magnetron sputtering of a 50-nm-thick ITO layer. In the sputtering step, a 2-inch circular ITO target (90 wt% In_2O_3 and 10 wt% SnO_2) was connected to a direct-current (DC) power supply (120 W). The base and working pressure in the chamber were pumped to 8 μTorr and 3 mTorr, respectively. The flow rate of Ar (FR(Ar)) was fixed at 20 sccm, and that of O_2 (FR(O_2)) was configured in the range between 0.2 sccm and 4 sccm. Thus, the derived oxygen partial pressure ratio

(P_{O2}=FR(O_2)/(FR(O_2)+FR(Ar))) varied from 0.99% to 16.67%. Next, a 50-nm-thick hybrid-phase ITO-stabilized ZnO channels, a 150-nm-thick PECVD SiO_2 GI stacks, and 100-nm-thick ITO gates were formed in sequence. The details have been described elsewhere [7][8]. After thermal annealing at 300 °C in air for 1.5 h, the devices were covered by a 300-nm-thick PECVD SiO_2 passivation layer. Then, contact holes were opened atop the S/D and gate pads using reactive ion etching (RIE) in CHF_3 plasmas, followed by the formation of 100-nm-thick ITO contact pads and interconnections. Finally, the devices were subjected to post-annealing at 300 °C in air for 2.5 h or 10 h.

The electrical characteristics of the TFTs and the circuits were measured in a dark probe station using a semiconductor parameter analyzer (Keysight B1500). The work function of the ITO S/D pads was measured by ambient Kelvin probe (KP Technology Ltd.).

3. Results and Discussion

Fig. 2(a) shows the work function (Φ_{ITO}) of the ITO S/D pads under different P_{O2}. The results are all located in a narrow range (4.4~4.5 eV). Considering the band diagram of the ITO-stabilized ZnO channels, Schottky junctions with a barrier height ($q\Delta\varphi_B$) of ~0.9 eV are expected to exist between the S/D pads and the channels, as illustrated in Fig. 2(b). The barriers help to restrict carrier transport and probably regulate I_d@0 V to the noise level. However, the fact is not in agreement with our analysis.

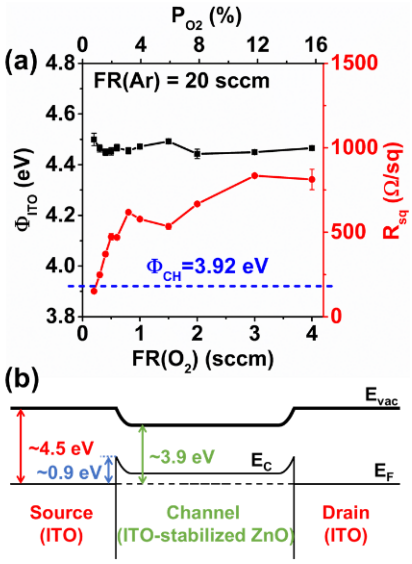

Figure 2. (a) Work function (Φ_{ITO}) and sheet resistance (R_{sq}) of the ITO S/D pads under different oxygen partial pressure ratios (P_{O2}). (b) Band diagram for the source-drain current path.

Fig. 3(a)-(b) compare output curves of the all-oxide TFTs with low-compensation (LC), medium-compensation (MC), and high-compensation (HC) ITO S/D pads. The corresponding FR(O_2) (P_{O2}) is 0.2 sccm (0.99%), 0.4 sccm (1.96%) and 0.6 sccm (2.91%), respectively. For the HC devices, their S/D contacts are non-ohmic, but the rectifying I-V characteristic is not distinct when a low V_{gs} (≤5 V) is applied. For the LC and MC devices, they have quasi-ohmic other than non-ohmic S/D contacts with a slight current clamping effect. A plausible explanation for the S/D contact discrepancy among the devices is that ITO sputtered at a low P_{O2} level generates too many positively charged oxygen vacancies (V_O^+) and substituted Sn^{4+}, which may diffuse as dopants from the S/D pads to the channels during post-annealing [11]-[13]. Thus, the quasi-ohmic S/D contacts are formed in the LC and MC devices with depletion regions between the S/D pads and the channels highly doped. These positively charged dopants should be sensitive to an electric field, so the ones in the depletion regions may also drift back to the S/D pads when a positive V_{gs} is applied. That is why the S/D contacts of the HC TFTs with less dopants inside look more and more like junctions with the increase of V_{gs}. Fig. 3(c) describes the relationship between total device resistance (R_{tot}=2R_{SD}+R_{CH}*L) and channel length (L) in the all-oxide TFTs. R_{SD} denotes the S/D contact resistance, and R_{CH} represents the channel sheet resistance. In the LC devices, their R_{CH} is increasingly larger with the elongation of the channels, reflecting that the channels' central region is more resistive than their marginal region near the ITO S/D pads. This is consistent with the explanation that the dopants origin from the S/D pads and diffuse along the channel length direction in the post-annealing process.

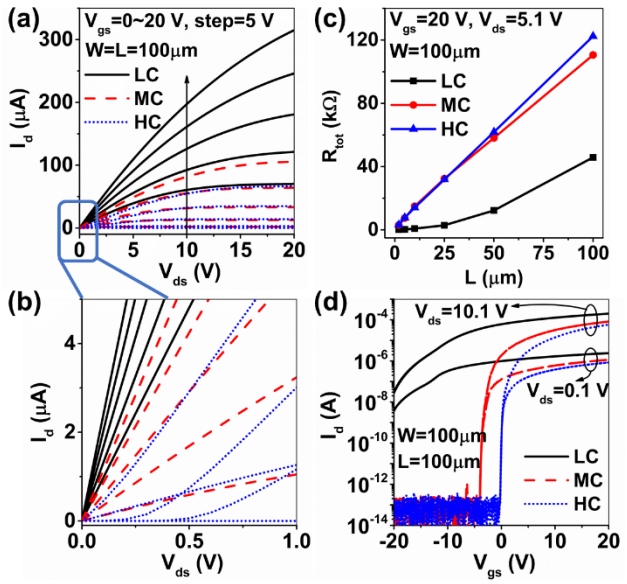

Figure 3. (a) Output and (d) transfer curves of the all-oxide TFTs with the LC, MC and HC ITO S/D pads. (b) is a magnification of (a). (c) Total device resistance (R_{tot}) as a function of channel length (L) in the all-oxide TFTs with the LC, MC and HC ITO S/D pads.

Fig. 3(d) shows transfer curves of the all-oxide TFTs with different ITO S/D pads. The LC devices with junction-less S/D contacts almost lose their switching behavior, and the MC devices have a negative V_{on} of -4 V. In contrast, the HC devices with S/D junctions well regulate the onset of channel accumulation, exhibiting a V_{on} of -0.3 V, an I_d@0 V of below 1 nA, and an on-off ratio of $>10^{10}$. These electrical characteristics allow the one-volt operation of the HC TFTs, but additional voltage conversion designs for generating negative electric levels between -1 V and 0 V are needed to fully turn off the channels. Otherwise, the practical on-off ratio (i.e., I_{on} divided by I_d@0 V) is only $1.4*10^2$, which is far below the minimum requirement (i.e., $\geq 10^5$) of qualified switching TFTs.

If the HC TFTs with a negative V_{on} is classified as normally-on devices, our next task should be to obtain normally-off devices with a positive V_{on}. Fig. 4(a) shows the transfer curves of the all-oxide TFTs with different over-compensated (OC) ITO S/D pads.

Unfortunately, a larger FR(O_2) (>0.6 sccm) or a higher P_{O2} (>2.91%) is useless for the positive shift of V_{on}. This is presumably because the ITO S/D pads and the channels have formed stable contacts, which are less affected by the oxygen-related factors.

Now that the adjustment on the P_{O2} is hard to access the normally-off TFTs, we then attempted to perform a longer post-annealing for the HC devices since post-annealing is an effective method to reduce N_e in the channels and diminish defects in the devices. Fig. 4(b) plots the transfer curve of the HC TFTs after 10-hour post-annealing. Compared with the normally-on devices, the normally-off devices suffer an I_{on} reduction by ~3 times, but their I_d@0 V is significantly decreased by at least two orders of magnitude at the same time. Therefore, the practical on-off ratio reaches as high as ~10^6, indicating that the one-volt operation with no need for negative electric levels is feasible. The key electrical parameters of both normally-off and normally-on all oxide devices under the one-volt operation are summarized in Table 1.

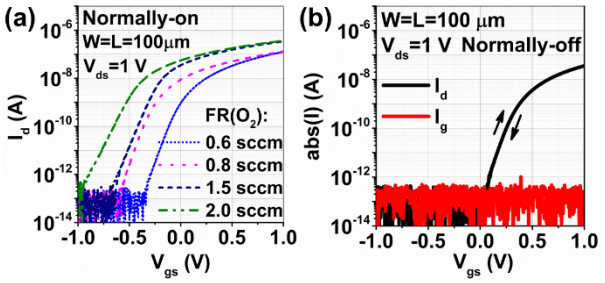

Figure 4. Transfer curves of the all-oxide TFTs (a) with the different OC ITO S/D pads after 2.5-hour post-annealing and (b) with the HC ITO S/D pads after 10-hour post-annealing.

Table 1. Key electrical parameters of the all-oxide TFTs under the one-volt operation

	Normally-on	Normally-off
μ_{fe} (cm^2/Vs)	11.1	5.1
SS (mV/decade)	76.5	69.1
V_{on} (V)	-0.33	0.06
Max. on-off ratio	6.3*10^7	1.2*10^7
Practical on-off ratio	1.4*10^2	10^6

Utilizing the one-volt all-oxide TFTs, we fabricated a zero-V_{gs} inverter in Fig. 5. The inverter exhibits a gain of 9.2 V/V, a maximum P_{static} of ~402 pW, and an output power consumption (P_{out}=V_{out}*I_{dd}) ~72 pW under a V_{dd} of 1 V. Therefore, it is possible to be driven by sub-nanowatt power sources. Considering that the output current (I_{dd}) passing through the devices is quite low, the semiconductor parameter analyzer was used to detect output signals. Through loading square wave signals with a frequency of 200 Hz to the input, the rise time (t_r) and fall time (t_f) of the output signal can be measured as ~538 μs and ~204 μs, respectively. The long propagation delay (τ_{pd}~742 μs) is caused by the low I_{dd}. For unipolar-TFT-based inverters, their I_{dd} is intrinsically large in a certain logic state, leading to a high power consumption. In this work, due to a good confinement of both I_g and I_d by introducing the PECVD SiO_2 GI stacks, transparent ITO gates and non-ohmic S/D contacts, the inverter has a sub-nanoampere I_{dd} and an excellent power-delay product (V_{dd}*I_{dd}*τ_{pd}) of only ~0.35 pJ. To authors' knowledge, this power-delay product is the lowest among the inverters built with the n-type MO TFTs. Although the inverter operation frequency (~1347 Hz) is not high, but it covers the common frequency band of human body signals. Therefore, the inverter and other integrated circuits composed of the low-voltage all-oxide TFTs is applicable to wearable electronics for personal medical monitoring and human-machine interaction.

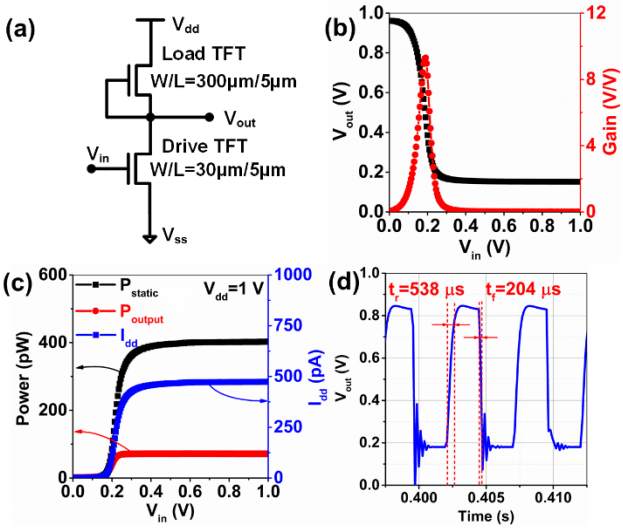

Figure 5. (a) Schematic circuit of the zero-V_{gs} inverter composed of the low-voltage all-oxide TFTs. (b) Measured output voltage (V_{out}) and gain, (c) quasi-static current (I_{dd}), static power consumption (P_{static}) and output power consumption (P_{output}) as a function of input voltage (V_{in}). (d) Output waveform of the inverter with a 200-Hz square wave input.

4. Conclusions

In this work, we demonstrated the low-voltage operation of the all-oxide fully transparent TFTs by employing the non-ohmic S/D contacts. While the work function difference between the S/D and the channels varied slightly, the S/D contacts could evolve from a junction-less type to a junction-like type with the increase of P_{O2} during the ITO S/D pad deposition. Only the HC TFTs with the non-ohmic S/D contacts owned an on-off ratio of >10^5 under the one-volt operation. Depending on the post-annealing time, both normally-on and normally-off TFTs were further fabricated. The inverter composed of the one-volt all-oxide TFTs exhibited a sub-nanowatt power consumption, a kilohertz operation frequency, and a record small power-delay product of ~0.35 pJ among unipolar-TFT-based inverters. These devices and circuits are useful for the development of energy-efficient wearable electronics.

5. Acknowledgements

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6. References

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