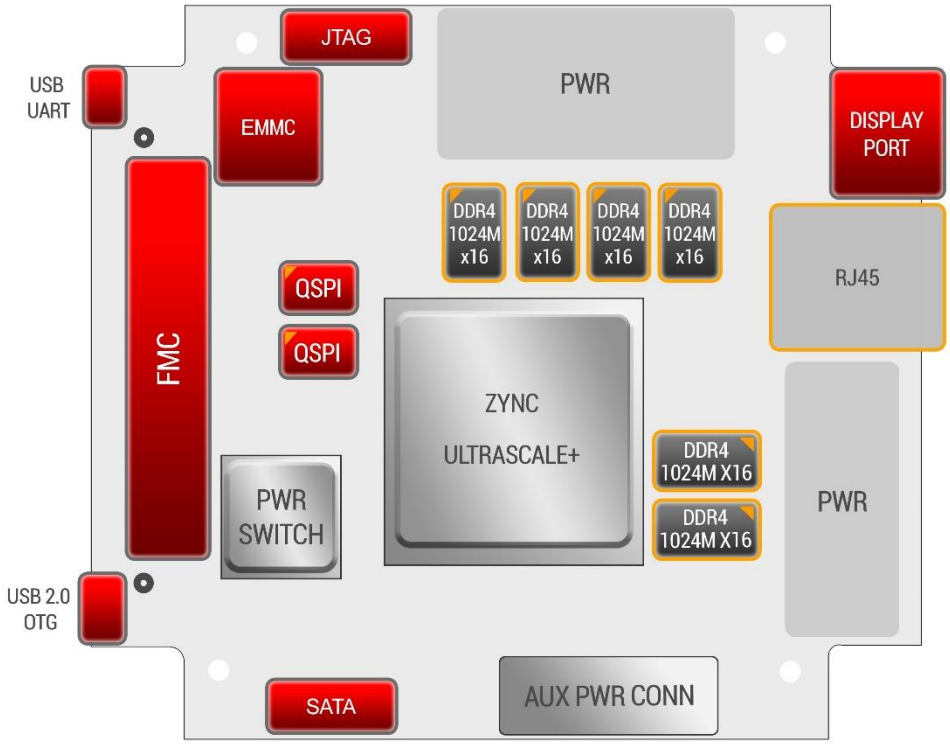
Unit / Module Description:	ZU+ based, PC/104 form factor, FMC carrier board
Unit / Module Number:	PCIe104Z
Document Issue Number:	1.1
Issue Date:	04/05/19
Original Author:	Timoteo Garcia

Product Specification for PCIe104Z



Sundance Multiprocessor Technology Ltd, Chiltern House, Waterside, Chesham, Bucks. HP5 1PS.

Revision History

Issue	Changes Made	Date	Initials
1.0	First draft	15/04/19	TG
1.1	Updated diagram	04/05/19	TG

Table of Contents

Figures

Tables

1 Introduction

This document describes the hardware specifications of the PCIe104Z card. This board is a carrier based on Zynq Ultrascale+ MPSoC architecture from Xilinx, with PC/104 form factor, for scalable solutions, and in compliance with FMC standards, to amplify the connectivity with FMC-compatible daughter cards.

2 Main features

PCIe104Z's main processing device is a Xilinx Zynq Ultrascale+ MPSoC. The user can order any of the following: XCZU7EV, XCZU7EG, XCZU11EG, XCZU7CG (C1156 package), essentially offering:

- Processor: Dual-coreARM® Cortex™-A53 MPCore™ up to 1.3GHz (XCZU7CG), or Quad-coreARM® Cortex™-A53 MPCore™ up to 1.5GHz (XCZU7EV, XCZU7EG, XCZU11EG)
- Real-Time processor: Dual-coreARM Cortex-R5 MPCoreup to 533MHz (XCZU7CG) and up to 600MHz (XCZU7EV, XCZU7EG, XCZU11EG)
- GPU Mali™-400 MP2 up to 667MHz (XCZU7EV, XCZU7EG, XCZU11EG only)
- Video codec H.265/H.264 in the Programmable Logic (XCZU7EV only)

Through different characteristics of the PS/PL, the ZU+ device, along with the peripherals of PCIe104Z, these are the main features of the board:

- Scalable through PCIe.
  - PCIe Switch PEX8606 to stack up 4 cards
  - 4x PCIe Gen2 in the Processing System
  - Gen3x16/Gen4x8 in the Programmable Logic
- Expandable through FMC
  - Direct access to FMC cards through the PL, 10xGTH at 16.3Gb/s transceivers and 80 LVDS IO pairs
- External DDR4 memory, 8GB (PS), 4GB (PL)
- Configuration/booting
  - Flash memory for QSPI boot
  - eMMC flash (8GB)
  - JTAG interface for programmability/debug
- 4x Tri-mode Gigabit Ethernet through RJ45 connector
- Display 1.2 port/connector
- 1x Micro-USB 2.0 connector with OTG
- 1x USB 3.0 interface via (PCIe connector)
- 1x SATA 3.0
- USB-UART

Documentation of the Xilinx device family provide more information regarding specific details of the architecture for the different parts.

For a deep understanding of the interfaces, refer to the technical reference manual (UG1085)

3 Acronyms, Abbreviations and Definitions

3.1 Acronyms and Abbreviations

MPSoC	Multi-Processor System-On-Chip
GPU	Graphics Processing Unit
IP	Intellectual Property
JTAG	Joint Test Action Group
QSPI	Quad Serial Peripheral Interface
eMMC	Embedded Multimedia Card
DDR	Double Data Rate
I2C	Inter-Integrated Circuit
RGMII	Reduced Gigabit Media Independent Interface
IC	Integrated Circuit
PCIe	Peripheral Component Interconnect Express
USB	Universal Serial Bus
SATA	Serial AT Attachment
UART	Universal Asynchronous Receiver/Transmitter
FMC	FPGA Mezzanine Card
ULPI	Utmi+ Low Pin Interface

4 Functional Description

4.1 Block Diagram

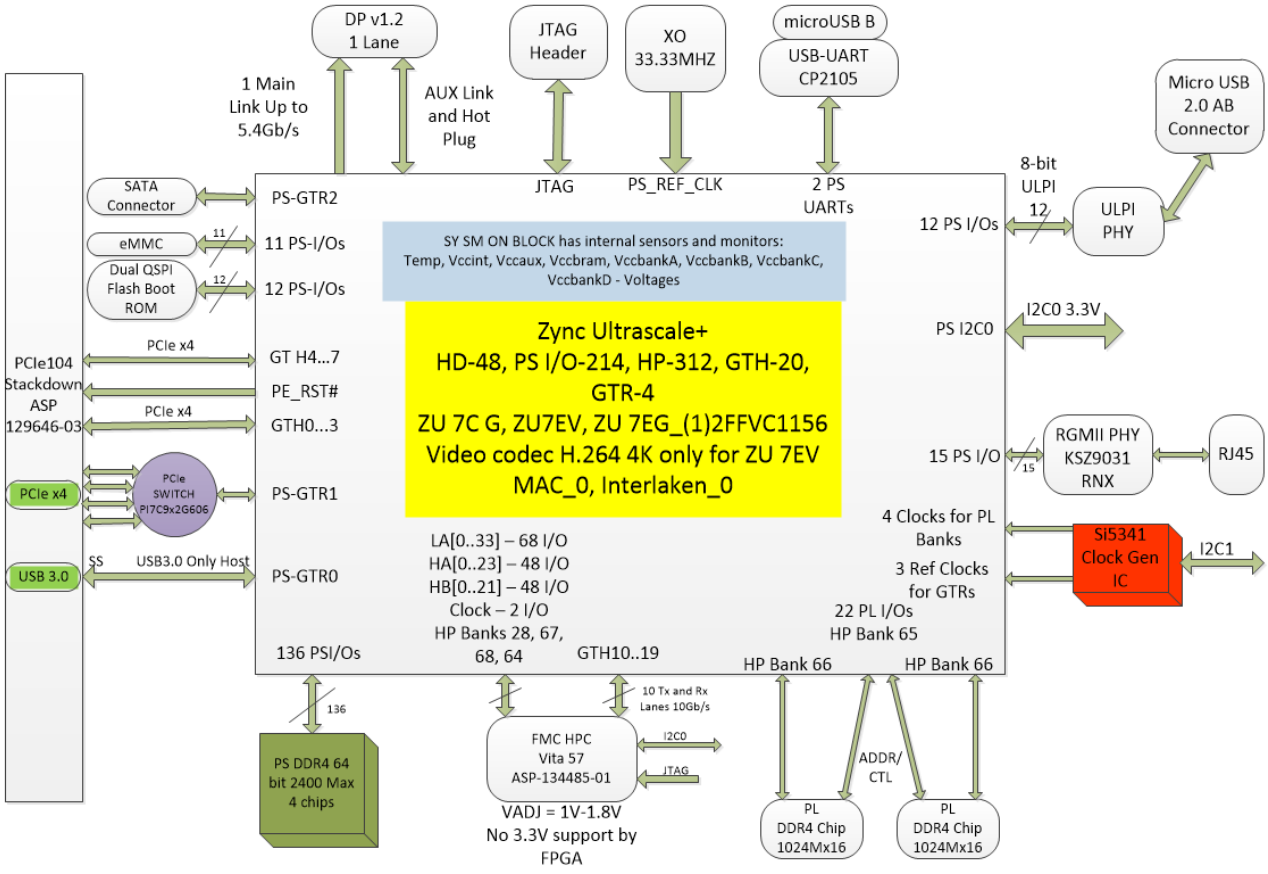


Figure 1- PCIE104Z diagram

4.2 Module Description

4.2.1 Xilinx Zynq Ultrascale+ device

The main processing device is a Xilinx Zynq Ultrascale+ MPSoC. The user can order any of the following: XCZU7EV, XCZU7EG, XCZU11EG, XCZU7CG (C1156 package).

The Zynq Ultrascale+ architecture responds to a well defined structure divided in two main parts, called Processing System and Programmable Logic. Depending on the device chosen by the user (CG, EG or EV), some features in the PS/PL differ. In Figures 2, 3 and 4, the architectures for CG, EG and EV are shown:

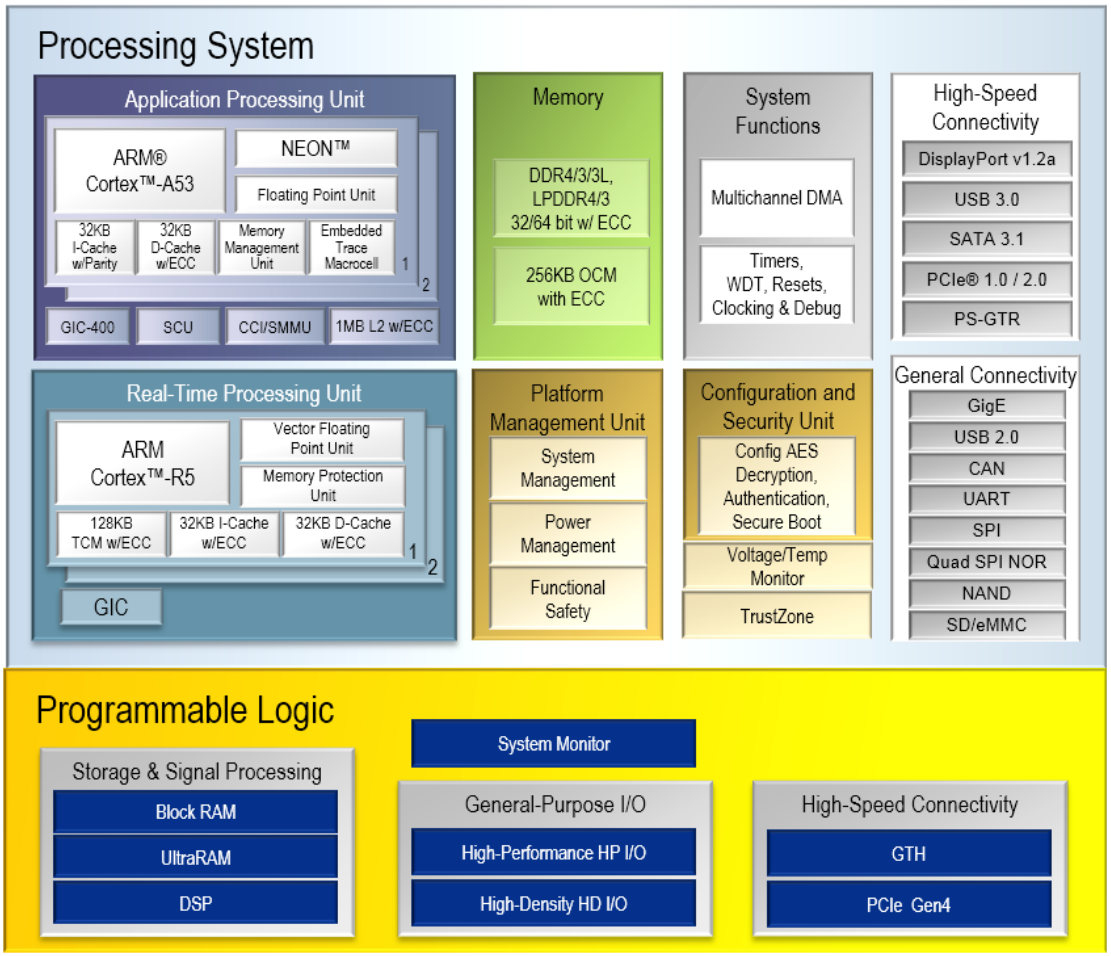


Figure 2- PCIE104Z with ZU+ (CG)

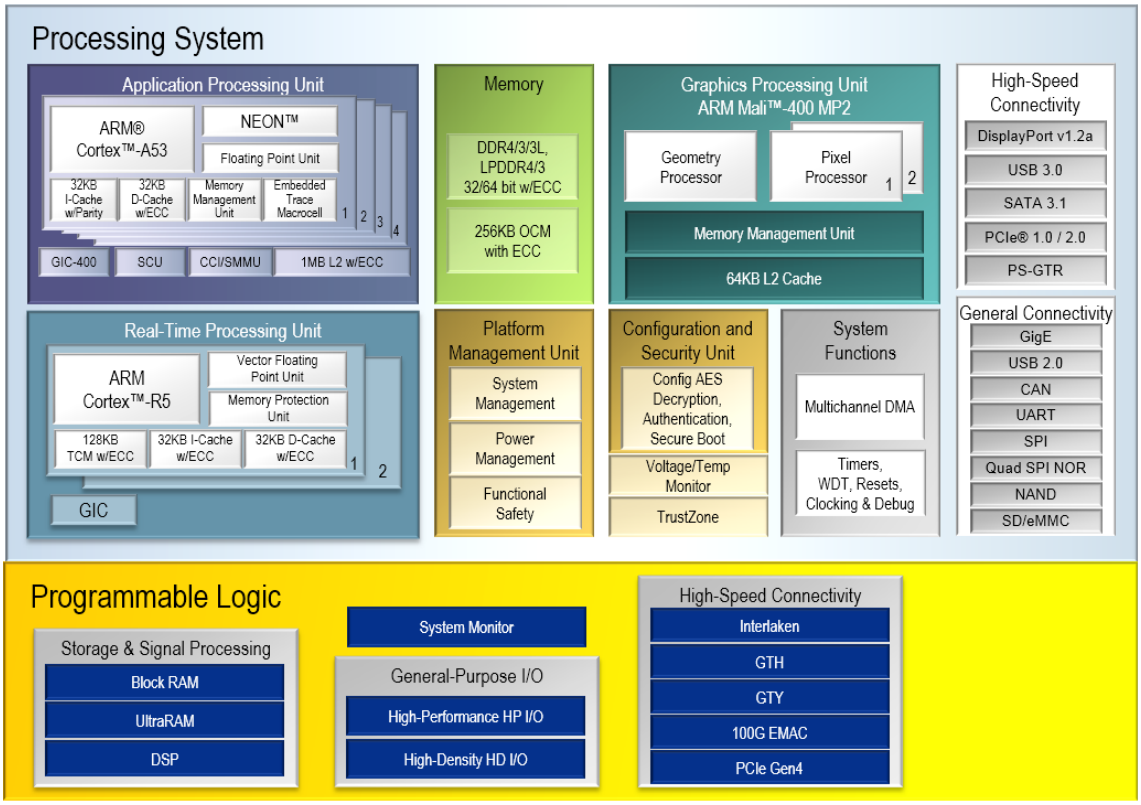


Figure 3- PCIE104Z with ZU+ (EG)

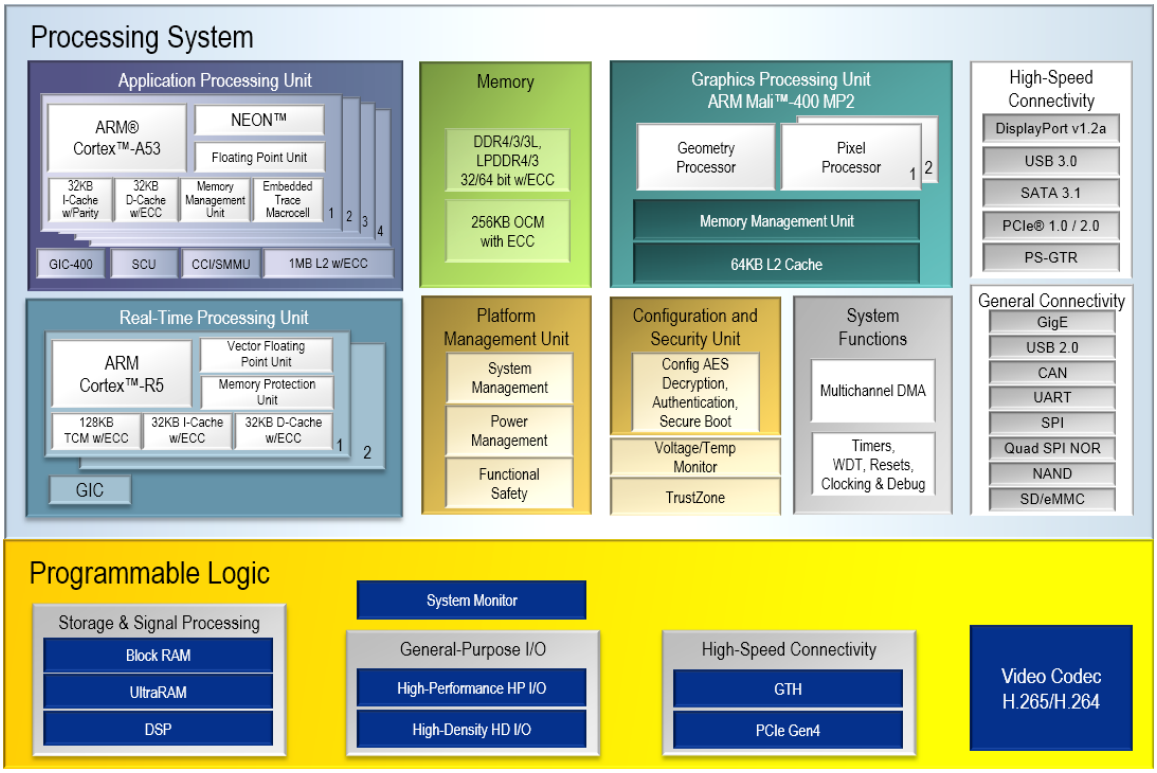


Figure 4- PCIE104Z with ZU+ (EV)

The essential difference relies on the Dual/Quad core structure in the Application Processing Unit, and the presence of GPU in the PS. On the other hand, the presence of transceivers and a built-in video codec in the PL as part of the embedded primitives.

Xilinx offers full documentation of the different controllers within the PS, including drivers and support for both standalone and OS-based applications. Also, the majority of IPs available in Xilinx tools for the PL implementation are license-free, and fully documented.

4.2.2 Power

The power is supplied at 12V and 5V through PC/104 or alternatively from an external connector.

On board power supply provides all the necessary voltages for the modules.

Built-in SYSMON module in FPGA provide temperature and on chip voltage monitoring. All necessary connections are made inside the device.

NOTE! User must check their design in Xilinx power estimation spreadsheet and make sure that the MPSOC device consumes less than 50Amps by VCORE, otherwise design may work but with instability or lead to board damage.

Other board components' average consumption equals approximately 40W (including USB ports).

VADJ voltage selected with logic levels at nets VADJ_V(2:0), levels must be changed when EN_VADJ is 0. After selecting required level EN_VADJ must be set to logic 1

Voltage	VADJ_V2	VADJ_V1	VADJ_V0
1.0 Default	0	0	0
1.2	0	0	1
1.25	0	1	0
1.35	1	0	0
1.45	0	1	1
1.55	1	0	1
1.6	1	1	0
1.8	1	1	1

Table 1- VADJ

4.2.3 Configuration and booting process

The Zynq Ultrascale+ device can be configured/booted in different ways. The following table summarises the boot modes:

Boot mode selected through SW1 DIP switch.

Boot Mode	SW1.1	SW1.2	SW1.3	SW1.4
JTAG	ON	ON	ON	ON
QSPI24 mode (default)	OFF	ON	ON	ON
QSPI32 mode	ON	OFF	ON	ON
eMMC boot	ON	OFF	OFF	ON
Others unsupported				

Table 2- SW1 Boot configuration

- JTAG

Reference designator of connector is X1, located on page 2 of schematic. All signals, except VREF_3V3, are ESD and short-circuit protected.

GND	1	2	VREF_3V3
NC	3	4	JTAG_TMS
GND	5	6	JTAG_TCK
GND	7	8	JTAG_TDO (O)
GND	9	10	JTAG_TDI (I)
GND	11	12	JTAG_TRST#
GND	13	14	SRST#

Table 3- JTAG pinout

- QSPI Flash

The Quad-SPI flash memory located at D16 and D17 provides 2 x 512 Mb of non-volatile storage that can be used for configuration and data storage.

  - Part number: MT25QU512ABB8E12 – Micron
  - Supply voltage: 1.8V
  - Data path width: 4 bit
  - Maximum clock: 108 MHz
  - Package: BGA-24

Connections between SPI flashes and MPSoC are listed below:

XCZU7EV		Schematic Net Name	QSPI Device	
Pin Name	**Pin Number**		**Pin Number**	**Pin Name**
PS_MIO4	A25	SPI0_DQ0	D3	DQ0/DIN
PS_MIO1	C24	SPI0_DQ1	D2	DQ1/DOUT
PS_MIO2	B24	SPI0_DQ2	C4	W#/Vpp/DQ2
PS_MIO3	E25	SPI0_DQ3	D4	DQ3/HOLD#
PS_MIO0	A24	SPI0_CLK	B2	C
PS_MIO5	D25	SPI0_CS#	C2	S#
PS_MIO8	D26	SPI1_DQ0	D3	DQ0/DIN
PS_MIO9	C26	SPI1_DQ1	D2	DQ1/DOUT
PS_MIO10	F26	SPI1_DQ2	C4	W#/Vpp/DQ2
PS_MIO11	B26	SPI1_DQ3	D4	DQ3/HOLD#
PS_MIO12	C27	SPI1_CLK	B2	C
PS_MIO7	B25	SPI1_CS#	C2	S#

Table 4- QSPI pinout

- eMMC interface

The SDIO interface connected to eMMC 8GByte chip, also this interface provides boot capability.

  - IC part number: KLM8G1GEAC-B031;
  - Supply voltage: 3.3V;
  - I/O voltage: 1.8V
  - Data path width: 8 bit;

Connections between SDIO interface and chip are listed below:

XCZU7EV		Schematic Net Name
Pin Name	Pin Number	
PS_MIO13	D27	MIO_MMC_D0
PS_MIO14	A27	MIO_MMC_D1
PS_MIO15	E27	MIO_MMC_D2
PS_MIO16	A28	MIO_MMC_D3
PS_MIO17	C29	MIO_MMC_D4
PS_MIO18	F27	MIO_MMC_D5
PS_MIO19	B28	MIO_MMC_D6
PS_MIO20	E29	MIO_MMC_D7
PS_MIO21	C28	MIO_MMC_CMD
PS_MIO22	F28	MIO_MMC_CLK
PS_MIO23	B29	MIO_MMC_RST#

Table 5- eMMC pinout

4.2.4 Memory

External DDR4 memory is available for the PS to manage, which stores up to 8GB of data, distributed in four chips of 2400MT/s.

There are 4GB of external DDR4 memory accessible from the PL to additional data storage.

HP Banks 65, 66 used for DDR4 interface. VRP pin connected via 240ohms resistor to ground.

XCZU7EV banks 65,66 VCCIO 1.2V			Name and description
Ball Name	Ball Num	Direction MpSoC	
IO_L1P_N0_65	AP19	Out	PL_DDR_CKE
IO_L1N_N1_65	AP20		PL_DDR_BG0
IO_L2P_N2_65	AM19		DDR4 ODT signal
IO_L2N_N3_65	AN19		PL_DDR_WE#(DDR_A14)
IO_L3P_N4_65	AP21		PL_DDR_A6
IO_L3N_N5_65	AP22		PL_DDR_A11
IO_L4P_N6_65	AM21		PL_DDR_A0
IO_L4N_N7_65	AN21		PL_DDR_BA0
IO_L5P_N8_65	AN22		PL_DDR_A2
IO_L5N_N9_65	AP23		PL_DDR_A8
IO_L6P_N10_65	AM23		DDR PARITY Signal
IO_L6N_N11_65	AN23		DDR RESET#
IO_L7P_N0_65	AL20		PL_DDR_ACT#
IO_L7N_N1_65	AL21		PL_DDR_CAS#(DDR_A15)
IO_L8P_N2_65	AL22		PL_DDR_A1
IO_L8N_N3_65	AL23		PL_DDR_A4
IO_L9P_N4_65	AJ19		PL_DDR_A12
IO_L9N_N5_65	AK19		PL_DDR_CS#
IO_L10P_QBC_65	AK22		PL_DDR_BA1
IO_L10N_QBC_65	AK23		PL_DDR_A10

IO_L11P_N8_65	AJ20	In/Out	DDR4 ALERT# in to MpSoC in normal mode, out in test mode	
IO_L11N_N9_65	AK20	Out	PL_DDR_A3	
IO_L12P_GC_65	AJ21	In	System 300MHz clock input for core, from SI5341 OUT0	
IO_L12N_GC_65	AJ22			
IO_T1U_N12_65	AH19	Out	PL_DDR_BG1	
IO_L13P_N0_65	AH22	In/Out	PL_DDR_A9	
IO_L13N_N1_65	AH23	Out	PL_DDR_A13	
IO_L14P_N0_65	AG21		PL_DDR_A5	
IO_L14N_N1_65	AH21		PL_DDR_A7	
IO_L15P_N4_65	AG19		PL_DDR_RAS#(DDR_A16)	
IO_L15N_N5_65	AG20		PL_DDR_TEN test enable, Low for normal operation	
IO_L16P_N6_65	AF23		DDR4 clock for chips	
IO_L16N_N7_65	AG23			
IO_L24N_PERSTN0	AA20		PCIE RESET – reset for PCIe EP	
BANK 66 DEDICATED TO DATA BUS DATA BYTE 0				
IO_L1P_N0_66	AN12	BiDir.	PL_DDR_DM0	Chip 1 DML
IO_L2P_N2_66	AP10		PL_DDR_D3	Chip 1 DQ3
IO_L2N_N3_66	AP9		PL_DDR_D1	Chip 1 DQ1
IO_L3P_N4_66	AN11		PL_DDR_D5	Chip 1 DQ5
IO_L3N_N5_66	AP11		PL_DDR_D7	Chip 1 DQ7
IO_L4P_N6_DBC_66	AN9		PL_DDR_DQS0+	Chip 1 DQS_L+
IO_L4N_N7_DBC_66	AN8		PL_DDR_DQS0-	Chip 1 DQS_L-
IO_L5P_N8_66	AM11		PL_DDR_D2	Chip 1 DQ2
IO_L5N_N9_66	AM10		PL_DDR_D0	Chip 1 DQ0
IO_L6P_N10_66	AM9		PL_DDR_D4	Chip 1 DQ4
IO_L6N_N11_66	AM8		PL_DDR_D6	Chip 1 DQ6
DATA BYTE 1				
IO_L7P_N0_66	AK13	BiDir.	PL_DDR_DM1	Chip 1 DMU
IO_L8P_N2_66	AL11		PL_DDR_D15	Chip 1 DQ15
IO_L8N_N3_66	AL10		PL_DDR_D9	Chip 1 DQ9
IO_L9P_N4_66	AK12		PL_DDR_D13	Chip 1 DQ13
IO_L9N_N5_66	AL12		PL_DDR_D14	Chip 1 DQ14
IO_L10P_DBC_66	AK8		PL_DDR_DQS1+	Chip 1 DQS_U+
IO_L10N_DBC_66	AL8		PL_DDR_DQS1-	Chip 1 DQS_U-
IO_L11P_N8_66	AJ10		PL_DDR_D12	Chip 1 DQ12
IO_L11N_N9_66	AK10		PL_DDR_D11	Chip 1 DQ11
IO_L12P_N10_66	AJ9		PL_DDR_D10	Chip 1 DQ10
IO_L12N_N11_66	AK9		PL_DDR_D8	Chip 1 DQ8
DATA BYTE 2				
IO_L13P_N0_66	AH12	BiDir	PL_DDR_DM2	Chip 2 DML
IO_L14P_N2_66	AH11		PL_DDR_D16	Chip 2 DQ0
IO_L14N_N3_66	AJ11		PL_DDR_D18	Chip 2 DQ2
IO_L15P_N4_66	AG13		PL_DDR_D19	Chip 2 DQ3
IO_L15N_N5_66	AH13		PL_DDR_D23	Chip 2 DQ7
IO_L16P_DBC_66	AG9		PL_DDR_DQS2+	Chip 2 DQS_L+
IO_L16N_DBC_66	AH9		PL_DDR_DQS2-	Chip 2 DQS_L-
IO_L17P_N8_66	AG11		PL_DDR_D17	Chip 2 DQ1
IO_L17N_N9_66	AG10		PL_DDR_D21	Chip 2 DQ5
IO_L18P_N10_66	AF8		PL_DDR_D20	Chip 2 DQ4
IO_L18N_N11_66	AG8		PL_DDR_D22	Chip 2 DQ6
DATA BYTE 3				
IO_L19P_N0_66	AF11	BiDir	PL_DDR_DM3	Chip 2 DMU
IO_L19N_66	AF10	In	PG_1V2	Power GOOD signal
IO_L20P_N2_66	AD14		PL_DDR_D25	Chip 2 DQ9

IO_L20N_N3_66	AE14	BiDir	PL_DDR_D31	Chip 2 DQ15
IO_L21P_N4_66	AE13		PL_DDR_D24	Chip 2 DQ8
IO_L21N_N5_66	AF13	BiDir	PL_DDR_D26	Chip 2 DQ10
IO_L22P_DBC_66	AC12		PL_DDR_DQS3+	Chip 2 DQS_U+
IO_L22N_DBC_66	AD12		PL_DDR_DQS3-	Chip 2 DQS_U-
IO_L23P_N8_66	AE12		PL_DDR_D30	Chip 2 DQ14
IO_L23N_N9_66	AF12		PL_DDR_D28	Chip 2 DQ12
IO_L24P_N10_66	AB13		PL_DDR_D27	Chip 2 DQ11
IO_L24N_N11_66	AC13		PL_DDR_D29	Chip 2 DQ13

Table 6- DDR Memory pinout

Refer to Xilinx documentation for the implementation of a memory controller in the Programmable Logic.

4.2.5 Clock synthesiser

A clock synthesiser is present on the board, Si5341, which provides up to 10 output clocks, with a frequency range of 100MHz to 1028MHz (differential) or 250MHz (single-ended).

In order to configure the clock synth, a software tool, ClockBuilder Pro can be used to generate the register values, which can be given to the chip through serial interface.

For main and primary clocks SI5341A-B-GM is used it is 10 channel, multi frequency low jitter generator IC, configurable via I2C (address 0x74). It consists of 5 independent fractional dividers and 10 independent integer dividers for each output. This provides capability of 0.001ppb frequency tuning. This IC must be programmed with correct values after board start-up via I2C, or this part can be programmed by factory, using customer values.

During start-up on board oscillator provides 33.333MHz clock to PS part of MPSoC, after booting there is an I2C1 interface, which must be used for interfacing with SI5341A.

Reference clock frequencies for various interfaces

Interface	Required Clock
DDR4 banks	300 MHz
USB Super Speed	100 MHz
SATA	150 MHz
Display port	135 MHz

Table 7- Clock configuration

4.2.6 Ethernet

RGMII interface with PHY provide 10/100/1000BASE-T Connectivity via RJ45 connector.

- PHY IC: KSZ9031RNXIC – Micrel;
- Speed modes: 10/100/1000BASE;
- Link capabilities: Auto MDI/MDI-X, Cable diagnostics.

Connections between RGMII PHY interface and MPSoC are listed below:

XCZU7EV		Schematic Net Name	PHY IC	
Pin Name	Pin Number		Pin number	Pin name
PS_MIO[65:68]	J32,J34,K28,K29	RGMII_TX_D[0:3]	19 - 22	TXD[0:3]
PS_MIO69	K30	RGMII_TX_CTL	25	TX_EN
PS_MIO64	J31	RGMII_TX_CLK	24	GTX_CLK
PS_MIO[71:74]	K32-K34, L29	RGMII_RX_D[0:3]	27,28,31,32	RXD[0:3]
PS_MIO75	L30	RGMII_RX_CTL	33	RX_DV
PS_MIO70	K31	RGMII_RX_CLK	35	RX_CLK
PS_MIO76	L33	RGMII_MDC	36	MDC
PS_MIO77	L34	RGMII_MDIO	37	MDIO
PS_MIO38	C34	RGMII_RST#	42	RESET_N
PS_MIO43	E30	RGMII_INT#	38	INT_N

Table 8- Ethernet pinout

4.2.7 UARTs to USB bridge

Bridge provide UART signalling with hardware flow control via USB interface. This is intended for debug or for data exchange between various devices. Both UARTs from ARM routed to bridge IC.

- Connector Part number: 10118193-0001LF – FCI, micro USB B;
- Bridge IC: CP2105;

4.2.8 ULPI interface

ULPI interface with ULPI PHY provide USB2.0 Connectivity. Supported USB mode – OTG.

- PHY IC: USB3320C-EZK – SMC, now Microchip
- Speed modes: USB 2.0 HS, USB 2.0 FS, USB 2.0 LS;
- Supported roles: OTG.

Connections between ULPI PHY interface and MPSoC are listed below:

XCZU7EV		Schematic Net Name	PHY IC	
Pin Name	Pin Number		Pin number	Pin name
PS_MIO56	G34	ULPI_DAT0	3	DATA0
PS_MIO57	H29	ULPI_DAT1	4	DATA1
PS_MIO54	G31	ULPI_DAT2	5	DATA2
PS_MIO59	H32	ULPI_DAT3	6	DATA3
PS_MIO60	H33	ULPI_DAT4	7	DATA4
PS_MIO61	H34	ULPI_DAT5	9	DATA5
PS_MIO62	J29	ULPI_DAT6	10	DATA6
PS_MIO63	J30	ULPI_DAT7	13	DATA7
PS_MIO58	H31	ULPI_STP	29	STP
PS_MIO55	G33	ULPI_NXT	2	NXT
PS_MIO53	G30	ULPI_DIR	31	DIR
PS_MIO52	G29	ULPI_CLK	1	CLKOUT
PS_MIO37	C33	ULPI_RST#	27	RESETB

Table 9- ULPI pinout

4.2.9 USB 3.0 Super Speed

Base for USB 3.0 port interface is built in MPSoC PS part GTR transceivers.

All lanes are ESD protected. Supported mode – HOST only. Signals routed to PCIe/104 connector.

4.2.10 Display Port

Display port provides connectivity to various monitors. Base for Display port interface is built in MPSoC PS part GTR transceivers. Also, there is an AUX channel for data path for sound and command transmission. All lanes are ESD protected.

- Connector Part number: 472720011 – Molex;
- Lane number and maximum speed: 1- Lane, 5.4 Gbps;
- Supported Resolution: up to UHD@30Hz;
- Audio: up to two channels, sample size up to 24bit, 48kHz sample rate;
- Level shifter for AUX: 74AVC4T245BQ;
- Differential transmitter IC for AUX: FIN1019MTCX.

Connections between Display port interface and connector are listed below:

XCZU7EV		Schematic Net Name	Display port connector	
Pin Name	Pin Number		Pin Number	Pin Name
PS_MGTRTXP3_505	N29	DP_CH0+	1	Lane_0p
PS_MGTRTXN3_505	N30	DP_CH0-	3	Lane_0n
PS_MIO27	A30	DP_DATAOUT	15 – AUXp 17 – AUXn 18 – Hot plug det	
PS_MIO28	A31	DP_HP_DETECT		
PS_MIO29	A32	DP_DAT_OE		
PS_MIO30	A33	DP_DAT_IN		

Table 10- Display port pinout

4.2.11 PCIe

Standard PCIe/104 has two stacking signals STK1 and STK2. This board acts as TYPE 2 host. User must do some action described below, while getting STACK ERROR condition. STACK ERROR condition when STK1# signal not equal "0", **OR** STK2# signal not equal "1". Actions to do:

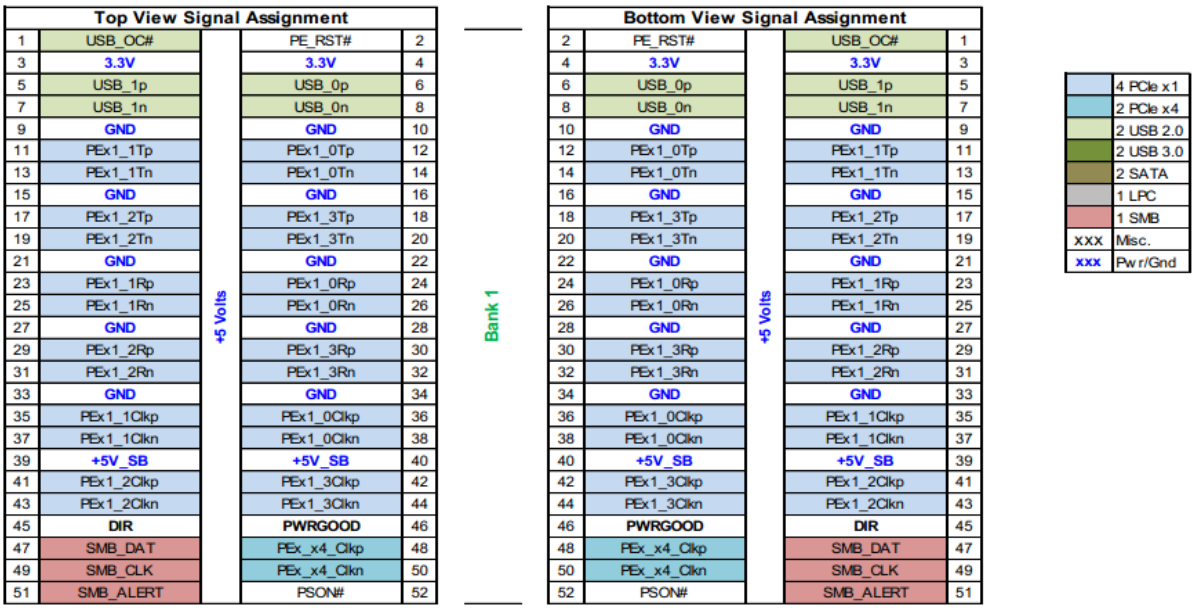
- PCIe104_CLK_EN signal must be driven Low;
- PCIe104_RST_1V2 signal(Bank 65) must be driven High;
- PCIe_SW_RST# signal must be driven Low;
- Stacking error led must be on(Bank 88).

HD Bank 88 dedicated to PCIe104 , PCIe and user controls:

XCZU7EV bank 88 VCC_3V3			Net Name	Description
Ball Name	**Ball Num**	**Direction MpSoC**		
L1P_AD15P_88	E1	In	PCIx1_SW_LNKST_0	Link status from Switch
L1N_AD15N_88	D1		PCIx1_SW_LNKST_1	
L2P_AD14P_88	C1		PCIx1_SW_LNKST_2	
L2N_AD14N_88	B1		PCIx1_SW_LNKST_3	
L3P_AD13P_88	A3		PCIx1_SW_LNKST_4	
L3N_AD13N_88	A2	Out	PCIe104 Stack Error LED. See **Error! Reference source not found.** chapter	
L4P_AD12P_88	E3	In	RGMII_INT	Interrupt signal from ETH PHY
L4N_AD12N_88	E2	Out	USB_RST#	USB PHY reset signal
L5P_GC_88	D2		RGMII_RST#	ETH PHY reset signal
L5N_GC_88	C2	-	-	-
L6P_GC_88	C3	Out	USER_LED1	User LED 1
L6N_GC_88	B3		USER_LED2	User LED 2
L7P_GC_88	C4		USER_LED3	User LED 3
L7N_GC_88	B4		USER_LED4	User LED 4
L8P_GC_88	E4	In	CLK_SYS+	Clock input, from SI5341 OUT1
L8N_GC_88	D4		CLK_SYS-	
L9P_AD11P_88	F5	-	-	-
L9N_AD11N_88	F4	-	-	-
L10P_AD10P_88	B5	In	STK1#	Inverted PCIe/104 stacking signals. See **Error! Reference source not found.** chapter
L10N_AD10N_88	A5		STK2#	
L11P_AD9P_88	D6	Out	PCIe_SW_I2CAD1	PCIe switch I2C address selection
L11N_AD9N_88	D5		PCIe_SW_I2CAD2	
L12P_AD8P_88	F6	Out	PCIe104_CLK_EN	PCIe x1 clocks enable
L12N_AD8N_88	E5		PCIe_SW_RST#	Reset PCIe switch

Table 11- PCIe pinout

Pinout for ASP-129646-03:



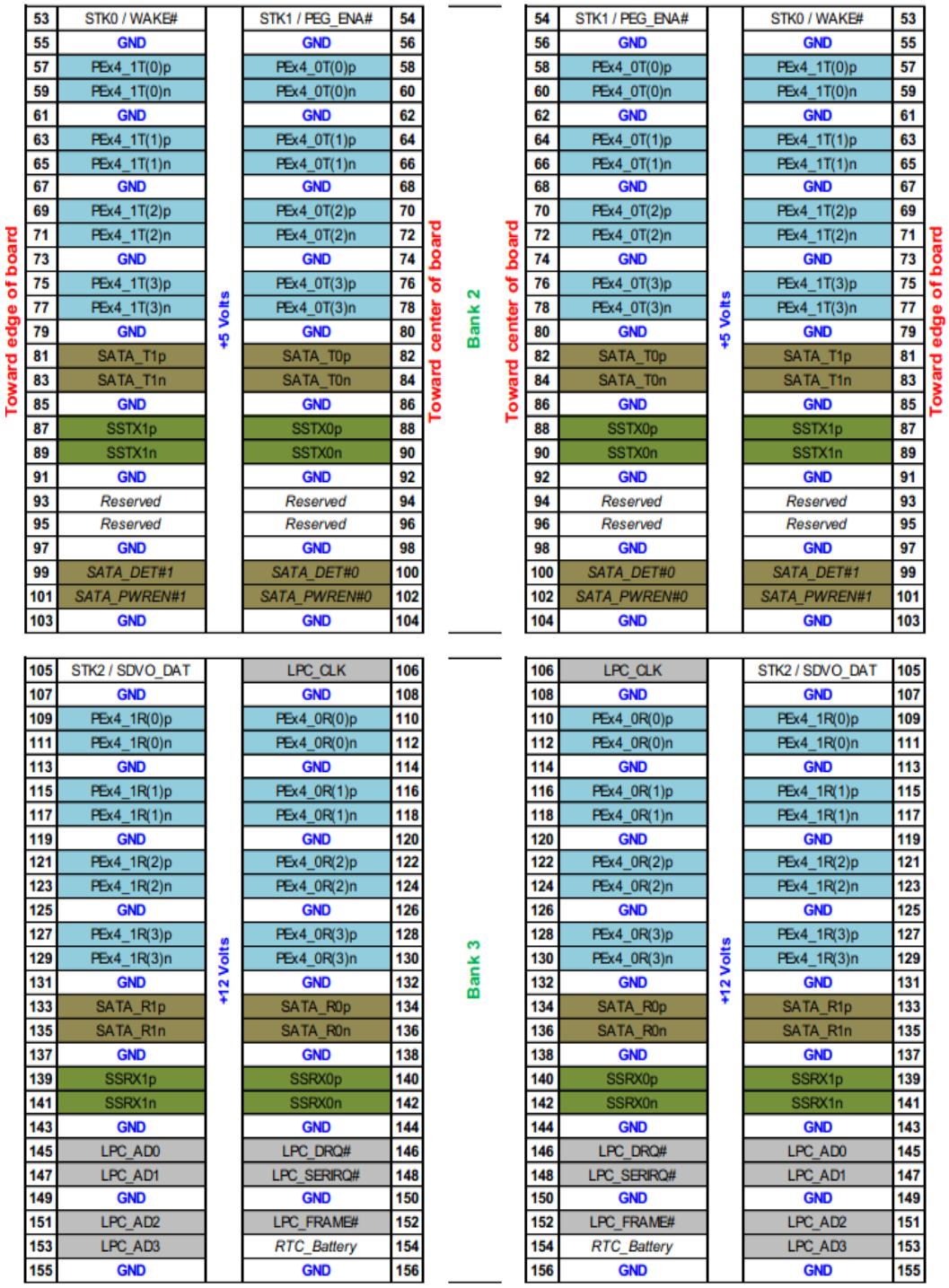


Figure 5- PCIe stack pinout

4.2.12 SATA

There is one SATA interface located on the board. Base for SATA interface is built in MPSoC PS part GTR transceivers. All SATA interfaces are ESD protected, from static discharge.

- Connector Part number: 678005001– Molex;
- Interface: SATA 3.0 Host, up to 6Gb/s;

- Supply voltage for hard drives: NO, there is AC coupling capacitors, SO no damage to device or chip.

Connections between SATA interface and connector are listed below.

XCZU7EV		Schematic Net Name	SATA connectors	
Pin Name	Pin Number		Pin Number	Pin Name
PS_MGTRTXP2_505	P31	SATA0_TX+	2	TXp_+
PS_MGTRTXN2_505	P32	SATA0_TX-	3	TXp_-
PS_MGTRRXP2_505	R33	SATA0_RX+	6	RXp_+
PS_MGTRRXN2_505	R34	SATA0_RX-	5	RXp_-

Table 12- SATA pinout

4.2.13 FMC

Banks 28, 67, 68, 64 are fully used for FMC interface only. VRP pin connected via 240 ohm resistor to ground:

XCZU7EV banks VCCIO - VADJ			Name	Goes to FMC
Ball Name	Ball Num	Direction MpSoC		
IO_L1P_N0_DBC_67	A17	Bidir	FMC_LA_09+	**Goes to FMC pins as named according vita 57.1**
IO_L1N_N1_DBC_67	A16		FMC_LA_09-	
IO_L2P_N2_67	B16		FMC_LA_04+	
IO_L2N_N3_67	B15		FMC_LA_04-	
IO_L3P_N4_67	A15	Bidir	FMC_LA_06+	**Goes to FMC pins as named according vita 57.1**
IO_L3N_N5_67	A14		FMC_LA_06-	
IO_L4P_N6_DBC_67	B14		FMC_LA_10+	
IO_L4N_N7_DBC_67	B13		FMC_LA_10-	
IO_L5P_N8_67	A13		FMC_LA_11+	
IO_L5N_N9_67	A12		FMC_LA_11-	
IO_L6P_N10_67	C13		NC	
IO_L6N_N11_67	C12		NC	
IO_L7P_N0_QBC_67	D16		FMC_LA_05+	
IO_L7N_N1_QBC_67	C16		FMC_LA_05-	
IO_L8P_N2_67	D17		FMC_LA_12+	
IO_L8N_N3_67	C17		FMC_LA_12-	
IO_L9P_N4_67	E18		FMC_LA_08+	
IO_L9N_N5_67	E17		FMC_LA_08-	
IO_L10P_QBC_67	G14		NC	
IO_L10N_QBC_67	F13		NC	
IO_L11P_N8_GC_67	D15		FMC_LA_01_CC+	
IO_L11N_N9_GC_67	D14		FMC_LA_01_CC-	
IO_L12P_N10_GC_67	E15	Input	FMC_CLK_0+	
IO_L12N_N11_GC_67	E14		FMC_CLK_0-	
IO_L13P_N0_GC_67	F17	Input	CLK_SYS2+	Clock input, from SI5341 OUT6
IO_L13N_N1_GC_67	F16		CLK_SYS2-	
IO_L14P_N2_GC_67	G15	Bidir	FMC_LA_00_CC+	**Goes to FMC pins as named according vita 57.1**
IO_L14N_N3_GC_67	F15		FMC_LA_00_CC-	

IO_L15P_N4_67	H19	Bidir	FMC_LA_13+	**Goes to FMC pins as named according vita 57.1**
IO_L15N_N5_67	G19		FMC_LA_13-	
IO_L16P_QBC_67	H18		FMC_LA_15+	
IO_L16N_QBC_67	H17		FMC_LA_15-	
IO_L17P_N8_67	G18		FMC_LA_07+	
IO_L17N_N9_67	F18		FMC_LA_07-	
IO_L18P_N10_67	H16		FMC_LA_03+	
IO_L18N_N11_67	G16		FMC_LA_03-	
IO_L19P_N0_DBC_67	L20		FMC_LA_14+	
IO_L19N_N1_DBC_67	K20		FMC_LA_14-	
IO_L20P_N2_67	J16	Bidir	FMC_LA_02+	**Goes to FMC pins as named according vita 57.1**
IO_L20N_N3_67	J15		FMC_LA_02-	
IO_L23P_N8_67	K19		FMC_LA_16+	
IO_L23N_N9_67	K18		FMC_LA_16-	
BANK 68				
IO_L1P_N0_DBC_68	M13	Bidir	FMC_LA_27+	**Goes to FMC pins as named according vita 57.1**
IO_L1N_N1_DBC_68	L13		FMC_LA_27-	
IO_L2P_N2_68	K10		FMC_LA_33+	
IO_L2N_N3_68	J10		FMC_LA_33-	
IO_L3P_N4_68	L12		FMC_LA_24+	
IO_L3N_N5_68	L11		FMC_LA_24-	
IO_L4P_N6_DBC_68	K12		FMC_LA_25+	
IO_L4N_N7_DBC_68	J11		FMC_LA_25-	
IO_L5P_N8_68	K14		FMC_LA_32+	
IO_L5N_N9_68	J14		FMC_LA_32-	
IO_L6P_N10_68	L14		NC	
IO_L6N_N11_68	K13		NC	
IO_L7P_N0_QBC_68	F7		FMC_LA_30+	
IO_L7N_N1_QBC_68	E7		FMC_LA_30-	
IO_L8P_N2_68	C9		FMC_LA_26+	
IO_L8N_N3_68	C8		FMC_LA_26-	
IO_L9P_N4_68	F8		FMC_LA_29+	
IO_L9N_N5_68	E8		FMC_LA_29-	
IO_L10P_QBC_68	E9	Bidir	FMC_LA_28+	**Goes to FMC pins as named according vita 57.1**
IO_L10N_QBC_68	D9		FMC_LA_28-	
IO_L11P_N8_GC_68	H9		FMC_LA_18_CC+	
IO_L11N_N9_GC_68	G9		FMC_LA_18_CC-	
IO_L12P_N10_GC_68	G10	Input	FMC_CLK1+	
IO_L12N_N11_GC_68	F10		FMC_CLK1-	
IO_L13P_N0_GC_68	H11	Bidir	FMC_LA_17_CC+	
IO_L13N_N1_GC_68	G11		FMC_LA_17_CC-	
IO_L14P_GC_68	F11		FMC_CLK3_BDIR+	
IO_L14N_GC_68	E10		FMC_CLK3_BDIR-	
IO_L15P_N4_68	H13		FMC_LA_21+	
IO_L15N_N5_68	H12		FMC_LA_21-	
IO_L16P_QBC_68	D11		FMC_CLK2_BDIR+	
IO_L16N_QBC_68	D10		FMC_CLK2_BDIR-	
IO_L19P_N0_DBC_68	C7		FMC_LA_31+	
IO_L19N_N1_DBC_68	C6		FMC_LA_31-	
IO_L20P_N2_68	B9		FMC_LA_22+	
IO_L20N_N3_68	B8		FMC_LA_22-	
IO_L21P_N4_68	B6		FMC_LA_19+	
IO_L21N_N5_68	A6		FMC_LA_19-	
IO_L22P_DBC_68	B10		FMC_LA_23+	
IO_L22N_DBC_68	A10		FMC_LA_23-	
IO_L23P_N8_68	A8		FMC_LA_20+	
IO_L23N_N9_68	A7		FMC_LA_20-	

BANK 28				
IO_L1P_N0_DBC_28	L21	Bidir	FMC_HA_05+	Goes to FMC pins as named according vita 57.1
IO_L1N_N1_DBC_28	L22		FMC_HA_05-	
IO_L2P_N2_28	L23		FMC_HA_23+	
IO_L2N_N3_28	K24		FMC_HA_23-	
IO_L3P_N4_28	J21		FMC_HA_04+	
IO_L3N_N5_28	J22		FMC_HA_04-	
IO_L4P_N6_DBC_28	K22		FMC_HA_22+	
IO_L4N_N7_DBC_28	K23		FMC_HA_22-	
IO_L5P_N8_28	J25	Bidir	FMC_HA_21+	Goes to FMC pins as named according vita 57.1
IO_L5N_N9_28	H26		FMC_HA_21-	
IO_L6P_N10_28	J24		FMC_HA_19+	
IO_L6N_N11_28	H24		FMC_HA_19-	
IO_L7P_N0_QBC_28	E19		FMC_HA_09+	
IO_L7N_N1_QBC_28	D19		FMC_HA_09-	
IO_L8P_N2_28	H21		FMC_HA_13+	
IO_L8N_N3_28	H22		FMC_HA_13-	
IO_L9P_N4_28	D20		FMC_HA_03+	
IO_L9N_N5_28	D21		FMC_HA_03-	
IO_L10P_QBC_28	G20		FMC_HA_10+	
IO_L10N_QBC_28	F20		FMC_HA_10-	
IO_L11P_N8_GC_28	F22		FMC_HA_01_CC+	
IO_L11N_N9_GC_28	E22		FMC_HA_01_CC-	
IO_L12P_N10_GC_28	G21		FMC_HA_00_CC+	
IO_L12N_N11_GC_28	F21		FMC_HA_00_CC-	
IO_L13P_N0_GC_28	F23		FMC_HA_18_CC+	
IO_L13N_N1_GC_28	E23		FMC_HA_18_CC-	
IO_L14P_N2_GC_28	G23		FMC_HA_17_CC+	
IO_L14N_N3_GC_28	G24		FMC_HA_17_CC-	
IO_L15P_N4_28	C21		FMC_HA_11+	
IO_L15N_N5_28	C22		FMC_HA_11-	
IO_L16P_QBC_28	E24		FMC_HA_14+	
IO_L16N_QBC_28	D24		FMC_HA_14-	
IO_L17P_N8_28	D22		FMC_HA_15+	
IO_L17N_N9_28	C23		FMC_HA_15-	
IO_L18P_N10_28	G25	Bidir	FMC_HA_20+	Goes to FMC pins as named according vita 57.1
IO_L18N_N11_28	G26		FMC_HA_20-	
IO_L19P_N0_DBC_28	A18		FMC_HA_07+	
IO_L19N_N1_DBC_28	A19		FMC_HA_07-	
IO_L20P_N2_28	C18		FMC_HA_02+	
IO_L20N_N3_28	C19		FMC_HA_02-	
IO_L21P_N4_28	A20		FMC_HA_12+	
IO_L21N_N5_28	A21		FMC_HA_12-	
IO_L22P_N6_DBC_28	B18		FMC_HA_08+	
IO_L22N_N7_DBC_28	B19		FMC_HA_08-	
IO_L23P_N8_28	A22		FMC_HA_16+	
IO_L23N_N9_28	A23		FMC_HA_16-	
IO_L24P_N10_28	B20		FMC_HA_06+	
IO_L24N_N11_28	B21		FMC_HA_06-	
BANK 64 VCCIO IS VIO_B_M2C				
IO_L3P_64	AM18	Bidir	FMC_HB_18+	Goes to FMC pins as named according vita 57.1
IO_L3N_64	AN18		FMC_HB_18-	
IO_L4P_64	AM14		FMC_HB_05+	
IO_L4N_64	AN14		FMC_HB_05-	
IO_L5P_64	AP16		FMC_HB_03+	
IO_L5N_64	AP15		FMC_HB_03-	
IO_L6P_64	AN17		FMC_HB_02+	

IO_L6N_64	AN16		FMC_HB_02-	
IO_L7P_64	AM16		FMC_HB_01+	
IO_L7N_64	AM15		FMC_HB_01-	
IO_L8P_64	AL16		FMC_HB_04+	
IO_L8N_64	AL15		FMC_HB_04-	
IO_L9P_64	AK18		FMC_HB_21+	
IO_L9N_64	AL18		FMC_HB_21-	
IO_L10P_64	AK15	Bidir	FMC_HB_20+	**Goes to FMC pins as named according vita 57.1**
IO_L10N_64	AK14		FMC_HB_20-	
IO_L11P_GC_64	AJ17		FMC_HB_14+	
IO_L11N_GC_64	AK17		FMC_HB_14-	
IO_L12P_GC_64	AJ16		FMC_HB_17_CC+	
IO_L12N_GC_64	AJ15		FMC_HB_17_CC-	
IO_L13P_GC_64	AH18		FMC_HB_00_CC+	
IO_L13N_GC_64	AH17		FMC_HB_00_CC-	
IO_L14P_GC_64	AF18		FMC_HB_06_CC+	
IO_L14N_GC_64	AG18		FMC_HB_06_CC-	
IO_L15P_64	AE17		FMC_HB_15+	
IO_L15N_64	AF17		FMC_HB_15-	
IO_L16P_64	AH14		FMC_HB_19+	
IO_L16N_64	AJ14		FMC_HB_19-	
IO_L17P_64	AF16		FMC_HB_16+	
IO_L17N_64	AF15		FMC_HB_16-	
IO_L18P_64	AG15		FMC_HB_11+	
IO_L18N_64	AG14		FMC_HB_11-	
IO_L19P_64	AD15		FMC_HB_10+	
IO_L19N_64	AE15		FMC_HB_10-	
IO_L20P_64	AC17		FMC_HB_09+	
IO_L20N_64	AC16		FMC_HB_09-	
IO_L21P_64	AB16		FMC_HB_12+	
IO_L21N_64	AB15		FMC_HB_12-	
IO_L22P_64	AA16		FMC_HB_13+	
IO_L22N_64	AA15		FMC_HB_13-	
IO_L23P_64	AA14		FMC_HB_08+	
IO_L23N_64	AB14		FMC_HB_08-	
IO_L24P_64	AD17		FMC_HB_07+	
IO_L24N_64	AD16		FMC_HB_07-	

Table 13- FMC Interface pinout

4.2.14 I2C Interface

There are two I2C interfaces on the board. I2C interface belong to PS part of MPSoC. For connected device listing and their addresses see **Error! Reference source not found. Error! Reference source not found.**.

- Modes: Master and slave
- Addressing: 7-bit, 10 bit in master mode only

Connections between I2C interfaces and MPSoC are listed below:

XCZU7EV		Schematic Net Name
Pin Name	Pin Number	
PS_MIO34	B34	SCL_3V3

PS_MIO35	C31	SDA_3V3
PS_MIO24	E28	SCL_1V8
PS_MIO25	D29	SDA_1V8

Table 14- I2C pinout

4.2.15 Fan connector

A fan connector is available on-board.

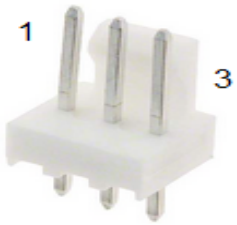


Figure 6- Fan connector

1. Tacho signal from FAN Yellow wire of FAN,
2. 12V, red wire of FAN
3. Ground, Black wire of FAN

5 Footprint

5.1 Top View

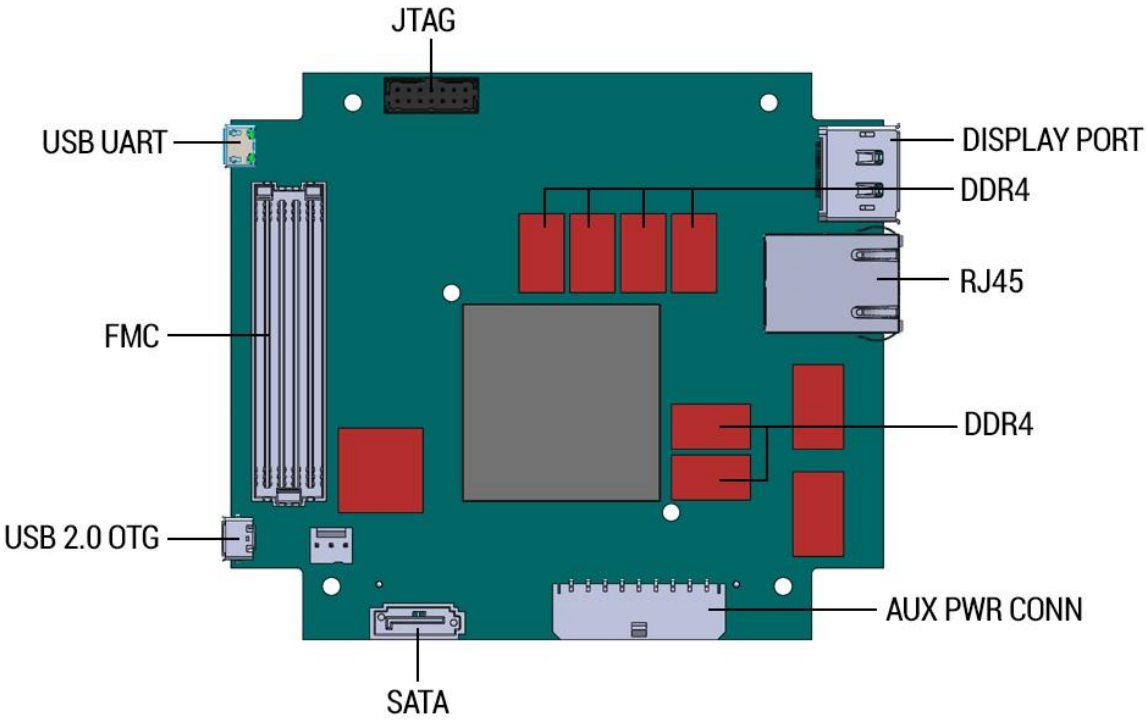


Figure 7- PCIE104Z top view

5.2 Bottom View

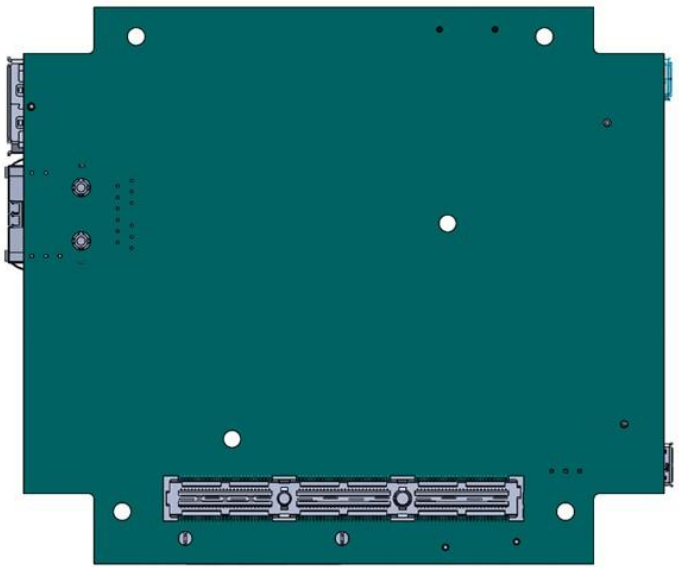


Figure 8- PCIE104Z bottom view

6 Physical Properties

Dimensions		
Weight		
Supply Voltages		
Supply Current	+12V	
	+5V	
MTBF		

7 Safety

This module presents no hazard to the user when in normal use.

8 EMC

This module is designed to operate from within an enclosed host system, which is build to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system.

This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the output cables.

Short circuiting any output to ground does not cause the host PC system to lock up or reboot.