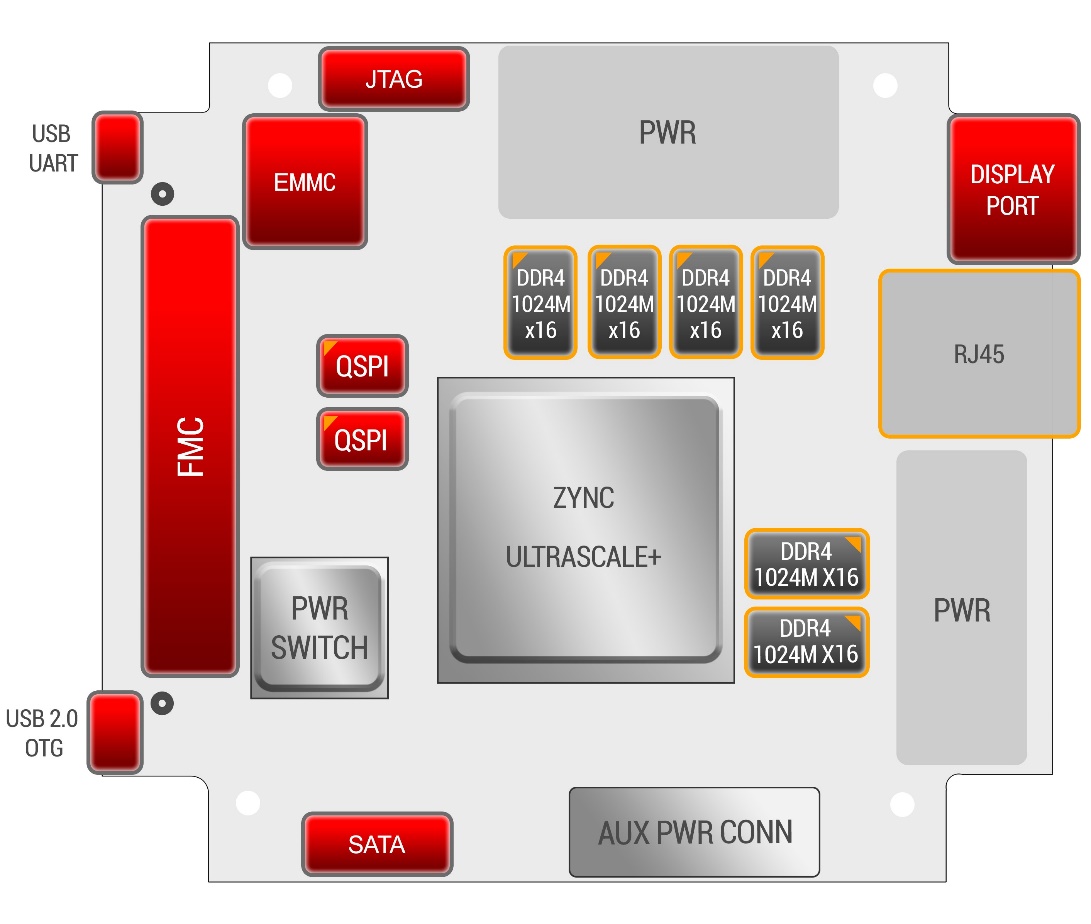
|  |  |
| --- | --- |
| **Unit / Module Description:** | ZU+ based, PC/104 form factor, FMC carrier board |
| **Unit / Module Number:** | PCIe104Z |
| **Document Issue Number:** | 1.1 |
| **Issue Date:** | 04/05/19 |
| **Original Author:** | Timoteo Garcia |

**Product Specification  
for**

**PCIe104Z**

|  |  |
| --- | --- |
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**Revision History**

|  |  |  |  |
| --- | --- | --- | --- |
| **Issue** | **Changes Made** | **Date** | **Initials** |
| 1.0 | First draft | 15/04/19 | TG |
| 1.1 | Updated diagram | 04/05/19 | TG |
|  |  |  |  |

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# Introduction

This document describes the hardware specifications of the PCIe104Z card. This board is a carrier based on [Zynq Ultrascale+ MPSoC](https://www.xilinx.com/products/silicon-devices/soc/zynq-ultrascale-mpsoc.html) architecture from [Xilinx](https://www.xilinx.com/), with [PC/104](https://pc104.org/) form factor, for [scalable solutions](https://www.sundance.technology/som-cariers/pc104-boards/), and in compliance with [FMC](https://www.vita.com/fmc) standards, to amplify the connectivity with FMC-compatible daughter cards.

# Main features

PCIe104Z’s main processing device is a Xilinx Zynq Ultrascale+ MPSoC. The user can order any of the following: XCZU7EV, XCZU7EG, XCZU11EG, XCZU7CG (C1156 package), essentially offering:

* Processor: Dual-coreARM® Cortex™-A53 MPCore™ up to 1.3GHz (XCZU7CG), or Quad-coreARM® Cortex™-A53 MPCore™ up to 1.5GHz (XCZU7EV, XCZU7EG, XCZU11EG)
* Real-Time processor: Dual-coreARM Cortex-R5 MPCoreup to 533MHz (XCZU7CG) and up to 600MHz (XCZU7EV, XCZU7EG, XCZU11EG)
* GPU Mali™-400 MP2 up to 667MHz (XCZU7EV, XCZU7EG, XCZU11EG only)
* Video codec H.265/H.264 in the Programmable Logic (XCZU7EV only)

Through different characteristics of the PS/PL, the ZU+ device, along with the peripherals of PCIe104Z, these are the main features of the board:

* Scalable through PCIe.
  + PCIe Switch PEX8606 to stack up 4 cards
  + 4x PCIe Gen2 in the Processing System
  + Gen3x16/Gen4x8 in the Programmable Logic
* Expandable through FMC
  + Direct access to FMC cards through the PL, 10xGTH  at 16.3Gb/s transceivers and 80 LVDS IO pairs
* External DDR4 memory, 8GB (PS), 4GB (PL)
* Configuration/booting
  + Flash memory for QSPI boot
  + eMMC flash (8GB)
  + JTAG interface for programmability/debug
* 4x Tri-mode Gigabit Ethernet through RJ45 connector
* Display 1.2 port/connector
* 1x Micro-USB 2.0 connector with OTG
* 1x USB 3.0 interface via (PCIe connector)
* 1x SATA 3.0
* USB-UART

Documentation of the Xilinx [device family](https://www.xilinx.com/support/documentation/selection-guides/zynq-ultrascale-plus-product-selection-guide.pdf) provide more information regarding specific details of the architecture for the different parts.

For a deep understanding of the interfaces, refer to the [technical reference manual (UG1085)](https://www.xilinx.com/support/documentation/user_guides/ug1085-zynq-ultrascale-trm.pdf)

# Acronyms, Abbreviations and Definitions

## Acronyms and Abbreviations

MPSoC Multi-Processor System-On-Chip

GPU Graphics Processing Unit

IP Intellectual Property

JTAG Joint Test Action Group

QSPI Quad Serial Peripheral Interface

eMMC Embedded Multimedia Card

DDR Double Data Rate

I2C Inter-Integrated Circuit

RGMII Reduced Gigabit Media Independent Interface

IC Integrated Circuit

PCIe Peripheral Component Interconnect Express

USB Universal Serial Bus

SATA Serial AT Attachment

UART Universal Asynchronous Receiver/Transmitter

FMC FPGA Mezzanine Card

ULPI Utmi+ Low Pin Interface

# Functional Description

## Block Diagram

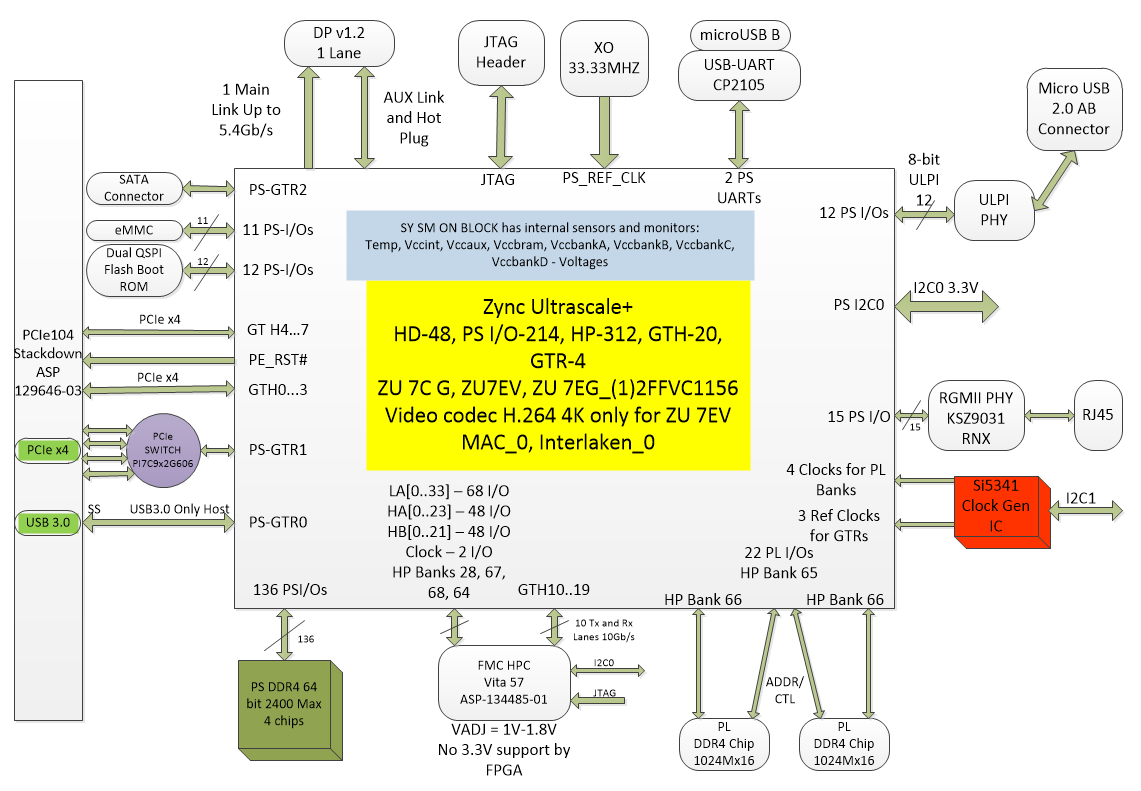


Figure - PCIE104Z diagram

## Module Description

### Xilinx Zynq Ultrascale+ device

The main processing device is a Xilinx Zynq Ultrascale+ MPSoC. The user can order any of the following: XCZU7EV, XCZU7EG, XCZU11EG, XCZU7CG (C1156 package).

The Zynq Ultrascale+ architecture responds to a well defined structure divided in two main parts, called Processing System and Programmable Logic. Depending on the device chosen by the user (CG, EG or EV), some features in the PS/PL differ. In Figures 2, 3 and 4, the architectures for CG, EG and EV are shown:

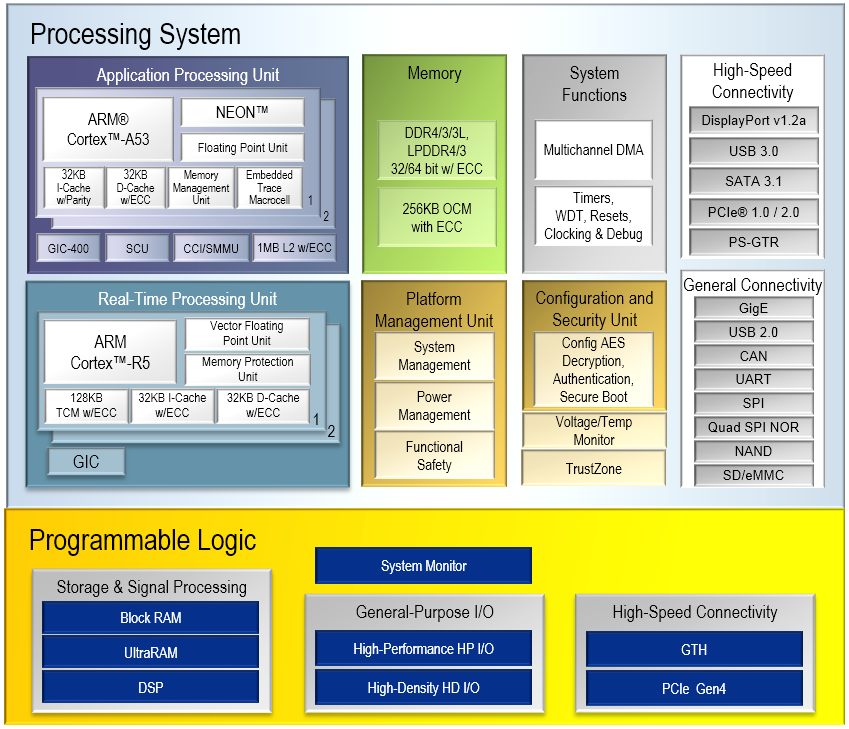


Figure - PCIE104Z with ZU+ (CG)

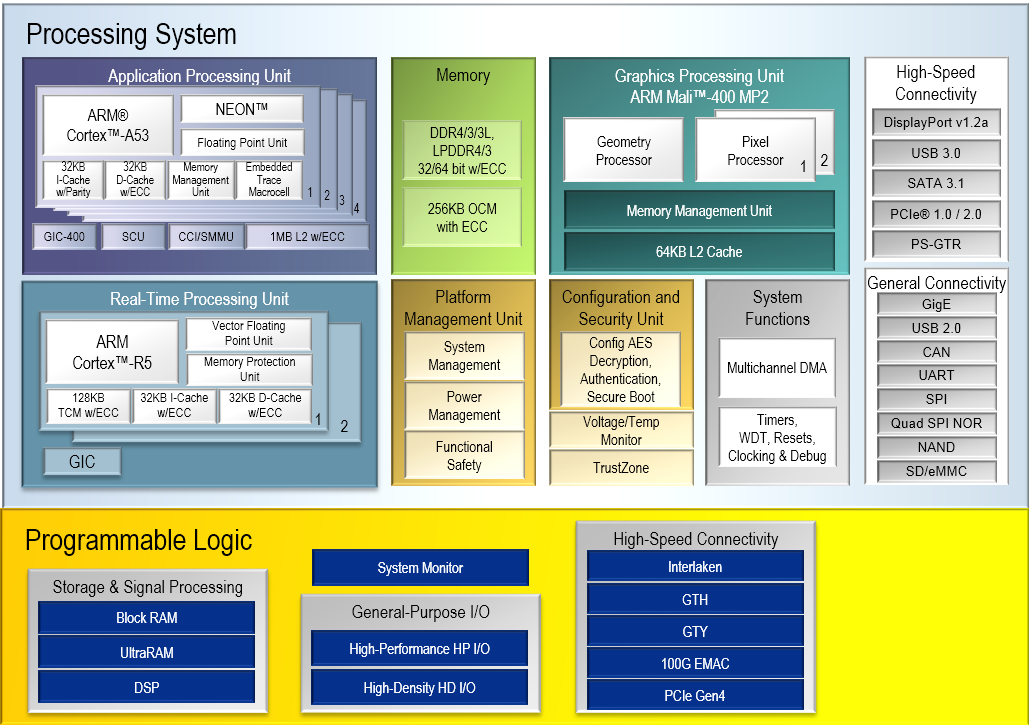


Figure - PCIE104Z with ZU+ (EG)

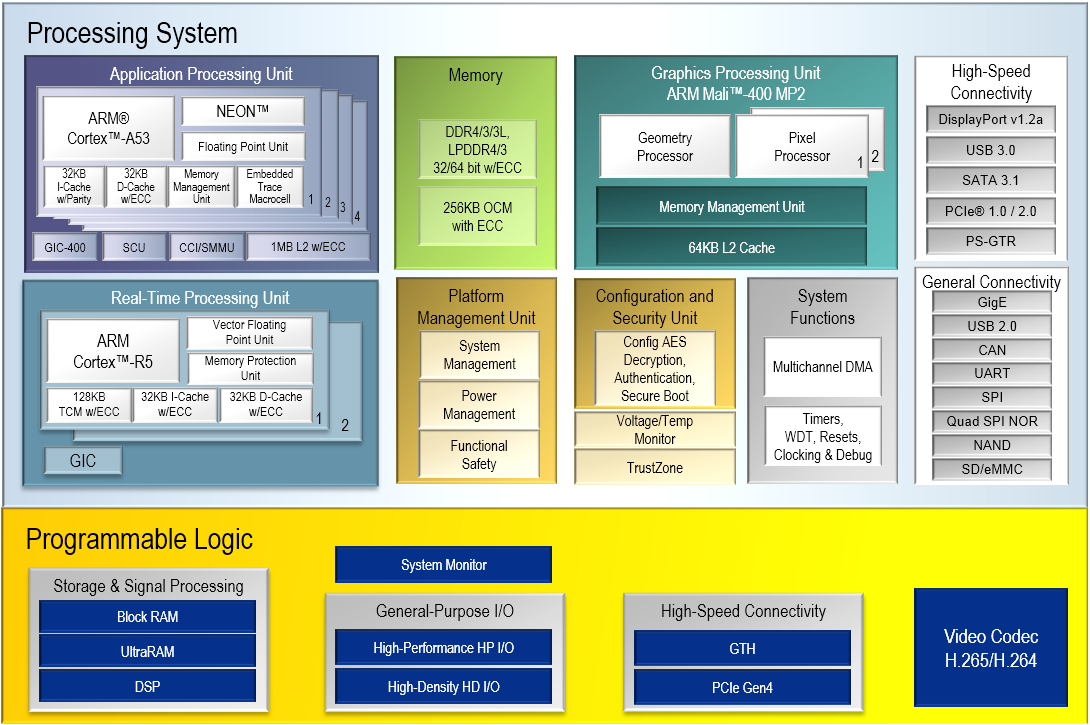


Figure - PCIE104Z with ZU+ (EV)

The essential difference relies on the Dual/Quad core structure in the Application Processing Unit, and the presence of GPU in the PS. On the other hand, the presence of transceivers and a built-in video codec in the PL as part of the embedded primitives.

Xilinx offers full documentation of the different controllers within the PS, including drivers and support for both standalone and OS-based applications. Also, the majority of IPs available in Xilinx tools for the PL implementation are license-free, and fully documented.

### Power

The power is supplied at 12V and 5V through PC/104 or alternatively from an external connector.

On board power supply provides all the necessary voltages for the modules.

Built-in SYSMON module in FPGA provide temperature and on chip voltage monitoring. All necessary connections are made inside the device.

**NOTE! User must check their design in Xilinx power estimation spreadsheet and make sure that the MPSOC device consumes less than 50Amps by VCORE, otherwise design may work but with instability or lead to board damage.**

Other board components’ average consumption equals approximately 40W (including USB ports).

VADJ voltage selected with logic levels at nets VADJ\_V(2:0), levels must be changed when EN\_VADJ is 0. After selecting required level EN\_VADJ must be set to logic 1

|  |  |  |  |
| --- | --- | --- | --- |
| **Voltage** | **VADJ\_V2** | **VADJ\_V1** | **VADJ\_V0** |
| **1.0 Default** | 0 | 0 | 0 |
| **1.2** | 0 | 0 | 1 |
| **1.25** | 0 | 1 | 0 |
| **1.35** | 1 | 0 | 0 |
| **1.45** | 0 | 1 | 1 |
| **1.55** | 1 | 0 | 1 |
| **1.6** | 1 | 1 | 0 |
| **1.8** | 1 | 1 | 1 |

Table - VADJ

### Configuration and booting process

The Zynq Ultrascale+ device can be configured/booted in different ways. The following table summarises the boot modes:

Boot mode selected through SW1 DIP switch.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Boot Mode** | **SW1.1** | **SW1.2** | **SW1.3** | **SW1.4** |
| **JTAG** | ON | ON | ON | ON |
| **QSPI24 mode (default)** | OFF | ON | ON | ON |
| **QSPI32 mode** | ON | OFF | ON | ON |
| **eMMC boot** | ON | OFF | OFF | ON |
| Others unsupported | | | | |

Table - SW1 Boot configuration

* JTAG

Reference designator of connector is X1, located on page 2 of schematic. All signals, except VREF\_3V3, are ESD and short-circuit protected.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| GND | 1 |  | 2 | VREF\_3V3 |
| NC | 3 |  | 4 | JTAG\_TMS |
| GND | 5 |  | 6 | JTAG\_TCK |
| GND | 7 |  | 8 | JTAG\_TDO (O) |
| GND | 9 |  | 10 | JTAG\_TDI (I) |
| GND | 11 |  | 12 | JTAG\_TRST# |
| GND | 13 |  | 14 | SRST# |

Table - JTAG pinout

* QSPI Flash

The Quad-SPI flash memory located at D16 and D17 provides 2 x 512 Mb of non-volatile storage that can be used for configuration and data storage.

* Part number: MT25QU512ABB8E12 – Micron
* Supply voltage: 1.8V
* Data path width: 4 bit
* Maximum clock: 108 MHz
* Package: BGA-24

Connections between SPI flashes and MPSoC are listed below:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **XCZU7EV** | | **Schematic Net Name** | **QSPI Device** | |
| **Pin Name** | **Pin Number** | **Pin Number** | **Pin Name** |
| PS\_MIO4 | A25 | SPI0\_DQ0 | D3 | DQ0/DIN |
| PS\_MIO1 | C24 | SPI0\_DQ1 | D2 | DQ1/DOUT |
| PS\_MIO2 | B24 | SPI0\_DQ2 | C4 | W#/Vpp/DQ2 |
| PS\_MIO3 | E25 | SPI0\_DQ3 | D4 | DQ3/HOLD# |
| PS\_MIO0 | A24 | SPI0\_CLK | B2 | C |
| PS\_MIO5 | D25 | SPI0\_CS# | C2 | S# |
| PS\_MIO8 | D26 | SPI1\_DQ0 | D3 | DQ0/DIN |
| PS\_MIO9 | C26 | SPI1\_DQ1 | D2 | DQ1/DOUT |
| PS\_MIO10 | F26 | SPI1\_DQ2 | C4 | W#/Vpp/DQ2 |
| PS\_MIO11 | B26 | SPI1\_DQ3 | D4 | DQ3/HOLD# |
| PS\_MIO12 | C27 | SPI1\_CLK | B2 | C |
| PS\_MIO7 | B25 | SPI1\_CS# | C2 | S# |

Table - QSPI pinout

* eMMC interface

The SDIO interface connected to eMMC 8GByte chip, also this interface provides boot capability.

* IC part number: KLM8G1GEAC-B031;
* Supply voltage: 3.3V;
* I/O voltage: 1.8V
* Data path width: 8 bit;

Connections between SDIO interface and chip are listed below:

|  |  |  |
| --- | --- | --- |
| **XCZU7EV** | | **Schematic Net Name** |
| **Pin Name** | **Pin Number** |
| PS\_MIO13 | D27 | MIO\_MMC\_D0 |
| PS\_MIO14 | A27 | MIO\_MMC\_D1 |
| PS\_MIO15 | E27 | MIO\_MMC\_D2 |
| PS\_MIO16 | A28 | MIO\_MMC\_D3 |
| PS\_MIO17 | C29 | MIO\_MMC\_D4 |
| PS\_MIO18 | F27 | MIO\_MMC\_D5 |
| PS\_MIO19 | B28 | MIO\_MMC\_D6 |
| PS\_MIO20 | E29 | MIO\_MMC\_D7 |
| PS\_MIO21 | C28 | MIO\_MMC\_CMD |
| PS\_MIO22 | F28 | MIO\_MMC\_CLK |
| PS\_MIO23 | B29 | MIO\_MMC\_RST# |

Table - eMMC pinout

### Memory

External DDR4 memory is available for the PS to manage, which stores up to 8GB of data, distributed in four chips of 2400MT/s.

There are 4GB of external DDR4 memory accessible from the PL to additional data storage.

HP Banks 65, 66 used for DDR4 interface. VRP pin connected via 240ohms resistor to ground.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **XCZU7EV banks 65,66 VCCIO 1.2V** | | | **Name and description** | |
| **Ball Name** | **Ball Num** | **Direction MpSoC** |
| IO\_L1P\_N0\_65 | AP19 | Out | PL\_DDR\_CKE | |
| IO\_L1N\_N1\_65 | AP20 | PL\_DDR\_BG0 | |
| IO\_L2P\_N2\_65 | AM19 | DDR4 ODT signal | |
| IO\_L2N\_N3\_65 | AN19 | PL\_DDR\_WE#(DDR\_A14) | |
| IO\_L3P\_N4\_65 | AP21 | PL\_DDR\_A6 | |
| IO\_L3N\_N5\_65 | AP22 | PL\_DDR\_A11 | |
| IO\_L4P\_N6\_65 | AM21 | PL\_DDR\_A0 | |
| IO\_L4N\_N7\_65 | AN21 | PL\_DDR\_BA0 | |
| IO\_L5P\_N8\_65 | AN22 | PL\_DDR\_A2 | |
| IO\_L5N\_N9\_65 | AP23 | PL\_DDR\_A8 | |
| IO\_L6P\_N10\_65 | AM23 | DDR PARITY Signal | |
| IO\_L6N\_N11\_65 | AN23 | DDR RESET# | |
| IO\_L7P\_N0\_65 | AL20 | PL\_DDR\_ACT# | |
| IO\_L7N\_N1\_65 | AL21 | PL\_DDR\_CAS#(DDR\_A15) | |
| IO\_L8P\_N2\_65 | AL22 | PL\_DDR\_A1 | |
| IO\_L8N\_N3\_65 | AL23 | PL\_DDR\_A4 | |
| IO\_L9P\_N4\_65 | AJ19 | PL\_DDR\_A12 | |
| IO\_L9N\_N5\_65 | AK19 | PL\_DDR\_CS# | |
| IO\_L10P\_QBC\_65 | AK22 | PL\_DDR\_BA1 | |
| IO\_L10N\_QBC\_65 | AK23 | PL\_DDR\_A10 | |
| IO\_L11P\_N8\_65 | AJ20 | In/Out | DDR4 ALERT# in to MpSoC in normal mode, out in test mode | |
| IO\_L11N\_N9\_65 | AK20 | Out | PL\_DDR\_A3 | |
| IO\_L12P\_GC\_65 | AJ21 | In | System 300MHz clock input for core, from SI5341 OUT0 | |
| IO\_L12N\_GC\_65 | AJ22 |
| IO\_T1U\_N12\_65 | AH19 | Out | PL\_DDR\_BG1 | |
| IO\_L13P\_N0\_65 | AH22 | In/Out | PL\_DDR\_A9 | |
| IO\_L13N\_N1\_65 | AH23 | Out | PL\_DDR\_A13 | |
| IO\_L14P\_N0\_65 | AG21 | PL\_DDR\_A5 | |
| IO\_L14N\_N1\_65 | AH21 | PL\_DDR\_A7 | |
| IO\_L15P\_N4\_65 | AG19 | PL\_DDR\_RAS#(DDR\_A16) | |
| IO\_L15N\_N5\_65 | AG20 | PL\_DDR\_TEN test enable, Low for normal operation | |
| IO\_L16P\_N6\_65 | AF23 | DDR4 clock for chips | |
| IO\_L16N\_N7\_65 | AG23 |
| IO\_L24N\_PERSTN0 | AA20 | PCIE RESET – reset for PCIe EP | |
| **BANK 66 DEDICATED TO DATA BUS**  **DATA BYTE 0** | | | | |
| IO\_L1P\_N0\_66 | AN12 | BiDir. | PL\_DDR\_DM0 | Chip 1 DML |
| IO\_L2P\_N2\_66 | AP10 | PL\_DDR\_D3 | Chip 1 DQ3 |
| IO\_L2N\_N3\_66 | AP9 | PL\_DDR\_D1 | Chip 1 DQ1 |
| IO\_L3P\_N4\_66 | AN11 | PL\_DDR\_D5 | Chip 1 DQ5 |
| IO\_L3N\_N5\_66 | AP11 | PL\_DDR\_D7 | Chip 1 DQ7 |
| IO\_L4P\_N6\_DBC\_66 | AN9 | PL\_DDR\_DQS0+ | Chip 1 DQS\_L+ |
| IO\_L4N\_N7\_DBC\_66 | AN8 | PL\_DDR\_DQS0- | Chip 1 DQS\_L- |
| IO\_L5P\_N8\_66 | AM11 | PL\_DDR\_D2 | Chip 1 DQ2 |
| IO\_L5N\_N9\_66 | AM10 | PL\_DDR\_D0 | Chip 1 DQ0 |
| IO\_L6P\_N10\_66 | AM9 | PL\_DDR\_D4 | Chip 1 DQ4 |
| IO\_L6N\_N11\_66 | AM8 | PL\_DDR\_D6 | Chip 1 DQ6 |
| **DATA BYTE 1** | | | | |
| IO\_L7P\_N0\_66 | AK13 | BiDir. | PL\_DDR\_DM1 | Chip 1 DMU |
| IO\_L8P\_N2\_66 | AL11 | PL\_DDR\_D15 | Chip 1 DQ15 |
| IO\_L8N\_N3\_66 | AL10 | PL\_DDR\_D9 | Chip 1 DQ9 |
| IO\_L9P\_N4\_66 | AK12 | PL\_DDR\_D13 | Chip 1 DQ13 |
| IO\_L9N\_N5\_66 | AL12 | PL\_DDR\_D14 | Chip 1 DQ14 |
| IO\_L10P\_DBC\_66 | AK8 | PL\_DDR\_DQS1+ | Chip 1 DQS\_U+ |
| IO\_L10N\_DBC\_66 | AL8 | PL\_DDR\_DQS1- | Chip 1 DQS\_U- |
| IO\_L11P\_N8\_66 | AJ10 | PL\_DDR\_D12 | Chip 1 DQ12 |
| IO\_L11N\_N9\_66 | AK10 | PL\_DDR\_D11 | Chip 1 DQ11 |
| IO\_L12P\_N10\_66 | AJ9 | PL\_DDR\_D10 | Chip 1 DQ10 |
| IO\_L12N\_N11\_66 | AK9 | PL\_DDR\_D8 | Chip 1 DQ8 |
| **DATA BYTE 2** | | | | |
| IO\_L13P\_N0\_66 | AH12 | BiDir | PL\_DDR\_DM2 | Chip 2 DML |
| IO\_L14P\_N2\_66 | AH11 | PL\_DDR\_D16 | Chip 2 DQ0 |
| IO\_L14N\_N3\_66 | AJ11 | PL\_DDR\_D18 | Chip 2 DQ2 |
| IO\_L15P\_N4\_66 | AG13 | PL\_DDR\_D19 | Chip 2 DQ3 |
| IO\_L15N\_N5\_66 | AH13 | PL\_DDR\_D23 | Chip 2 DQ7 |
| IO\_L16P\_DBC\_66 | AG9 | PL\_DDR\_DQS2+ | Chip 2 DQS\_L+ |
| IO\_L16N\_DBC\_66 | AH9 | PL\_DDR\_DQS2- | Chip 2 DQS\_L- |
| IO\_L17P\_N8\_66 | AG11 | PL\_DDR\_D17 | Chip 2 DQ1 |
| IO\_L17N\_N9\_66 | AG10 | PL\_DDR\_D21 | Chip 2 DQ5 |
| IO\_L18P\_N10\_66 | AF8 | PL\_DDR\_D20 | Chip 2 DQ4 |
| IO\_L18N\_N11\_66 | AG8 | PL\_DDR\_D22 | Chip 2 DQ6 |
| **DATA BYTE 3** | | | | |
| IO\_L19P\_N0\_66 | AF11 | BiDir | PL\_DDR\_DM3 | Chip 2 DMU |
| IO\_L19N\_66 | AF10 | In | PG\_1V2 | Power GOOD signal |
| IO\_L20P\_N2\_66 | AD14 | BiDir | PL\_DDR\_D25 | Chip 2 DQ9 |
| IO\_L20N\_N3\_66 | AE14 | PL\_DDR\_D31 | Chip 2 DQ15 |
| IO\_L21P\_N4\_66 | AE13 | PL\_DDR\_D24 | Chip 2 DQ8 |
| IO\_L21N\_N5\_66 | AF13 | BiDir | PL\_DDR\_D26 | Chip 2 DQ10 |
| IO\_L22P\_DBC\_66 | AC12 | PL\_DDR\_DQS3+ | Chip 2 DQS\_U+ |
| IO\_L22N\_DBC\_66 | AD12 | PL\_DDR\_DQS3- | Chip 2 DQS\_U- |
| IO\_L23P\_N8\_66 | AE12 | PL\_DDR\_D30 | Chip 2 DQ14 |
| IO\_L23N\_N9\_66 | AF12 | PL\_DDR\_D28 | Chip 2 DQ12 |
| IO\_L24P\_N10\_66 | AB13 | PL\_DDR\_D27 | Chip 2 DQ11 |
| IO\_L24N\_N11\_66 | AC13 | PL\_DDR\_D29 | Chip 2 DQ13 |

Table - DDR Memory pinout

Refer to Xilinx documentation for the implementation of a memory controller in the Programmable Logic.

### Clock synthesiser

A clock synthesiser is present on the board, [Si5341](https://www.silabs.com/documents/public/data-sheets/Si5341-40-D-DataSheet.pdf), which provides up to 10 output clocks, with a frequency range of 100MHz to 1028MHz (differential) or 250MHz (single-ended).

In order to configure the clock synth, a software tool, [ClockBuilder Pro](https://www.silabs.com/products/development-tools/software/clockbuilder-pro-software) can be used to generate the register values, which can be given to the chip through serial interface.

For main and primary clocks SI5341A-B-GM is used it is 10 channel, multi frequency low jitter generator IC, configurable via I2C (address 0x74). It consists of 5 independent fractional dividers and 10 independent integer dividers for each output. This provides capability of 0.001ppb frequency tuning. This IC must be programmed with correct values after board start-up via I2C, or this part can be programmed by factory, using customer values.

During start-up on board oscillator provides 33.333MHz clock to PS part of MPSoC, after booting there is an I2C1 interface, which must be used for interfacing with SI5341A.

Reference clock frequencies for various interfaces

|  |  |
| --- | --- |
| **Interface** | **Required Clock** |
| DDR4 banks | 300 MHz |
| USB Super Speed | 100 MHz |
| SATA | 150 MHz |
| Display port | 135 MHz |

Table - Clock configuration

### Ethernet

RGMII interface with PHY provide 10/100/1000BASE-T Connectivity via RJ45 connector.

* PHY IC: KSZ9031RNXIC – Micrel;
* Speed modes: 10/100/1000BASE;
* Link capabilities: Auto MDI/MDI-X, Cable diagnostics.

Connections between RGMII PHY interface and MPSoC are listed below:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **XCZU7EV** | | **Schematic Net Name** | **PHY IC** | |
| **Pin Name** | **Pin Number** | **Pin number** | **Pin name** |
| PS\_MIO[65:68] | J32,J34,K28,K29 | RGMII\_TX\_D[0:3] | 19 - 22 | TXD[0:3] |
| PS\_MIO69 | K30 | RGMII\_TX\_CTL | 25 | TX\_EN |
| PS\_MIO64 | J31 | RGMII\_TX\_CLK | 24 | GTX\_CLK |
| PS\_MIO[71:74] | K32-K34, L29 | RGMII\_RX\_D[0:3] | 27,28,31,32 | RXD[0:3] |
| PS\_MIO75 | L30 | RGMII\_RX\_CTL | 33 | RX\_DV |
| PS\_MIO70 | K31 | RGMII\_RX\_CLK | 35 | RX\_CLK |
| PS\_MIO76 | L33 | RGMII\_MDC | 36 | MDC |
| PS\_MIO77 | L34 | RGMII\_MDIO | 37 | MDIO |
| PS\_MIO38 | C34 | RGMII\_RST# | 42 | RESET\_N |
| PS\_MIO43 | E30 | RGMII\_INT# | 38 | INT\_N |

Table - Ethernet pinout

### UARTs to USB bridge

Bridge provide UART signalling with hardware flow control via USB interface. This is intended for debug or for data exchange between various devices. Both UARTs from ARM routed to bridge IC.

* Connector Part number: 10118193-0001LF – FCI, micro USB B;
* Bridge IC: CP2105;

### ULPI interface

ULPI interface with ULPI PHY provide USB2.0 Connectivity. Supported USB mode – OTG.

* PHY IC: USB3320C-EZK – SMC, now Microchip
* Speed modes: USB 2.0 HS, USB 2.0 FS, USB 2.0 LS;
* Supported roles: OTG.

Connections between ULPI PHY interface and MPSoC are listed below:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **XCZU7EV** | | **Schematic Net Name** | **PHY IC** | |
| **Pin Name** | **Pin Number** | **Pin number** | **Pin name** |
| PS\_MIO56 | G34 | ULPI\_DAT0 | 3 | DATA0 |
| PS\_MIO57 | H29 | ULPI\_DAT1 | 4 | DATA1 |
| PS\_MIO54 | G31 | ULPI\_DAT2 | 5 | DATA2 |
| PS\_MIO59 | H32 | ULPI\_DAT3 | 6 | DATA3 |
| PS\_MIO60 | H33 | ULPI\_DAT4 | 7 | DATA4 |
| PS\_MIO61 | H34 | ULPI\_DAT5 | 9 | DATA5 |
| PS\_MIO62 | J29 | ULPI\_DAT6 | 10 | DATA6 |
| PS\_MIO63 | J30 | ULPI\_DAT7 | 13 | DATA7 |
| PS\_MIO58 | H31 | ULPI\_STP | 29 | STP |
| PS\_MIO55 | G33 | ULPI\_NXT | 2 | NXT |
| PS\_MIO53 | G30 | ULPI\_DIR | 31 | DIR |
| PS\_MIO52 | G29 | ULPI\_CLK | 1 | CLKOUT |
| PS\_MIO37 | C33 | ULPI\_RST# | 27 | RESETB |

Table - ULPI pinout

### USB 3.0 Super Speed

Base for USB 3.0 port interface is built in MPSoC PS part GTR transceivers.

All lanes are ESD protected. Supported mode – HOST only. Signals routed to PCIe/104 connector.

### Display Port

Display port provides connectivity to various monitors. Base for Display port interface is built in MPSoC PS part GTR transceivers. Also, there is an AUX channel for data path for sound and command transmission. All lanes are ESD protected.

* Connector Part number: 472720011 – Molex;
* Lane number and maximum speed: 1- Lane, 5.4 Gbps;
* Supported Resolution: up to UHD@30Hz;
* Audio: up to two channels, sample size up to 24bit, 48kHz sample rate;
* Level shifter for AUX: 74AVC4T245BQ;
* Differential transmitter IC for AUX: FIN1019MTCX.

Connections between Display port interface and connector are listed below:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **XCZU7EV** | | **Schematic Net Name** | **Display port connector** | |
| **Pin Name** | **Pin Number** | **Pin Number** | **Pin Name** |
| PS\_MGTRTXP3\_505 | N29 | DP\_CH0+ | 1 | Lane\_0p |
| PS\_MGTRTXN3\_505 | N30 | DP\_CH0- | 3 | Lane\_0n |
| PS\_MIO27 | A30 | DP\_DATAOUT | 15 – AUXp  17 – AUXn  18 – Hot plug det | |
| PS\_MIO28 | A31 | DP\_HP\_DETECT |
| PS\_MIO29 | A32 | DP\_DAT\_OE |
| PS\_MIO30 | A33 | DP\_DAT\_IN |

Table - Display port pinout

### PCIe

Standard PCIe/104 has two stacking signals STK1 and STK2. This board acts as TYPE 2 host. User must do some action described below, while getting STACK ERROR condition. STACK ERROR condition when STK1# signal not equal “0”, **OR** STK2# signal not equal “1”. Actions to do:

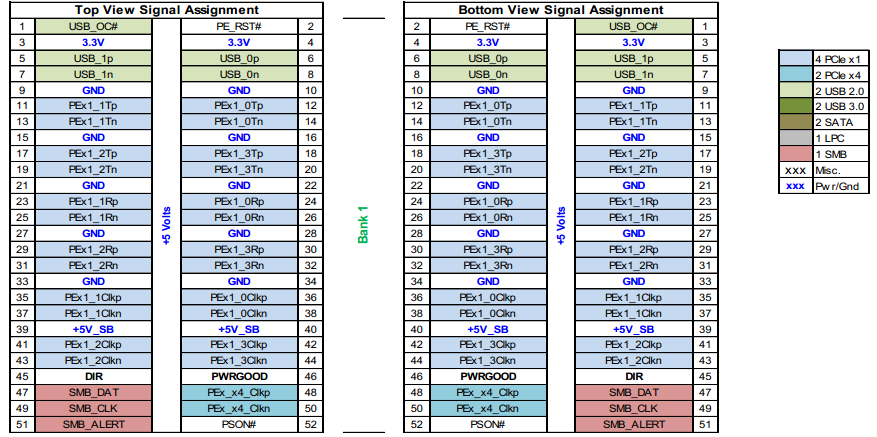
* PCIe104\_CLK\_EN signal must be driven Low;
* PCIe104\_RST\_1V2 signal(Bank 65) must be driven High;
* PCIe\_SW\_RST# signal must be driven Low;
* Stacking error led must be on(Bank 88).

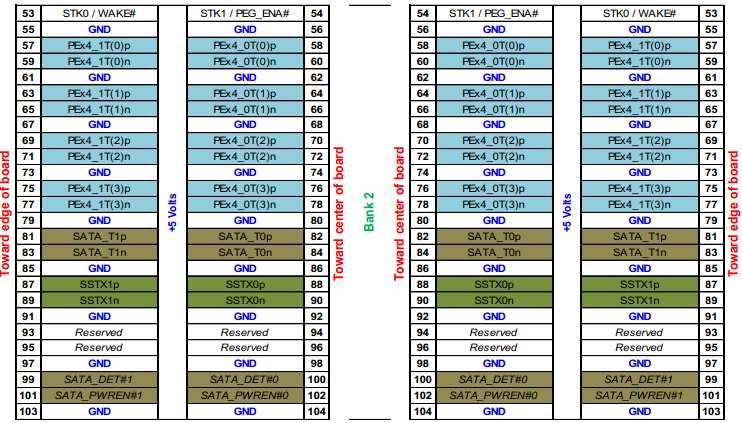
HD Bank 88 dedicated to PCIe104 , PCIe and user controls:

| **XCZU7EV bank 88 VCC\_3V3** | | | **Net Name** | **Description** |
| --- | --- | --- | --- | --- |
| **Ball Name** | **Ball Num** | **Direction MpSoC** |
| L1P\_AD15P\_88 | E1 | In | PCIx1\_SW\_LNKST\_0 | Link status from Switch |
| L1N\_AD15N\_88 | D1 | PCIx1\_SW\_LNKST\_1 |
| L2P\_AD14P\_88 | C1 | PCIx1\_SW\_LNKST\_2 |
| L2N\_AD14N\_88 | B1 | PCIx1\_SW\_LNKST\_3 |
| L3P\_AD13P\_88 | A3 | PCIx1\_SW\_LNKST\_4 |
| L3N\_AD13N\_88 | A2 | Out | PCIe104 Stack Error LED. See PCIe/104 logic chapter | |
| L4P\_AD12P\_88 | E3 | In | RGMII\_INT | Interrupt signal from ETH PHY |
| L4N\_AD12N\_88 | E2 | Out | USB\_RST# | USB PHY reset signal |
| L5P\_GC\_88 | D2 | RGMII\_RST# | ETH PHY reset signal |
| L5N\_GC\_88 | C2 | - | - | - |
| L6P\_GC\_88 | C3 | Out | USER\_LED1 | User LED 1 |
| L6N\_GC\_88 | B3 | USER\_LED2 | User LED 2 |
| L7P\_GC\_88 | C4 | USER\_LED3 | User LED 3 |
| L7N\_GC\_88 | B4 | USER\_LED4 | User LED 4 |
| L8P\_GC\_88 | E4 | In | CLK\_SYS+ | Clock input, from SI5341 OUT1 |
| L8N\_GC\_88 | D4 | CLK\_SYS- |
| L9P\_AD11P\_88 | F5 | - | - | - |
| L9N\_AD11N\_88 | F4 | - | - | - |
| L10P\_AD10P\_88 | B5 | In | STK1# | Inverted PCIe/104 stacking signals. See PCIe/104 logic chapter |
| L10N\_AD10N\_88 | A5 | STK2# |
| L11P\_AD9P\_88 | D6 | Out | PCIe\_SW\_I2CAD1 | PCIe switch I2C address selection |
| L11N\_AD9N\_88 | D5 | PCIe\_SW\_I2CAD2 |
| L12P\_AD8P\_88 | F6 | Out | PCIe104\_CLK\_EN | PCIe x1 clocks enable |
| L12N\_AD8N\_88 | E5 | PCIe\_SW\_RST# | Reset PCIe switch |

Table - PCIe pinout

Pinout for ASP-129646-03:





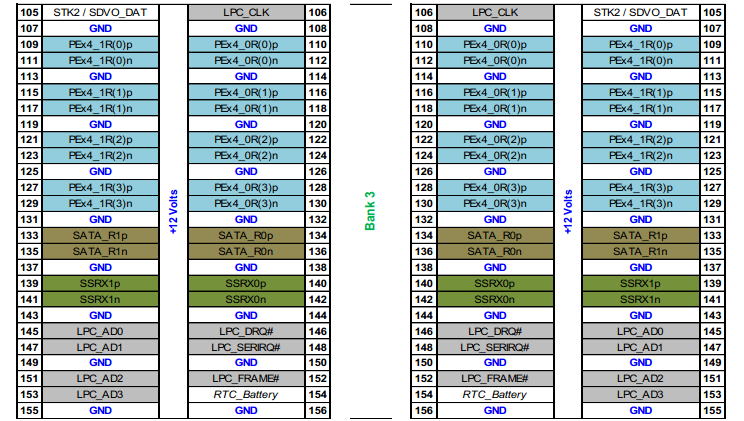


Figure - PCIe stack pinout

### SATA

There is one SATA interface located on the board. Base for SATA interface is built in MPSoC PS part GTR transceivers. All SATA interfaces are ESD protected, from static discharge.

* Connector Part number: 678005001– Molex;
* Interface: SATA 3.0 Host, up to 6Gb/s;
* Supply voltage for hard drives: NO, there is AC coupling capacitors, SO no damage to device or chip.

Connections between SATA interface and connector are listed below.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **XCZU7EV** | | **Schematic Net Name** | **SATA connectors** | |
| **Pin Name** | **Pin Number** | **Pin Number** | **Pin Name** |
| PS\_MGTRTXP2\_505 | P31 | SATA0\_TX+ | 2 | TXp\_+ |
| PS\_MGTRTXN2\_505 | P32 | SATA0\_TX- | 3 | TXp\_- |
| PS\_MGTRRXP2\_505 | R33 | SATA0\_RX+ | 6 | RXp\_+ |
| PS\_MGTRRXN2\_505 | R34 | SATA0\_RX- | 5 | RXp\_- |

Table - SATA pinout

### FMC

Banks 28, 67, 68, 64 are fully used for FMC interface only. VRP pin connected via 240 ohm resistor to ground:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **XCZU7EV banks VCCIO - VADJ** | | | **Name** | **Goes to FMC** |
| **Ball Name** | **Ball Num** | **Direction MpSoC** |
| IO\_L1P\_N0\_DBC\_67 | A17 | Bidir | FMC\_LA\_09+ | **Goes to FMC pins as named according vita 57.1** |
| IO\_L1N\_N1\_DBC\_67 | A16 | FMC\_LA\_09- |
| IO\_L2P\_N2\_67 | B16 | FMC\_LA\_04+ |
| IO\_L2N\_N3\_67 | B15 | FMC\_LA\_04- |
| IO\_L3P\_N4\_67 | A15 | Bidir | FMC\_LA\_06+ | **Goes to FMC pins as named according vita 57.1** |
| IO\_L3N\_N5\_67 | A14 | FMC\_LA\_06- |
| IO\_L4P\_N6\_DBC\_67 | B14 | FMC\_LA\_10+ |
| IO\_L4N\_N7\_DBC\_67 | B13 | FMC\_LA\_10- |
| IO\_L5P\_N8\_67 | A13 | FMC\_LA\_11+ |
| IO\_L5N\_N9\_67 | A12 | FMC\_LA\_11- |
| IO\_L6P\_N10\_67 | C13 | NC |
| IO\_L6N\_N11\_67 | C12 | NC |
| IO\_L7P\_N0\_QBC\_67 | D16 | FMC\_LA\_05+ |
| IO\_L7N\_N1\_QBC\_67 | C16 | FMC\_LA\_05- |
| IO\_L8P\_N2\_67 | D17 | FMC\_LA\_12+ |
| IO\_L8N\_N3\_67 | C17 | FMC\_LA\_12- |
| IO\_L9P\_N4\_67 | E18 | FMC\_LA\_08+ |
| IO\_L9N\_N5\_67 | E17 | FMC\_LA\_08- |
| IO\_L10P\_QBC\_67 | G14 | NC |
| IO\_L10N\_QBC\_67 | F13 | NC |
| IO\_L11P\_N8\_GC\_67 | D15 | FMC\_LA\_01\_CC+ |
| IO\_L11N\_N9\_GC\_67 | D14 | FMC\_LA\_01\_CC- |
| IO\_L12P\_N10\_GC\_67 | E15 | Input | FMC\_CLK\_0+ |
| IO\_L12N\_N11\_GC\_67 | E14 | FMC\_CLK\_0- |
| IO\_L13P\_N0\_GC\_67 | F17 | Input | CLK\_SYS2+ | Clock input, from SI5341 OUT6 |
| IO\_L13N\_N1\_GC\_67 | F16 | CLK\_SYS2- |
| IO\_L14P\_N2\_GC\_67 | G15 | Bidir | FMC\_LA\_00\_CC+ | **Goes to FMC pins as named according vita 57.1** |
| IO\_L14N\_N3\_GC\_67 | F15 | FMC\_LA\_00\_CC- |
| IO\_L15P\_N4\_67 | H19 | Bidir | FMC\_LA\_13+ | **Goes to FMC pins as named according vita 57.1** |
| IO\_L15N\_N5\_67 | G19 | FMC\_LA\_13- |
| IO\_L16P\_QBC\_67 | H18 | FMC\_LA\_15+ |
| IO\_L16N\_QBC\_67 | H17 | FMC\_LA\_15- |
| IO\_L17P\_N8\_67 | G18 | FMC\_LA\_07+ |
| IO\_L17N\_N9\_67 | F18 | FMC\_LA\_07- |
| IO\_L18P\_N10\_67 | H16 | FMC\_LA\_03+ |
| IO\_L18N\_N11\_67 | G16 | FMC\_LA\_03- |
| IO\_L19P\_N0\_DBC\_67 | L20 | FMC\_LA\_14+ |
| IO\_L19N\_N1\_DBC\_67 | K20 | FMC\_LA\_14- |
| IO\_L20P\_N2\_67 | J16 | Bidir | FMC\_LA\_02+ | **Goes to FMC pins as named according vita 57.1** |
| IO\_L20N\_N3\_67 | J15 | FMC\_LA\_02- |
| IO\_L23P\_N8\_67 | K19 | FMC\_LA\_16+ |
| IO\_L23N\_N9\_67 | K18 | FMC\_LA\_16- |
| **BANK 68** | | | | |
| IO\_L1P\_N0\_DBC\_68 | M13 | Bidir | FMC\_LA\_27+ | **Goes to FMC pins as named according vita 57.1** |
| IO\_L1N\_N1\_DBC\_68 | L13 | FMC\_LA\_27- |
| IO\_L2P\_N2\_68 | K10 | FMC\_LA\_33+ |
| IO\_L2N\_N3\_68 | J10 | FMC\_LA\_33- |
| IO\_L3P\_N4\_68 | L12 | FMC\_LA\_24+ |
| IO\_L3N\_N5\_68 | L11 | FMC\_LA\_24- |
| IO\_L4P\_N6\_DBC\_68 | K12 | FMC\_LA\_25+ |
| IO\_L4N\_N7\_DBC\_68 | J11 | FMC\_LA\_25- |
| IO\_L5P\_N8\_68 | K14 | FMC\_LA\_32+ |
| IO\_L5N\_N9\_68 | J14 | FMC\_LA\_32- |
| IO\_L6P\_N10\_68 | L14 | NC |
| IO\_L6N\_N11\_68 | K13 | NC |
| IO\_L7P\_N0\_QBC\_68 | F7 | FMC\_LA\_30+ |
| IO\_L7N\_N1\_QBC\_68 | E7 | FMC\_LA\_30- |
| IO\_L8P\_N2\_68 | C9 | FMC\_LA\_26+ |
| IO\_L8N\_N3\_68 | C8 | FMC\_LA\_26- |
| IO\_L9P\_N4\_68 | F8 | FMC\_LA\_29+ |
| IO\_L9N\_N5\_68 | E8 | FMC\_LA\_29- |
| IO\_L10P\_QBC\_68 | E9 | Bidir | FMC\_LA\_28+ | **Goes to FMC pins as named according vita 57.1** |
| IO\_L10N\_QBC\_68 | D9 | FMC\_LA\_28- |
| IO\_L11P\_N8\_GC\_68 | H9 | FMC\_LA\_18\_CC+ |
| IO\_L11N\_N9\_GC\_68 | G9 | FMC\_LA\_18\_CC- |
| IO\_L12P\_N10\_GC\_68 | G10 | Input | FMC\_CLK1+ |
| IO\_L12N\_N11\_GC\_68 | F10 | FMC\_CLK1- |
| IO\_L13P\_N0\_GC\_68 | H11 | Bidir | FMC\_LA\_17\_CC+ |
| IO\_L13N\_N1\_GC\_68 | G11 | FMC\_LA\_17\_CC- |
| IO\_L14P\_GC\_68 | F11 | FMC\_CLK3\_BDIR+ |
| IO\_L14N\_GC\_68 | E10 | FMC\_CLK3\_BDIR- |
| IO\_L15P\_N4\_68 | H13 | FMC\_LA\_21+ |
| IO\_L15N\_N5\_68 | H12 | FMC\_LA\_21- |
| IO\_L16P\_QBC\_68 | D11 | FMC\_CLK2\_BDIR+ |
| IO\_L16N\_QBC\_68 | D10 | FMC\_CLK2\_BDIR- |
| IO\_L19P\_N0\_DBC\_68 | C7 | FMC\_LA\_31+ |
| IO\_L19N\_N1\_DBC\_68 | C6 | FMC\_LA\_31- |
| IO\_L20P\_N2\_68 | B9 | FMC\_LA\_22+ |
| IO\_L20N\_N3\_68 | B8 | FMC\_LA\_22- |
| IO\_L21P\_N4\_68 | B6 | FMC\_LA\_19+ |
| IO\_L21N\_N5\_68 | A6 | FMC\_LA\_19- |
| IO\_L22P\_DBC\_68 | B10 | FMC\_LA\_23+ |
| IO\_L22N\_DBC\_68 | A10 | FMC\_LA\_23- |
| IO\_L23P\_N8\_68 | A8 | FMC\_LA\_20+ |
| IO\_L23N\_N9\_68 | A7 | FMC\_LA\_20- |
| **BANK 28** | | | | |
| IO\_L1P\_N0\_DBC\_28 | L21 | Bidir | FMC\_HA\_05+ | **Goes to FMC pins as named according vita 57.1** |
| IO\_L1N\_N1\_DBC\_28 | L22 | FMC\_HA\_05- |
| IO\_L2P\_N2\_28 | L23 | FMC\_HA\_23+ |
| IO\_L2N\_N3\_28 | K24 | FMC\_HA\_23- |
| IO\_L3P\_N4\_28 | J21 | FMC\_HA\_04+ |
| IO\_L3N\_N5\_28 | J22 | FMC\_HA\_04- |
| IO\_L4P\_N6\_DBC\_28 | K22 | FMC\_HA\_22+ |
| IO\_L4N\_N7\_DBC\_28 | K23 | FMC\_HA\_22- |
| IO\_L5P\_N8\_28 | J25 | Bidir | FMC\_HA\_21+ | **Goes to FMC pins as named according vita 57.1** |
| IO\_L5N\_N9\_28 | H26 | FMC\_HA\_21- |
| IO\_L6P\_N10\_28 | J24 | FMC\_HA\_19+ |
| IO\_L6N\_N11\_28 | H24 | FMC\_HA\_19- |
| IO\_L7P\_N0\_QBC\_28 | E19 | FMC\_HA\_09+ |
| IO\_L7N\_N1\_QBC\_28 | D19 | FMC\_HA\_09- |
| IO\_L8P\_N2\_28 | H21 | FMC\_HA\_13+ |
| IO\_L8N\_N3\_28 | H22 | FMC\_HA\_13- |
| IO\_L9P\_N4\_28 | D20 | FMC\_HA\_03+ |
| IO\_L9N\_N5\_28 | D21 | FMC\_HA\_03- |
| IO\_L10P\_QBC\_28 | G20 | FMC\_HA\_10+ |
| IO\_L10N\_QBC\_28 | F20 | FMC\_HA\_10- |
| IO\_L11P\_N8\_GC\_28 | F22 | FMC\_HA\_01\_CC+ |
| IO\_L11N\_N9\_GC\_28 | E22 | FMC\_HA\_01\_CC- |
| IO\_L12P\_N10\_GC\_28 | G21 | FMC\_HA\_00\_CC+ |
| IO\_L12N\_N11\_GC\_28 | F21 | FMC\_HA\_00\_CC- |
| IO\_L13P\_N0\_GC\_28 | F23 | FMC\_HA\_18\_CC+ |
| IO\_L13N\_N1\_GC\_28 | E23 | FMC\_HA\_18\_CC- |
| IO\_L14P\_N2\_GC\_28 | G23 | FMC\_HA\_17\_CC+ |
| IO\_L14N\_N3\_GC\_28 | G24 | FMC\_HA\_17\_CC- |
| IO\_L15P\_N4\_28 | C21 | FMC\_HA\_11+ |
| IO\_L15N\_N5\_28 | C22 | FMC\_HA\_11- |
| IO\_L16P\_QBC\_28 | E24 | FMC\_HA\_14+ |
| IO\_L16N\_QBC\_28 | D24 | FMC\_HA\_14- |
| IO\_L17P\_N8\_28 | D22 | FMC\_HA\_15+ |
| IO\_L17N\_N9\_28 | C23 | FMC\_HA\_15- |
| IO\_L18P\_N10\_28 | G25 | Bidir | FMC\_HA\_20+ | **Goes to FMC pins as named according vita 57.1** |
| IO\_L18N\_N11\_28 | G26 | FMC\_HA\_20- |
| IO\_L19P\_N0\_DBC\_28 | A18 | FMC\_HA\_07+ |
| IO\_L19N\_N1\_DBC\_28 | A19 | FMC\_HA\_07- |
| IO\_L20P\_N2\_28 | C18 | FMC\_HA\_02+ |
| IO\_L20N\_N3\_28 | C19 | FMC\_HA\_02- |
| IO\_L21P\_N4\_28 | A20 | FMC\_HA\_12+ |
| IO\_L21N\_N5\_28 | A21 | FMC\_HA\_12- |
| IO\_L22P\_N6\_DBC\_28 | B18 | FMC\_HA\_08+ |
| IO\_L22N\_N7\_DBC\_28 | B19 | FMC\_HA\_08- |
| IO\_L23P\_N8\_28 | A22 | FMC\_HA\_16+ |
| IO\_L23N\_N9\_28 | A23 | FMC\_HA\_16- |
| IO\_L24P\_N10\_28 | B20 | FMC\_HA\_06+ |
| IO\_L24N\_N11\_28 | B21 | FMC\_HA\_06- |
| **BANK 64 VCCIO IS VIO\_B\_M2C** | | | | |
| IO\_L3P\_64 | AM18 | Bidir | FMC\_HB\_18+ | **Goes to FMC pins as named according vita 57.1** |
| IO\_L3N\_64 | AN18 | FMC\_HB\_18- |
| IO\_L4P\_64 | AM14 | FMC\_HB\_05+ |
| IO\_L4N\_64 | AN14 | FMC\_HB\_05- |
| IO\_L5P\_64 | AP16 | FMC\_HB\_03+ |
| IO\_L5N\_64 | AP15 | FMC\_HB\_03- |
| IO\_L6P\_64 | AN17 | FMC\_HB\_02+ |
| IO\_L6N\_64 | AN16 | FMC\_HB\_02- |
| IO\_L7P\_64 | AM16 | FMC\_HB\_01+ |
| IO\_L7N\_64 | AM15 | FMC\_HB\_01- |
| IO\_L8P\_64 | AL16 | FMC\_HB\_04+ |
| IO\_L8N\_64 | AL15 | FMC\_HB\_04- |
| IO\_L9P\_64 | AK18 | FMC\_HB\_21+ |
| IO\_L9N\_64 | AL18 | FMC\_HB\_21- |
| IO\_L10P\_64 | AK15 | Bidir | FMC\_HB\_20+ | **Goes to FMC pins as named according vita 57.1** |
| IO\_L10N\_64 | AK14 | FMC\_HB\_20- |
| IO\_L11P\_GC\_64 | AJ17 | FMC\_HB\_14+ |
| IO\_L11N\_GC\_64 | AK17 | FMC\_HB\_14- |
| IO\_L12P\_GC\_64 | AJ16 | FMC\_HB\_17\_CC+ |
| IO\_L12N\_GC\_64 | AJ15 | FMC\_HB\_17\_CC- |
| IO\_L13P\_GC\_64 | AH18 | FMC\_HB\_00\_CC+ |
| IO\_L13N\_GC\_64 | AH17 | FMC\_HB\_00\_CC- |
| IO\_L14P\_GC\_64 | AF18 | FMC\_HB\_06\_CC+ |
| IO\_L14N\_GC\_64 | AG18 | FMC\_HB\_06\_CC- |
| IO\_L15P\_64 | AE17 | FMC\_HB\_15+ |
| IO\_L15N\_64 | AF17 | FMC\_HB\_15- |
| IO\_L16P\_64 | AH14 | FMC\_HB\_19+ |
| IO\_L16N\_64 | AJ14 | FMC\_HB\_19- |
| IO\_L17P\_64 | AF16 | FMC\_HB\_16+ |
| IO\_L17N\_64 | AF15 | FMC\_HB\_16- |
| IO\_L18P\_64 | AG15 | FMC\_HB\_11+ |
| IO\_L18N\_64 | AG14 | FMC\_HB\_11- |
| IO\_L19P\_64 | AD15 | FMC\_HB\_10+ |
| IO\_L19N\_64 | AE15 | FMC\_HB\_10- |
| IO\_L20P\_64 | AC17 | FMC\_HB\_09+ |
| IO\_L20N\_64 | AC16 | FMC\_HB\_09- |
| IO\_L21P\_64 | AB16 | FMC\_HB\_12+ |
| IO\_L21N\_64 | AB15 | FMC\_HB\_12- |
| IO\_L22P\_64 | AA16 | FMC\_HB\_13+ |
| IO\_L22N\_64 | AA15 | FMC\_HB\_13- |
| IO\_L23P\_64 | AA14 | FMC\_HB\_08+ |
| IO\_L23N\_64 | AB14 | FMC\_HB\_08- |
| IO\_L24P\_64 | AD17 | FMC\_HB\_07+ |
| IO\_L24N\_64 | AD16 | FMC\_HB\_07- |

Table - FMC Interface pinout

### I2C Interface

There are two I2C interfaces on the board. I2C interface belong to PS part of MPSoC. For connected device listing and their addresses see 4.7 COnfiguration and initialization.

* Modes: Master and slave
* Addressing: 7-bit, 10 bit in master mode only

Connections between I2C interfaces and MPSoC are listed below:

|  |  |  |
| --- | --- | --- |
| **XCZU7EV** | | **Schematic Net Name** |
| **Pin Name** | **Pin Number** |
| PS\_MIO34 | B34 | SCL\_3V3 |
| PS\_MIO35 | C31 | SDA\_3V3 |
| PS\_MIO24 | E28 | SCL\_1V8 |
| PS\_MIO25 | D29 | SDA\_1V8 |

Table - I2C pinout

### Fan connector

A fan connector is available on-board.

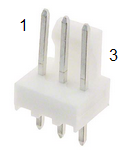


Figure - Fan connector

1. Tacho signal from FAN Yellow wire of FAN,
2. 12V, red wire of FAN
3. Ground, Black wire of FAN

# Footprint

## Top View

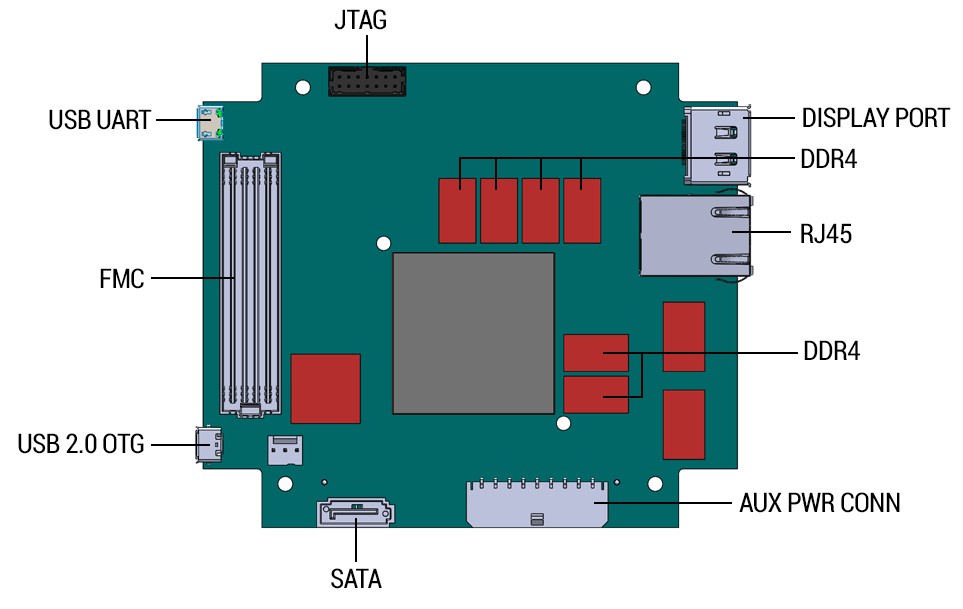


Figure - PCIE104Z top view

## Bottom View

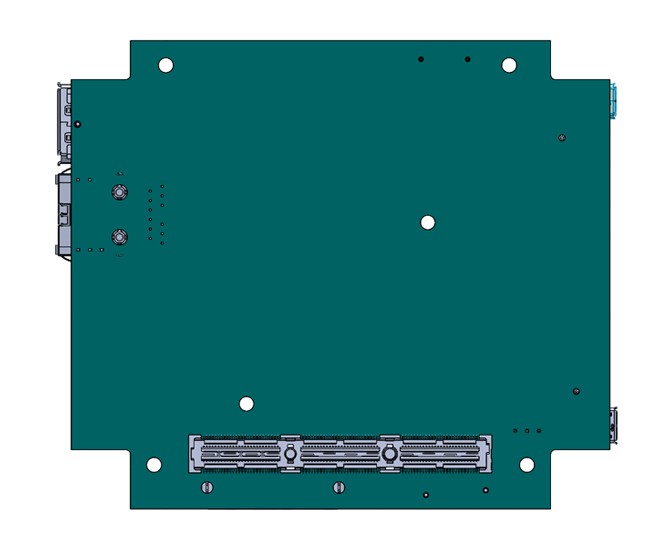


Figure - PCIE104Z bottom view

# Physical Properties

|  |  |  |
| --- | --- | --- |
| Dimensions |  |  |
| Weight |  |  |
| Supply Voltages |  |  |
| Supply Current | +12V |  |
|  | +5V |  |
| MTBF |  |  |

# Safety

This module presents no hazard to the user when in normal use.

# EMC

This module is designed to operate from within an enclosed host system, which is build to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system.

This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the output cables.

Short circuiting any output to ground does not cause the host PC system to lock up or reboot.