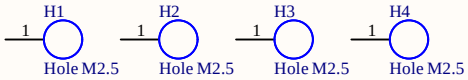
Revision History

1v0 Initial release.
1v1 Finalised USB circuit.
1v2 Added ESD to USB 3.
Corrected camera lanes 2 & 3.
Added pull-up on MCU RST/NMI pin.
UART2 TX & RX pins swapped.
Added 33R series termination for USB clocks.
JTAG connector pin 10 (nRESET) conencted to PS_SRST_B.
1v3 Replaced 1.2 VCCO power rail with LDO.
Added PL & PS VCCINT DCDCs to I2C bus.
Added ESD protection on USB3.
Added test points.

Notes

See part description for case size.
All resistors are 1%.
Ceramic cap voltages are a minimum.
Net names are global.



PCB

PCB

ODKv3 PCB Revision 1v0

Company: Sundance / Opteran	Project: ODK v1
Title: Cover Sheet	Revision: 1v3
Date: 13/4/22	Sheet: 1 of 15
Filename: Cover Sheet.SchDoc	Drawn: GKP

CLK from PL, 3.3V CLK to camera, max 2.8V

CAM_A_CLK — R70 100R — CAM_A_CLK_28; R71 560R; GND
CAM_B_CLK — R72 100R — CAM_B_CLK_28; R73 560R; GND
CAM_C_CLK — R74 100R — CAM_C_CLK_28; R75 560R; GND
CAM_D_CLK — R76 100R — CAM_D_CLK_28; R77 560R; GND

CAM_A Matched Net Lengths [Tolerance = 0.5mm]
CAM_B Matched Net Lengths [Tolerance = 0.5mm]
CAM_C Matched Net Lengths [Tolerance = 0.5mm]
CAM_D Matched Net Lengths [Tolerance = 0.5mm]

PA — J1 10051922-2210ELF
PB — J3 10051922-2210ELF
PC — J4 10051922-2210ELF
PD — J5 10051922-2210ELF

CAM_A_D0_N, CAM_A_D0_P, CAM_A_D1_N, CAM_A_D1_P, CAM_A_CK_N, CAM_A_CK_P, CAM_A_D2_N, CAM_A_D2_P, CAM_A_D3_N, CAM_A_D3_P, CAM_A_EN, CAM_A_CLK_28, CAM_A_SCL, CAM_A_SDA
CAM_B_D0_N, CAM_B_D0_P, CAM_B_D1_N, CAM_B_D1_P, CAM_B_CK_N, CAM_B_CK_P, CAM_B_D2_N, CAM_B_D2_P, CAM_B_D3_N, CAM_B_D3_P, CAM_B_EN, CAM_B_CLK_28, CAM_B_SCL, CAM_B_SDA
CAM_C_D0_N, CAM_C_D0_P, CAM_C_D1_N, CAM_C_D1_P, CAM_C_CK_N, CAM_C_CK_P, CAM_C_D2_N, CAM_C_D2_P, CAM_C_D3_N, CAM_C_D3_P, CAM_C_EN, CAM_C_CLK_28, CAM_C_SCL, CAM_C_SDA
CAM_D_D0_N, CAM_D_D0_P, CAM_D_D1_N, CAM_D_D1_P, CAM_D_CK_N, CAM_D_CK_P, CAM_D_D2_N, CAM_D_D2_P, CAM_D_D3_N, CAM_D_D3_P, CAM_D_EN, CAM_D_CLK_28, CAM_D_SCL, CAM_D_SDA

3V3 — C88 10uF, C90 100nF — GND
3V3 — C91 10uF, C92 100nF — GND
3V3 — C93 10uF, C94 100nF — GND
3V3 — C95 10uF, C96 100nF — GND

R57 4k7 — CAM_A_SCL
R61 4k7 — CAM_A_SDA
R58 4k7 — CAM_B_SCL
R62 4k7 — CAM_B_SDA
R59 4k7 — CAM_C_SCL
R63 4k7 — CAM_C_SDA
R60 4k7 — CAM_D_SCL
R64 4k7 — CAM_D_SDA

I2C bus for cameras only.

3V3 — C70 4u7F — GND

U6 PCA9546A-RGY

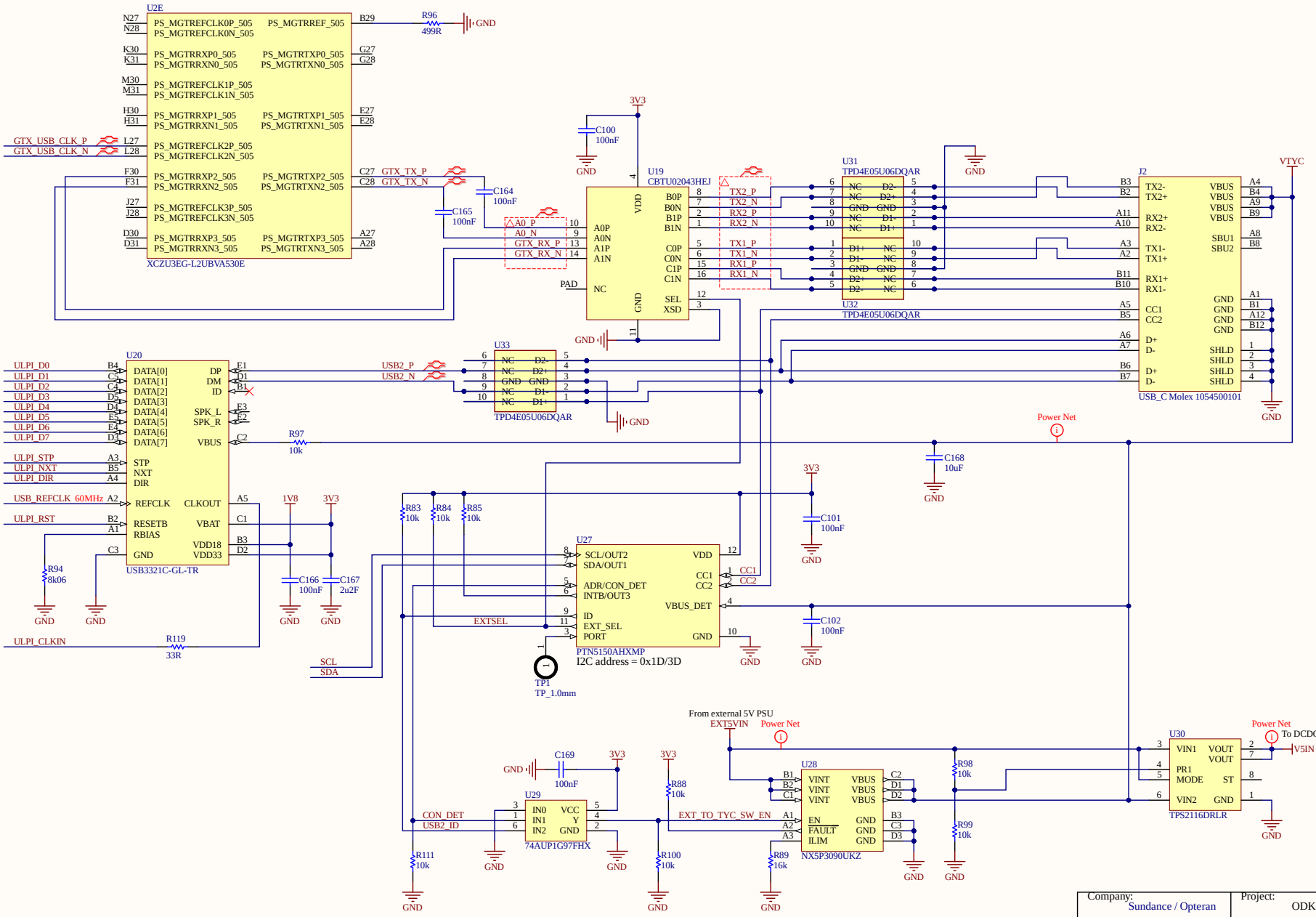
Pin	Name	Net
16	VCC	3V3
14	SCL	CAM_SCL
15	SDA	CAM_SDA
3	RESET	CAM_I2C_RST
1	A0	GND
2	A1	GND
13	A2	GND
8	GND	GND
17	TPAD	GND
5	SC0	CAM_A_SCL
4	SD0	CAM_A_SDA
7	SC1	CAM_B_SCL
6	SD1	CAM_B_SDA
10	SC2	CAM_C_SCL
9	SD2	CAM_C_SDA
12	SC3	CAM_D_SCL
11	SD3	CAM_D_SDA

3V3 — R65 4k7, R66 4k7, R67 10k — CAM_SCL, CAM_SDA

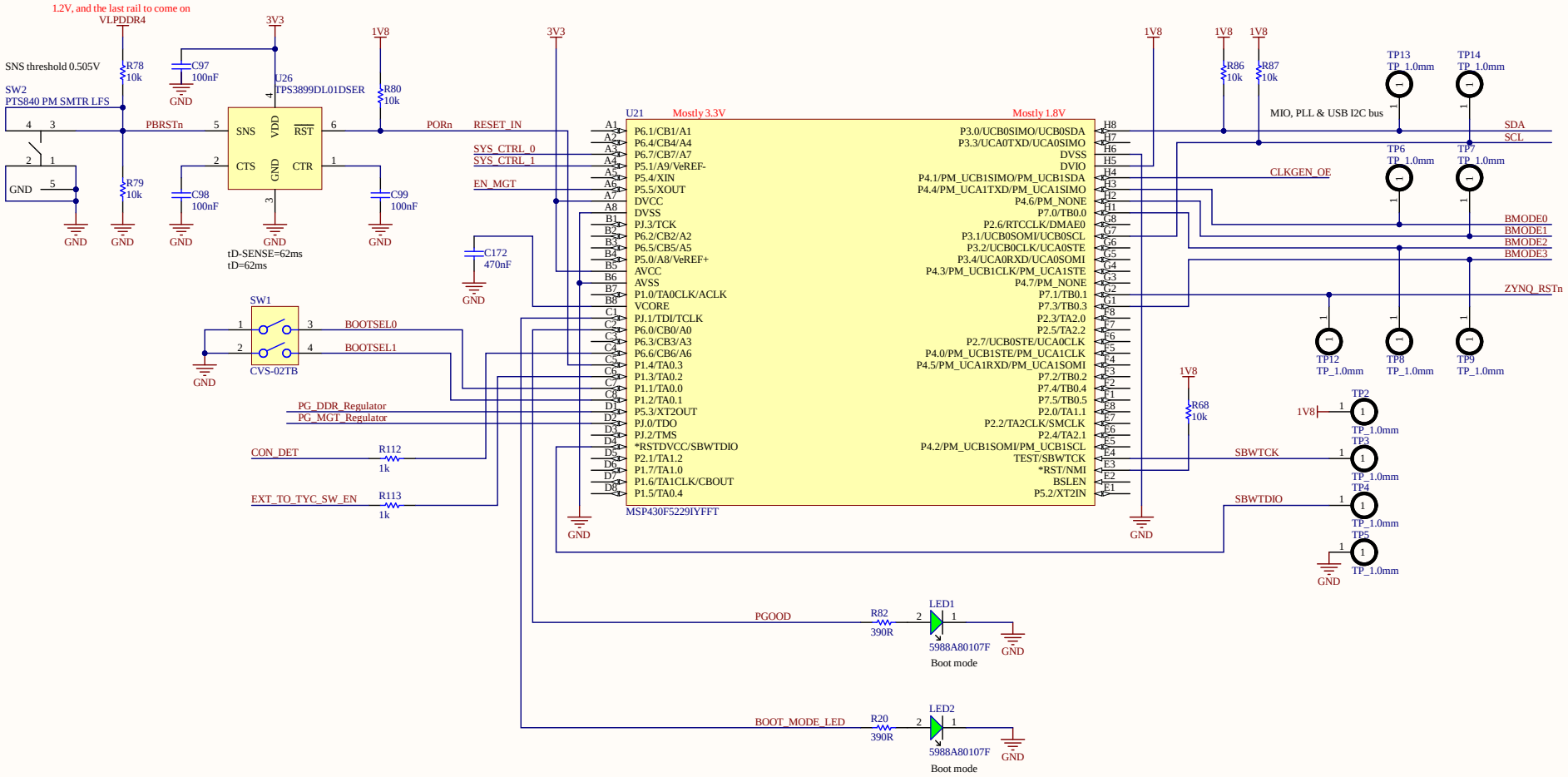
CAM_I2C_RST — TP10 TP_1.0mm; TP11 TP_1.0mm

I2C address = 0x70

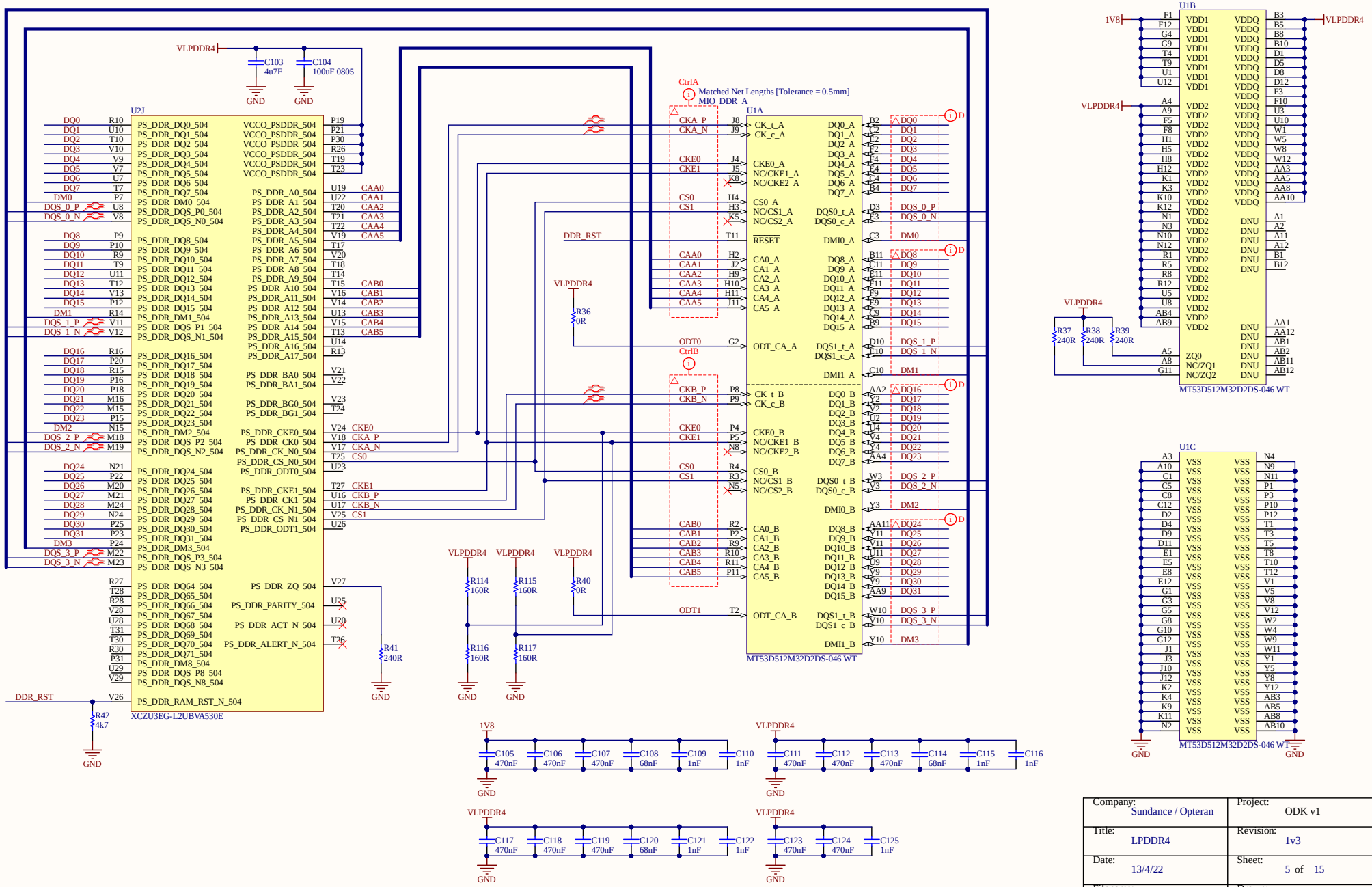
Company: Sundance / Opteran	Project: ODK v1
Title: Camera	Revision: 1v3
Date: 13/4/22	Sheet: 2 of 15
Filename: Camera.SchDoc	Drawn: GKP



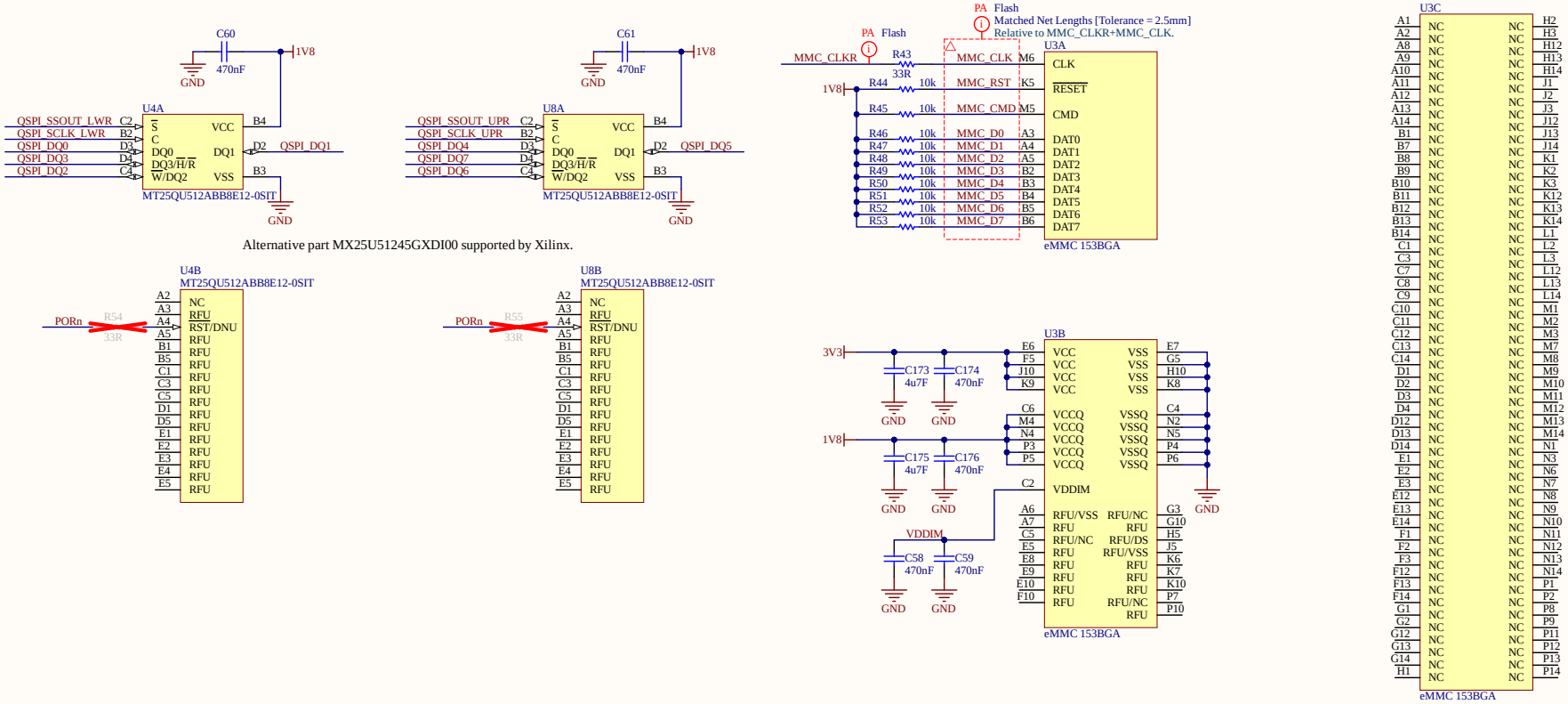
Company: Sundance / Opteran	Project: ODK v1
Title: USB	Revision: 1v3
Date: 13/4/22	Sheet: 3 of 15
Filename: USB.SchDoc	Drawn: GKP



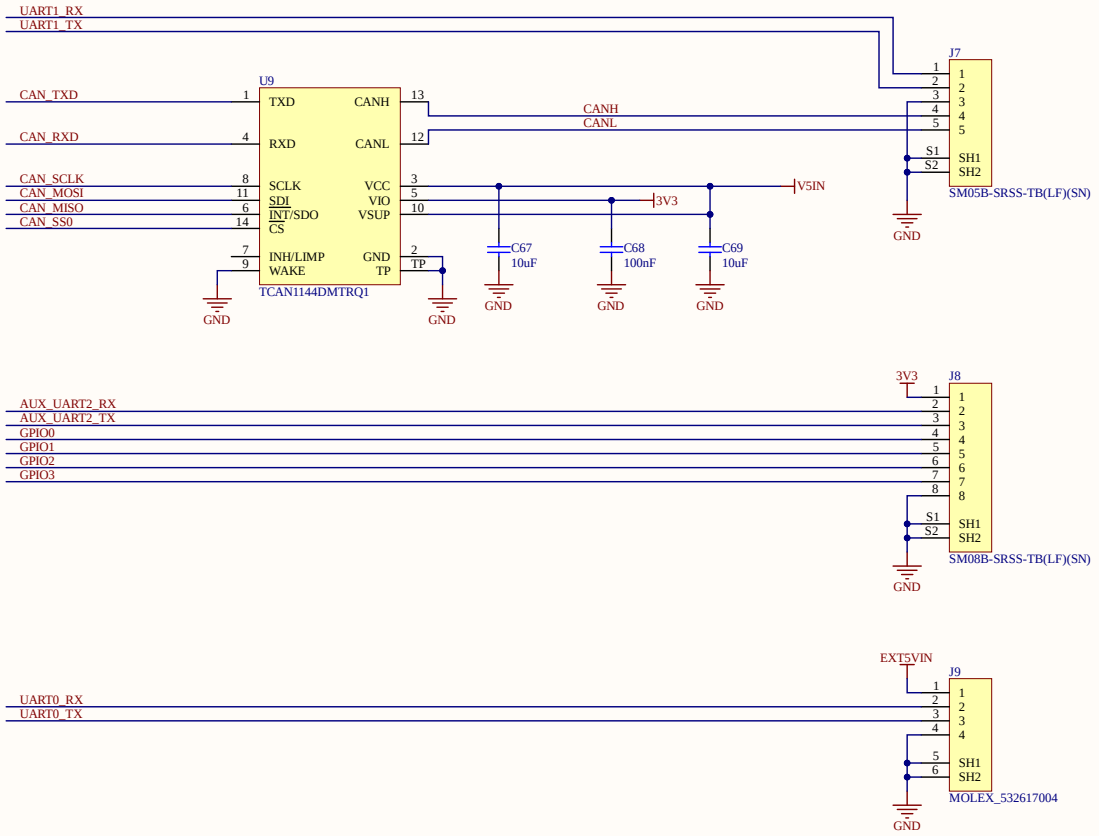
Company: Sundance / Opteran	Project: ODK v1
Title: MCU	Revision: 1v2
Date: 13/4/22	Sheet: 4 of 15
Filename: MCU.SchDoc	Drawn: GKP



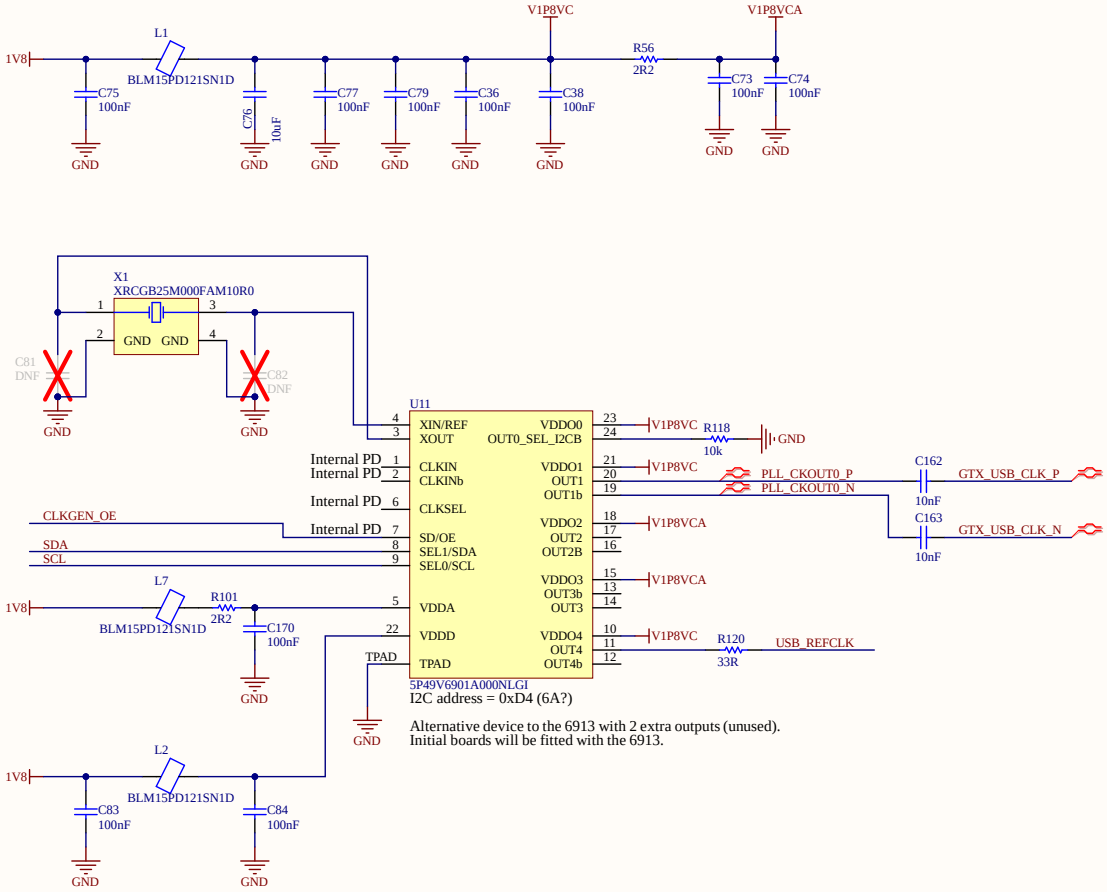
Company: Sundance / Opteran	Project: ODK v1
Title: LPDDR4	Revision: 1v3
Date: 13/4/22	Sheet: 5 of 15
Filename: DDR.SchDoc	Drawn: GKP



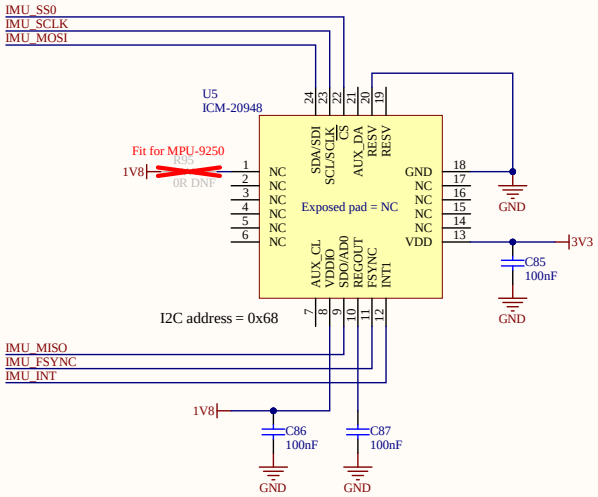
Company: Sundance / Opteran	Project: ODK v1
Title: Flash	Revision: 1v3
Date: 13/4/22	Sheet: 6 of 15
Filename: Flash.SchDoc	Drawn: GKP



Company: Sundance / Opteran	Project: ODK v1
Title: CAN GPIO misc	Revision: 1v3
Date: 13/4/22	Sheet: 7 of 15
Filename: CAN misc.SchDoc	Drawn: GKP

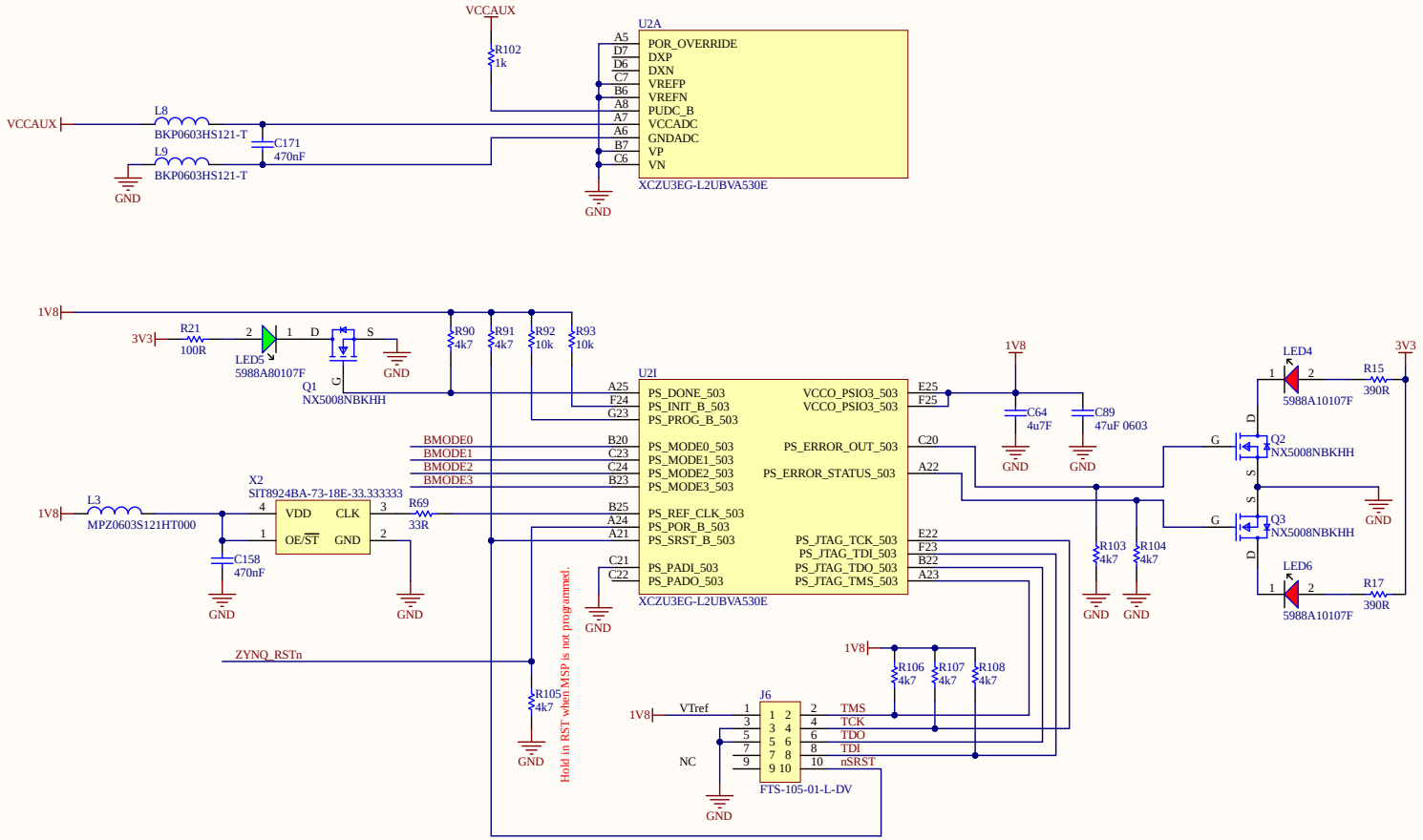


Company: Sundance / Opteran	Project: ODK v1
Title: Clock PLL	Revision: 1v3
Date: 13/4/22	Sheet: 8 of 15
Filename: Clock PLL.SchDoc	Drawn: GKP

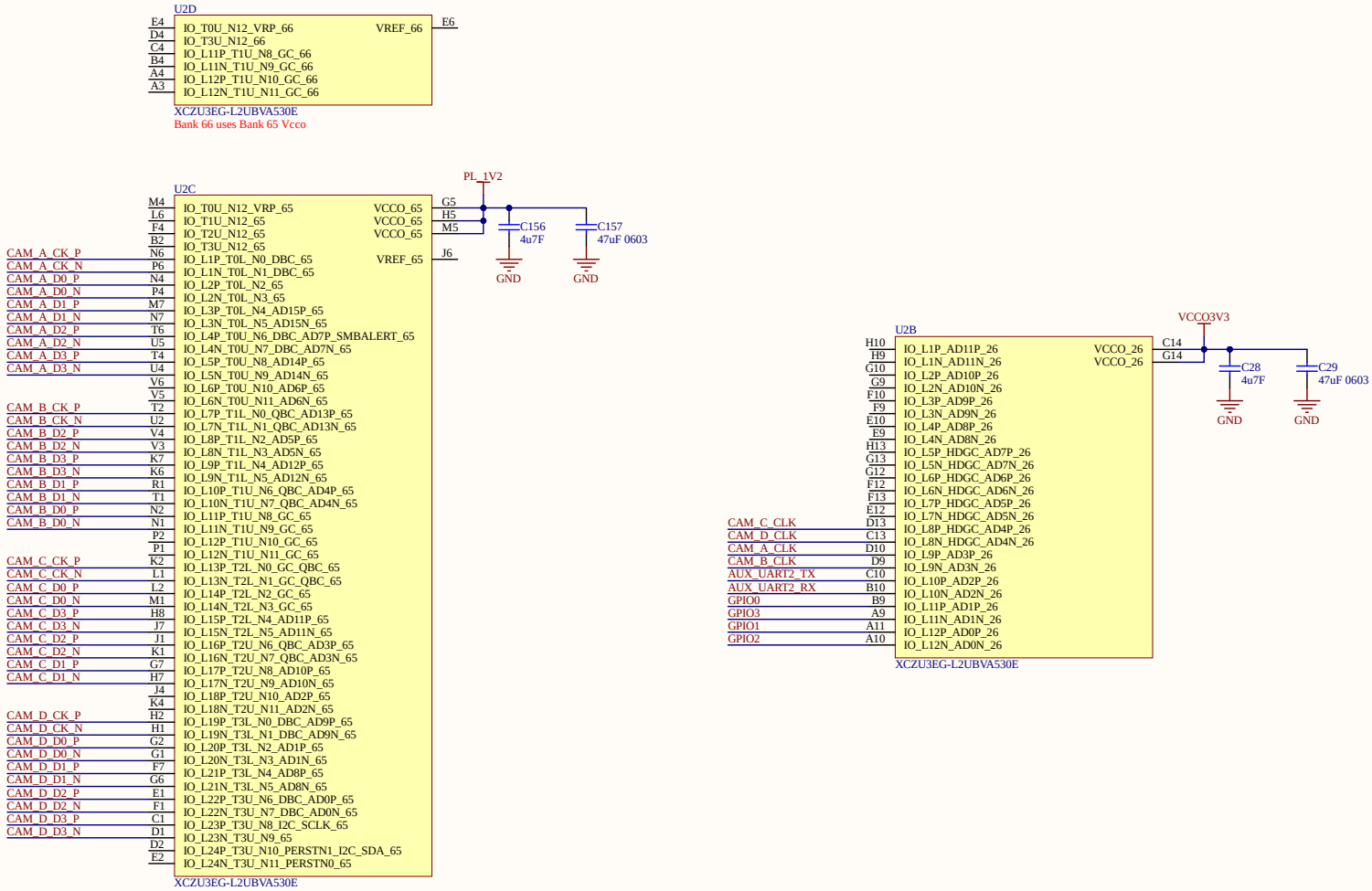


Company: Sundance / Opteran	Project: ODK v1
Title: IMU	Revision: 1v3
Date: 13/4/22	Sheet: 9 of 15
Filename: IMU.SchDoc	Drawn: GKP

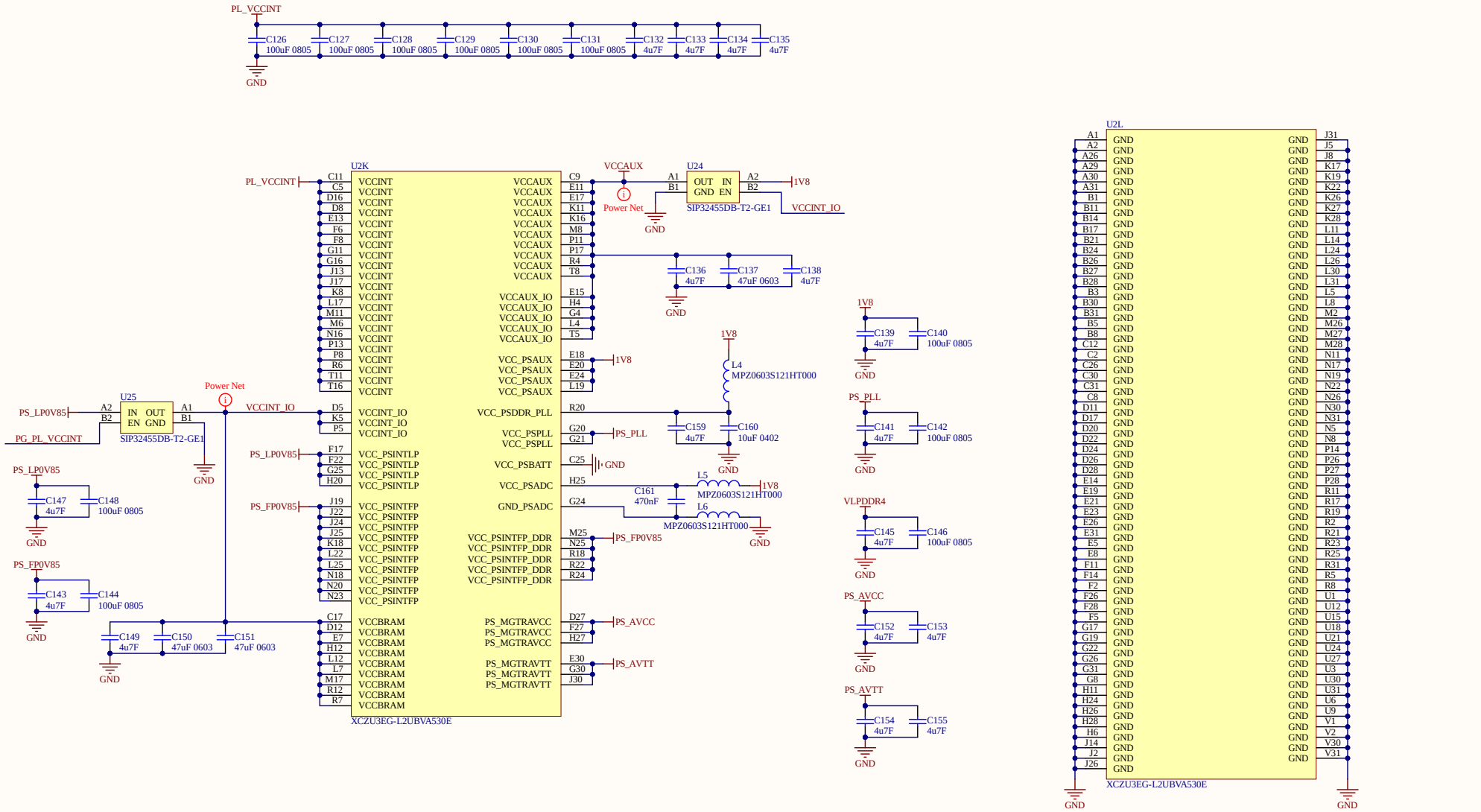
Company: Sundance / Opteran	Project: ODK v1
Title: MIO 1	Revision: 1v3
Date: 13/4/22	Sheet: 10of 15
Filename: MIO 500-502.SchDoc	Drawn: GKP



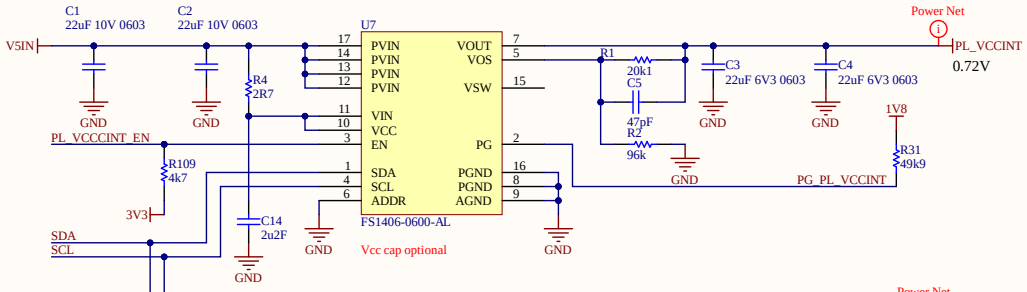
Company: Sundance / Opteran	Project: ODK v1
Title: FPGA JTAG	Revision: 1v3
Date: 13/4/22	Sheet: 11of 15
Filename: FPGA JTAG.SchDoc	Drawn: GKP

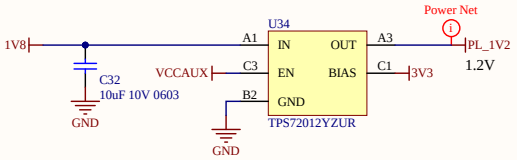


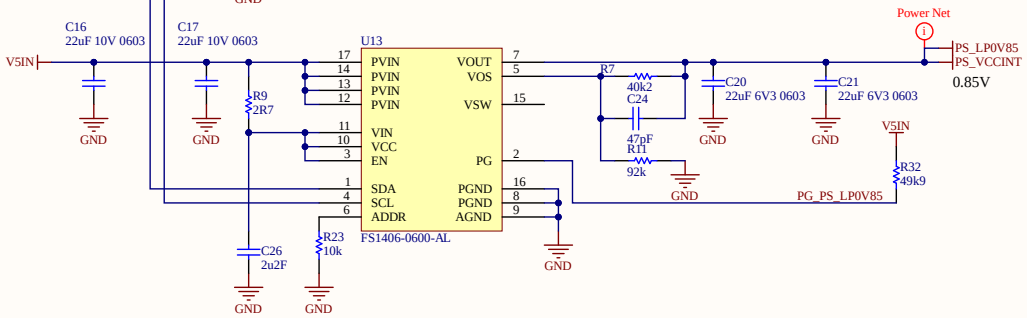
Company: Sundance / Opteran	Project: ODK v1
Title: FPGA PL 1	Revision: 1v3
Date: 13/4/22	Sheet: 12of 15
Filename: FPGA PL.SchDoc	Drawn: GKP

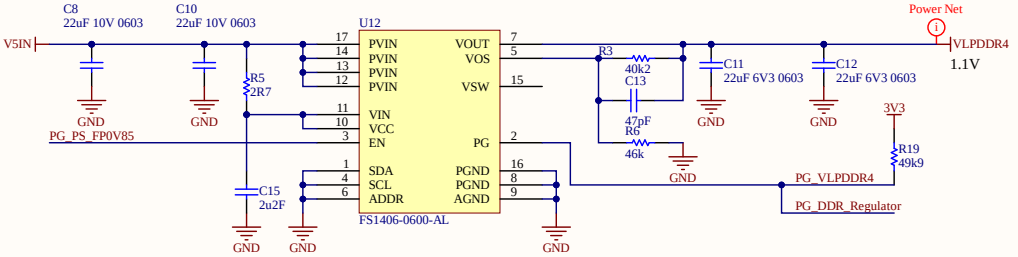


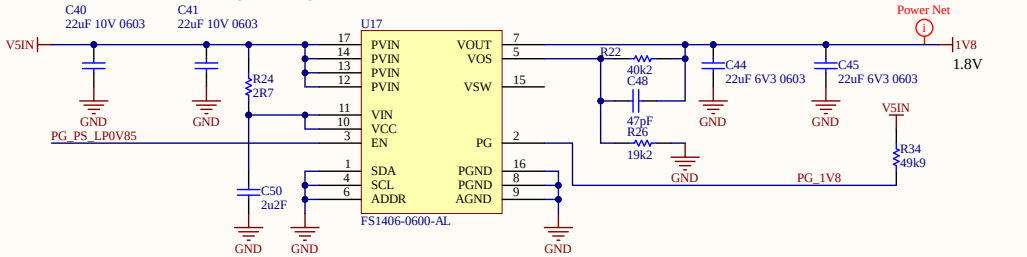
Company: Sundance / Opteran	Project: ODK v1
Title: FPGA Power	Revision: 1v3
Date: 13/4/22	Sheet: 13of 15
Filename: FPGA Power.SchDoc	Drawn: GKP

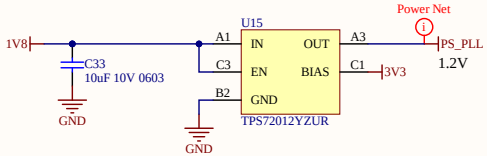


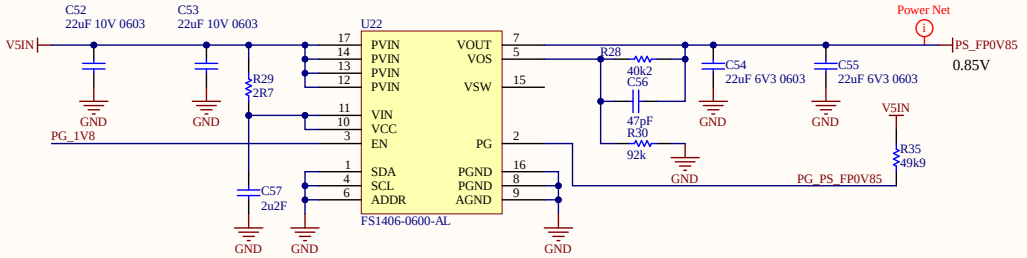


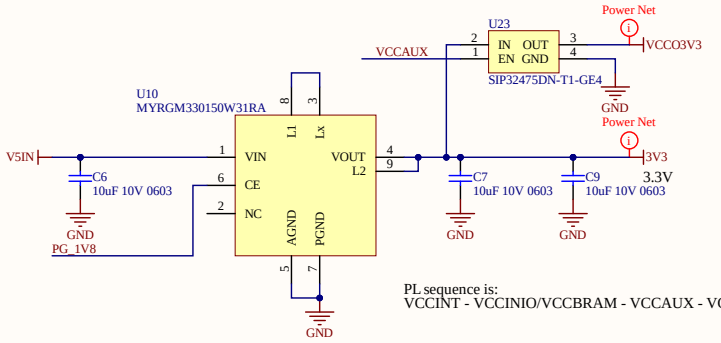






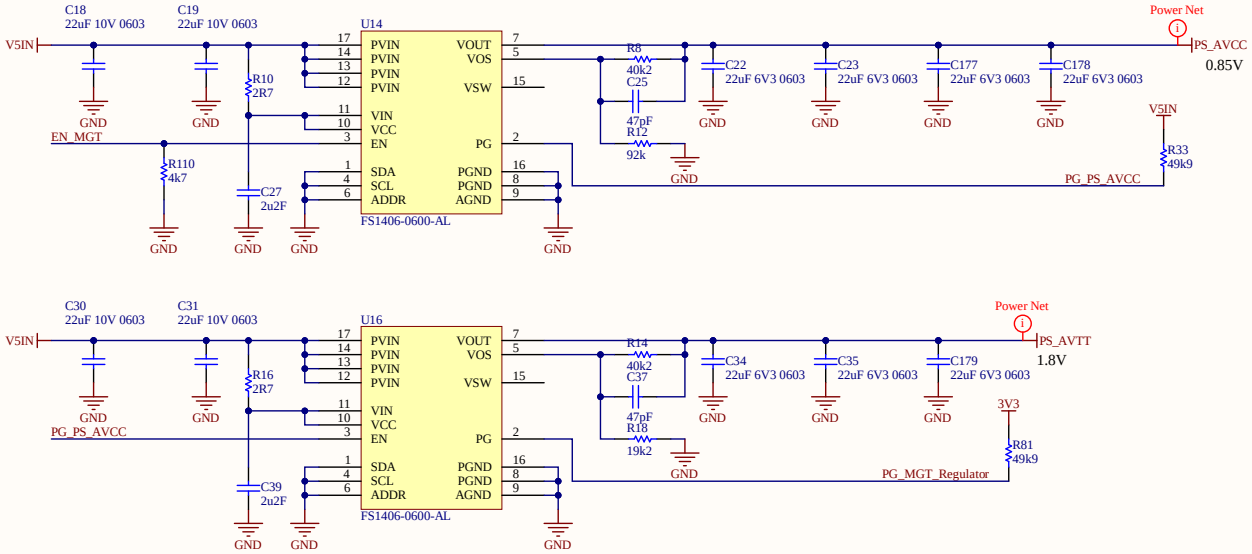






POWER ON	V5IN > PS_VCCINT/PS_LP0V85 > 1V8 > PS_PLL/3V3 > PS_FP0V85 > PG_VLPDDR4
SIGNAL FROM PS	PL_VCCINT_EN > PL_VCCINT > VCCINT_IO > VCCAUX > VCCO3V3
SIGNAL FORM MSP	EN_MGT > PS_AVCC > PS_AVTT

Company: Sundance / Opteran	Project: ODK v1
Title: Power Supply	Revision: 1v3
Date: 13/4/22	Sheet: 14of 15
Filename: Power Supply.SchDoc	Drawn: GKP



Company: Sundance / Opteran	Project: ODK v1
Title: Power Supply 2	Revision: 1v3
Date: 13/4/22	Sheet: 15of 15
Filename: Power Supply 2.SchDoc	Drawn: GKP