Unit / Module Description:	Video Controls Sensors Development Platform
Unit / Module Number:	VCS-3
Document Issue Number:	1.2
Issue Date:	31st August 2022
Original Author:	Graeme Parker

Design Specification for VCS-3

Sundance Multiprocessor Technology Ltd, Chiltern House, Waterside, Chesham, Bucks. HP5 1PS.

Revision History

Issue	Changes Made	Date	Initials
1.0	First draft	26/8/2022	GKP
1.1	Major update.	31/8/2022	GKP
1.2	Name change. Typo corrections.	31/8/2022	GKP

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1 Introduction

The VCS-3 is a standalone autonomy solution, providing a streamlined means for the robot integrator to design AI algorithms and IP into their autonomous systems.

2 Data Sheets

Xilinx Zynq UltraScale+ MPSoC Data Sheeet:

https://docs.xilinx.com/v/u/en-US/ds891-zynq-ultrascale-plus-overview

eMMC datasheet

https://www.issi.com/WW/pdf/IS21_22ES08G.pdf

SPI ROM datasheet

https://media-www.micron.com/-/media/client/global/documents/products/data-sheet/nor-flash/serial-nor/mt25q/die-rev-b/mt25q_qlkt_u_512_abb_0.pdf

USB controller datasheet

https://www.mouser.co.uk/datasheet/2/268/332x-467932.pdf

LPDDR4 datasheet

https://www.micron.com/products/dram/lpdram/part-catalog/mt53d512m32d2ds-053-aut

PLL datasheet

https://www.renesas.com/us/en/document/dst/5p49v6901-datasheet

IMU datasheet

https://invensense.tdk.com/wp-content/uploads/2016/06/DS-000189-ICM-20948-v1.3.pdf?ref_disty=digikey

DCDC datasheets

https://product.tdk.com/en/system/files?file=dam/doc/product/power/switching-power/micro-pol/data_sheet/fs1406_datasheet.pdf

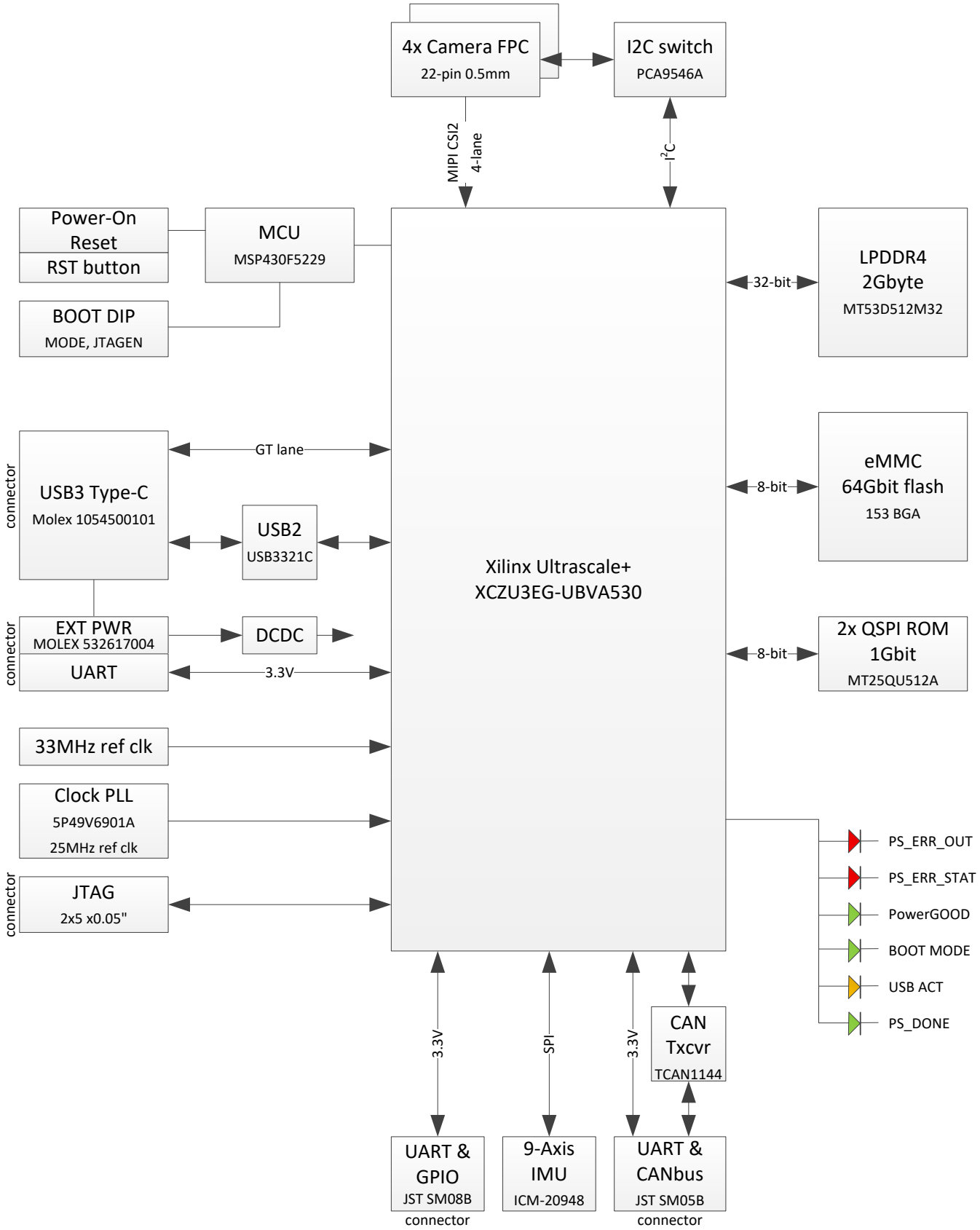
https://www.murata.com/products/productdata/8807035797534/MYRGM-b-w.pdf?1583754814000

3 Acronyms and Abbreviations

BER	Bit error rate.
bps	Bits per second.
CAN	Controller Area Network. Automotive serial bus.
DDR	Double Data Rate. Typically in reference to memories.
eMMC	embedded Multi-Media Card. Flash memory device.
ESD	Electrostatic Discharge.
FPC	Flexible Printed Circuit.
FPGA	Field Programmable Gate Array.
Gbps	Giga (10^9) bits per second.
GPIO	General Purpose I/O.
GTX	High speed serial interface.
I^2C	Inter-Integrated Circuit. Multi-master, multi-slave, serial bus.
IMU	Inertial Measurement Unit. Accelerometer.
JTAG	Joint Test Action Group. Serial interface for chip testing.
LED	Light Emitting Diode
LPDDR4	Low Power DDR memory, 4^{th} generation.
MCU	Microcontroller Unit
MGT	See GTX.
MPSoC	Multi-Processor System on a Chip.
PLL	Phase Locked Loop.
PSU	Power Supply Unit.
ROM	Read Only Memory.
SoC	System on Chip.
SPI	Serial Peripheral Interface.
UART	Universal Asynchronous Receiver Transmitter.
ULPI	UTMI Low Pin Interface.
USB	Universal Serial Bus.
UTMI	USB Transceiver Macrocell Interface.
VBUS	USB power signal/pin.
VCS	Video Controls Sensors.

4 Functional Description

4.1 Block Diagram



4.2 Module Description

The VCS-3 utilizes a Xilinx UltraScale+ MPSoC coupled with high speed LPDDR4 memory to produce a highly compact evaluation platform. Together with 4 digital camera interfaces, a 9-axis IMU, and a CANBus interface, this platform is ideally suited for autonomous machine research.

Device booting can be from either SPI ROMs or eMMC flash, with no bulky, fiddly or unreliable SD cards.

Numerous on-board power rails are generated from a single external 5V supply, or via a USB3 Type-C interface.

Several LEDs indicate board functionality, and numerous test points allow access to the various interfaces.

4.3 Functional Description

4.3.1 Xilinx UltraScale+ MPSoC

This is an XCZU3EG device in a UBVA530 BGA package. It requires 13 power rails (some of them common). Refer to the power supply section, page 10.

Device booting is controlled by the microcontroller, page 11, and can be from eMMC or SPI ROM.

A 33MHz clock is used as the system clock, and a separate PLL based clock used for the GTX. See page 11.

The UltraScale+ device interfaces are detailed following.

The pin-out is given in the pinout section, page 24.

4.3.2 LPDDR4

A single 32-bit wide MT53D512M32D2DS device provides 2Gbytes of memory.

This device connects directly to the PS side of the UltraScale+. Termination is provided on-die with the exception CKE (clock enable) which use discrete resistors at the track ends.

The LPDDR4 is powered at 1.8V and 1.1V internal, with 1.1V I/O.

4.3.3 eMMC

This flash memory provides 8Gbytes of non-volatile storage in a 153 BGA package.

It connects directly to the MIO pins of the PS.

It is powered at 3.3V with 1.8V I/O.

4.3.4 SPI ROM

Two 4-bit wide MT25QU512 devices form an 8-bit SPI ROM interface to the UltraScale+ on its PS interface.

Each device is 512Mbits thus the two provide 1Gbit of storage.

They are powered at 1.8V.

4.3.5 Camera FPC

Four CSI-2 4-lane interfaces are provided over separate 22 pin 0.5mm FPC. The interfaces' differential signals are routed as high-speed nets (length and skew matched) to the UltraScale+ on its PL bus. Each lane supports data rates up to 900Mb/s.

The pin-out is shown here: https://www.arducam.com/raspberry-pi-camera-pinout/

The camera interface I2C connection is supplied via a PCA9546A-RGY I2C switch. This has the ability to access cameras individually or via a broadcast to all cameras simultaneously. The I2C is connected to the PS interface.

The camera clock is from the PL interface via a potential divider to ensure the voltage is less than 2.8V.

The cameras are powered at 3.3V.

4.3.6 IMU

An ICM-20948 9-axis MEMS device is connected as an SPI device to the PS interface.

It is powered at 3.3V and the interface includes an interrupt.

Alternative parts, e.g. MPU9250, may be fitted as they have compatible footprints.

4.3.7 UART

Three UART interfaces are provided; one on the CANbus connector (JST SM05B-SRSS-TB(LF)(SN)), one on the GPIO connector (JST SM08B-SRSS-TB(LF)(SN)), and the third on the external power input connector (MOLEX 532617004).

UARTs 0 & 1 are provided by MIO pins on the PS interface. AUX_UART2 is via the PL interface. All 3 are at 3.3V levels.

4.3.8 GPIO

Four GPIO signal are connected to the PL interface at 3.3V, and share a connector with the AUX_UART2.

4.3.9 CANBus

A TCAN1144DMTRQ1 CAN transceiver supports data rates up to 5Mb/s. This is connected to the PS as an SPI device.

This device has both 5V and 3.3V power supplies.

4.3.10 USB

USB3 signalling is provided directly by the UltraScale+ device using a single PS MGT lane.

The MGT clock is provided by a PLL based clock generator, page 11.

USB2 signalling is via a USB3321C controller. This part connects to the UltraScale+ as an 8-bit ULPI interface. The ULPI reference clock, 60MHz, is also provided by the PLL.

The Type-C connector's USB3 signals are switched using a CBTU02043HEJ USB switching device. This device selects the connector's active differential pairs. [USB Type-C allows for cable insertion in either orientation, thus two sets of Rx/Tx pairs are available.]

ESD protection is provided for all of the Type-C's signals.

Power to the VCS-3 module may be derived from the USB connector, or power from the external power connector can be provided to the USB connector. Whether this module is a USB host or device is determined by the MCU which in turn controls the required power switches.

4.3.11 Power Supply

Several TDK FS1406-0600 DCDC converters are used to generate a range of local power rails. A single MYRGM330150 DCDC generates the local 3.3V rail. The DCDCs are supplemented by a couple of linear regulators (TPS72012) and further power switches (SIP32455) to ensure the power rail sequencing is correct for the UltraScale+.

Rail	Voltage	Device
PL_VCCINT	0.72V	FS1406
1V8	1.8V	FS1406
PL_1V2	1.2V	TPS72012
PS_PLL	1.2V	TPS72012
PS_AVCC	0.85V	FS1406
VCCINT_IO	0.85	SIP32455

Rail	Voltage	Device
PS_VCCINT, PS_LP0V85	0.85V	FS1406
PS_FP0V85	0.85V	FS1406
VLPDDR4	1.1V	FS1406
VCCO3V3	3.3V	MYRGM330150
PS_AVTT	1.8V	FS1406
VCCAUX	1.8V	SIP32455

Both the PS_VCCINT and PL_VCCINT DCDC converters are connected to the PS via I2C. This allows for the UltraScale+ to adjust these voltage rails (minimum 0.6V).

The PL_VCCINT power rail can be disabled using MIO pin MIO42 (pin J9).

The PS_AVCC power rail can be disabled using MCU pin A6 (port P5.5).

4.3.12 Clocks

A 33.33MHz oscillator provides the UltraScale+ reference clock (PS_REF_CLK_503, pin B25).

A Renesas 5P49V6901A000NLGI PLL can be configured using the I2C bus in order to provide the USB GTX clock (PLL OUT1). The PLL reference clock is 25MHz.

The PLL also produces the 60MHz USB2 reference clock on OUT4.

4.3.13 MCU Booting

A Texas Instruments MSP430F5229IYFFT MCU is programmed to control the UltraScale+ boot mode, reset and USB3 port direction.

Boot mode is selected by 2 dip switches. The MCU uses the state of these switches to control the UltraScale+ bootmode using the BMODE pins.

BMODE Pins [3:0]	Function
0000	PS JTAG
0001	QSPI (24 bit)
0010	QSPI (32 bit)
0110	eMMC

The MCU is programmed using a 2-wire interface accessible on surface mount pads compatible with spring-loaded pins.

The MCU also monitors the power good signals from the DDR and MGT regulators, and in turn illuminates a power good LED.

Overall system reset is via a TPS3899DL01DSER voltage supervisor. This has a reset input from a push button switch.

Refer to full circuit diagrams for full connectivity.

The device pinout is shown on page 30.

4.3.14 LEDs

Six LEDs are grouped together and indicate the following:

LED	Colour	Function
LED5	Green	PS_DONE
LED4	Red	PS_ERROR_OUT
LED6	Red	PS_ERROR_STATUS
LED3	Orange	USB activity
LED1	Green	Power good
LED2	Green	Boot mode

4.3.15 Test Points

Test Point	Function
1	PORT (USB)
2	1.8V
3	SBWTCK
4	SBWTDIO
5	GND
6	BMODE0
7	BMODE1

Test Point	Function
8	BMODE2
9	BMODE3
10	CAM_SCL
11	CAM_SDA
12	ZYNQ-RST#
13	SDA (MCU)
14	SCL (MCU)

5 Verification & Validation Procedures

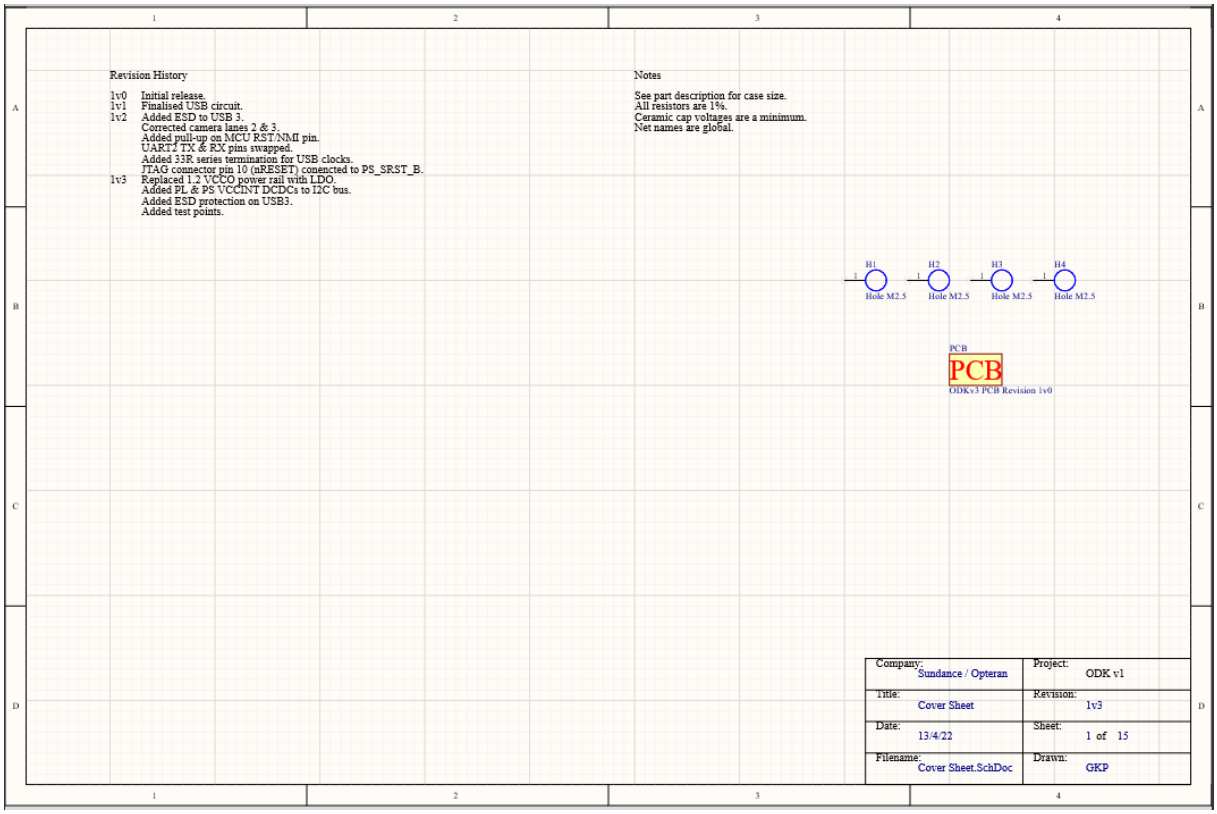
In accordance with Sundance Quality Procedures.

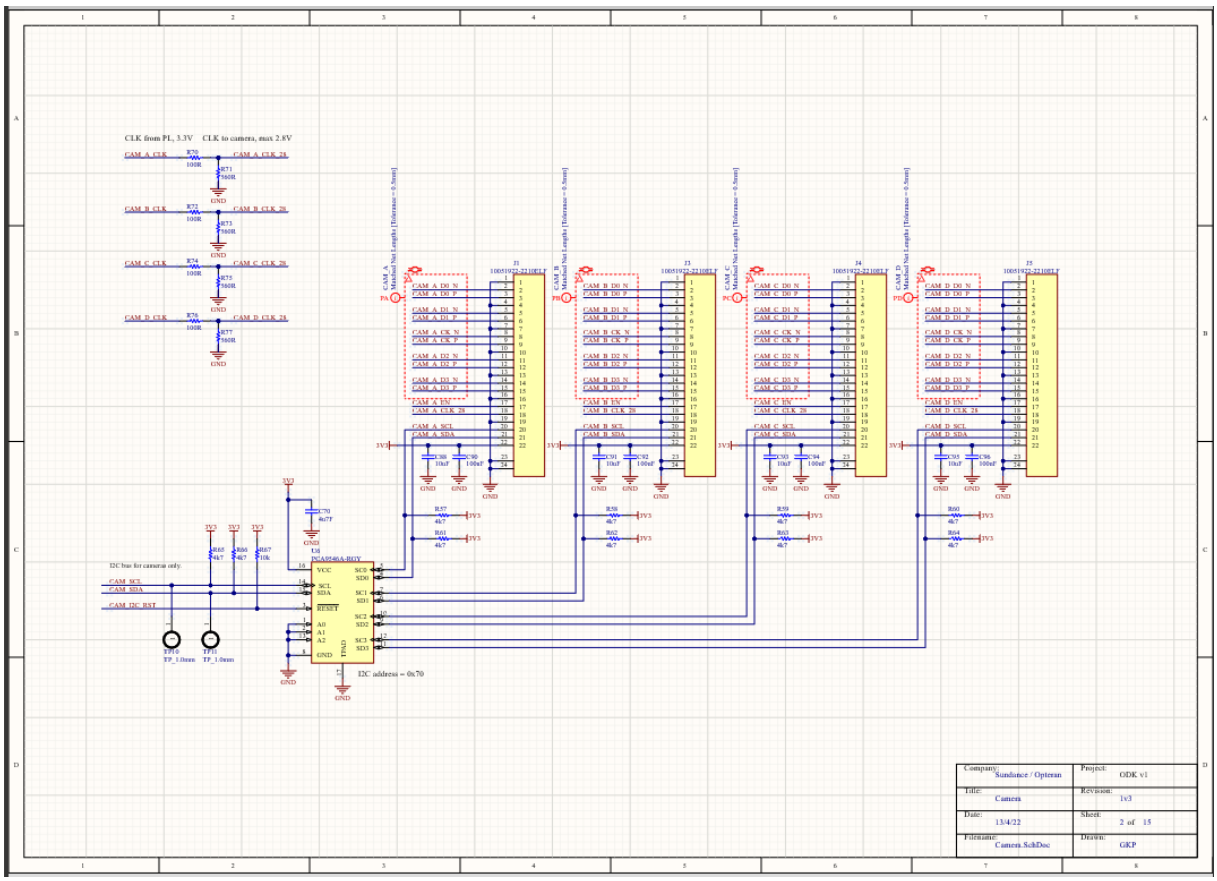
6 Review Procedures

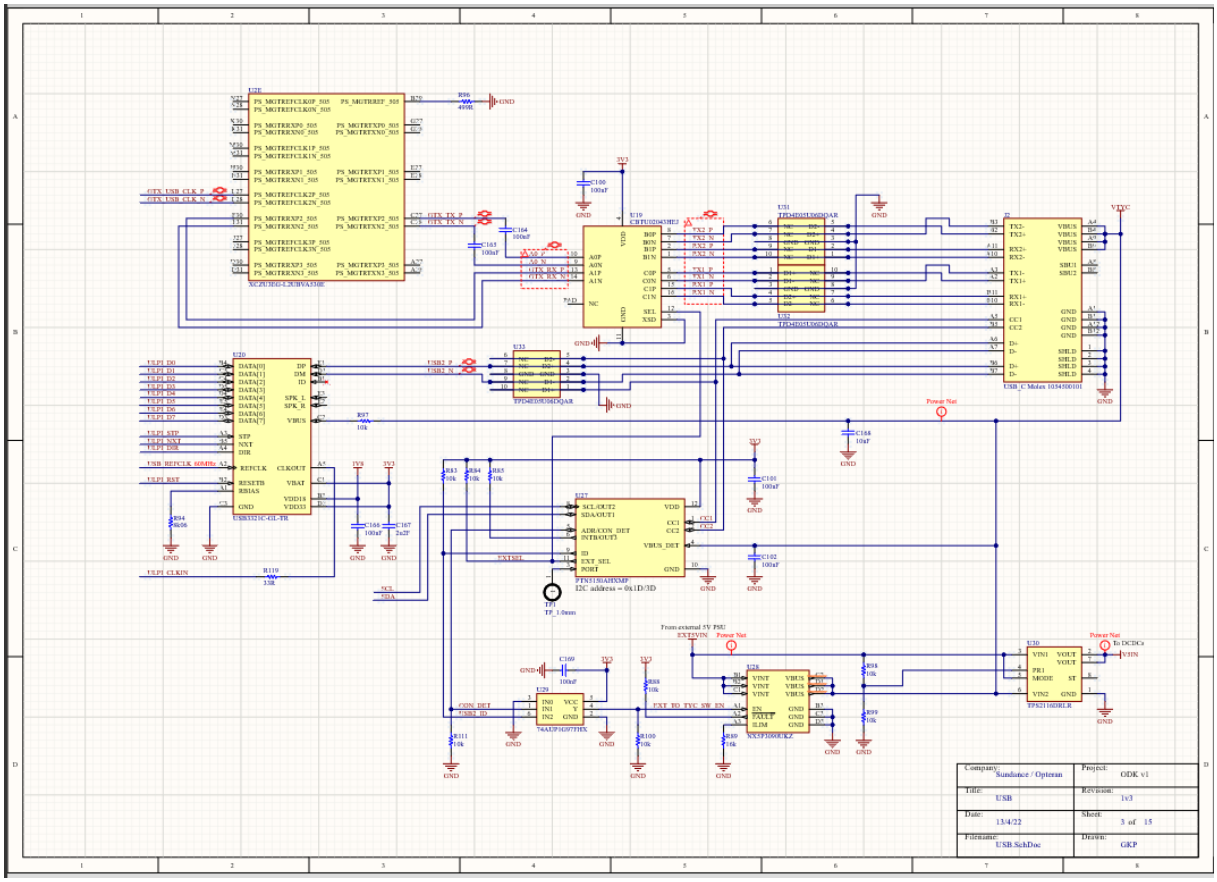
In accordance with Sundance Quality Procedures.

7 Circuit Description / Diagrams

Full resolution schematics are also available in pdf.




CLK from PL, 3.3V
CLK to camera, max 2.8V
I2C bus for cameras only.
I2C address = 0x70
Company: Sundance / Opteran
Project: ODK v1
Title: Camera
Revision: 1v3
Date: 13/4/22
Sheet: 2 of 15
Filename: Camera.SchDoc
Drawn: GKP


I2C address = 0x1D/3D
Company: Sundance / Opteran
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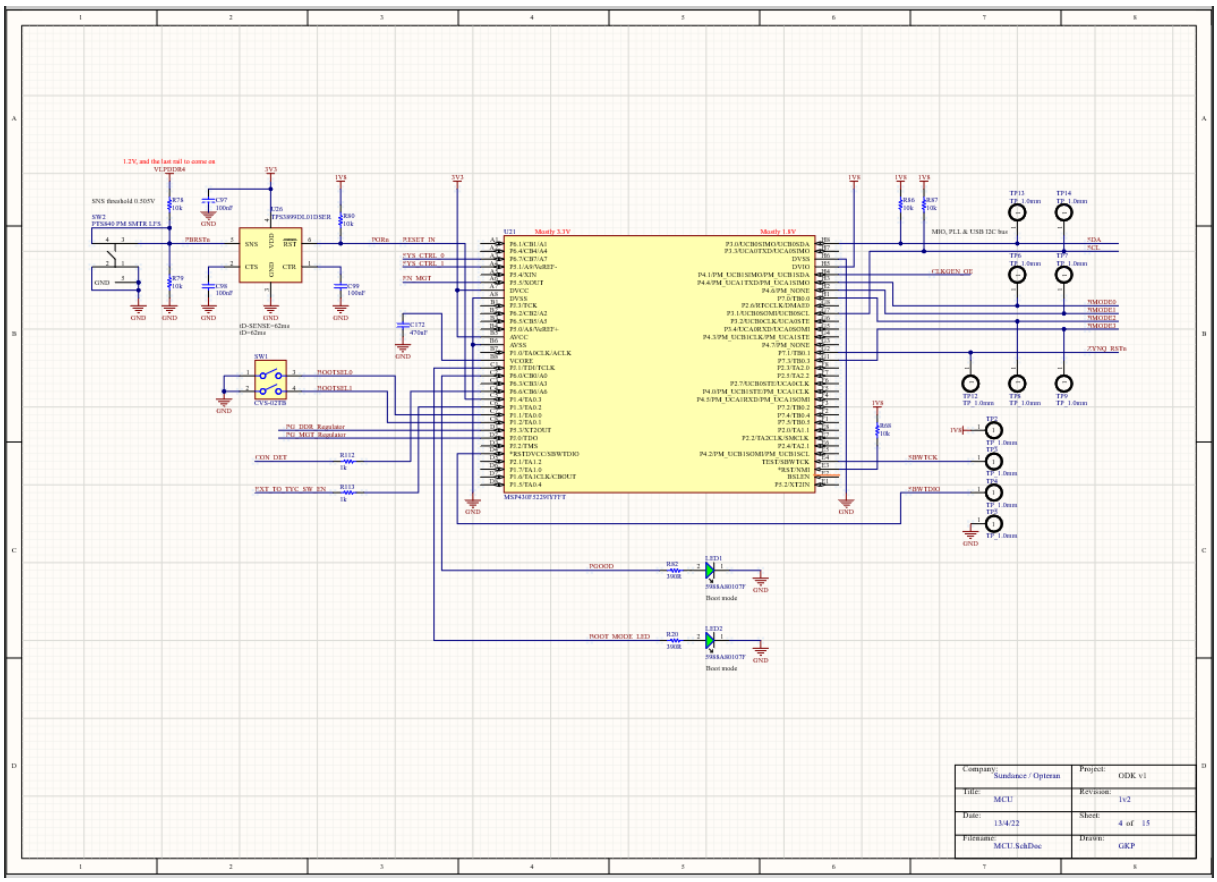
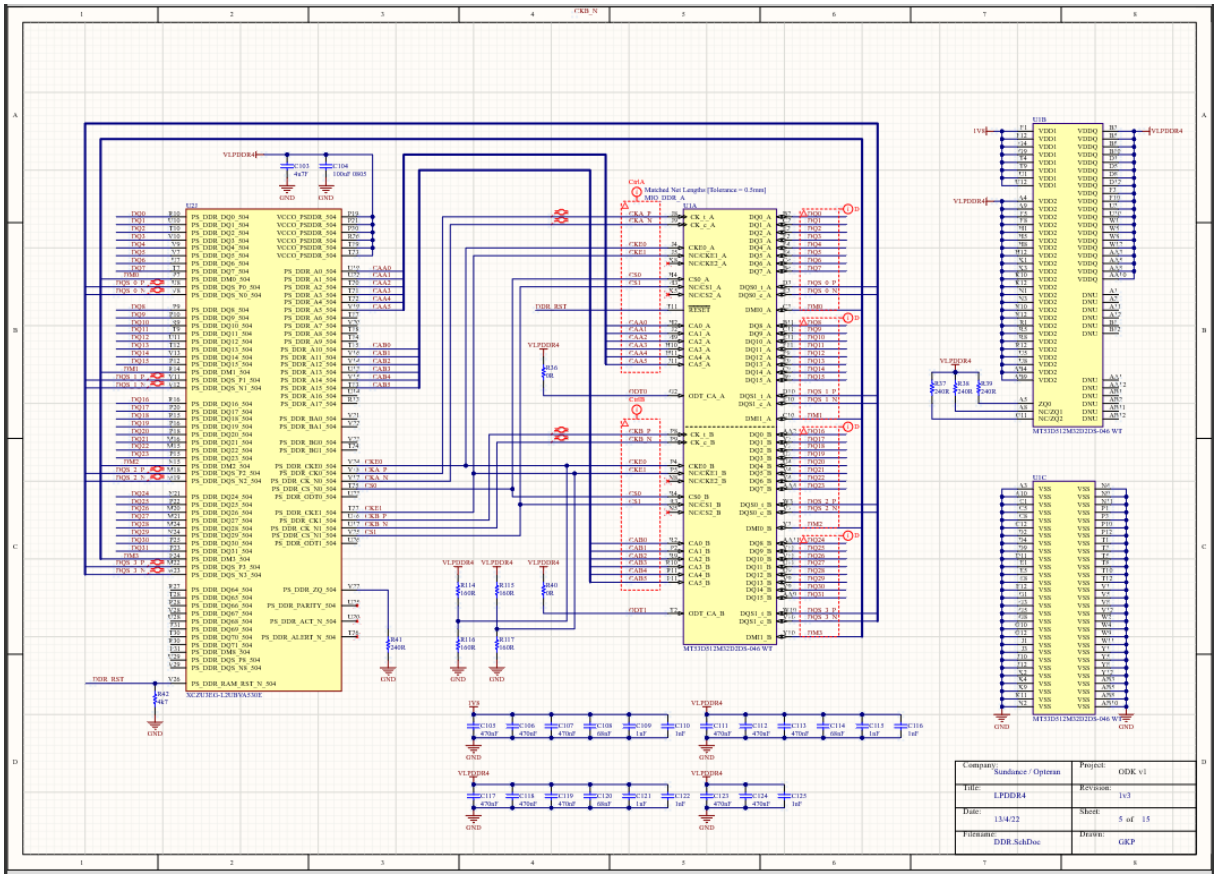
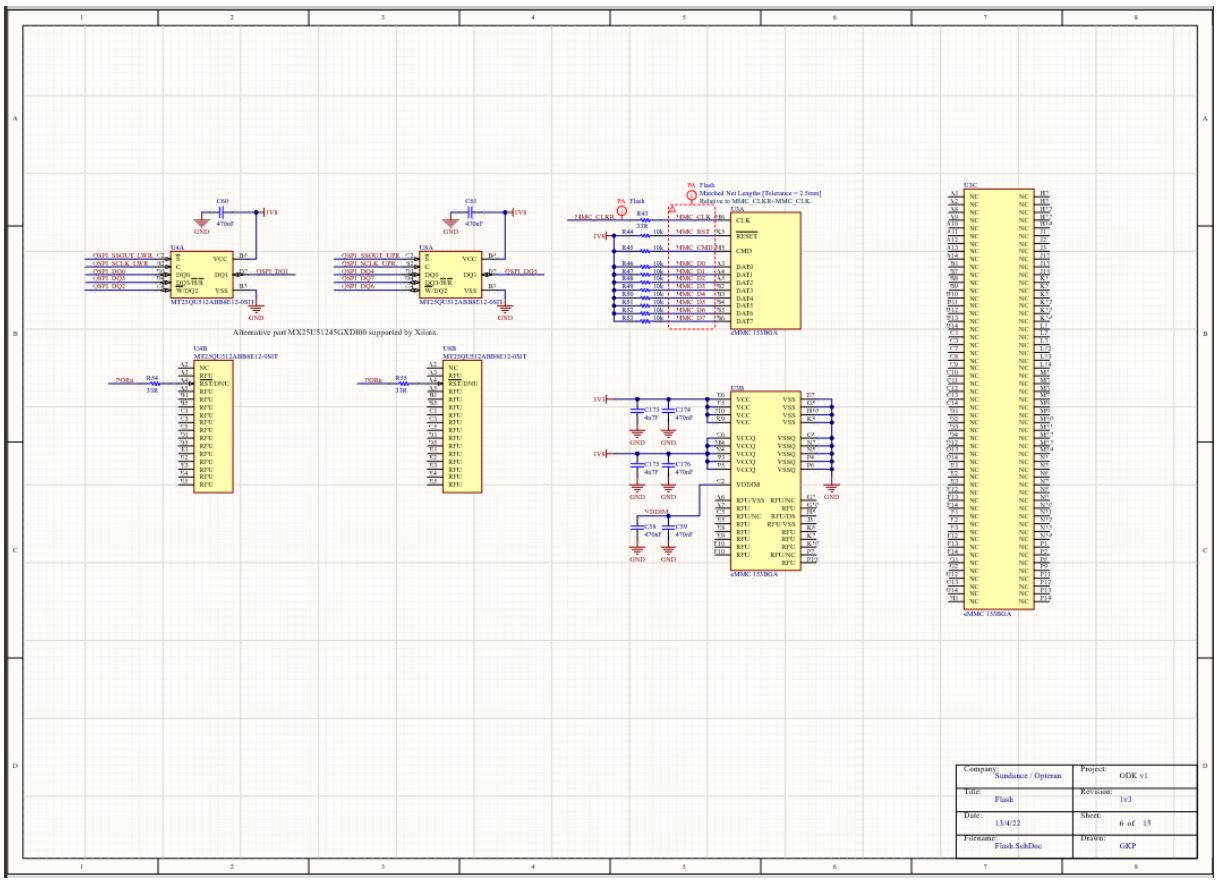
Drawn: GKP



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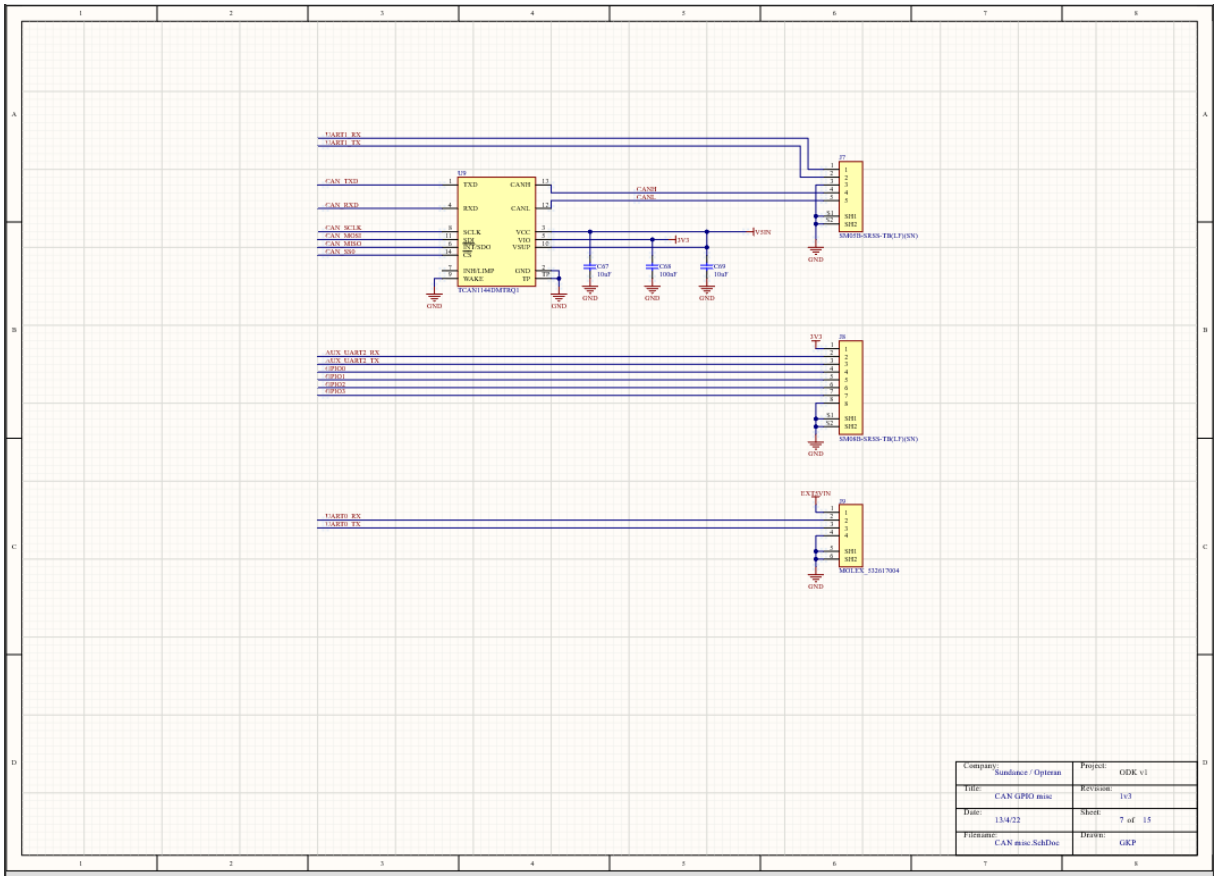
Revision: 1v3
Date: 13/4/22
Sheet: 6 of 15
Filename: Flash.SchDoc
Drawn: GKP


Company: Sundance / Opteran
Project: GDK v1
Title: CAN GPIO misc
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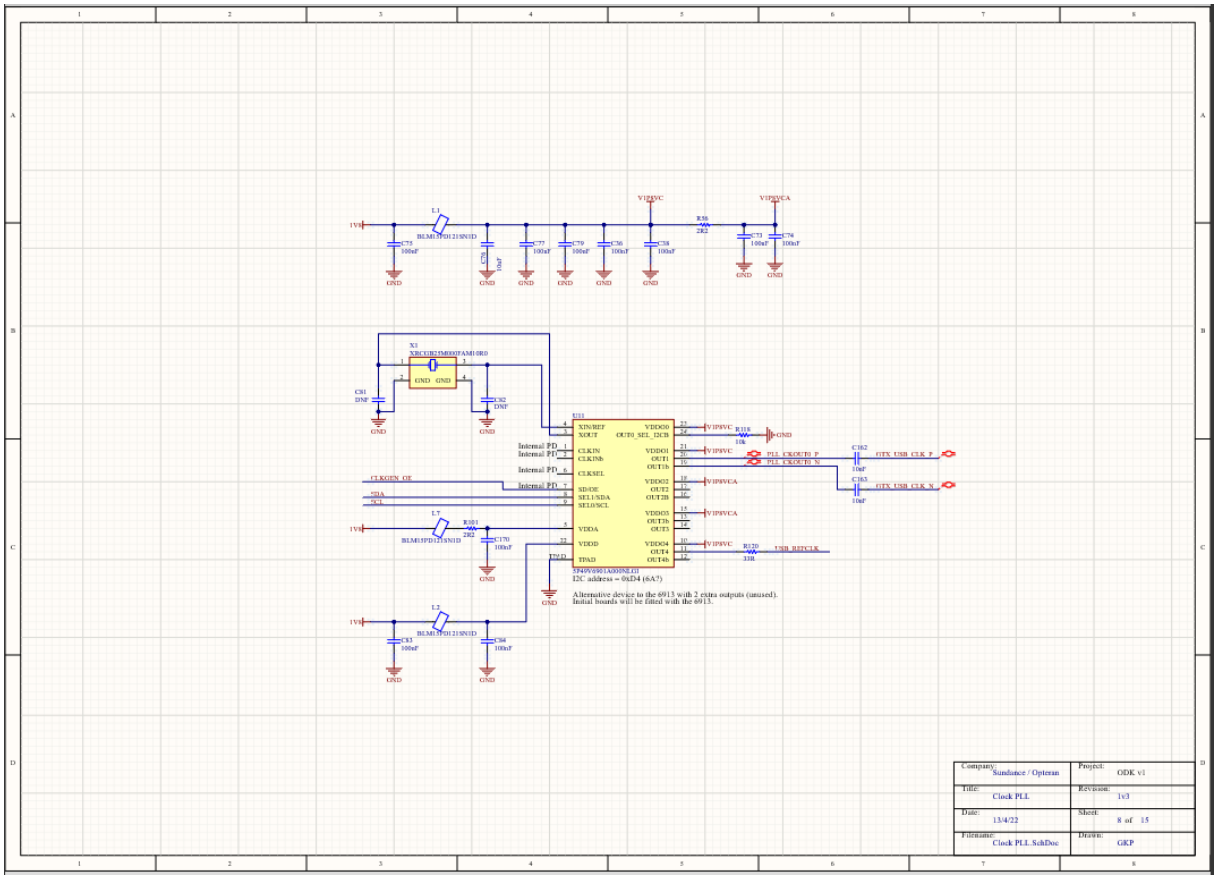
Date: 13/4/22
Sheet: 7 of 15
Filename: CAN misc.SchDoc
Drawn: GKP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Project: ODK v1
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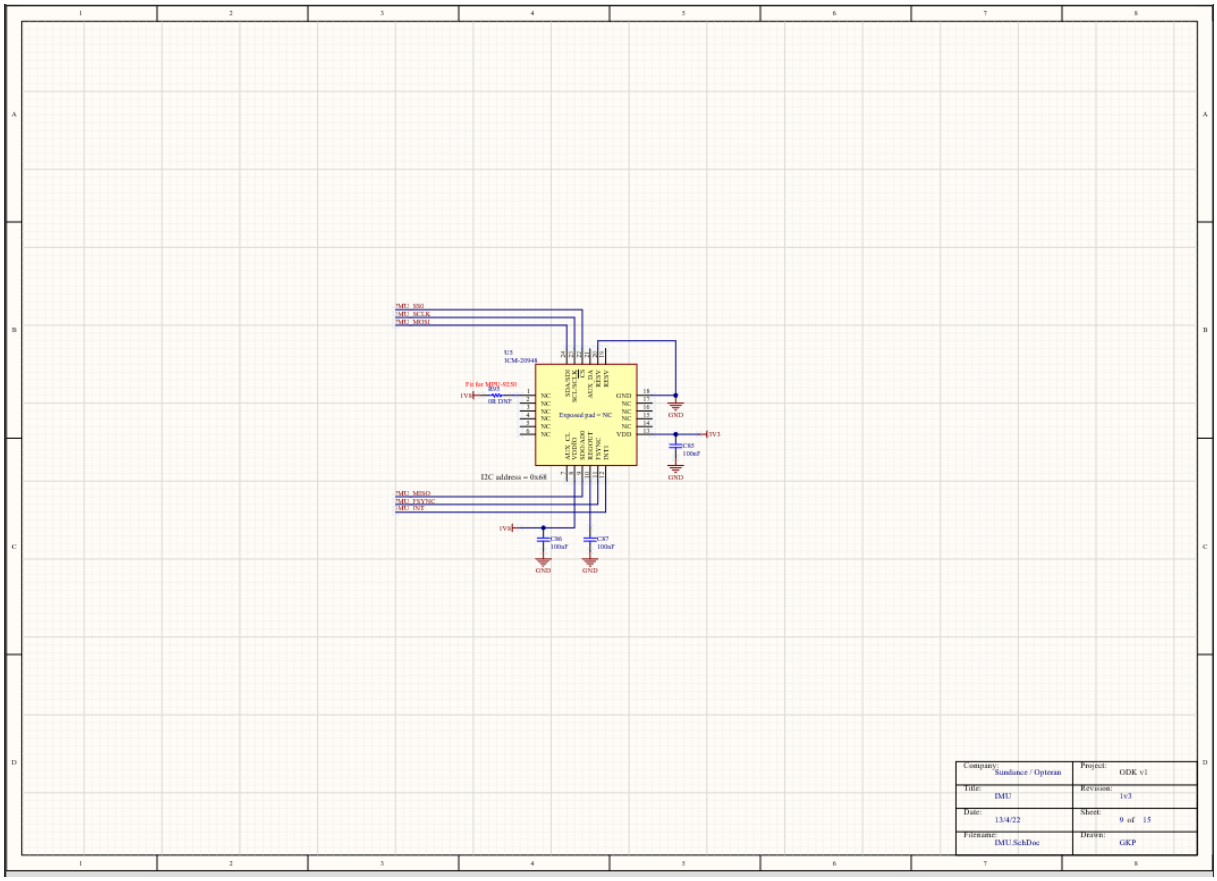
Date: 13/4/22
Sheet: 8 of 15
Filename: Clock PLL.SchDoc
Drawn: GKP


Company: Sundance / Opteran
Project: ODK v1
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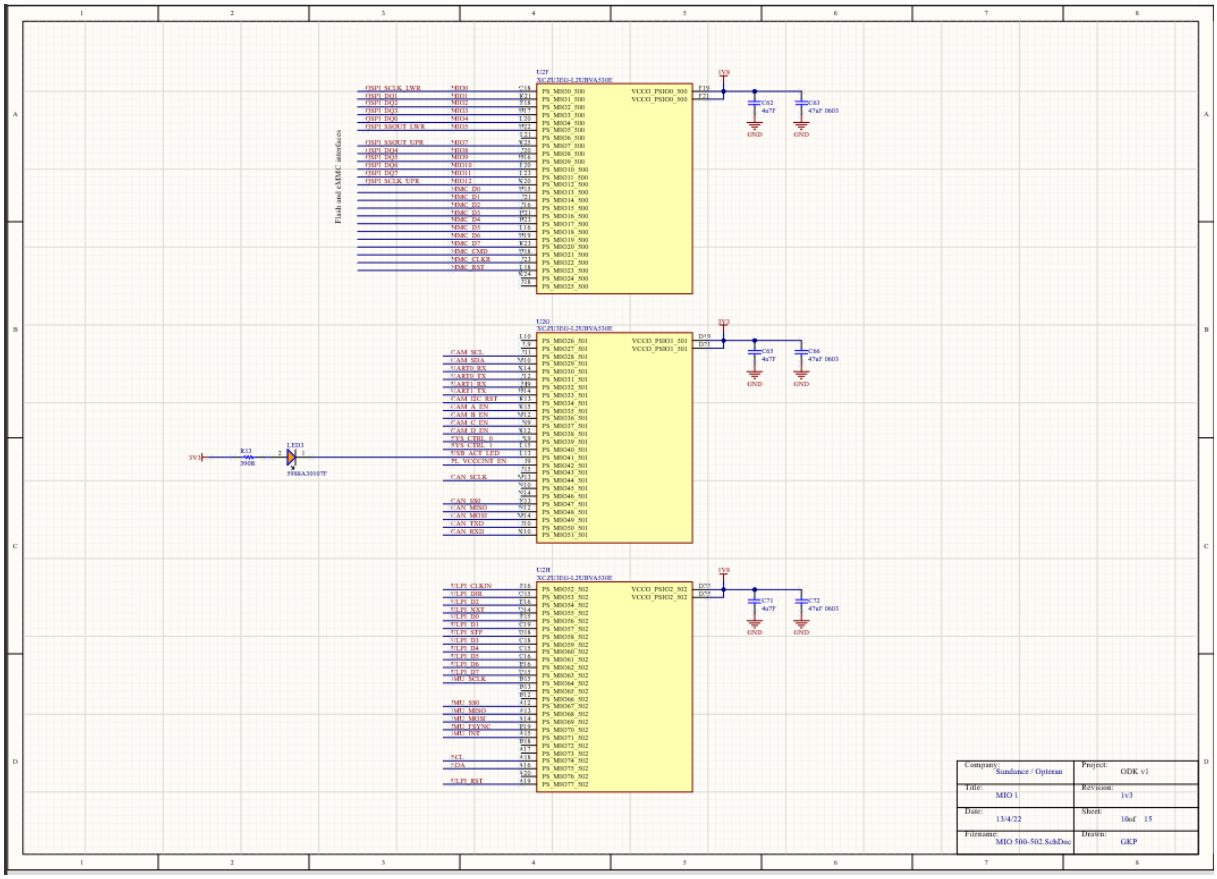
Drawn: GKP


Flash and eMMC interfaces
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Title: MIO 1
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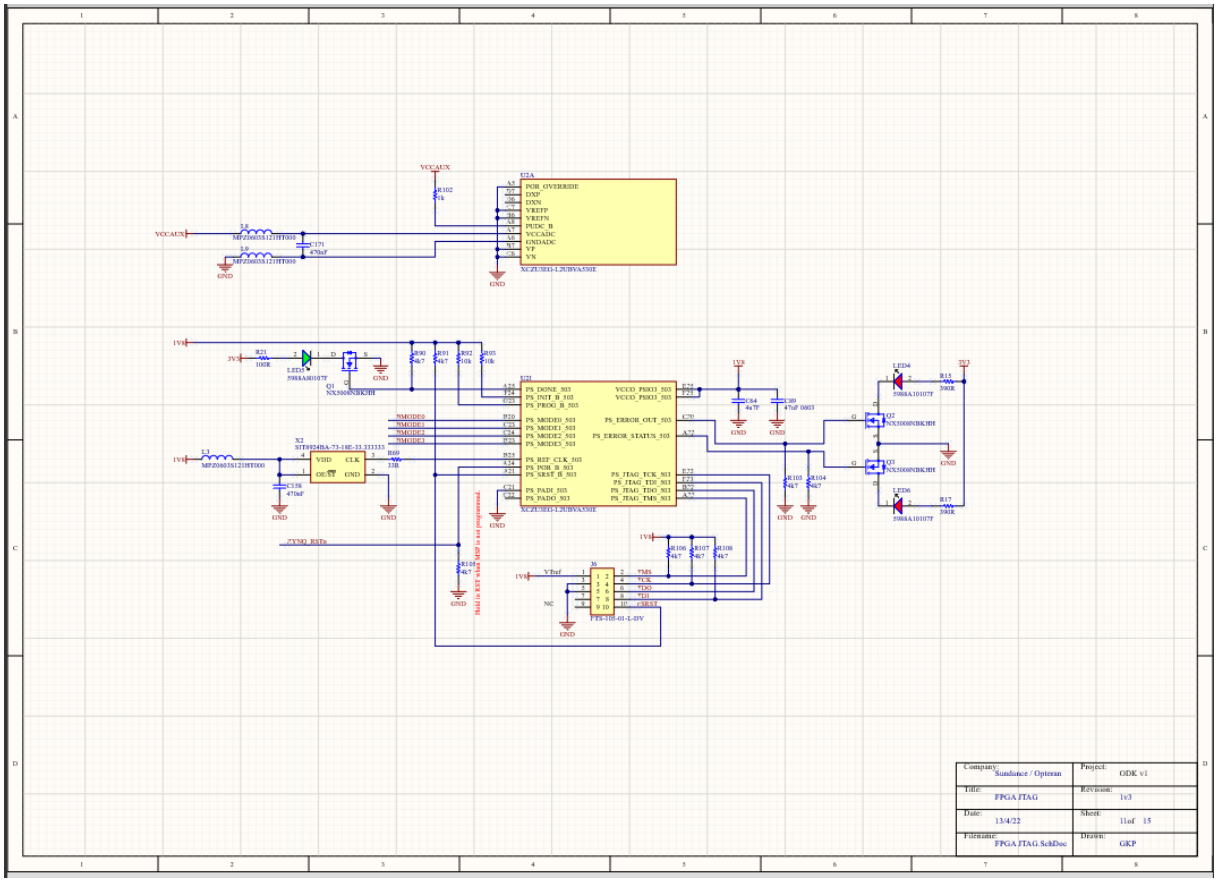
Sheet: 10of 15
Filename: MIO 500-502.SchDoc
Drawn: GKP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Project: ODK v1
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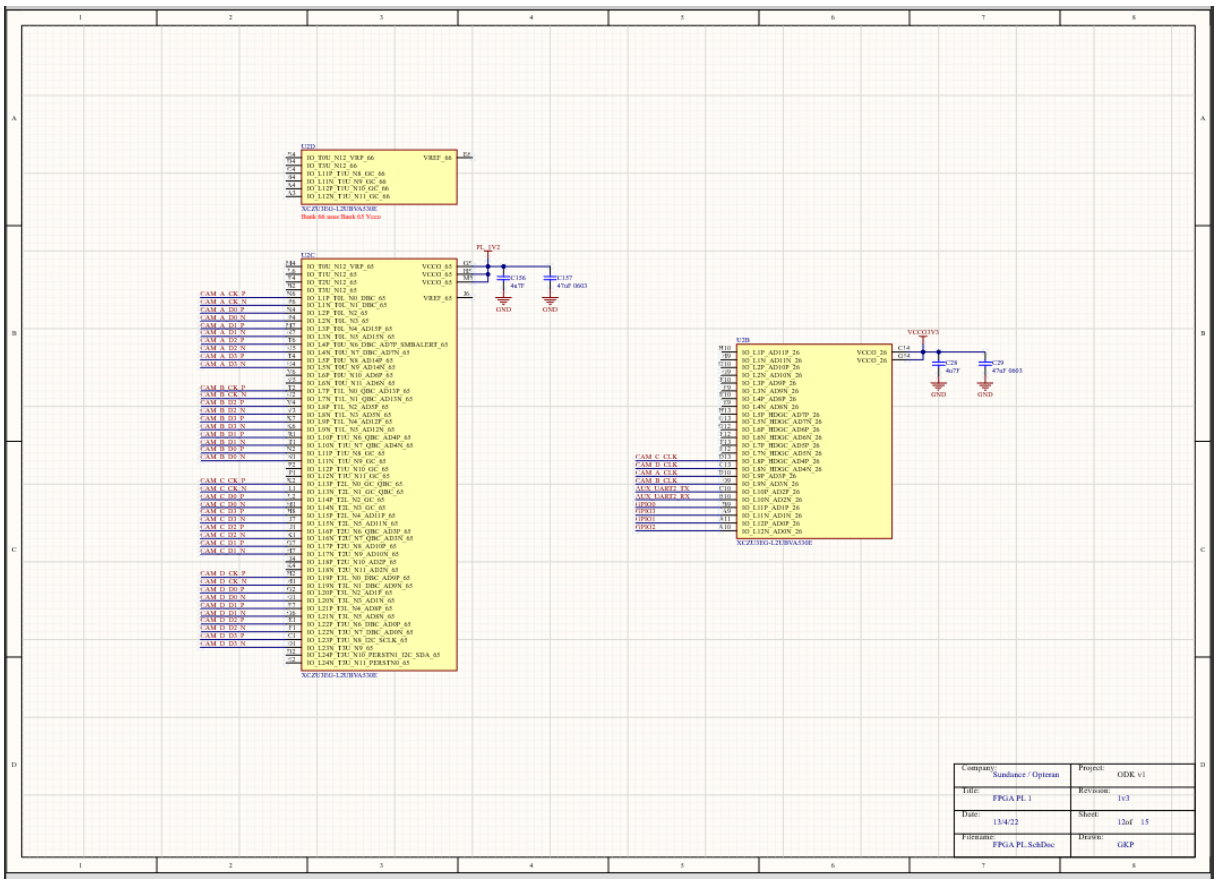
Filename: FPGA JTAG.SchDoc
Drawn: GKP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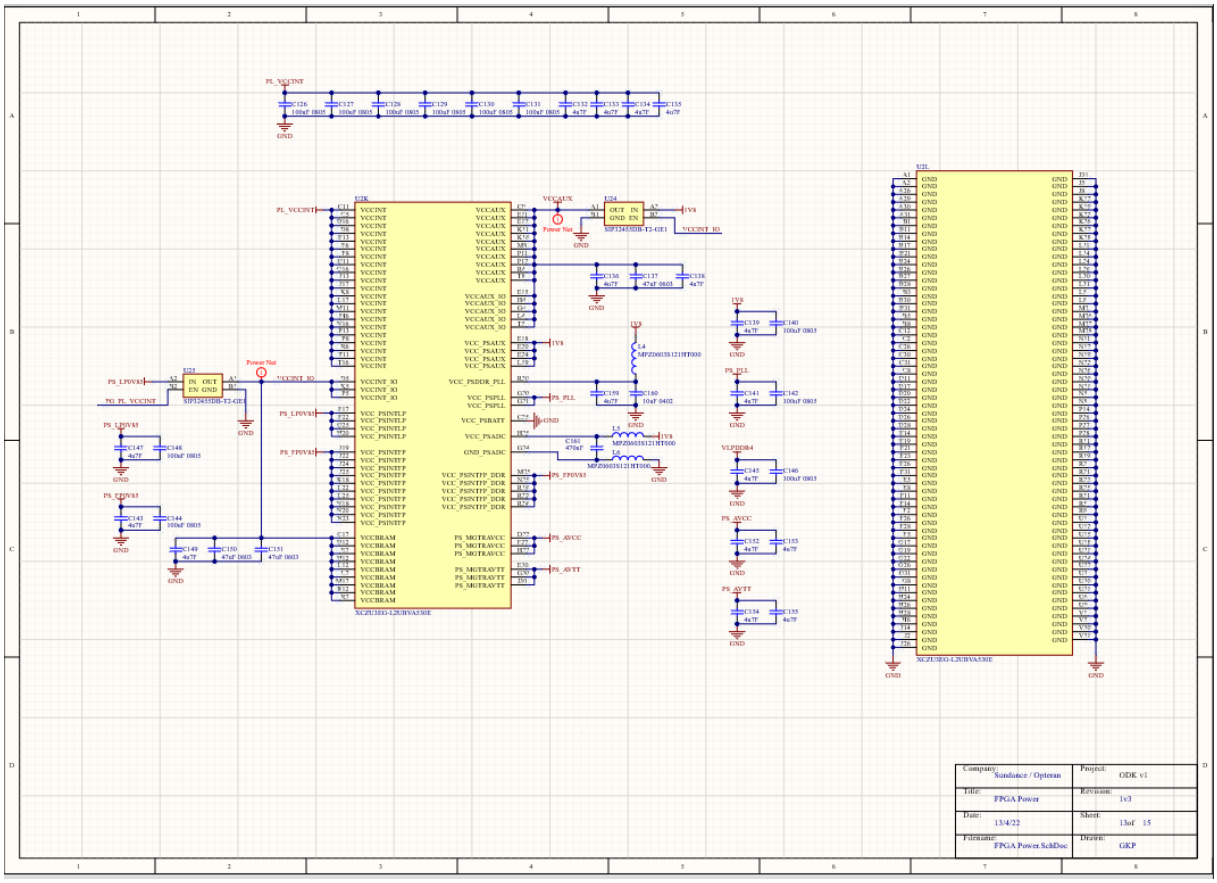
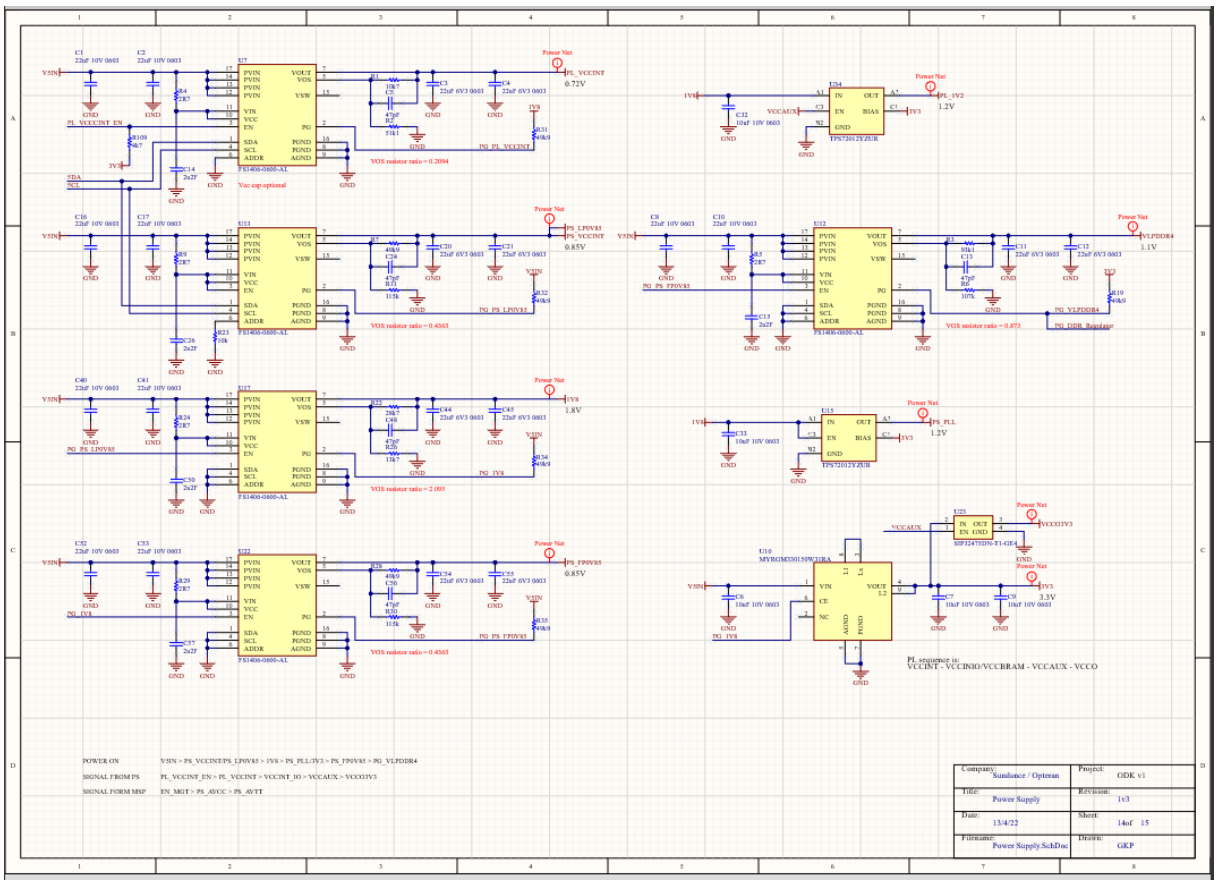
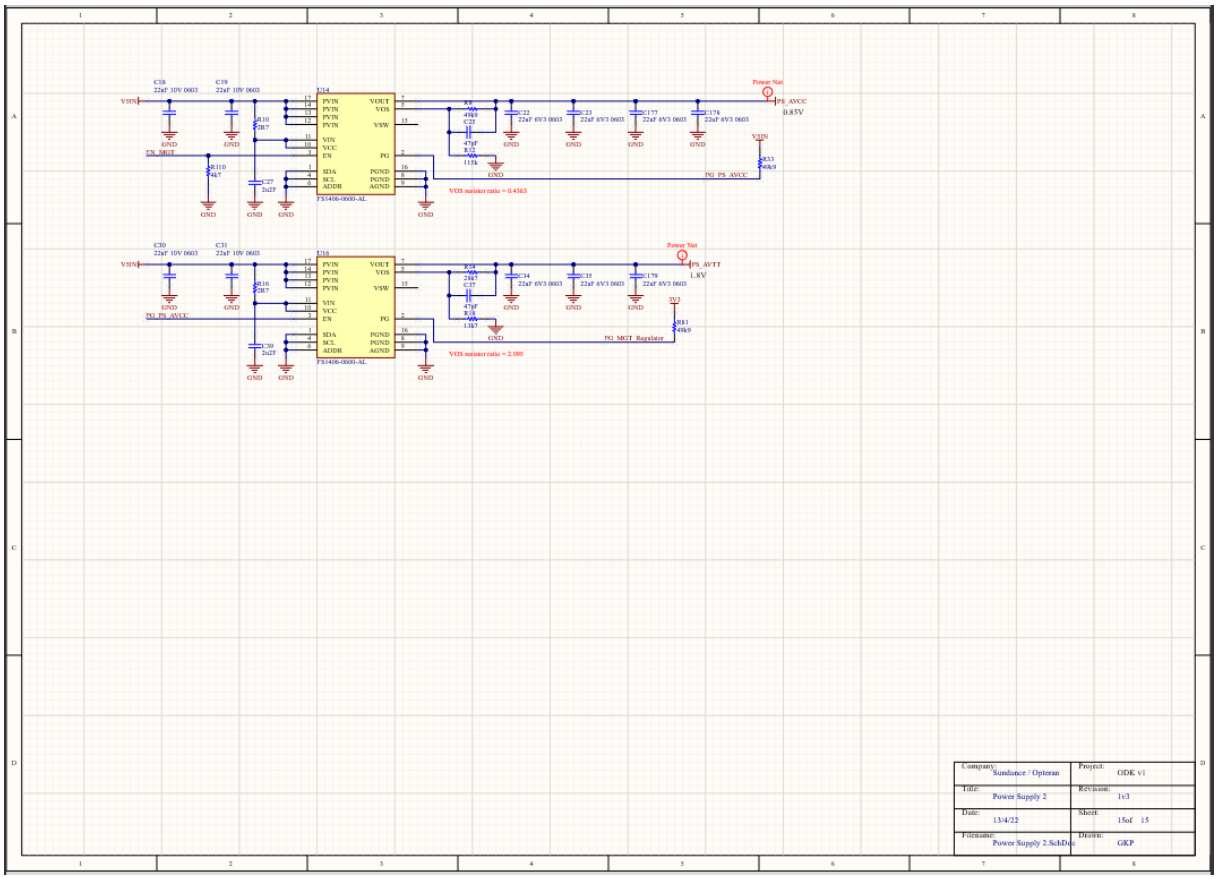
Project: ODK v1
Title: FPGA PL 1
Revision: 1v3
Date: 13/4/22
Sheet: 12of 15
Filename: FPGA PL.SchDoc
Drawn: GKP


Company: Sundance / Opteran
Project: ODK v1
Title: FPGA Power
Revision: 1v3
Date: 13/4/22
Sheet: 13of 15
Filename: FPGA Power.SchDoc
Drawn: GKP


POWER ON
VSIN > PS_VCCINT/PS_LPDVR5 > 1V8 > PS_PLL/3V3 > PS_FPDVR5 > PG_VLPDDR4
SIGNAL FROM PS
PL_VCCINT_EN > PL_VCCINT > VCCINT_IO > VCCAUX > VCCO3V3
SIGNAL FORM MSP
EN_MGT > PS_AVCC > PS_AVTT
PL sequence is:
VCCINT - VCCINIO/VCCBRAM - VCCAUX - VCCO
Company: Sundance / Opteran
Project: ODK v1
Title: Power Supply
Revision: 1v3
Date: 13/4/22
Sheet: 14of 15
Filename: Power Supply.SchDoc
Drawn: GKP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Project: ODK v1
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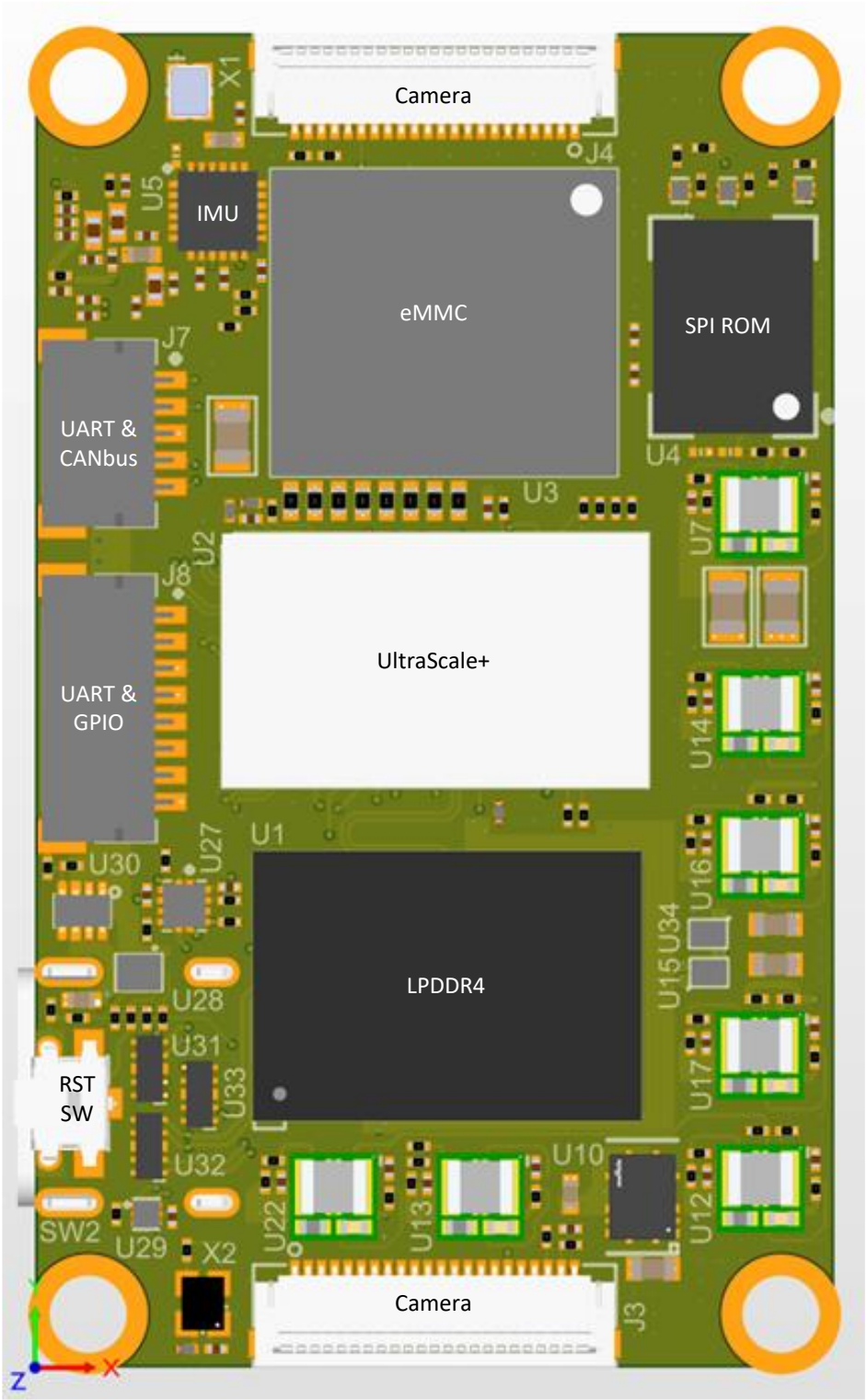
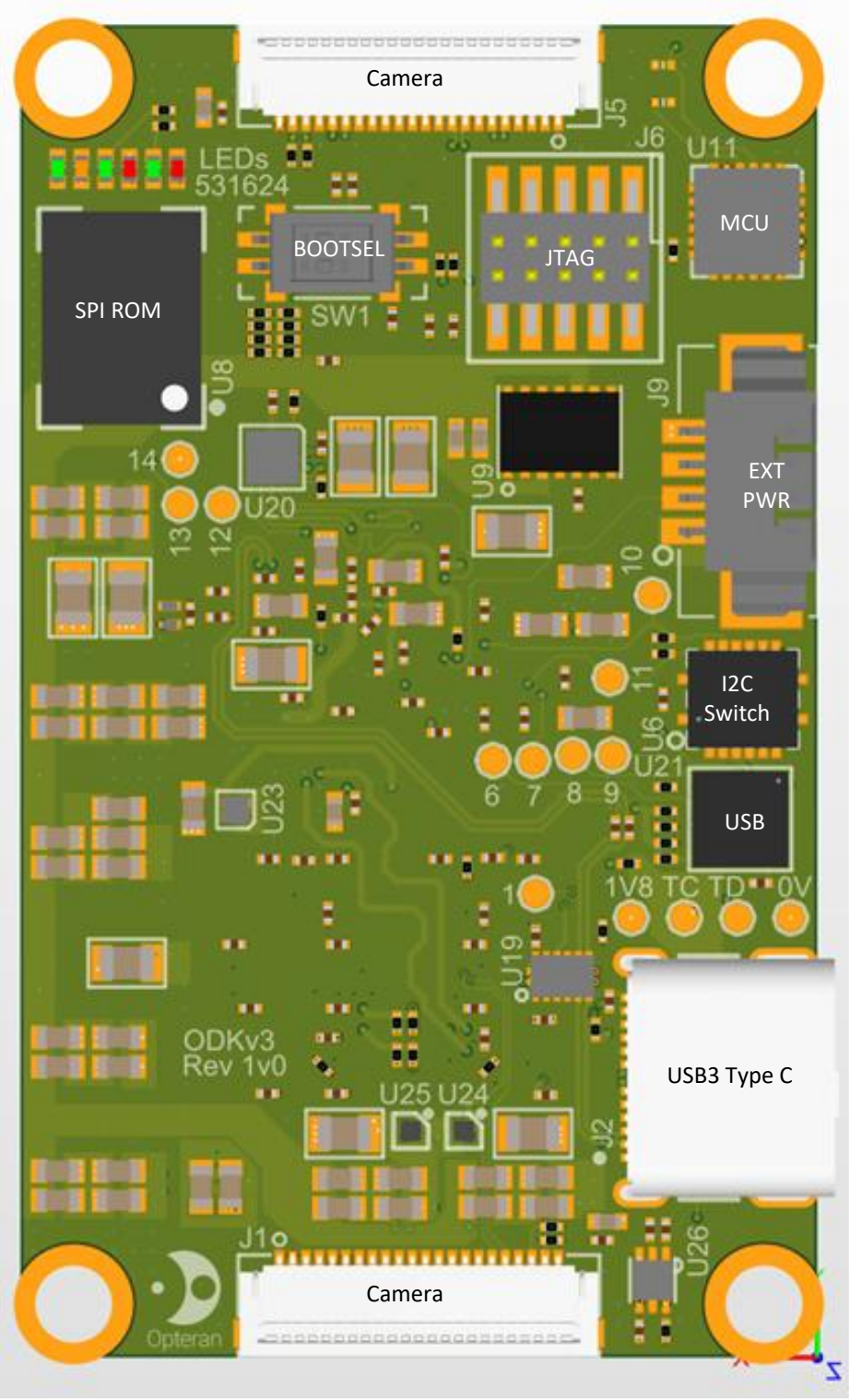
8 Footprint

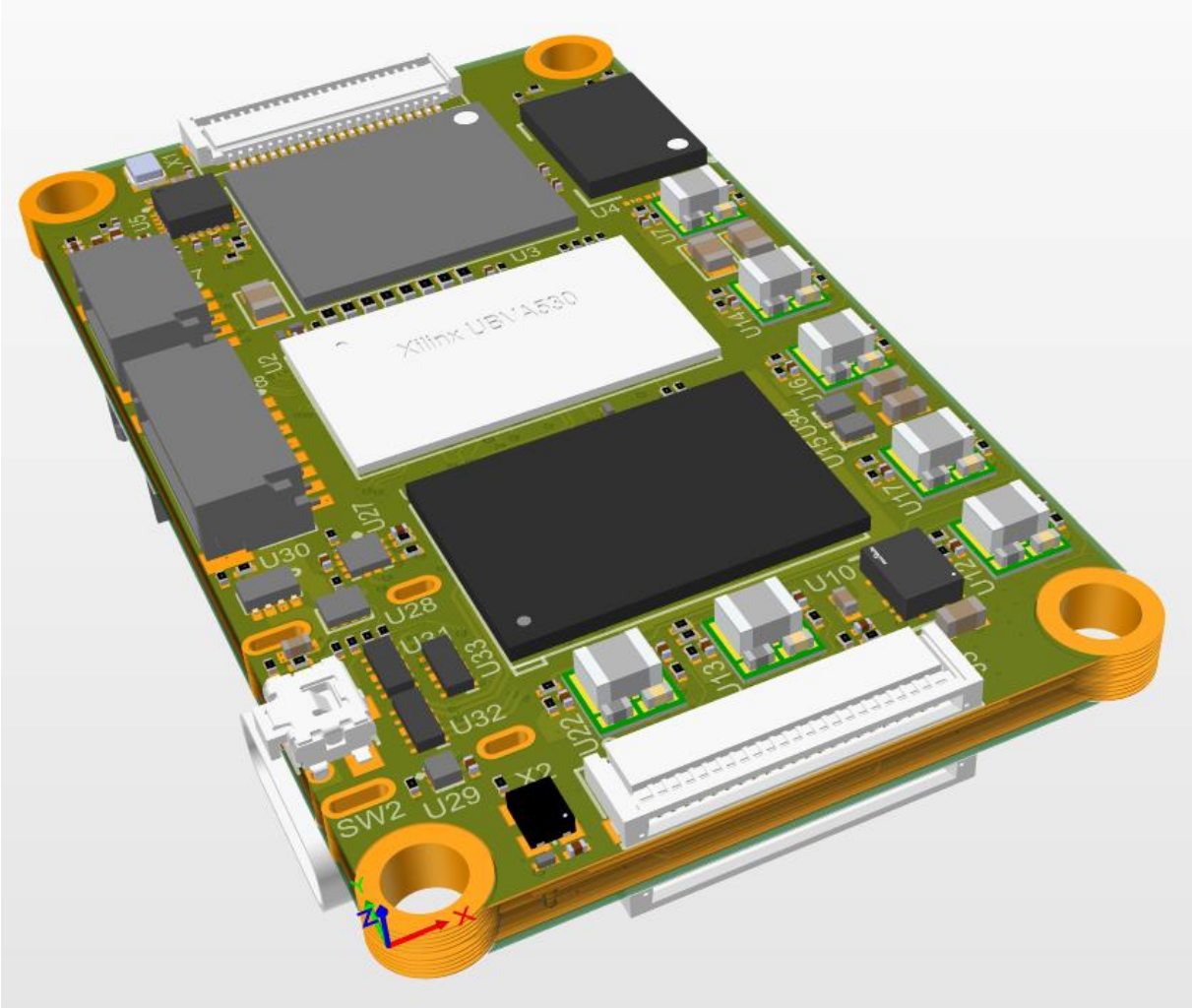
8.1 Top View



8.2 Bottom View



8.3 3D View



9 Device Pinouts

9.1 Zynq UltraScale+ Pinout

Following is the full pinout of the used pins of the Xilinx FPGA.

N4	IO_L2P_T0L_N2_65	mipi_cam0_data_p[0]
M7	IO_L3P_T0L_N4_AD15P_65	mipi_cam0_data_p[1]
T6	IO_L4P_T0U_N6_DBC_AD7P_SMBALERT_65	mipi_cam0_data_p[2]
T4	IO_L5P_T0U_N8_AD14P_65	mipi_cam0_data_p[3]
P4	IO_L2N_T0L_N3_65	mipi_cam0_data_n[0]
N7	IO_L3N_T0L_N5_AD15N_65	mipi_cam0_data_n[1]
U5	IO_L4N_T0U_N7_DBC_AD7N_65	mipi_cam0_data_n[2]
U4	IO_L5N_T0U_N9_AD14N_65	mipi_cam0_data_n[3]
V4	IO_L8P_T1L_N2_AD5P_65	mipi_cam1_data_p[0]
K7	IO_L9P_T1L_N4_AD12P_65	mipi_cam1_data_p[1]
R1	IO_L10P_T1U_N6_QBC_AD4P_65	mipi_cam1_data_p[2]
N2	IO_L11P_T1U_N8_GC_65	mipi_cam1_data_p[3]
V3	IO_L8N_T1L_N3_AD5N_65	mipi_cam1_data_n[0]
K6	IO_L9N_T1L_N5_AD12N_65	mipi_cam1_data_n[1]
T1	IO_L10N_T1U_N7_QBC_AD4N_65	mipi_cam1_data_n[2]
N1	IO_L11N_T1U_N9_GC_65	mipi_cam1_data_n[3]
L2	IO_L14P_T2L_N2_GC_65	mipi_cam2_data_p[0]
H8	IO_L15P_T2L_N4_AD11P_65	mipi_cam2_data_p[1]
J1	IO_L16P_T2U_N6_QBC_AD3P_65	mipi_cam2_data_p[2]
G7	IO_L17P_T2U_N8_AD10P_65	mipi_cam2_data_p[3]
M1	IO_L14N_T2L_N3_GC_65	mipi_cam2_data_n[0]
J7	IO_L15N_T2L_N5_AD11N_65	mipi_cam2_data_n[1]
K1	IO_L16N_T2U_N7_QBC_AD3N_65	mipi_cam2_data_n[2]
H7	IO_L17N_T2U_N9_AD10N_65	mipi_cam2_data_n[3]
G2	IO_L20P_T3L_N2_AD1P_65	mipi_cam3_data_p[0]
F7	IO_L21P_T3L_N4_AD8P_65	mipi_cam3_data_p[1]
E1	IO_L22P_T3U_N6_DBC_AD0P_65	mipi_cam3_data_p[2]
C1	IO_L23P_T3U_N8_I2C_SCLK_65	mipi_cam3_data_p[3]
G1	IO_L20N_T3L_N3_AD1N_65	mipi_cam3_data_n[0]
G6	IO_L21N_T3L_N5_AD8N_65	mipi_cam3_data_n[1]
F1	IO_L22N_T3U_N7_DBC_AD0N_65	mipi_cam3_data_n[2]
D1	IO_L23N_T3U_N9_65	mipi_cam3_data_n[3]
C13	IO_L8N_HDGC_AD4N_26	CAM_CLK[3]
D13	IO_L8P_HDGC_AD4P_26	CAM_CLK[2]
D9	IO_L9N_AD3N_26	CAM_CLK[1]
D10	IO_L9P_AD3P_26	CAM_CLK[0]

A9	IO_L11N_AD1N_26	AUX_GPIO_tri_io[3]
A10	IO_L12N_AD0N_26	AUX_GPIO_tri_io[2]
A11	IO_L12P_AD0P_26	AUX_GPIO_tri_io[1]
B9	IO_L11P_AD1P_26	AUX_GPIO_tri_io[0]
N6	IO_L1P_T0L_N0_DBC_65	mipi_cam0_clk_p
P6	IO_L1N_T0L_N1_DBC_65	mipi_cam0_clk_n
T2	IO_L7P_T1L_N0_QBC_AD13P_65	mipi_cam1_clk_p
U2	IO_L7N_T1L_N1_QBC_AD13N_65	mipi_cam1_clk_n
K2	IO_L13P_T2L_N0_GC_QBC_65	mipi_cam2_clk_p
L1	IO_L13N_T2L_N1_GC_QBC_65	mipi_cam2_clk_n
H2	IO_L19P_T3L_N0_DBC_AD9P_65	mipi_cam3_clk_p
H1	IO_L19N_T3L_N1_DBC_AD9N_65	mipi_cam3_clk_n
B10	IO_L10N_AD2N_26	AUX_UART2_rxd
C10	IO_L10P_AD2P_26	AUX_UART2_txd
L28	PS_MGTREFCLK2N_505	GTX_USB_CLK_N
L27	PS_MGTREFCLK2P_505	GTX_USB_CLK_P
F31	PS_MGTRRXN2_505	GTX_RX_N
F30	PS_MGTRRXP2_505	GTX_RX_P
C28	PS_MGTRTXN2_505	GTX_TX_N
C27	PS_MGTRTXP2_505	GTX_TX_P
G18	PS_MIO0_500	SCLK_OUT
F20	PS_MIO10_500	MO_UPPER_2
L23	PS_MIO11_500	MO_UPPER_3
K20	PS_MIO12_500	SCLK_OUT_UPPER
H15	PS_MIO13_500	DATA_OUT_0
J21	PS_MIO14_500	DATA_OUT_1
J16	PS_MIO15_500	DATA_OUT_2
H21	PS_MIO16_500	DATA_OUT_3
H23	PS_MIO17_500	DATA_OUT_4
L16	PS_MIO18_500	DATA_OUT_5
H19	PS_MIO19_500	DATA_OUT_6
K21	PS_MIO1_500	MISO_MO1
K23	PS_MIO20_500	DATA_OUT_7
H18	PS_MIO21_500	CMD_OUT
J23	PS_MIO22_500	CLK_OUT
L18	PS_MIO23_500	RESET / BUS_PWR
F18	PS_MIO2_500	MO2
H17	PS_MIO3_500	MO3
L20	PS_MIO4_500	MI0
H22	PS_MIO5_500	SS_OUT
L21	PS_MIO6_500	FEEDBACK
K25	PS_MIO7_500	SS_OUT_UPPER
J20	PS_MIO8_500	MO_UPPER_0
H16	PS_MIO9_500	MO_UPPER_1

J11	PS_MIO28_501	SCL_OUT
M10	PS_MIO29_501	SDA_OUT
K14	PS_MIO30_501	RX
J12	PS_MIO31_501	TX
M9	PS_MIO32_501	RX
H14	PS_MIO33_501	TX
K13	PS_MIO34_501	I2C1_RST
K15	PS_MIO35_501	CAM_EN_0
M12	PS_MIO36_501	CAM_EN_1
N9	PS_MIO37_501	CAM_EN_2
K12	PS_MIO38_501	CAM_EN_3
K9	PS_MIO39_501	SYS_CTRL_0
L15	PS_MIO40_501	SYS_CTRL_1
L13	PS_MIO41_501	USB_ACT_LED
J9	PS_MIO42_501	PL_VCCCINT_EN
M13	PS_MIO44_501	SCLK
N13	PS_MIO47_501	SS0
N12	PS_MIO48_501	MISO
M14	PS_MIO49_501	MOSI
J10	PS_MIO50_501	PHY_TX
K10	PS_MIO51_501	PHY_RX
F16	PS_MIO52_502	ULPI_CLK_IN
G15	PS_MIO53_502	ULPI_DIR
E16	PS_MIO54_502	ULPI_TX_DATA_2
D14	PS_MIO55_502	ULPI_NXT
F15	PS_MIO56_502	ULPI_TX_DATA_0
C19	PS_MIO57_502	ULPI_TX_DATA_1
D18	PS_MIO58_502	ULPI_STP
C18	PS_MIO59_502	ULPI_TX_DATA_3
C15	PS_MIO60_502	ULPI_TX_DATA_4
C16	PS_MIO61_502	ULPI_TX_DATA_5
B16	PS_MIO62_502	ULPI_TX_DATA_6
D15	PS_MIO63_502	ULPI_TX_DATA_7
B15	PS_MIO64_502	SCLK
A12	PS_MIO67_502	SS0
A13	PS_MIO68_502	MISO
A14	PS_MIO69_502	MOSI
B19	PS_MIO70_502	IMU_FSNC
A15	PS_MIO71_502	IMU_INT
A18	PS_MIO74_502	SCL
A16	PS_MIO75_502	SDA
A19	PS_MIO77_502	ULPI_RST
A25	PS_DONE_503	PS_DONE_503
C20	PS_ERROR_OUT_503	PS_ERROR_OUT_503

A22	PS_ERROR_STATUS_503	PS_ERROR_STATUS_503
F24	PS_INIT_B_503	PS_INIT_B_503
E22	PS_JTAG_TCK_503	PS_JTAG_TCK_503
F23	PS_JTAG_TDI_503	PS_JTAG_TDI_503
B22	PS_JTAG_TDO_503	PS_JTAG_TDO_503
A23	PS_JTAG_TMS_503	PS_JTAG_TMS_503
B20	PS_MODE0_503	PS_MODE0_503
C23	PS_MODE1_503	PS_MODE1_503
C24	PS_MODE2_503	PS_MODE2_503
B23	PS_MODE3_503	PS_MODE3_503
A24	PS_POR_B_503	PS_POR_B_503
G23	PS_PROG_B_503	PS_PROG_B_503
B25	PS_REF_CLK_503	PS_REF_CLK_503
A21	PS_SRST_B_503	PS_SRST_B_503
U19	PS_DDR_A0_504	PS_DDR_A0_504
T15	PS_DDR_A10_504	PS_DDR_A10_504
V16	PS_DDR_A11_504	PS_DDR_A11_504
V14	PS_DDR_A12_504	PS_DDR_A12_504
U13	PS_DDR_A13_504	PS_DDR_A13_504
V15	PS_DDR_A14_504	PS_DDR_A14_504
T13	PS_DDR_A15_504	PS_DDR_A15_504
U14	PS_DDR_A16_504	PS_DDR_A16_504
R13	PS_DDR_A17_504	PS_DDR_A17_504
U22	PS_DDR_A1_504	PS_DDR_A1_504
T20	PS_DDR_A2_504	PS_DDR_A2_504
T21	PS_DDR_A3_504	PS_DDR_A3_504
T22	PS_DDR_A4_504	PS_DDR_A4_504
V19	PS_DDR_A5_504	PS_DDR_A5_504
T17	PS_DDR_A6_504	PS_DDR_A6_504
V20	PS_DDR_A7_504	PS_DDR_A7_504
T18	PS_DDR_A8_504	PS_DDR_A8_504
T14	PS_DDR_A9_504	PS_DDR_A9_504
U20	PS_DDR_ACT_N_504	PS_DDR_ACT_N_504
T26	PS_DDR_ALERT_N_504	PS_DDR_ALERT_N_504
V21	PS_DDR_BA0_504	PS_DDR_BA0_504
V22	PS_DDR_BA1_504	PS_DDR_BA1_504
V23	PS_DDR_BG0_504	PS_DDR_BG0_504
T24	PS_DDR_BG1_504	PS_DDR_BG1_504
V18	PS_DDR_CK0_504	PS_DDR_CK0_504
U16	PS_DDR_CK1_504	PS_DDR_CK1_504
V24	PS_DDR_CKE0_504	PS_DDR_CKE0_504
T27	PS_DDR_CKE1_504	PS_DDR_CKE1_504
V17	PS_DDR_CK_N0_504	PS_DDR_CK_N0_504
U17	PS_DDR_CK_N1_504	PS_DDR_CK_N1_504

T25	PS_DDR_CS_N0_504	PS_DDR_CS_N0_504
V25	PS_DDR_CS_N1_504	PS_DDR_CS_N1_504
P7	PS_DDR_DM0_504	PS_DDR_DM0_504
R14	PS_DDR_DM1_504	PS_DDR_DM1_504
N15	PS_DDR_DM2_504	PS_DDR_DM2_504
P24	PS_DDR_DM3_504	PS_DDR_DM3_504
P31	PS_DDR_DM8_504	PS_DDR_DM8_504
R10	PS_DDR_DQ0_504	PS_DDR_DQ0_504
R9	PS_DDR_DQ10_504	PS_DDR_DQ10_504
T9	PS_DDR_DQ11_504	PS_DDR_DQ11_504
U11	PS_DDR_DQ12_504	PS_DDR_DQ12_504
T12	PS_DDR_DQ13_504	PS_DDR_DQ13_504
V13	PS_DDR_DQ14_504	PS_DDR_DQ14_504
P12	PS_DDR_DQ15_504	PS_DDR_DQ15_504
R16	PS_DDR_DQ16_504	PS_DDR_DQ16_504
P20	PS_DDR_DQ17_504	PS_DDR_DQ17_504
R15	PS_DDR_DQ18_504	PS_DDR_DQ18_504
P16	PS_DDR_DQ19_504	PS_DDR_DQ19_504
U10	PS_DDR_DQ1_504	PS_DDR_DQ1_504
P18	PS_DDR_DQ20_504	PS_DDR_DQ20_504
M16	PS_DDR_DQ21_504	PS_DDR_DQ21_504
M15	PS_DDR_DQ22_504	PS_DDR_DQ22_504
P15	PS_DDR_DQ23_504	PS_DDR_DQ23_504
N21	PS_DDR_DQ24_504	PS_DDR_DQ24_504
P22	PS_DDR_DQ25_504	PS_DDR_DQ25_504
M20	PS_DDR_DQ26_504	PS_DDR_DQ26_504
M21	PS_DDR_DQ27_504	PS_DDR_DQ27_504
M24	PS_DDR_DQ28_504	PS_DDR_DQ28_504
N24	PS_DDR_DQ29_504	PS_DDR_DQ29_504
T10	PS_DDR_DQ2_504	PS_DDR_DQ2_504
P25	PS_DDR_DQ30_504	PS_DDR_DQ30_504
P23	PS_DDR_DQ31_504	PS_DDR_DQ31_504
V10	PS_DDR_DQ3_504	PS_DDR_DQ3_504
V9	PS_DDR_DQ4_504	PS_DDR_DQ4_504
V7	PS_DDR_DQ5_504	PS_DDR_DQ5_504
R27	PS_DDR_DQ64_504	PS_DDR_DQ64_504
T28	PS_DDR_DQ65_504	PS_DDR_DQ65_504
R28	PS_DDR_DQ66_504	PS_DDR_DQ66_504
V28	PS_DDR_DQ67_504	PS_DDR_DQ67_504
U28	PS_DDR_DQ68_504	PS_DDR_DQ68_504
T31	PS_DDR_DQ69_504	PS_DDR_DQ69_504
U7	PS_DDR_DQ6_504	PS_DDR_DQ6_504
T30	PS_DDR_DQ70_504	PS_DDR_DQ70_504
R30	PS_DDR_DQ71_504	PS_DDR_DQ71_504

T7	PS_DDR_DQ7_504	PS_DDR_DQ7_504
P9	PS_DDR_DQ8_504	PS_DDR_DQ8_504
P10	PS_DDR_DQ9_504	PS_DDR_DQ9_504
V8	PS_DDR_DQS_N0_504	PS_DDR_DQS_N0_504
V12	PS_DDR_DQS_N1_504	PS_DDR_DQS_N1_504
M19	PS_DDR_DQS_N2_504	PS_DDR_DQS_N2_504
M23	PS_DDR_DQS_N3_504	PS_DDR_DQS_N3_504
V29	PS_DDR_DQS_N8_504	PS_DDR_DQS_N8_504
U8	PS_DDR_DQS_P0_504	PS_DDR_DQS_P0_504
V11	PS_DDR_DQS_P1_504	PS_DDR_DQS_P1_504
M18	PS_DDR_DQS_P2_504	PS_DDR_DQS_P2_504
M22	PS_DDR_DQS_P3_504	PS_DDR_DQS_P3_504
U29	PS_DDR_DQS_P8_504	PS_DDR_DQS_P8_504
U23	PS_DDR_ODT0_504	PS_DDR_ODT0_504
U26	PS_DDR_ODT1_504	PS_DDR_ODT1_504
U25	PS_DDR_PARITY_504	PS_DDR_PARITY_504
V26	PS_DDR_RAM_RST_N_504	PS_DDR_RAM_RST_N_504
V27	PS_DDR_ZQ_504	PS_DDR_ZQ_504

9.2 MCU Pinout

Function/Signal	Port	Pin	Comment
SYS_CTRL_0	P6.7	A3	To Zynq.
SYS_CTRL_1	P5.1	A4	To Zynq.
EN_MGT	P5.5	A6	Active high MGT power enable.
BOOT_MODE_LED	PJ.1	C1	High to illuminate LED2.
PGOOD LED	P6.0	C2	High to illuminate LED1.
CON_DET	P6.6	C4	Active high USB connection detect.
RESET_IN#	P1.4	C5	Active low reset input from supervisor.
EXT_TO_TYC_SW_EN	P1.3	C6	Active high EXT5V to USB VBUS enable.
BOOTSEL0	P1.1	C7	From DIP SW.
BOOTSEL1	P1.2	C8	From DIP SW.
PG_DDR_REG	P5.3	D1	Active low pwr good from LPDDR4 DCDC.
PG_MGT_REG	PJ.0	D2	Active low pwr good from PS_AVTT DCDC.
SBWTDIO	-	D4	Programming data pin.
RST/NMI	-	E3	Pull-up.
SBWTCK	-	E4	Programming clock pin.
BMODE3	P7.3	G1	Zynq boot mode.
ZYNQ_RST#	P7.1	G2	Active low Zynq reset.
SCL	P3.1	G7	Primary I2C bus clock.
BMODE2	P7.0	H1	Zynq boot mode.
BMODE1	P4.6	H2	Zynq boot mode.
BMODE0	P4.4	H3	Zynq boot mode.
CLKGEN_OE	P4.1	H4	Active high PLL output enable.
SDA	P3.0	H8	Primary I2C bus data.

10 Connector Pinouts

10.1 Camera

Pin	Function
1	GND
2	D0_N
3	D0_P
4	GND
5	D1_N
6	D1_P
7	GND
8	CK_N
9	CK_P
10	GND
11	D2_N
12	D2_P
13	GND
14	D3_N
15	D3_P
16	GND
17	EN
18	CLK (2.8V)
19	GND
20	SCL
21	SDA
22	3.3V

10.2 CAN Bus (UART1)

Pin	Function
1	RX
2	TX
3	GND
4	CAN H
5	CAN L

10.3 GPIO (UART2)

Pin	Function
1	3.3V
2	RX
3	TX
4	GPIO0
5	GPIO1
6	GPIO2
7	GPIO3
8	GND

10.4 External Power (UART0)

Pin	Function
1	EXT 5V IN
2	RX
3	TX
4	GND

10.5 JTAG

Function	Pin	Pin	Function
VTref	1	2	TMS
GND	3	4	TCK
GND	5	6	TDO
NC	7	8	TDI
NC	9	10	/SRST

11 Physical Properties

Dimensions	50mm x 30mm
Weight	TBA.
Supply Voltage	+5V ±5%
Supply Current	3A max.
MTBF	

12 Safety

This module presents no hazard to the user when in normal use, unless it's in a drone and flies into your face!

13 EMC

This module is designed to operate from within an enclosed host system, which is built to provide EMC shielding. Operation within the UK/EU EMC guidelines is not guaranteed unless it is installed within an adequate host system.

This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the output cables.

Short circuiting any output to ground does not cause a host PC system to lock up or reboot.

14 Ordering Information

Part number: VCS-3

15 Compliance Matrix

Feature	Spec Reference	Implementation
UltraScale+	4.3.1	U2, XCZU3EG-UBVA530.
LPDDR4	4.3.2	U1, MT53D512M32D.
eMMC	4.3.3	U3.
SPI ROM	4.3.4	U4 & U8, MT25QU512A.
Camera FPC	4.3.5	J1, 3, 4 & 5. I2C U6, PCA9546A.
IMU	4.3.6	U5, ICM-20948.
UART	4.3.7	J7, J8 & J9.
GPIO	4.3.8	J8.
CAN Bus	4.3.9	U9, TCAN1144D. J7.
USB	4.3.10	U2 (GTX), U20, USB3321C.
Power supply	4.3.11	U7, 13, 17, 22, 34, 15, 10, 23, 14, 16, 24 & 25.
Clocks	4.3.12	X1, U11, 5P49V6901, X2.
MCU / Booting	4.3.13	SW2, U26, SW1, U21, MSP430F5229.
LEDs	4.3.14	LED1-6.
Test Points	4.3.15	As described.