MCC150-Implementation of Digital Signal Processing
Lab 2: BPSK Transceiver

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I. INTRODUCTION

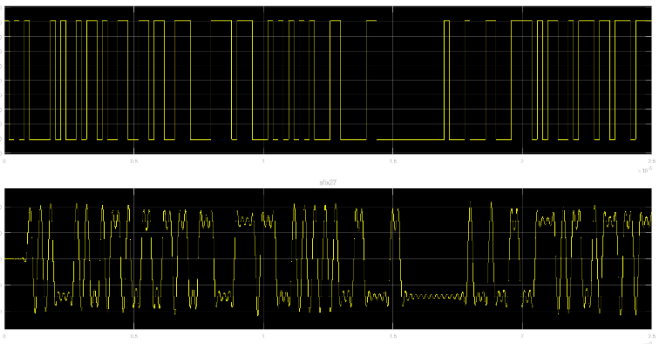
The RF transmitter which was built in lab 1 is expanded for improvement by adding a root-raise cosine (RRC) pulse shaping filter. A simple receiver with a matched filter and a simple symbol timing recovery (STR) unit is also built alongside. The DSP architecture is built using Simulink and hardware is generated in VHDL. The model is built and then examined and synthesized using Quartus prime.

II. DSP BUILDER MODEL

The subsystems used in the building of the transmitter part of the transceiver are a PRBS Generator which generates Pseudo Random Binary Sequence or bitstream which is the data to be transmitted. The output of the Sequence Generator is then passed through a modulator. The modulator fuses the input signal with a carrier signal which is produced by the Local Oscillator. The output of the modulator is scaled and added below. The *Interpolating FIR* block increases the sampling frequency of the input signal. A *Scale* block is the added to the output of the *interpolating FIR* in order to reduce the precision which can perform rounding and saturation to provide the required output precision. The display resources block is also added to view the utilization of resources. A Control block is set up to generate the HDL code which can be used for synthesis. In the control block, generation options and clock frequency can be specified. The bandwidth used in real time communication systems is limited. Also, a square wave shaped is hard to be transmitted since its bandwidth is infinite. Hence, a low pass filter can be used to limit the bandwidth of the signal which converts the shape of the signal which will no longer be a square. Hence it is called as a pulse shaping filter. It has a longer time domain response. The Finite Impulse Response filter is a type of digital filter used for digital signal processing. The main purpose of this filter is signal conditioning. Some examples are phone line. These frequencies are limited in such a way that it cannot be heard by human beings (very low frequencies). The middle point of each pulse is the best sampling point with no Inter-Symbol Interference. The process of looking for the best sampling points is called symbol time recovery (STR). It is mandatory for every primitive subsystem to have a *Channel in* and *Channel out* block to mark the boundary of the system. Additionally, a *synthesis info* block is also required to achieve pipelining (to achieve higher clock frequency) and latency (to assume zero latency). Also, delays are added to the subsystems whenever needed to meet the clock frequency target.

3.1 Reflection Questions:

1. The below plot represents the input and output of the FIR filter.



The output of the FIR matches with the input but with a phase offset and bandwidth limitation. The latency is due to the addition of lowpass filter which limits the bandwidth. The value of delay is found to be 778ns.

2. Two 12 bit samples are multiplied which becomes 24 bits and then when upsampled by the *FIR* filter, the extra coefficients are considered and the output becomes 27 bits.

3. The input signal is left shifted by -1 using the *scale* block in order to prevent clipping of the signal as it goes beyond the limits and to prevent excess bits and overflow.

III. RECEIVER ARCHITECTURE

The receiver is built by adding a pulse shaping filter and a Symbol Timing Recovery unit. The *decimation* block is added to the *single rate FIR* filter. Decimation is nothing but down sampling of the signal (sample rate reduction) which is usually done to reduce the complexity in computation.

3.2 Reflection Questions:

1. Channel delay value should be maintained so that it is not outside the designer's control. The sample index has been set to 4 to find the best sampling point.

2. Clipping should be prevented which can be done by left shifting the signal using the *scale* block. Because we also

should be able to utilize as much of the 12 bit wordlength as much as possible.

IV. SYNTHESIS AND VERIFICATION IN QUARTUS PRIME

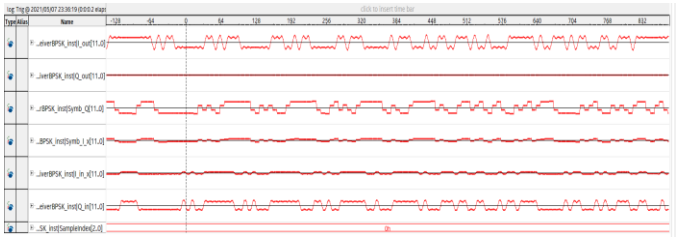
The HDL code of the transmitter which is generated using the DSP builder is loaded into Quartus prime for hardware synthesis. Symbol files are created for the transmitter and then the updated transceiver block is connected to the AD9361 controller. Then the design is compiled, and the compilation report is studied for design utilization, timing results and other design statistics.

V. IN-SYSTEM SOURCES AND PROBES

The In-system sources and probes editor facilitates us to control the internal FPGA signals from Quartus Prime. The *Altera In-System Sources & Probes* IP block is then added and renamed to *Debug source* which works as a signal source and as a probe. This allows us to analyse the internal device signals. Once the design is uploaded to the FGPA, the signal tap tool can be very helpful in debugging. The signal can be tapped to study the output waveform and then later processed in Matlab and the analysis can be done.

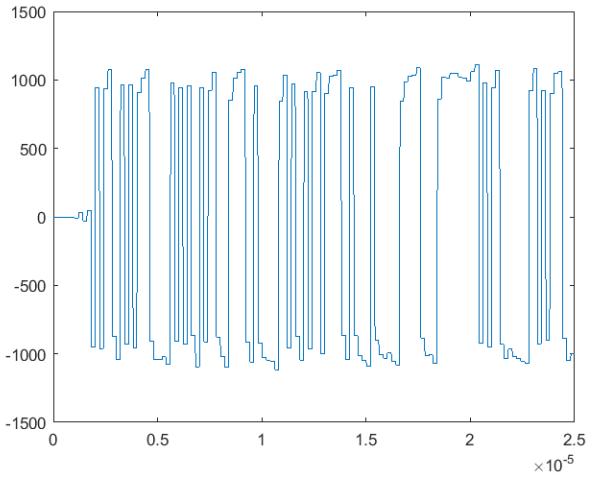
VI. POST LAB HOME ASSIGNMENT

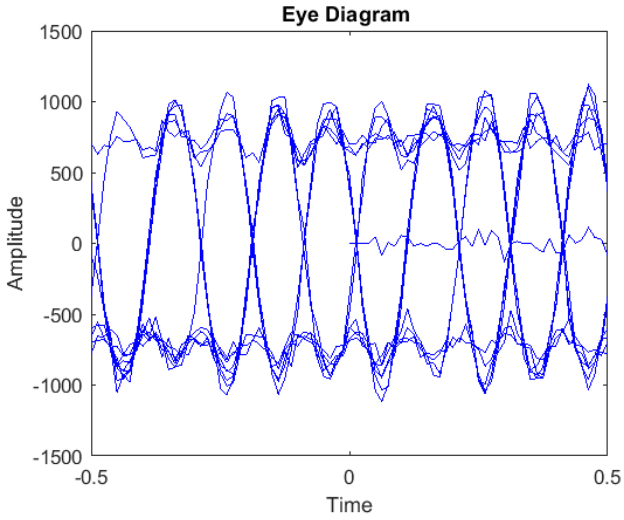
1. The captured signals are shown in the image below.



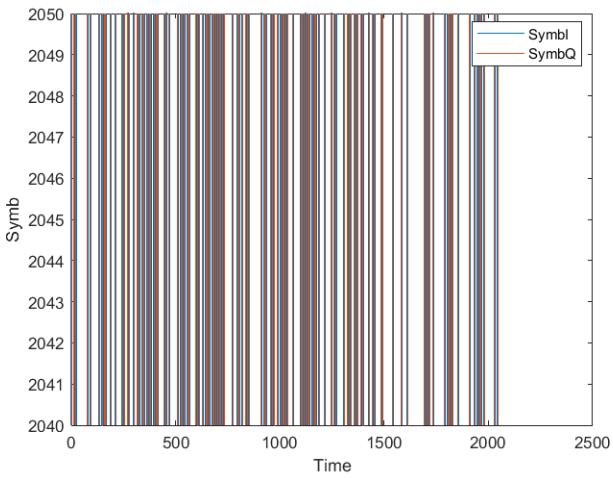
The signals captured are I_in, I_out, Q_in, Q_out, Sample Index, Symb_I and Symb_Q. I_in, I_out, Q_in, Q_out represents the In-phase and quadrature signals of the data (real and complex parts) respectively. The Sample Index signal changes continuously as the sample points are updated within a set window. The Symb_I and Symb_Q are the outputs from the decimation block.

2. The below plots represent the data processed by the transceiver as a function of time and the eye diagram of the received data. The eye diagram is reasonable as it shows a reduced bandwidth as it passes through the low pass filter.

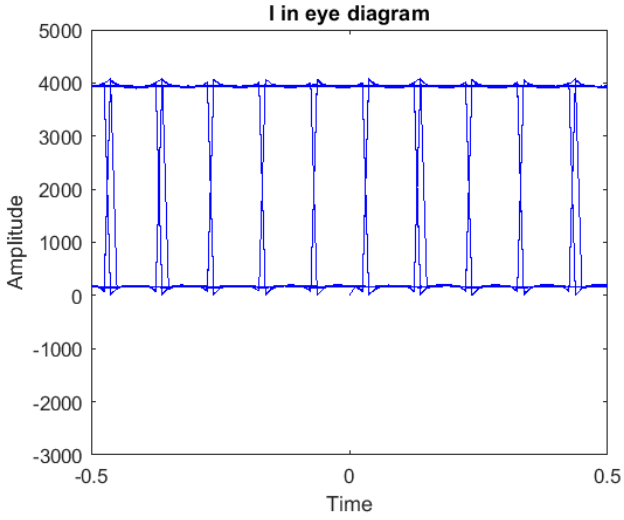


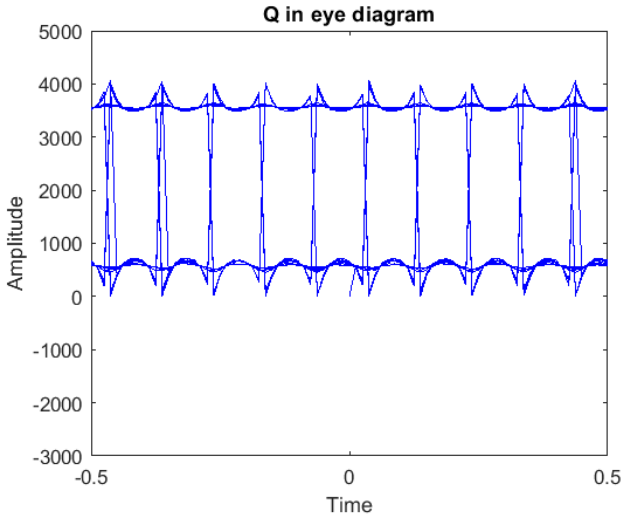


3. The downsampled signals Symb_I and Symb_Q are plotted as a function of time. Sample with the sampling index of 3 contains the best sampling points.



4. The below eye diagrams contain the oversampled received signals I_in and Q_in respectively. I_in has the best sampling points as the open part of the eye is more in I_in and the lines present in the boundary of the eye the termination is also better compared to Q_in.





5. By looking at the amplitude of the transmitted and received I and Q signals, the phase offset can be calculated using arctan since we know that the offset zero at the output of the transmitter.