MCC150-Implementation of Digital Signal Processing
Lab 1: BPSK Transmitter

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I. Introduction

A simple RF transmitter is designed using the Binary Phase Shift Keying (BPSK) method. A cyclone V Field Programmable Gate Array mounted on a Terasic DE-10 Standard development board is used to run the DSP system. The DSP architecture is built using Simulink and hardware is generated in VHDL. Control blocks, Primitive blocks and IP blocks such as filters, mixers and oscillators in the DSP builder advanced blockset are made use of. Quartus Prime is the IDE used to create hardware descriptions, synthesize, simulate and upload bitstreams to Intel FPGAs.

II. DSP BUILDER MODEL

The subsystems used in the building of the transmitter are a PRBS Generator which generates Pseudo Random Binary Sequence or bitstream which is the data to be transmitted. The output of the Sequence Generator is then passed through a modulator. The modulator fuses the input signal with a carrier signal which is produced by the Local Oscillator. The output of the modulator is added below. The display resources block is also added to view the utilization of resources. A Control block is set up to generate the HDL code which can be used for synthesis.

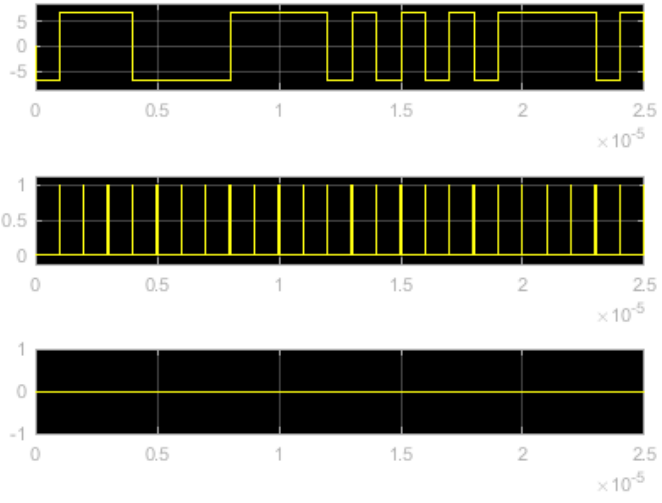


Figure 1Output of Modulator

3.1 Reflection Questions:

1. Wordlength refers to the number of bits transmitted. The transmitted data contains the symbols representing the data. These symbols are sent to a 12-bit Digital Analog Converter and converted to an analog signal. The reason to make use of as much of the wordlength as possible is that to transmit the whole data or else in case of using a lower magnitude, the output analog signal would be lower, and thus more sensitive to noise making it hard to capture at the receiver end. Longer the wordlength better the quality of the transmitted data.

2. When the wordlength value is 12, the resource utilization block shows resource estimates of 39 Look Up Tables and when the value is updated to 4, the resource estimate values change to 31 Look Up Tables. Thus, the resource utilization reduces with wordlength. This might result in quantization errors and overflows.

III. CHANNEL MODEL

Now a Simulink model of a transmission system is created imitating a phase offset and AWGN where the values of SNR can be changed. The values of delay can be changed by tuning the chan.dly variable. The delay block is connected to the output of the AWGN. The output of the transmitter and the output of the AWGN with the delay from the scopes are added below.

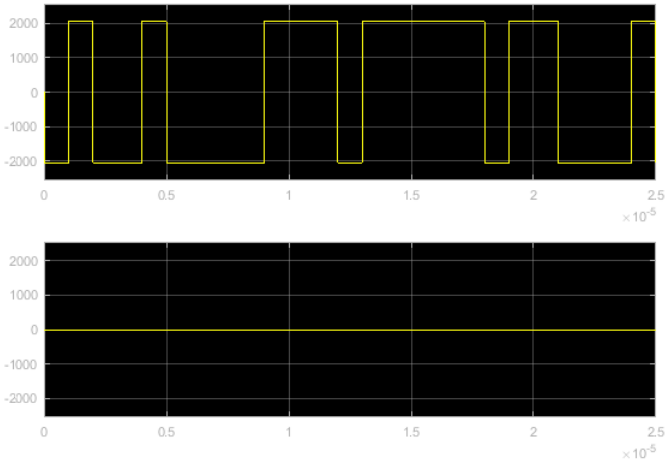


Figure 2 Transmitter Output

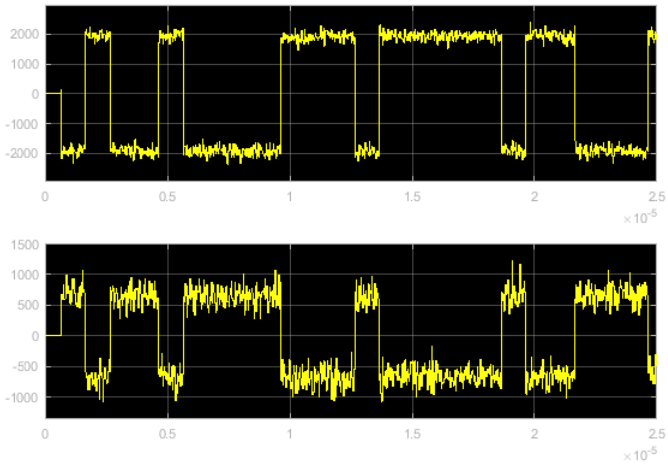


Figure 3Output with added SNR

3.2 Reflection Questions:

1. The phase offset in the channel mode is used to simulate the phase offset that will most likely be present in the received data. This impairment can be caused by e.g., phase difference of the carrier and the local oscillator.

2. When the SNR value is reduced to 10dB in the AWGN block, the noise level increases and it can be explicitly observed at the receiver block. Factors affecting SNR in real life include choice of transmitter and receiver module, magnetic field interference and bandwidth.

IV. SYNTHESIS IN QUARTUS PRIME

The HDL code of the transmitter which is generated using the DSP builder is loaded into Quartus prime for hardware synthesis. Symbol files are created for the transmitter and then the transmitter block is connected to the AD9361 controller. Then the design is compiled, and the compilation report is studied for design utilization, timing results and other design statistics.

3.3 Reflection Questions:

1. The resources used by the transmitter is studied in Quartus Prime in the flow summary chart inside analysis and synthesis: Resource utilization by entity.

Analysis & Synthesis Resource Utilization by Entity

<<Filter>>

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Block Memory Bits	DSP Blocks	Pins	Virtual Pins
1	|MCC150_top	2606 (1)	1648 (0)	128308	0	27	0
1	> |AD9361:AD9361_Inst|	2173 (7)	475 (7)	8500	0	0	0
2	|MCC150_TransmitterBPSKInst|	33 (0)	36 (0)	1024	0	0	0
1	|MCC150_TransmitterBPSK_Modulator:theModulator|	10 (10)	12 (12)	0	0	0	0
2	|MCC150_TransmitterBPSK_PRBSGenerator:thePRBSGenerator|	23 (23)	24 (20)	1024	0	0	0
1	|altera_syncram:DualMem_dmem|	0 (0)	0 (0)	1024	0	0	0
1	|altera_syncram_mh64auto_generated|	0 (0)	0 (0)	1024	0	0	0
1	|altsyncram_2ge4:altsyncram1|	0 (0)	0 (0)	1024	0	0	0
2	|dspba_delayreditst0_Sequence_rsrvd_fix_q_3|	0 (0)	3 (3)	0	0	0	0
3	|dspba_delayreditst1_DualMem_r_1|	0 (0)	1 (1)	0	0	0	0
3	> |sld_hubauto_hub|	93 (1)	91 (0)	0	0	0	0
4	> |sld_signaltapauto_signaltap_0|	306 (2)	1046 (116)	118784	0	0	0

Figure 4 Resource Utilization Report

In the transmitter which was designed which comprises of the PRBS Generator and the Modulator, the PRBS Generator is found to have the largest utility 23 out of 33 total combination ALUTs, 24 out of 36 logic registers and all the 1024 block memory bits when compared to the Modulator.

V. SIGNAL TAP

Once the design is uploaded to the FGPA, the signal tap tool can be very helpful in debugging. The signal can be tapped to study the output waveform and then later processed in Matlab and the analysis can be done. The microcontroller block is expanded and the Transmitted and the Received IQ signals along with the output from the PRBS Generator subsystem is inserted and compiled. Then the generated programming files are uploaded, and the hardware is setup. The captured signals are shown in the image below.

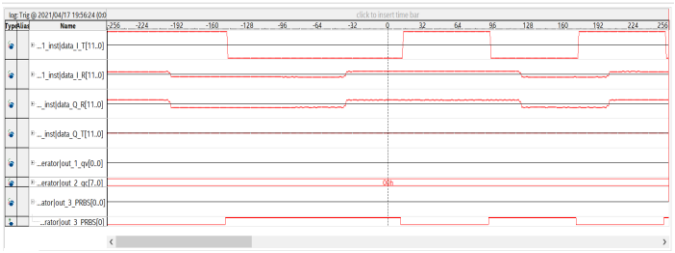
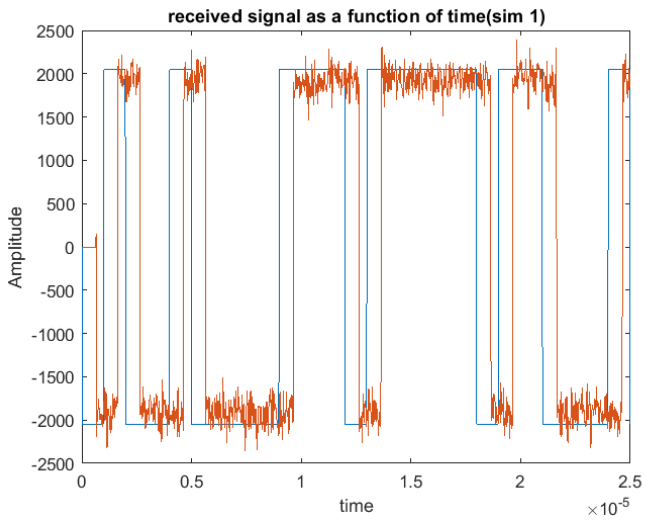
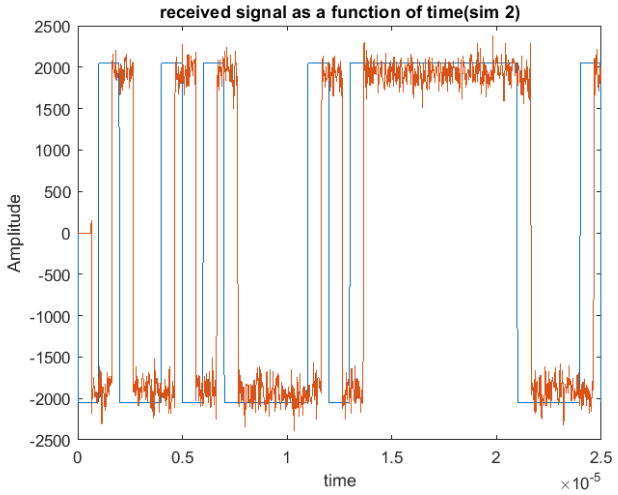


Figure 5 Captured signals after synthesis

VI. POST LAB HOME ASSIGNMENT

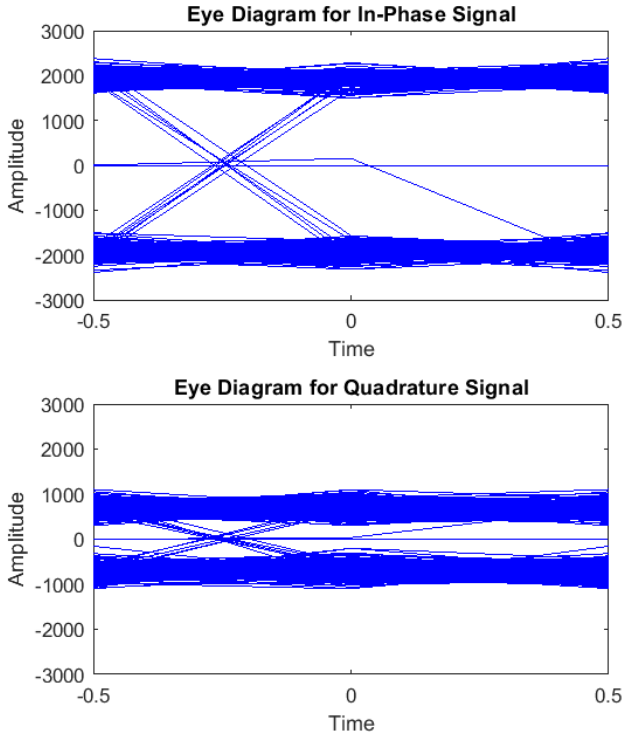
1. The transmitted and received signals are plotted as a function of time. The PRBS Generator generates random bitstreams during every simulation run and hence the difference between the signals of different simulations arises.





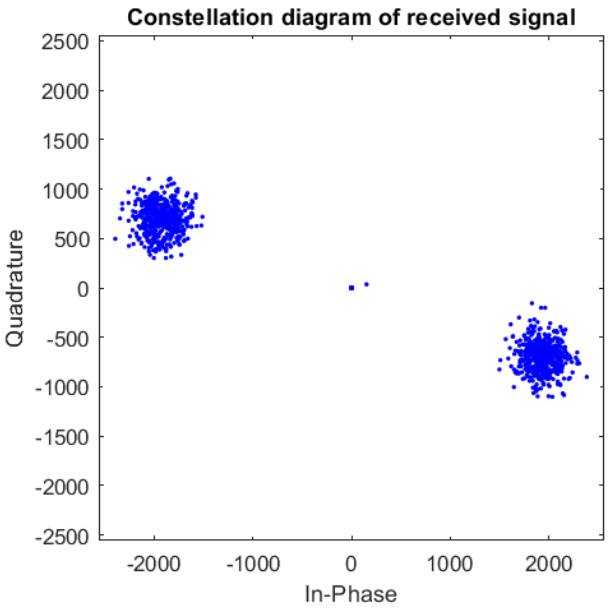
2. The received signals will have a phase offset corresponding to the value of SNR given in the AWGN block. The phase offset values are found to be,
Result1- -0.3366
Result2- -0.3508

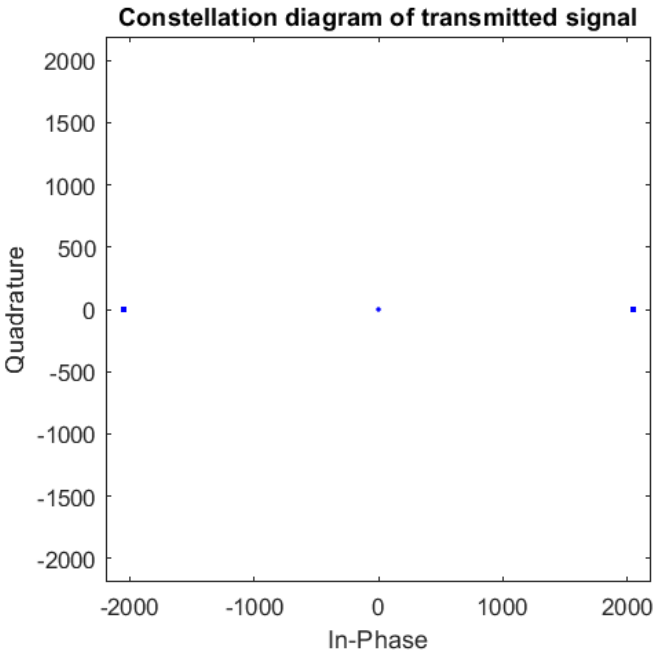
3. The eye diagram for simulation 2 is created and attached below. The parameters are selected such that the open part of the eye is more, and the amount of distortion is less and a smaller slope so that the sensitivity of the timing error is less. So, the value of period is given as 2 for my signal. This facilitates a clear view of one eye opening.

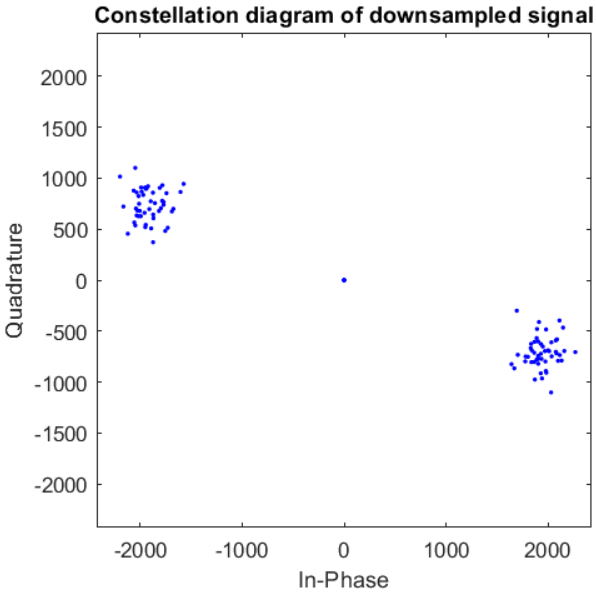


4. The received I and Q data are downsampled to one sample per signal. Downsampling is useful when the transmission of data takes place within a limited bandwidth making the signal smaller.

5. The constellation diagram of the transmitted, received and the downsampled I and Q signals are attached below. The downsampled plot contains less number of bits than generated by the sequence generator which is reasonable. The constellation points should be as far as possible with a reasonable gap and the cluster must have less data points(bits) as possible. And in our case, it seems reasonable.






Constellation diagram of downsampled signal
Quadrature
In-Phase
2000
1500
1000
500
0
-500
-1000
-1500
-2000
-2000
-1000
0
1000
2000