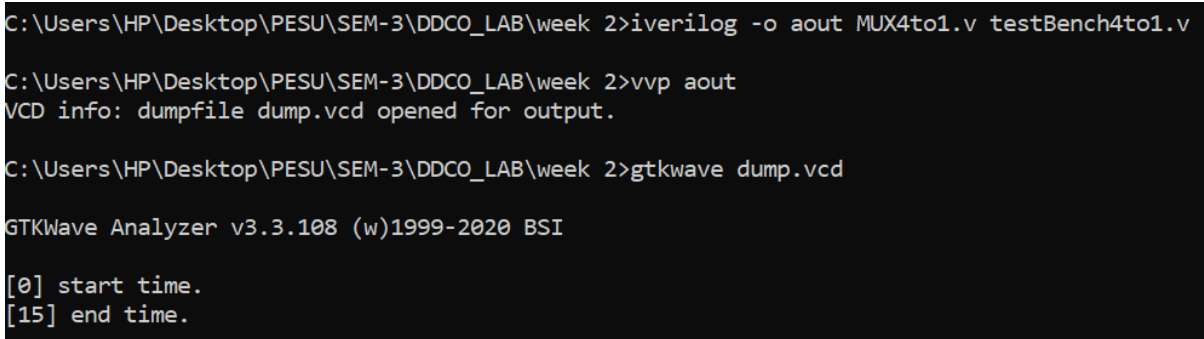
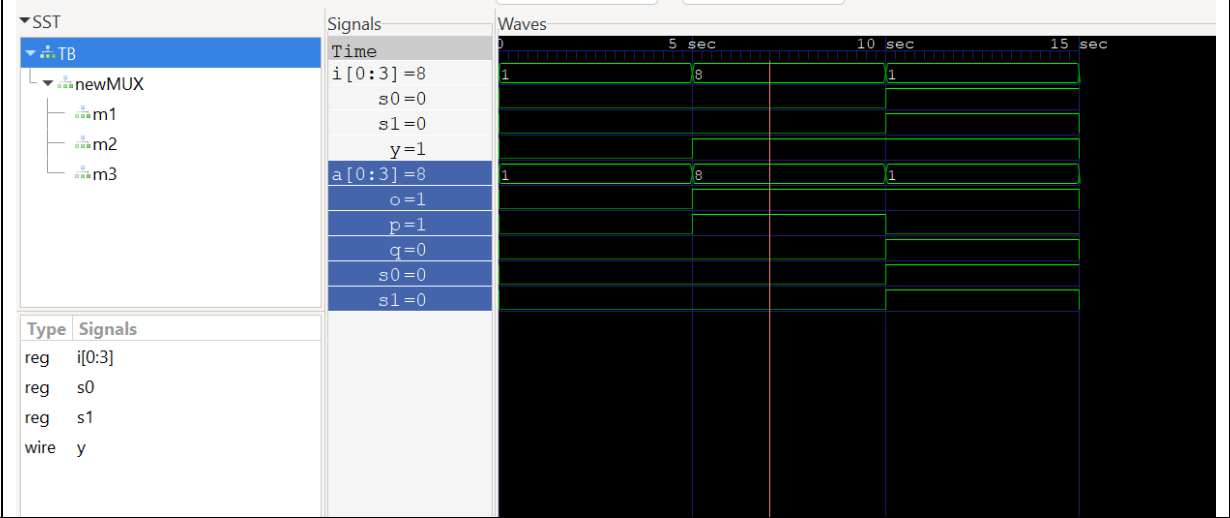
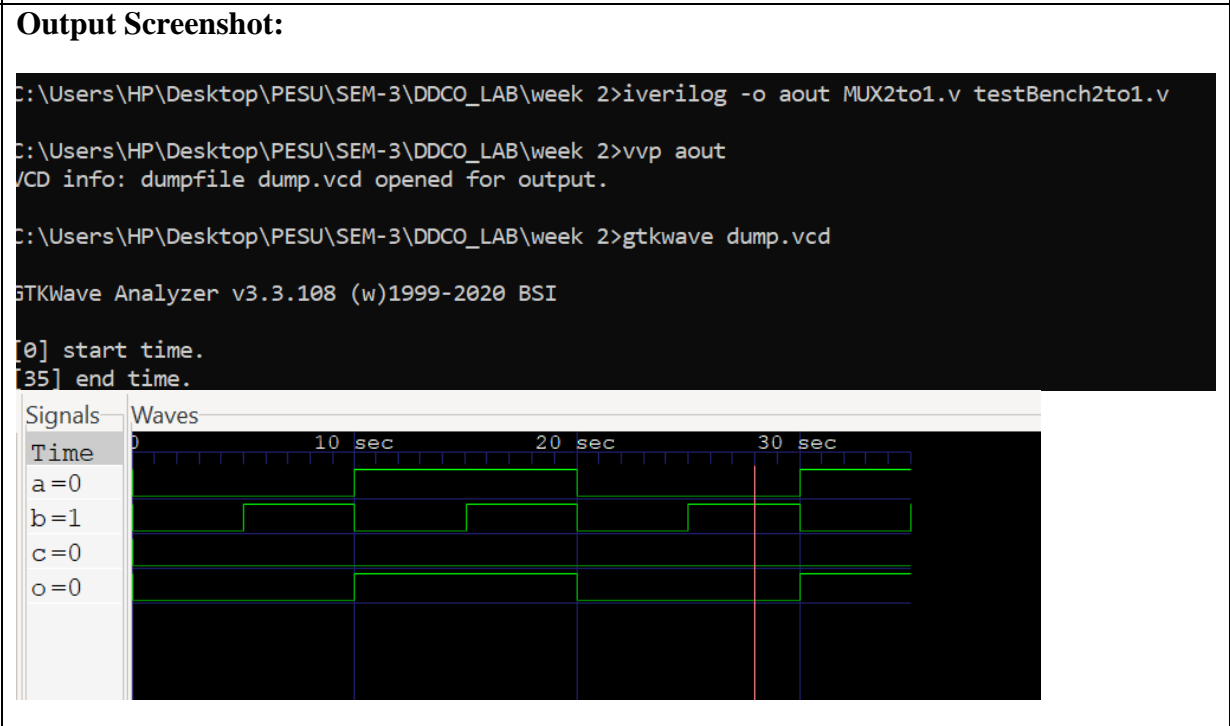


## Week 3: Programs on User Defined Functions

Name: SUNDEEP A	SRN: PES1UG20CS445	Section: H
	Date: 30-08-21	Week Number: 2

1	4 to 1 MUX
	<p><b>Program:</b></p> <pre> module mux2 (input wire i0, i1, j, output wire o);   assign o = (j==0)?i0:i1; endmodule  module mux4 (input wire [0:3]a, input wire s1, s0, output wire o);   wire p, q;    mux2 m1(a[0], a[1], s0, p);   mux2 m2(a[2], a[3], s0, q);   mux2 m3(p, q, s1, o);  endmodule </pre>
	<p><b>Output Screenshot:</b></p>  <pre> C:\Users\HP\Desktop\PESU\SEM-3\DDCO_LAB\week 2&gt;iverilog -o aout MUX4to1.v testBench4to1.v C:\Users\HP\Desktop\PESU\SEM-3\DDCO_LAB\week 2&gt;vvp aout VCD info: dumpfile dump.vcd opened for output. C:\Users\HP\Desktop\PESU\SEM-3\DDCO_LAB\week 2&gt;gtkwave dump.vcd GTKWave Analyzer v3.3.108 (w)1999-2020 BSI [0] start time. [15] end time. </pre>

## Week 3: Programs on User Defined Functions

	
2	2 to 1 MUX
	<p><b>Program:</b></p> <pre> module mux2 (input wire a, b, c, output wire o);   assign o = (c==0)?a:b; endmodule </pre>
	<p><b>Output Screenshot:</b></p> 

3	4 bit Ripple Carry adder
	<p><b>Program:</b></p> <pre> module fulladdR(input wire [3:0] a, b, input wire cin, output wire [3:0] sum, output wire cout);     wire [2:0] c;     fulladd f1(a[0], b[0], cin, sum[0], c[0]);     fulladd f2(a[1], b[1], c[0], sum[1], c[1]);     fulladd f3(a[2], b[2], c[1], sum[2], c[2]);     fulladd f4(a[3], b[3], c[2], sum[3], cout); endmodule </pre>
	<p><b>Output Screenshot:</b></p> 