IEEE SSCS CHIPATHON 2025

BUILDING BLOCKS FOR DIGITAL DESIGN

COMPARATOR STD CELL

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Our Experience

1. **Academic Experience**
   a. Finished 3rd year in Electrical Engineering, Institut Teknologi Bandung (ITB), Bandung, Indonesia;
   b. Have experience in VLSI design with VHDL and Verilog code;
   c. Layout and Synthesis from RTL to LVS/DRC checking in SKY130-PDK using open tools via IIC-OSIC-TOOLS.
2. **Work Experience**

No work experience regarding digital IC design.

Goals

- We are going to design digital comparator as a standard cell for the 9-track and 3.3 V library, especially the OSU library.
  - 1-bit digital comparator/2-input digital comparator 1x, 2x
  - 2-bit digital comparator/4-input digital comparator 1x, 2x
- The steps for our design: RTL, schematic design, schematic simulation (Functional and electrical), layouting, LVS, DRC, LEF files, characterization, synthesis, and place & route.
- Here are our targeted specifications.

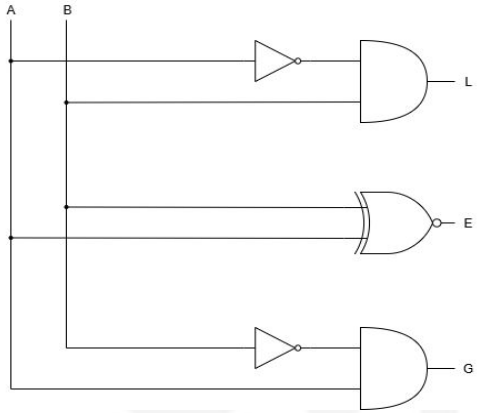
1-Bit Digital Comparator	
Parameters	Targeted Specification
VDD	3.3 V
Drive Strength	1x, 2x
Pin Capacitance	≤ 0.01 pf, ≤ 0.02 pf
Approximate Area	≤ 40 μm^2, ≤ 50 μm^2

2-Bit Digital Comparator	
Parameters	Targeted Specification
VDD	3.3 V
Drive Strength	1x, 2x
Pin Capacitance	≤ 0.02 pf, ≤ 0.03 pf
Approximate Area	≤ 80 μm^2, ≤ 100 μm^2

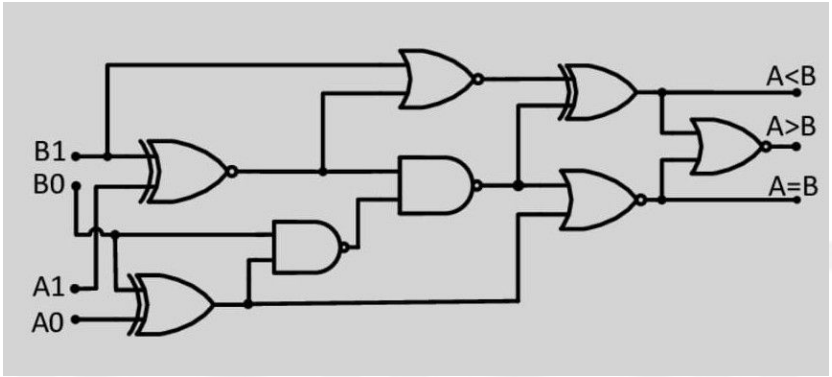
Functionality

- **A 2-input comparator** is a standard cell that **compares two binary numbers** and the result/the output ports are divided into **three signals**: a signal that represents **A > B**, a signal that represents **A = B**, and a signal that represents **A < B**.
- **A 4-input comparator** comprised of **two (2) 2-input comparator**. Hence, it can compares between **two 2-bit numbers**. Additional gates are needed for the result/output ports.

Digital Circuits (Schematics)

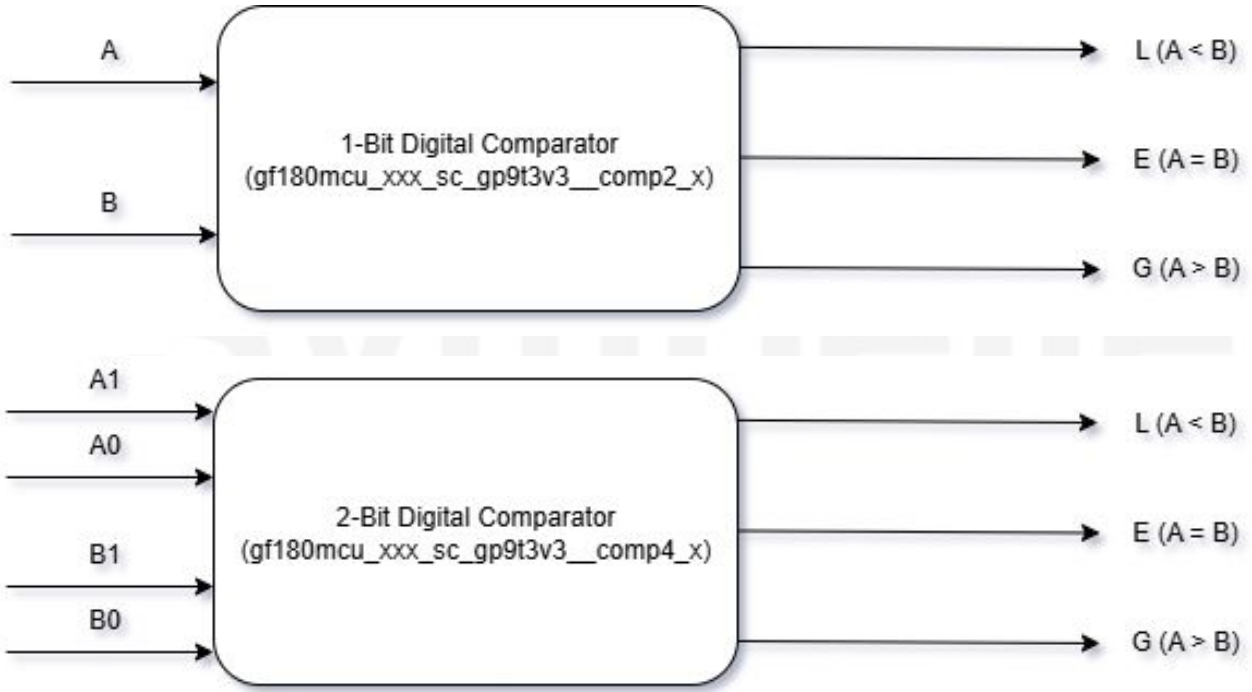


1-bit digital comparator/2-input comparator
(gf180mcu_osu_sc_gp9t3v3__comp2_x)



2-bit digital comparator/4-input comparator
(gf180mcu_osu_sc_gp9t3v3__comp4_x)

Top-Level Diagram



Application

- Analog-to-Digital Converter (ADC): Used to compare analog voltages to reference voltages
- CPU: used in if-else statements (e.g. a>b), decision maker in the controller logic, and to check status flags
- Memory: used to match the address to the location in the memory and determining the “hit” or “miss” in a cache

Tasks Scheduling

Task	July 2025			Aug. 2025					Sept. 2025			
	Week 28	Week 29	Week 30	Week 31	Week 32	Week 33	Week 34	Week 35	Week 36	Week 37	Week 38	Week 39
Proposal, Targeted Specifications & Documentation												
Schematic & Functional Simulation												
Layouting, LVS, and DRC												
Parasitic Extraction & Simulation												
Characterization & Abstraction												

Tasks Division

- Kean Malik Aji Santoso:
  - 1 bit comparator with fan-out drive 1x
  - 1 bit comparator with fan-out drive 2x
- Anas Fathurrahman & Muhammad Yoga Putratama:
  - 2 bit comparator with fan-out drive 1x
  - 2 bit comparator with fan-out drive 2x

References

- https://users.encs.concordia.ca/~asim/COEN_6511/Projects/final6511report.pdf
- https://www.elprocus.com/digital-comparator-and-magnitude-comparator/
- https://worldofcomputing.net/digital-electronics/magnitude-comparator.html
- https://skywater-pdk.readthedocs.io/en/main/contents/libraries/foundry-provided.html
- https://gf180mcu-pdk.readthedocs.io/en/latest/digital/standard_cells/gf180mcu_fd_sc_mcu9t5v0/index.html