Steps for determining the project (Digital building blocks):

1. Selecting the standard cell tracks (7T, 9T, or 12T)
2. Determining the wanted standard cell
3. Determining the datasheet of the digital building blocks (Functionality, block diagram, application)
4. Developing the week by-week schedule of the project

Available standard cells for 7T (5V):

- Full Adder
- Half Adder
- AND Gate (2-input, 3-input, 4-input)
- AND-OR-Invert Gate
  - aoi21: $(\overline{A1} \cdot \overline{B}) + (\overline{A2} \cdot \overline{B}) = (\overline{A1} + \overline{A2}) \cdot \overline{B}$
  - aoi211: $(\overline{A1} + \overline{A2}) \cdot \overline{B} \cdot \overline{C}$
  - aoi22: $(\overline{A1} + \overline{A2}) \cdot (\overline{B1} + \overline{B2})$
  - aoi221: $(\overline{A1} + \overline{A2}) \cdot (\overline{B1} + \overline{B2}) \cdot \overline{C}$
  - aoi222: $(\overline{A1} + \overline{A2}) \cdot (\overline{B1} + \overline{B2}) \cdot (\overline{C1} + \overline{C2})$
- OR-AND-Invert Gate
  - oai21: $(\overline{A1} \cdot \overline{A2}) + \overline{B}$
  - oai211: $(\overline{A1} \cdot \overline{A2}) + \overline{B} + \overline{C}$
  - oai22: $(\overline{A1} \cdot \overline{A2}) + (\overline{B1} \cdot \overline{B2})$
  - oai221: $(\overline{A1} \cdot \overline{A2}) + (\overline{B1} \cdot \overline{B2}) + \overline{C}$
  - oai222: $(\overline{A1} \cdot \overline{A2}) + (\overline{B1} \cdot \overline{B2}) + (\overline{C1} \cdot \overline{C2})$
  - oai31: $(\overline{A1} \cdot \overline{A2} \cdot \overline{A3}) + \overline{B}$
  - oai32: $(\overline{A1} \cdot \overline{A2} \cdot \overline{A3}) + (\overline{B1} + \overline{B2})$
  - oai33: $(\overline{A1} \cdot \overline{A2} \cdot \overline{A3}) + (\overline{B1} + \overline{B2} + \overline{B3})$
- D-type Flip-Flop
  - dffq: Q output
  - dffnq: Inverted Q output (NQ)
  - dffrnq: Asynchronous reset and inverted Q output (NQ)
  - dffsnq: Asynchronous set and inverted Q output (NQ)
  - dffrsnq: Reset, Set, and NQ
  - dffnrnq: Active-low reset and NQ
  - dffnsnq: Active-low set and NQ
  - dffnrsnq: Active-low set & reset, NQ
- Scan D-type Flip-Flop
  - sdffq: Q output

    - sdffrnq: Asynchronous reset and inverter Q output (NQ)
    - sdffrsnq: Reset, Set, and inverted Q output (NQ)
    - sdffsnq: Asynchronous set and inverter Q output (NQ)
- Latch
    - latq: Q output
    - latrnq: Asynchronous reset and inverter Q output (NQ)
    - latrsnq: Reset, Set, and inverter Q output (NQ)
    - latsnq: Asynchronous set and inverted Q output (NQ)
- Integrated Clock Gating Cell
- Delay Cell
- Antenna
- Tie-Low Cell
- Tie-High Cell
- Buffer & Tri-state buffer
- Clock (Inverting and Buffer)
- End-Cap Cell
- Filler Cell
- Filler Cell with Decoupling Capacitor
- Filler Cell with Tie-Off (Tie-Low Cell/Tie-High Cell)
- Multiplexer (2-input, 4-input)
- NOR Gate (2-input, 3-input, 4-input)
- NAND Gate (2-input, 3-input, 4-input)
- OR Gate (2-input, 3-input, 4-input)
- XNOR Gate (2-input, 3-input)
- XOR Gate (2-input, 3-input)

Available standard cells for 9T (3,3 V):

- Full Adder
- Half Adder
- AND Gate (2-input)
- Antenna Cell (Standard one and also with Filler Cell)
- AND-OR-Inverter Gate
    - aoi21: $(\overline{A1} \cdot \overline{B}) + (\overline{A2} \cdot \overline{B}) = (\overline{A1} + \overline{A2}) \cdot \overline{B}$
    - aoi22: $(\overline{A1} + \overline{A2}) \cdot (\overline{B1} + \overline{B2})$
- Buffer
- Clock (Buffer and Inverting)
- Decoupling Capacitor
- D Flip-Flop
    - dff: Standard

    - dffn: Inverted output (?)
    - dffsr: Set and Reset
- D Latch (Standard one and the one with inverted output)
- Filler cell
- Inverter
- Multiplexer (2-input)
- NAND Gate (2-input)
- NOR Gate (2-input)
- OR Gate (2-input)
- OR-AND-Inverter Gate
    - oai21: $(\overline{A1} \cdot \overline{A2}) + \overline{B}$
    - oai22: $(\overline{A1} \cdot \overline{A2}) + (\overline{B1} \cdot \overline{B2})$
    - oai31: $(\overline{A1} \cdot \overline{A2} \cdot \overline{A3}) + \overline{B}$
- Tie-Low Cell
- Tie-High Cell
- Tri-State Buffer
- Tri-State Inverter
- XNOR Gate (2-input)
- XOR Gate (2-input)

Available standard cells for 12T (3,3 V):

- Full Adder
- Half Adder
- AND Gate (2-input)
- AND-OR-Inverter Gate
    - aoi21: $(\overline{A1} \cdot \overline{B}) + (\overline{A2} \cdot \overline{B}) = (\overline{A1} + \overline{A2}) \cdot \overline{B}$
    - aoi22: $(\overline{A1} + \overline{A2}) \cdot (\overline{B1} + \overline{B2})$
- Buffer
- Clock (Buffer and Inverting)
- D Flip-Flop
    - dff: Standard
    - dffn: Inverted output (?)
    - dffr: Reset
    - dffrn: Active-low reset
    - dffs: Set
    - dffsn: Active-low set
    - dffsr: Set and Reset
    - dffsrn Active-low set and active-low reset
- D Latch (Standard one and the one with inverted output)

- Filler cell
- Inverter
- Logical Shift Down (Right-Shift)
- Logical Shift Up (Left-Shift)
- Multiplexer (2-input)
- NAND Gate (2-input)
- NOR Gate (2-input)
- OR Gate (2-input)
- OR-AND-Inverter Gate
  - oai21: $(\overline{A1} \cdot \overline{A2}) + \overline{B}$
  - oai22: $(\overline{A1} \cdot \overline{A2}) + (\overline{B1} \cdot \overline{B2})$
  - oai31: $(\overline{A1} \cdot \overline{A2} \cdot \overline{A3}) + \overline{B}$
- Tie-Low Cell
- Tie-High Cell
- Tri-State Buffer
- Tri-State Inverter
- XNOR Gate (2-input)
- XOR Gate (2-input)