

IEEE SSCS CHIPATHON 2025

BUILDING BLOCKS FOR DIGITAL DESIGN

DIGITAL COMPARATORS

D17-Symbelleuit

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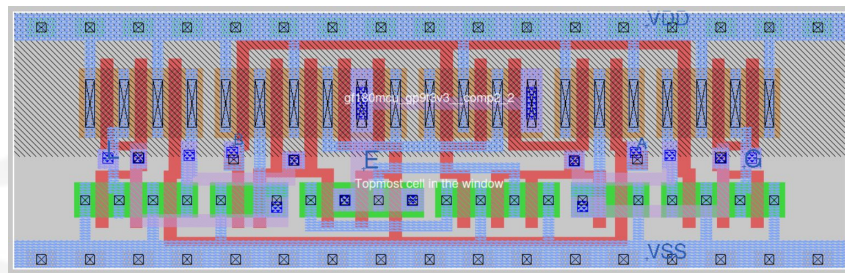
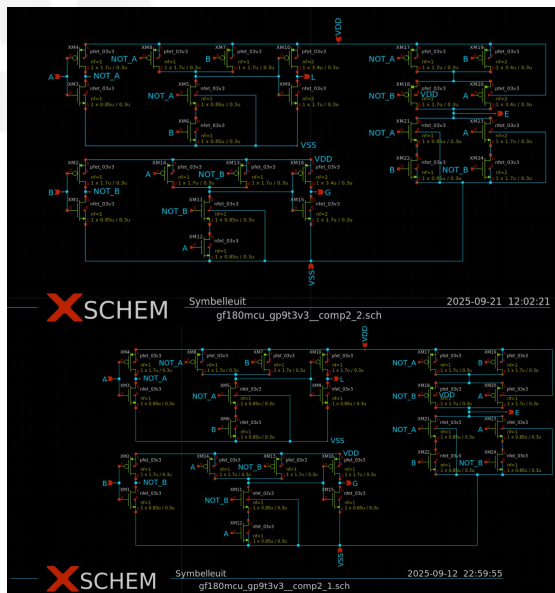
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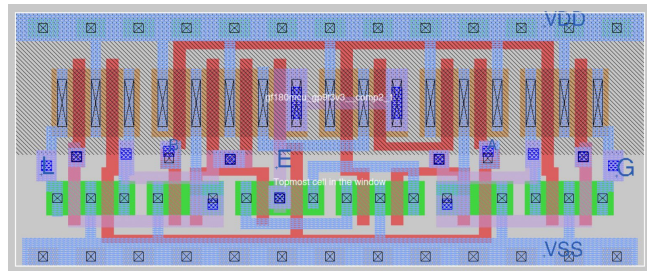
Design Summary

Our team had designed **2-inputs/1-bit digital comparators** as **standard cells** for **GF180MCU OSU** at **3V3** and **9-track**. We have built **two variations**: **1-bit digital comparator with 1x drive strength** & **2-bit digital comparator with 2x drive strength**.

The status of our design is **simulated**, **integrated to the digital track padframe**, and is **in progress of tape-out**.



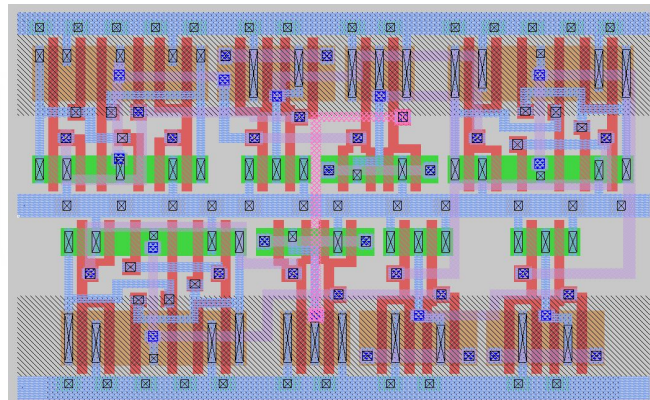
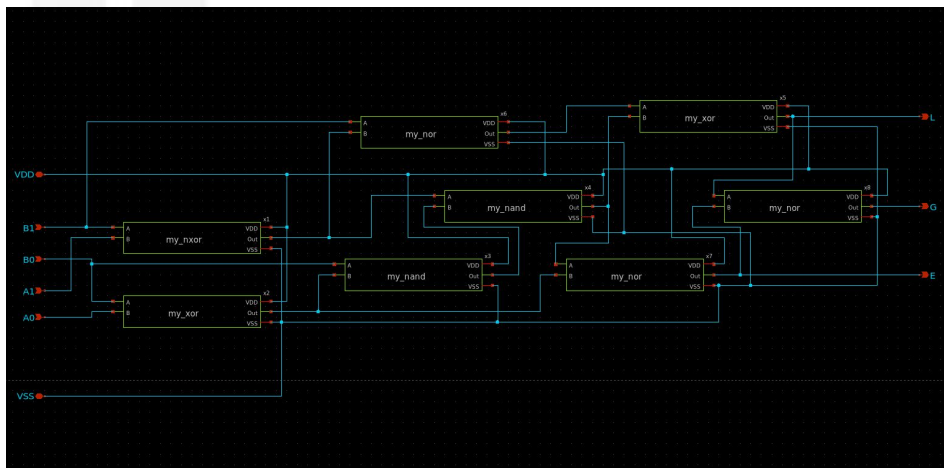
Area size: 20.590 x 6.350 (130.746 u²)



Area size: 15.790 x 6.350 (100.266 u²)

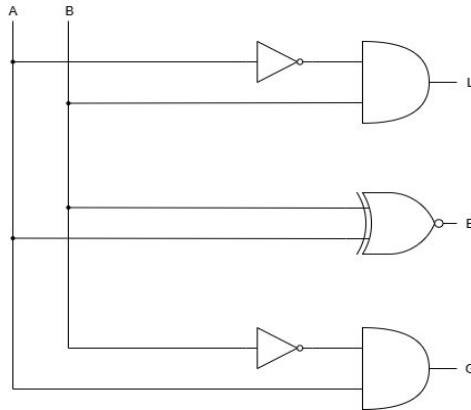
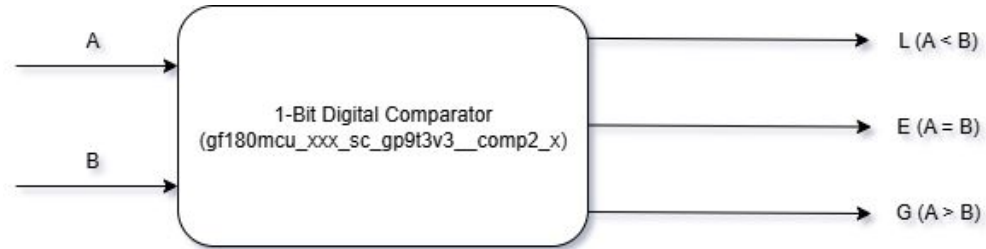
Design Summary

On the other hand, we also created an **experimental** cell that increases logic-gate density using the most optimal gate arrangement for a **2-bit comparator**. However, considering the total cell size and the committee's input stating that 2-row standard cells are not yet supported in the open-source software, we decided **not to include** this design for tape-out.



Area size: 240u x 3.92 (100.266 u²)

Top-Level Diagram & Schematics



Lessons Learned & Best Practices

What worked:

- It takes a **lot of creativity** to **design the digital comparators layout** because **there aren't any existing** digital comparator layout and the process is fun like Picasso on chip layouting!
- The layout designs surprisingly worked by **implementing finger technique** and they had **no DRC issues** so that the **LVS succeeded** and **post-layout simulation results** are as **same** as **schematics simulation**.

What didn't work:

- We were actually **planned to design 2-bit/4-inputs digital comparators**, but we **weren't sure** about the **area size** of the layout and **the routing** between pins and power pins at a **single-row cell** so we didn't design them.

What need to be improved:

- The layout designs are maybe **unoptimized in its area size**.
- The layouts are **not designed** based on the **grid configuration** of **9-track** of GF180MCU OSU, but we designed them to **match the height of the 9-track**, which is **6.350 um**.
- For the **digital track**, digital teams need to do **LVS** for the **integration layout**.

Reflection/Feedback:

Favourite Part:

- The layout design process was our favourite part because
 - We had to determine the best logic circuit stick diagram configuration (It is more than one possible configuration), especially XNOR gate;
 - We had to make stick diagrams for both of digital comparators; and
 - We had to make the layout with KLayout based on the stick diagram and ensure an optimized area of design that still comply with DRC rule checks and LVS.

LLM Usage:

- We used AI for understanding concepts about layout designs and certain step of designing standard cells and also making sure of our understanding so that it is correct.

Suggestions:

- Ensure that every track is well coordinated and information about milestones/phases of chipathon is well-informed to all participants; and
 - The digital track coordination and communication channel were limited and not as detailed as MOSBius track and thus digital track teams missed some deadlines or missed some important informations.
- Please make sure the track clarity about goals or purpose of the track so that every participant know what to achieve and what to be done before enroll chipathon in a certain track.
 - A digital track team, D22-Chipster, had a headstart and they designed a ML that can generate a basic logic gate circuits and designed an accelerator using Verilog and OpenLane, but at some point, what the team had done wasn't aligned with purpose of digital track.
 - Fortunately, they were still accepted and thus they continued their progress.