UNIVERSITY OF MAURITIUS
MODULE CATALOGUE

1. GENERAL INFORMATION

Academic Year: 2024/2025
Semester(s): 1 & 2

Title	Code	Duration (hrs)	No. of credits
COMPUTER ORGANISATION And ARCHITECTURE	**ICT 1206Y**	Lectures *: **40** *(2 hrs x 20 weeks) Online Delivery by Video Conferencing*	
		Practicals/Tutorials **: **20** *(1 hr x 20 weeks) Face-to-Face in Lab/Classroom*	
		Self-Learning: **180**	
		Other Learning Activities#: **180**	
		Total contact hours: **60**	**12**

#working on assignments, sitting for Class Tests and preparation time for same, sitting for Examinations and preparation time for same, group work, presentations among peers and guest lectures.

*Mode of Delivery of lectures (L) for this module will be ONLINE and/or face-to-face.

**Mode of Delivery of Praticals (P) and/or Tutorials (T) will be FACE-TO-FACE in classroom or Computer Labs (25-30 students per group).

2. PRE-REQUISITE(S)/PRE-REQUIREMENT(S)

NONE (Students are expected to have basic knowledge of IT/computing & Mathematics)

3. AIMS

Computer architecture is concerned with the structure and behaviour of the various functional modules of the computer; and how they interact to provide the processing needs of the user. In particular this module covers computer systems ranging from PCs through multiprocessors with respect to hardware design and instruction set architecture. This includes units and related technologies such as primary and secondary memory, caches, central processing unit (CPU), and pipelines.

After completing this module, you should be able to:

- Use binary mathematics, Boolean algebra and the digital representation of numbers.
- Recognize the fundamental digital circuits that implement basic digital functions.
- Describe the basic components of a central processing unit.
- Describe the instructions execution cycle of a CPU.
- Describe the components of the memory hierarchy, how these various components are utilized and how data is moved between them.
- Interpret the basic structure of common machine and assembly level instructions.
- Describe how peripheral devices communicate with the processor.

4. OUTLINE SYLLABUS

Through Contact Hours:

Number Systems and Computer Arithmetic, Signed Integer and Floating-Point Representation, Digital Logic and Boolean Algebra, Karnaugh Map (Don't Care Conditions), Combinational and Sequential Circuit Design, Von Neumann Machine Architecture, Instruction Cycle, Assembly-Level Machine Organisation, Memory System Organisation and Architecture, Functional Organisation (Pipelining), Computer System Performance and Reliability Metrics.

Through Self-Learning:

(Semester 1) Instruction Cycle, (Semester 2) Assembly-Level Machine Organisation

5. LEARNING OUTCOMES AND ASSESSMENT CRITERIA

Having studied this module, the students should be able to achieve the following learning outcomes. The assessment criteria used to reflect the expected learning outcomes are also given hereunder:

Learning Outcomes	Assessment Criteria
➢ Demonstrate the use of binary mathematics, Boolean algebra and the digital representation of numbers.	➢ Number Systems and Computer Arithmetic ➢ Convert numbers in base 10 to base 2, and numbers in base 2 to base 10. ➢ Convert numbers in base 16 to base 2, and numbers in base 2 to base 16. ➢ Express a number in two's complement. ➢ Give the range of valid numbers expressible in a given integer representation. ➢ Explain what overflow is, and how it can be detected when adding two's complement numbers. ➢ Name the three ways a signed binary number can be represented. ➢ Name the parts of floating point number. ➢ Express a floating-point number in IEEE 754 single-precision format.
➢ Recognize the fundamental digital circuits that implement basic digital functions and design circuits.	➢ Boolean Logic ➢ Identify the basic logic gates (AND, OR, NOT, XOR, NAND, NOR) and give their truth tables. ➢ Use Boolean identities to prove the equivalence of two expressions. ➢ Use DeMorgan's Law to rewrite an expression. ➢ Write a Boolean expression in sum-of-products or product-of-sum form. ➢ Derive a Boolean expression or truth table for a given logic circuit. ➢ Directly draw a logic circuit from a Boolean expression ➢ Explain what each of the following combinational devices does: full adder, decoder, multiplexer, shifter ➢ Identify the basic flip-flops (SR, JK, D) and give their characteristic tables. ➢ Write a simplified Boolean expression from a K-map. ➢ Create a K-map for a Boolean function.

➢ Demonstrate an understanding of the basic components of a central processing unit. ➢ Demonstrate an understanding of the instructions execution cycle of a CPU	➢ Name the characteristics of a von Neumann architecture. ➢ Describe the purpose of a CPU's datapath and control unit, system bus ➢ Describe how instructions are decoded by the control unit ➢ Calculate the maximum speed-up for a pipelined processor ➢ Calculate the speed-up ratio of a pipelined processor for a given number of tasks. ➢
➢ Analyse the components of the memory hierarchy, understand how these various components are utilized and how data is moved between them.	➢ Computer Architecture - Memory Systems ➢ Calculate the size of various aspects of a given memory system (number of memory chips needed, number of address lines for word and byte addressing, etc) ➢ Explain the concept of the memory hierarchy, and the memory pyramid ➢ Explain how the locality principle and the three types of locality influence the memory hierarchy ➢ Identify the three types of cache designs discussed in class (direct mapped, fully associative, N-way set associative) ➢ Determine the size of each field in a memory address for a given cache system. ➢ Determine the sizes of various cache structures (number of blocks, number of sets, words per block, number of main memory blocks) given a memory address broken into the tag, set/block, and word fields. ➢ Determine cache hits and misses for a series of main memory accesses. ➢ Determine the effective access time (EAT) for a particular program. ➢
➢ Understand how data flows among primary computer components, and how these data flows impact the	➢ Identify the physical and logical components of a magnetic hard disk drive.

efficiency of software applications.	➢ Calculate the access time for a hard disk drive.
➢ Write assembly programs, Interpret the basic structure of common machine and assembly level instructions.	➢ Programming – MARIE Assembly Language ➢ Give examples of immediate, direct, register, indirect, and indexed addressing. ➢ Write simple MARIE-type programs

6. COORDINATORS

	Programme Coordinator	Area Coordinator (if applicable)	Module Coordinator
Name	**Razvi Doomun**		**Razvi Doomun**
Department	**ICT**		**ICT**
Building	**Engineering Tower**		**Engineering Tower**
Room Number	**Level 4**		**Level 4**
Phone No.	**403 7836**		**403 7836**
E-mail address	**r.doomun@uom.ac.mu**		**r.doomun@uom.ac.mu**
Consultation Time			

7. LECTURER(S)

Name	**Razvi Doomun**	**Bikash Sonah**	
Department	**ICT**	**ICT**	
Building	**Engineering Tower**	**Phase II Bldg**	
Room Number	**Level 4**	**Level 2**	
Phone No.	**403 7836**	**57592416**	
E-mail address	**r.doomun@uom.ac.mu**	**b.sonah@uom.ac.mu**	
Contact Hours	**As per time-table**	**As per time-table**	
Consultation Time	**As per time-table/By appointment**	**As per time-table/By appointment**	
Contact Address (for P/T)			

8. VENUE AND HOURS/WEEK

All lectures/Tutorials and/or Practicals will normally be held in Room: (*as per your*

programme time-table)

Hours/week: **2 Hours Lecture + 1 Hour Lab/Tutorial/Practical**

9. MODULE MAP (TENTATIVE)
SEMESTER 1

Wk(s)	Hr(s)	Theme(s)	Lecture Title(s)	Further Reading and Self-Learning Activities	L, P, S, V, T , Test
1*	**2 + 1**	**Binary Number & Integers**	Conversion: Binary-Decimal, Hexadecimal; Signed Integer representation, Overflow	Textbook: Chapter 1 (Terminologies & basic components in a Computer System) *Reading & self-study (section 1.5, 1.6, 1.7)*	*Tutorial: Binary Number Operations*
2*	**2 + 1**	**Floating Point Numbers**	IEEE-754 single precision	Textbook: Chapter 2 (Data representation in computer Systems) *Reading & self-study (section 2.3, 2.4, 2.5)*	*Tutorial: Floating Point Operation*
3*	**2 + 1**	**Boolean Algebra**	Logic gates, Truth-table, Boolean Expression and Identities	Textbook: Chapter 3 *Reading & self-study (section 3.1, 3.2, 3.3)*	*Practical: Logisim*
4*	**2 + 1**	**Digital Logic & Digital Circuits**	Combinational Circuit: Adder & Decoder	Textbook: Chapter 3 *Reading & self-study (section 3.4, 3.5)*	*Practical: Logisim*
5*	**2 + 1**	**Minimizing circuits: Karnaugh Map**	Minimizing Boolean expressions, Minterms, Maxterms	Textbook: Chapter 3 *Reading & self-study (section 3A Karnaugh maps)*	*Practical: Logisim*
6		**Class TEST 1**		*Textbook: Revision Chapter 1, 2, 3*	*Tutorial*
7*	**2 + 1**	**Analysis & Design of Combinational Circuits**	ALU Design & BCD to 7-segment display controller	Textbook: Chapter 3 *Reading & self-study (section 3.6 & 3.7)*	*Practical: Logisim*
8*	**2 + 1**	**Sequential Circuits: Flip Flops & Clock**	SR, JK, D Flip flops	Textbook: Chapter 3 *Reading & self-study (section 3.6)*	*Practical: Logisim*
9*	**2 + 1**	**Designing Sequential Circuits**	State Machines	*Assignment Work on Designing Sequential Circuits*	*Practical: Logisim*
10*	**2 + 1**	**Simple Computer Design**	CPU Basics; Von Neumann Machine Architecture	Textbook: Chapter 4 *Reading & self-study (section 4.1)*	*Practical: Logisim*
11*	**2 + 1**	**Instruction Cycle**			*Practical: MARIE*

12		*Revision/Consultation (No Lecture)*			
13		*Revision/Consultation (No Lecture)*			

Abbreviations: L: Lectures, P: Practicals, T: Tutorials, V: Visits, S: Seminars

SEMESTER 2 WORKPLAN (TENTATIVE)

Wk(s)	Hr(s)	Theme(s)	Title(s)	Further Reading and Self-Learning Activities	L, P, S, V, T , Test
1*	**2 + 1**	Memory System and Organisation	Memory Hierarchy, Memory Organization | Simultaneous Vs Hierarchical	*Refer to module web page*	*Practical: MARIE*
2*	**2 + 1**	Cache Memory System and Architecture	Cache Memory, Multi-level Cache Organization Cache Mapping Techniques	*Refer to module web page*	*Practical: MARIE*
3*	**2 + 1**	Memory System Organisation and Architecture,	Direct Mapping Implementation & Formulas, Problems On Direct Mapping	*Refer to module web page*	*Practical: MARIE*
4*	**2 + 1**	Memory Organisation & Hierarchy	K-way Set Associative Mapping | Implementation & Formulas Problems On Set Associative Mapping	*Refer to module web page*	*Practical: MARIE*
5*	**2 + 1**	Cache Management & Design	Cache Line, Effects of Changing Cache Line Size	*Refer to module web page*	*Practical: MARIE*
6		**CLASS TEST 2**		*Refer to module web page*	
7*	**2 + 1**	Magnetic Disk	Magnetic Disk, Important Formulas, Practice Problems On Disk Formulas	*Refer to module web page*	*Practical: MARIE*
8*	**2 + 1**	Addressing Modes	Addressing Modes, Types and their Applications, Syntax of Addressing Modes	*Refer to module web page*	*Practical: MARIE*

9*	**2 + 1**	Modern Computer Architectures: System Bus	System Bus, Components of System Bus	*Refer to module web page*	*Practical Assessment*
10*	**2 + 1**	Functional Organisation: Pipelining	Introduction to Pipelining, Pipelined Architecture	*Refer to module web page*	*Practical: MARIE*
11*	**2 + 1**	Pipelining & Performance of Computer System	Pipeline Execution, Performance | Formulas, Problems On Pipelining	*Refer to module web page*	*Practical: MARIE*
12		*Revision/Consultation (No Lecture)*		*Refer to module web page*	
13		*Revision/Consultation (No Lecure)*		*Refer to module web page*	

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10. RECOMMENDED BOOKS/JOURNALS/WEBSITES

1. Computer Organization and Architecture: Designing for Performance, 8th Edition, William Stallings, Copyright: 2010, Publisher: Prentice Hall, (ISBN-10: 0136073735, ISBN-13: 9780136073734), Published: 04/03/2009.

2. Computer System Architecture, 3rd Edition, Morris Mano, Publisher: Prentice Hall

3. Computer Architecture, A quantitative approach, Fourth Edition, John L. Hennessy & David A. Paterson, Publisher, Morgan Kauffman

4. *The Essentials of Computer Organization and Architecture – by Linda Null and Julia Lobur*

11. ESSAY(S)/ASSIGNMENT(S)/PRACTICAL(S)

Title	Maximum Marks	Last Submission Date
1. Combinational & Sequential Circuit Design	**10%**	**Semester 1 (To Be Announced)**
2. Assembly-Level Machine Organisation	**10%**	**Semester 2 (To Be Announced)**

12. ASSESSMENT

(i) Written Examination

Paper Structure	
Sections (if any): (Section A) Semester 1 & (Section B) Semester 2	No. of questions to be answered: **FOUR (4)**
Multiple Choice Questions: TWO (2)	Compulsory Questions (if any): All
Exams date: **May-June 2025**	Paper Duration: ***(3) Hours***
Weighting (%): **60%**	
Total Marks: **100**	Pass Mark: **40**

(ii) Continuous Assessment

	Weighting (%)
Practical/Assignment(s): Semester 1	10%
Practical/Assignment(s): Semester 2	10%
Seminar(s):	-
Test(s): Semester 1 & 2	20% (10 + 10)
Other(s):	-
Total Marks:	**40%**

13. OFFICE HOURS

As per time-table or by appointment

14. PORTFOLIO REQUIREMENT

All students should keep a portfolio of all coursework for their respective Programme of studies and same should be made available upon request, to the Faculty/Centre Examination Office.

15. OTHER INFORMATION

On plagiarism and cheating:

Plagiarism and cheating will not be tolerated. It will be dealt with according to the policies of the University of Mauritius regarding academic dishonesty. Please read these policies at http://mysites.uom.ac.mu/uomintranet/students/Student_Charter.pdf

16. APPROVAL BY HEAD OF ICT DEPARTMENT

Module Catalogue approved at Departmental Meeting *(where applicable)* on: …….....

Head of ICT Department
Signature: …….....

A copy of the approved Module Catalogue has to be submitted to the relevant Dean of Faculty for records purposes.