Digital Logic Revision Questions for BCA first semester.

Objective Type Questions.

Circle (◯) the correct answer in the following questions.

1. Which one of the following is binary equivalent of $(101)_8$?
   a) 100000001 b) 111000001
   c) 001000001 d) 101101000
2. Which one of the following is 2's complement of 1010.101?
   a) 0101.011 b) 1101.011
   c) 0110.110 d) 1100.011
3. Which of the following is 1's complement of 10110.0110?
   a) 11001.100 b) 01001.1101
   c) 01001.1001 d) 01001.1000
4. Which of the following is 10's complement of 0.3267?
   a) 0.6734 b) 0.6733
   c) 0.7733 d) 0.5733
5. Which of the following is 9's complement of 25.639?
   b) 73.360 b) 74.361
   c) 75.630 d) 74.360
6. An IC has …….. size
   a) Very large
   b) Large
   c) Extremely small
   d) None of the above
7. ICs are generally made of ……
   a) Silicon
   b) Germanium
   c) Copper
   d) None of the above
8. ICs are the most commonly used
   a) Thin films
   b) Monolithic
   c) Hybrid
   d) None of the above
9. An audio amplifier is an example of ……
   a) Digital IC
   b) Linear IC
   c) Both digital and linear IC
   d) None of the above
10. If each successive code differs from its preceding code by a single bit only, then this code is called
    a) BCD Code
    b) Gray Code
    c) Weighted Code
    d) Binary Code
11. The ASCII code is basically
    a) 4 bit code
    b) 5 bit code
    c) 8 bit code
    d) 7 bit code
12. What is the BCD code of $(305)_{10}$?
    a) 011000101 b) 101000110
    c) 011011101 d) 011001101

13. Which of the following is Gray code of 1010?

a) 1111 b) 1000

c) 1001 d) 1010

14. Which one of the following is Excess-3 code of 1011?

a) 1111 b) 1011

c) 1110 d) 1101

15. The output of an AND gate with three inputs, A, B, and C, is HIGH when _____.
a) A=1, B=1, C=0
b) A=0, B=0, C=0
c) A=1, B=1, C=1
d) A=1, B=0, C=1

16. If a 3-input NOR gate has eight input possibilities, how many of those possibilities will result in a HIGH output?
a) 1
b) 3
c) 7
d) 8

17. Which of the following GATE's output is 1 only when all the input values are same?

a) NAND b) NOR

c) XOR d) XNOR

18. TTL operates from a _____.
a) 9 volt supply
b) 6 volt supply
c) 5 volt supply
d) 12 volt supply

19. The expression for Absorption law is given by _____

a) A + AB = A

b) A + AB = B

c) AB + AA' = A

d) A + B = B + A

20. According to Boolean law: A + 1 = ?

a) 1

b) A

c) 0

d) A'

21. De Morgan's theorem states that _____

a) (AB)' = A' + B'

b) (A + B)' = A' * B

c) A' + B' = A'B'

d) (AB)' = A' + B

22. Complement of the expression A'B + CD' is _____

a) (A' + B)(C' + D)

b) (A + B')(C' + D)

c) (A' + B)(C' + D)

d) (A + B')(C + D')

23. A Karnaugh map (K-map) is an abstract form of _____ diagram organized as a matrix of squares.

a) Venn Diagram

b) Cycle Diagram

c) Block diagram

d) Triangular Diagram

24. There are _____ squares in a 4-variable K-map.

a) 12

b) 16

c) 18

d) 8

25. Product-of-Sums expressions can be implemented using _____

a) 2-level OR-AND logic circuits

b) 2-level NOR logic circuits

c) 2-level XOR logic circuits

d) Both 2-level OR-AND and NOR logic circuits

26. Don't care conditions can be used for simplifying Boolean expressions in _____

a) Registers

b) Terms

c) K-maps

d) Latches

27. K-map is used for _____

a) logic minimization

b) expression maximization

c) summing of parity bits

d) logic gate creation

28. To display time in railway stations which digital circuit is used?

a) seven segment decoder

b) eight segment encoder

c) 8:3 multiplexer

d) 9 bit segment driver

29. A circuit that changes a code into a set of signals is called

a) Encoder

b) Decoder

c) Multiplexer

d) Data selector

30. Device which converts input device state into a binary representations of ones or zeros is termed as

a) Decoder

b) Encoder

c) Multiplexer

d) Data Selector

31. Which of the following is analogous to multiplexer?

a) Data selector

b) Data multiplexer

c) Data filter

d) None of the mentioned

32. Which of the following is not a multiplexer?

a) 8-to-1 line

b) 16-to-1 line

c) 4-to-1 line

d) 1-to-4 line

33. The two input multiplexer would have

a) 1 select line

b) 3 select lines

c) 4 select lines

d) 2 select lines

34. How many outputs are on a BCD decoder?

a) 4
b) 16
c) 10
d) 8

35. What is the function of an enable input on a multiplexer chip?

a) To apply V_{cc}
b) To connect ground
c) To active the entire chip
d) T active one half of the chip

36. Most DE multiplexers facilitate which type of conversion?

a) Decimal to hexadecimal
b) Single input, multiple outputs
c) AC to DC
d) Odd parity to even parity

37. Which of the following are building blocks of encoders?

a) NOT gate
b) AND gate
c) OR gates
d) XOR gate

38. BCD to seven segment conversion is a

a) Decoding process
b) Encoding process
c) Comparing process
d) None of the mentioned

39. Total number of inputs in a half adder is _____

a) 2

b) 3

c) 4

d) 1

40. If A and B are the inputs of a half adder, the sum is given by _____

a) A AND B

b) A OR B

c) A XOR B

d) A EX-NOR B

41. If A and B are the inputs of a half adder, the carry is given by _____
    a) A AND B
    b) A OR B
    c) A XOR B
    d) A EX-NOR B
42. If A, B and C are the inputs of a full adder then the sum is given by _____
    a) A AND B AND C
    b) A OR B AND C
    c) A XOR B XOR C
    d) A OR B OR C
43. How many AND, OR and EXOR gates are required for the configuration of full adder?
    a) 1, 2, 2
    b) 2, 1, 2
    c) 3, 1, 2
    d) 4, 0, 1
44. ROM has the capability to perform _____
    a) Write operation only
    b) Read operation only
    c) Both write and read operation
    d) Erase operation
45. Since, ROM has the capability to read the information only then also it has been designed, why?
    a) For controlling purpose
    b) For loading purpose
    c) For booting purpose
    d) For erasing purpose
46. The ROM is a _____
    a) Sequential circuit
    b) Combinational circuit
    c) Magnetic circuit
    d) Static circuit
47. ROM is made up of _____
    a) NAND and OR gates
    b) NOR and decoder
    c) Decoder and OR gates
    d) NAND and decoder
48. In ROM, each bit combination that comes out of the output lines is called _____
    a) Memory unit
    b) Storage class
    c) Data word
    d) Address

49. The inputs in the PLA is given through _____

a) NAND gates

b) OR gates

c) NOR gates

d) AND gates

50. PLA contains _____

a) AND and OR arrays

b) NAND and OR arrays

c) NOT and AND arrays

d) NOR and OR arrays

51. PLA is used to implement _____

a) A complex sequential circuit

b) A simple sequential circuit

c) A complex combinational circuit

d) A simple combinational circuit

52. A PLA is similar to a ROM in concept except that _____

a) It hasn't capability to read only

b) It hasn't capability to read or write operation

c) It doesn't provide full decoding to the variables

d) It hasn't capability to write only

53. PAL circuit consists of

a) Fixed OR and programmable AND logic

b) Programmable OR and fixed AND logic

c) Fixed OR and fixed AND logic

d) Programmable OR and programmable AND logic

54. The basic latch consists of_____

a) Two inverters

b) Two comparators

c) Two amplifiers

d) Two subtractors

55. If Q = 0, the output is said to be_____

a) Previous state

b) Current state

c) Set

d) Reset

56. Latches constructed with NOR and NAND gates tend to remain in the latched condition due to which configuration feature?

a) Low input voltages

b) Synchronous operation

c) Gate impedance

d) Cross coupling

57. The truth table for an S-R flip-flop has how many VALID entries?

a) 1

b) 2

c) 3

d) 4

58. How many types of sequential circuits are?
    a) 2
    b) 3
    c) 4
    d) 5

59. The sequential circuit is also called _____
    a) Flip-flop
    b) Latch
    c) Strobe
    d) Adder

60. The output of latches will remain in set/reset until _____
    a) The trigger pulse is given to change the state
    b) Any pulse given to go into previous state
    c) They don't get any pulse more
    d) The pulse is edge-triggered

61. How is a *J-K* flip-flop made to toggle?
    a) J=0, K=0
    b) J=1, K=0
    c) J=0, K=1
    d) J=1, K=1

62. On a master-slave flip-flop, when is the master enabled?
    a) When the gate is LOW
    b) When the gate is HIGH
    c) Both of the above
    d) Neither of the above

63. Which of the following is correct for a gated D flip-flop?
    a) The output toggles if one of the input is high
    b) Only one of the inputs can be HIGH at a time
    c) The output complement follows the input when enabled
    d) Q output follows the input D when the enable is HIGH

64. A J-K flip-flop is in a "no change" condition when _____.
    a) J=1, K=1
    b) J=1, K=0
    c) J=0, K=0
    d) J=0, K=1

65. The toggle condition in a master-slave J-K flip-flop means that Q and $\bar{Q}$ will switch to their _____ state(s) at the _____.
    a) Opposite, active clock edge
    b) Inverted , positive clock edge
    c) Quiescent, negative clock edge
    d) Reset, synchronous clock edge

66. What is one disadvantage of an S-R flip-flop?
    a) It has no enable state
    b) It has an invalid state
    c) It has no clock input
    d) It has only a single output

67. In digital logic, a counter is a device which _____
    a) Counts the number of outputs
    b) Stores the number of times a particular event or process has occurred
    c) Stores the number of times a clock pulse rises and falls
    d) Counts the number of inputs

68. A counter circuit is usually constructed of _____
    a) A number of latches connected in cascade form
    b) A number of NAND gates connected in cascade form
    c) A number of flip-flops connected in cascade
    d) A number of NOR gates connected in cascade form

69. Ripple counters are also called _____
    a) SSI counters
    b) Asynchronous counters
    c) Synchronous counters
    d) VLSI counters

70. Synchronous counter is a type of _____
    a) SSI counters
    b) LSI counters
    c) MSI counters
    d) VLSI counters

71. BCD counter is also known as _____
    a) Parallel counter
    b) Decade counter
    c) Synchronous counter
    d) VLSI counter

72. The parallel outputs of a counter circuit represent the _____
    a) Parallel data word
    b) Clock frequency
    c) Counter modulus
    d) Clock count

73. Based on how binary information is entered or shifted out, shift registers are classified into _____ categories.
    a) 2
    b) 3
    c) 4
    d) 5

74. A shift register that will accept a parallel input or a bidirectional serial load and internal shift features is called as?
    a) Tristate
    b) End around
    c) Universal
    d) Conversion

75. What is meant by the parallel load of a shift register?
    a) All FFs are preset with data
    b) Each FF is loaded with data, one at a time
    c) Parallel shifting of data
    d) All FFs are set with data

76. What type of register would have a complete binary number shifted in one bit at a time and have all the stored bits shifted out one at a time?
    a) Parallel-in Parallel-out
    b) Parallel-in Serial-out
    c) Serial-in Serial-out
    d) Serial-in Parallel-out

77. How much storage capacity does each stage in a shift register represent?
    a) One bit
    b) Two bits
    c) Four bits
    d) Eight bits

Short Questions:

Combinational Logic Circuit

Q. Explain Gray code with suitable examples along with its applications.
Q. Subtract (797.4 – 67.6) using both 10's and 9's complement.
Q. Subtract ($111000.110)_2 – (110100.101)_2$ using both 2's and 1's complement.
Q. Perform A – B, -A + B, A + B, B – A
i) A = +15 and B= - 25
ii) A= +10 and B = +25
iii) A=17 and B = -29
iv) A=8 and B = +12
Q. What is Boolean algebra? Write its common postulates.
Q. State duality principle.
Q. State and prove De-Morgan's Theorem.
Q. Simplify the given function using algebraic method to a minimum number of literals.
xy + x'z + yz
Q. Express the given function in sum of minterms.
F = y'z + wxy' + wzx' + w'x'z'
Q. Express the given function in product of maxterms.
F = xy + x'z
Q. What is Universal Logic Gate? Realize NAND Gate as an Universal Logic Gate.
Q. What is Universal Logic Gate? Realize NOR Gate as an Universal Logic Gate.
Q. Simplify (Using k-map) the given Boolean function in both SOP and POS using the don't care condition d:
F= BC'D' +BCD' + ABCD'
d = B'CD' + A'BC'D
Q. Simplify (Using k-map) the given Boolean function in both SOP and POS using the don't care condition d:

$$F(A,B,C,D) = \pi(0,1,3,7,8,12) and\ \pi d(10,13,14)$$

Q. Simplify (Using k-map) the given Boolean function in both SOP and POS using the don't care condition d:

$$F(A,B,C,D) = \sum m\,(0,1,3,7,8,12) and \sum m\,d\ (5,10,13,14)$$

Q. Write differences between combinational and Sequential logic circuits.
Q. What is Half-Adder?
Q. What is Half- Subtractor?
Q. Implement a full subtractor with two half subtractors and an OR Gate.
Q. Implement a full adder circuit with a decoder and two OR gates.
Q. What is Multiplexer?
Q. What is De-Multiplexer?
Q. What is decoder? Draw logic diagram and truth table of 3 – to – 8 line Decoder.
Q. What is encoder? Draw logic diagram and truth table of octal to binary encoder.
Q. Implement the given combinational logic function using ROM.

Inputs		Outputs	
A1	A0	F1	F2
0	0	0	1
0	1	1	0
1	0	1	1
1	1	1	0

Q. Differentiate between PLA and PAL.
Q. Mention any two differences between the edge triggering and level triggering.
Q. State a limitation of SR flip-flop.
Q. Realize T-FF from JK-FF.
Q. Convert JK flip-flop to T flip-flop.
Q. Compare the logics of synchronous counter and ripple counter.
Q. How do you eliminate the race around condition in a JK flip-flop?
Q. What are the applications of Flip-Flops?

Q. Define SR latch with logic diagram and truth table.

Long Questions:

1. Explain the steps to implement or design combinational logic circuit.
2. Explain BCD Adder with proper logic circuit diagram.
3. Explain BCD to Decimal Decoder with truth table and logic diagram.
4. Explain BCD to Excess-3 code converter with truth table and logic diagram.
5. What is 4 bit magnitude comparator? Design 4 bit magnitude comparator.
6. Explain full adder with proper logic circuit diagram.
7. Explain full subtractor with proper logic circuit diagram.
8. Design a combinational circuit whose input is a four-bit number and whose output is the2's complement of the input number.
9. Implement the following function:
   F= $\sum(0, 1, 3, 4, 5, 7)$ using
   i) Decoder
   ii) Multiplexer
   iii) PLA
10. Implement the following Boolean expression with the help of programmable logic array (PLA)
    X = AB + AC'
    Y = AB' +BC + AC'
11. Explain JK flip flop with logic diagram, Characteristic table and characteristic equation.
12. Define counters. Draw the logic diagram for ripple counter that count from 0000 to 1111. Explain how it counts the numbers.
13. Design a Mod-10 counter. Also draw the timing waveforms.
14. What is ring counter? Explain ring counter with diagram, timing sequence and timing diagram.
15. What is synchronous counter? Design Mod-7 Synchronous counter.
16. What do you mean by shift register? Explain the Serial-In-Serial-Out shift register.
17. Explain and draw logic diagram for 4 bit Serial In Parallel Out shift register.