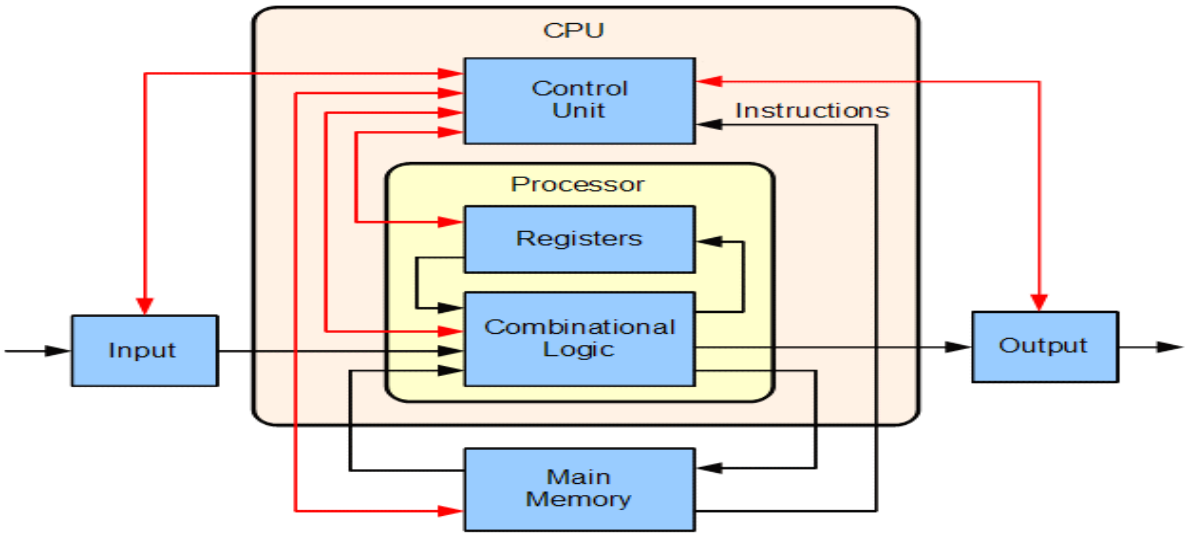
BHADRAK ENGINEERING SCHOOL & TECHNOLOGY
(BEST), ASURALI, BHADRAK

COMPUTER SYSTEM ARCHITECHTURE (TH-01)

(As per the 2020-21 syllabus of the SCTE&VT, Bhubaneswar, Odisha)



Third Semester

COMPUTER SCIENCE & ENGG.

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EXPECTED MARKS DISTRIBUTION

Chapter no	Chapter name	Expected marks
1	Basic structure of computer hardware	10
2	Instruction and instruction sequencing	15
3	Processor system	20
4	Memory system	20
5	Input output system	15
6	I/O interface and bus architecture	15
7	Parallel processing	10
Total mark		105

Chapter -1

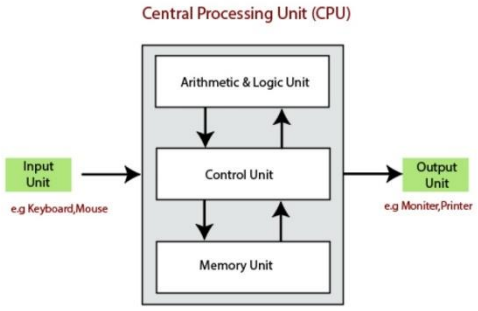
Basic structure of computer hardware

1.1 Basic structure of computer hardware

- It describes the function and design of the various unit of digital computers that store and process information.
- It also deals with the unit of the computer that receives information from the external sources and send computed result to external destinations.
- It consists of electronic circuit, displays, magnetic optical stores media and communication facilities.
- Computer architecture composess the specifications of an instruction set and the hardware units that implement the instructions.

1.2 Functional Unit

- The_computer_consists_of_five_fictional unit
  1. Input Unit
  2. Output Unit
  3. Memory Unit
  4. Arithmetic Logic Unit (ALU)
  5. Control Unit



- The input unit accepts coded information through the keyboard, mouse, scanner from the users.
- The information received is either store in the computer memory for later references or immediate used by the ALU.
- The processor process the data as per the user instructions and finally results are store in the memory and show through output unit.

1.Input Unit

- The main function of input devices is to direct to direct commands and data into computer.
- Data and institutions are entered by using various input device.
- This unit encode the data which is entered by input device.

Example-Keyboard, mouse, scanner, joystick etc.

2.Output Unit-

- The output unit receives the processed result from the processor and it decodes the processed information and show the result to the outside world.

Example-Monitor, printer, Visual Display Unit(VDU) etc.

3.Memory Unit-

- The function of memory unit is to store program and data. The program most be stored in memory while they are being executed.
- The memory contains large number of semiconductor storages each capabile of storing one bit of information.
- There are two types of storage
    a. Primary storage
    b. Secondary storage

a. Primary storage-
    - It is a fast memory that operates in electronic speed.
    - It is also named as main memory or internal memory.
      Ex-RAM, ROM

b. Secondary storage-
    - It is use when large amount of data and many programs have to be store.
    - It is also called as external memory or auxiliary memory.
      Ex-Magnetic disk, hard disk, optical disk, magnetic core, magnetic tape etc.

4.Arithmatic Logic Unit-(ALU)

- It perform the arithmetic and logic operations.
- Arithmetic operations are addition, subtraction, multiplication and division.
- Logic operations are some logical decision such as AND, OR, NOT, NOR etc.

5.Control Unit-(CU)

- CU controls the overall operations of computer and gives the decision for doing the task.

- Computer accept information and the total task and operations are control by control unit.
- It is the central nervous system of the computer.
- It manage and control all the components of computer system.

1.3 Computer Components-

- The activity in a computer is governed by instructions.
- To perform a given task an appropriate program consists of a list of instructions is store in the memory.
- Individual instructions are brought from the memory into the processor which execute the specified operations.
- Data to be use as operand are also store in the memory.
  Ex- ADD LOC A, Ro

Basic operational components of computer-

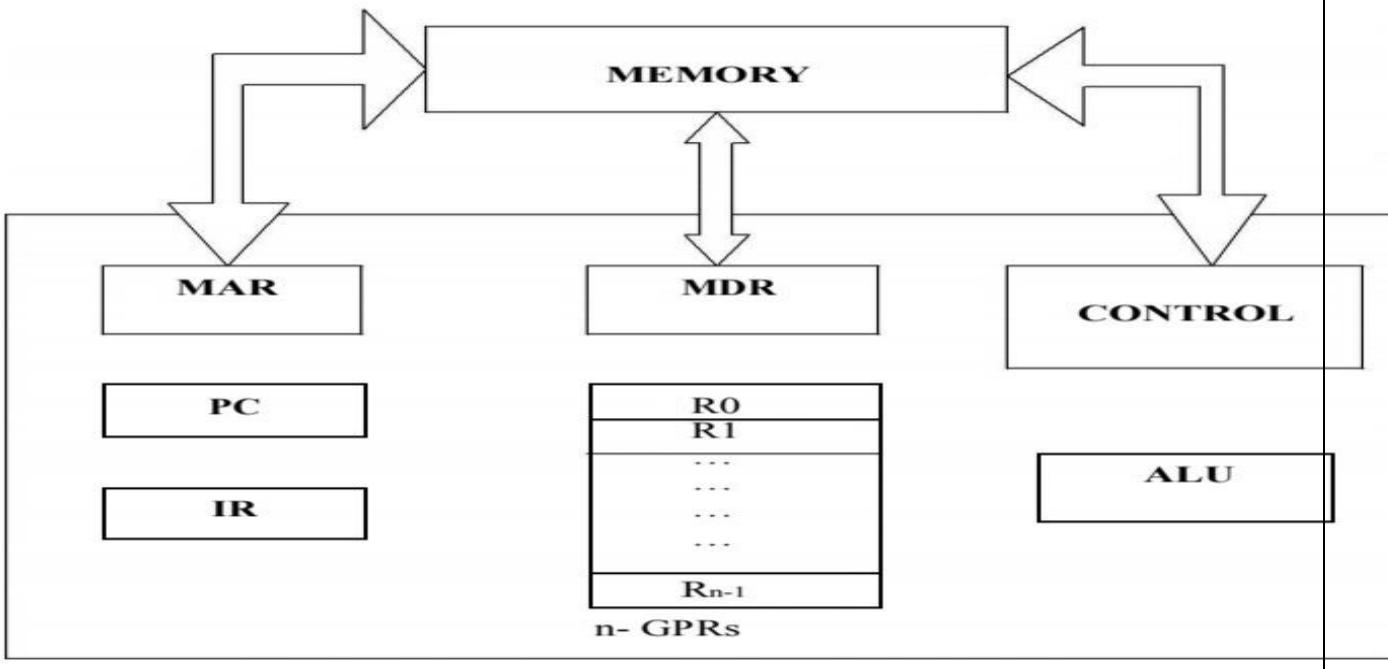


Fig b : Connections between the processor and the memory

The components used in the processor are

- MAR
- MDR
- PC
- IR
- GPR
- ALU

- CU

1.Memory Address Register-(MAR)

- MAR holds the address of the location to be accessed.
- It is a 16 bit Special purpose register.

2.Memory Data Register-(MDR)

- MDR contains the data to be written into or read out of the address location.
- Contained of MDR is transfer to IR and here instruction is decoded and executed.

3. Program counter-(PC)

- The contents of Program Counter transfer to memory address register (MAR) and read the control signal is send to the memory.
- It is one of the specialized register which contains the memory address of the next instruction to be executed.

4.Insruction Register-(IR)

- IR holds instruction that is currently being executed.
- It is also a Special purpose register.

5.General Purpose Register-(GPR)

- It is used to store temporary data to the processor.
- It contains Ro, R1…….. Rn-1 each 8 bit register.

6.Arithmatic Logic Unit-(ALU)

- ALU executed the instruction and send the result.
- It executes the all the arithmetic and logical operations.

7.Control Unit-(CU)

- It controls all the operations that are perform.
- It manage and control all the components of computer system.

1.4 Performance Measures-

- It is important to access the performance of a computer.
- Computer designer use performance estimated to evaluate the effectiveness of new features.
- Manufactural used performance indicator in marketing process.
- Based open the performance factors the System Performance Evacuation Corrupolation Estimation(SPECIAL) is given for different processors.

$$\text{SPEC rating} = \frac{\text{Running time on the reference computer}}{\text{Running time on the computer under test}}$$

1.5 Memory addressing and operation-

Memory Addressing-

- Memory consist of millions of storage which contain information in the form of 0 and 1.
- While accessing the memory a group of sell can access at a time.
- Each sell of the memory contains one bit of information.
- So a group of n- bit cab be stores and retrieved in a single operation.
- Each group of n-bits is the word of information where n is called as word length.
- For addressing of locations we use number from 0 to know for some suitable value of k.
- The memory can have up to 2^k addressable location.

Ex- if k=24 that means 24 bit address can generate 2^24=166777216

Memory operations-

- Memory operation is of two types
  1.Load-
- Load is used for both read and write operation.
  2. Store-
- Store is only used for write operation.

Short Question-

1. **What are the various functional unit used in computer ?**

- Ans- The computer consists of five fictional unit
  Input Unit
  Output Unit
  Memory Unit
  Arithmetic Logic Unit (ALU)
  Control Unit

2. **Define Program Counter? [2011 S]**

- Ans - The contents of Program Counter transfer to memory address register (MAR) and read the control signal is send to the memory.
- It is one of the specialized register which contains the memory address of the next instruction to be executed.

3. **What do you mean by IR ? [2011 S]**
   Ans-

- IR holds instruction that is currently being executed.
- It is also a Special purpose register.

4. **What is the function of MAR and MDR?**
   Ans-
   Memory Address Register-(MAR)

- MAR holds the address of the location to be accessed.

- It is a 16 bit Special purpose register.
  Memory Data Register-(MDR)

- MDR contains the data to be written into or read out of the address location.

- Contained of MDR is transfer to IR and here instruction is decoded and executed.

5.What is performance measure ?
Ans-

- It is important to access the performance of a computer.

- Computer designer use performance estimated to evaluate the effectiveness of new features.

- Based open the performance factors the System Performance Evacuation Corrupolation Estimation(SPECIAL) is given for different processors.

6.What is the function of CU ? [2011 S, 2018 W,2018 S]

Ans-

- It controls all the operations that are perform.
- It manage and control all the components of computer system.

7.What is the function of ALU ?

Ans-
ALU executed the instruction and send the result.

- It executes the all the arithmetic and logical operations.

Long Question-

1. **Give brief idea about the functional unit of computer ? [2013 S, 2020 W]**

Hints- article 1.2

2. **Explain basic operational components of computer ? [2019 W]**

Hints- article 1.3

3. **Explain the performance measure of a computer ? [2017 S, 2018 W, 2018 S, 2019 S]**

Hints- article 1.4

Chapter -2

Instruction and instruction Sequencing

2.1 Fundamental to Instruction-

- Instructions are the commands given to a computer processor buy a computer program to perform certain task searches adding two numbers ,testing for particular condition, reading a character from keyboard for sending a character to be displayed on a display screen.

Instruction sequence-

- Instruction Sequencing is the sequence order in which the instruction in a program are carried out.
- A computer must have instructions capable of performing basic operations like
- Data transfer between the memory and the processor register
- Arithmetic and logic operation on data
- Program Sequencing and control
- I/O transfer

Instruction execution-

Steps-

- The PC initialises with address that points to fist bite of instruction called opcode.
- The processes CU process the address and sends appropriate control signal to assess the bites.
- This byte is recorded to calculate the number of with the instruction.
- Now the content of PC is implemented by one.

- The final execution of the instruction is done and the result is stored in desire location. This process is called instruction execution which is known as straight line sequencing.

2.2 Operands-

- Operands are the variables at which the values are stored.
- Opcode perform their operation by the help of operands.
  Ex-ADD A, B
  A, B are the operand

2.3 Opcode-

- Opcode means operational code in machine language instruction it specify the operation to be performed.
- Their specification and format are laid out in the instruction set architecture of the processor.
  Ex-ADD, SUB, STAY, LDA, MOV

2.4 instruction formats-

- The format of an instruction is usually represented in a bits of instruction as they appear in memory records or in registers.
- The bits of instructions are divided into groups called as fields.
- The most common field found in instruction format are
  1. An **opcode field** that specifies the operation to be performed.
  2. The **address field** that specify the memory address on a processor register.
  3. A **mode field** that specifies the way that opcode of the effective address is terminated.

Types of instruction format-

- There are four types of instruction format
  1. Three address instruction
  2. Two address instruction
  3. One address instruction
  4. Zero address instruction

1.Three address instruction

- Computers with three address instruction format can use each address field to specify either a processor register or memory operand.

Ex- the program in an assembly level language that evacuate

X = (A + B)*(C + D)

Instruction operation field field	**address field**	**comments**
ADD	R1, A, B	R1←m[A]+m[B]
ADD	R2, C, D	R2←m[C]+m[D]
MUL	X, R1, R2	m[X]←R1*R2

R1 and R2 are to processor register m[X] denotes operand of memory address.

2. Two address instruction-

- Two address instruction are most common in commercial computers.
- Here each address bit can specify either a processor register or a memory word.

Ex- X = (A + B)*(C + D)

Instruction operation field field	**address field**	**comments**
MOV	R1, A	R1←m[A]
ADD	R1, B	R1←R1+m[B]
MOV	R2, C	R2←m[C]
ADD	R2, D	R2←R2+m[D]
MUL	R1, R2	R1←R1*R2
MOV	X, R	m[x]←R1

3.One address instruction-

- One address instruction use an accumulator register (AC)for data manipulation.
- For multiplication and division there is need for second register.
- Here we will neglate second register and assume that the accumulator contains the result of the operation.

Ex- X = (A + B)*(C + D)

Instruction operation field field	address field	comments
LOAD	A	AC←m[A]
ADD	B	AC←m[B]+AC
STORE	T	m[T]←AC
LOAD	C	AC←m[C]
ADD	D	AC←m[D]+AC
MUL	T	AC← AC* m[T]
STORE	X	m[x]←AC

4.Zero address instruction-

- A Stack organised computer does not use an address field or for instruction ADD and MUL.
- The PUSH and POP instruction are loaded to specify the operand that communicates in the Stack.
- This instructions are generally done by stack organised computer.
- **Ex- X = (A + B)*(C + D)**

Instruction operation field field	address field	comments
PUSH	A	TOS←A
PUSH	B	TOS←B
ADD		TOS←A+B
PUSH	C	TOS←C
PUSH	D	TOS←D
ADD		TOS←C+D
MUL		TOS←(C+D) *(A+B)
POP	X	m[x]←TOS

2.5 Addressing mode-

- The different ways in which the location of an operand is specified is an instruction are referred to as addressing mode.
- The technique of specifying the address of the operands are known as addressing modes.

- The address of the operand is known as the effective address. The operation field of an instruction specifies the operation to be performed after reading from memory and placed in the control unit of CPU.
- The operand may be in accumulator, general purpose register or in some specified memory location.

Types of addressing mode-

There are various types of addressing modes.

1. Direct addressing
2. Indirect addressing
3. Immediate addressing
4. Stack addressing
5. Register addressing
6. Register indirect addressing
7. Index addressing
8. Relative addressing
9. Implied addressing
10. Base register addressing
11. Auto increment
12. Auto decrement

1. Direct addressing-

- In this mode the operand resides in the memory and its address is given directly in the address part of the instruction.
- **Ex- LDA A** => load address of the operand store of memory location A into the accumulator
  MOV Y, X => move the content of memory location X to the content of memory location Y

Advantages-

- There is no need for upper and address calculation.

2. Indirect addressing-

- The effective address of the operand is the contents of Register or memory location.
- Whose address appear in the instructions.
- **Ex-MOV R1, (5000)**
- Here 5000 is the address specified in the instruction which contain the address of the data.

3. Immediate addressing-

- This mode is simple with no operand hedge activity.
- The instruction is self contains the operands.
- The # is used to indicate that the content following the sign is the immediate operand.
- **Ex- MOV #26, R1**
  Or MVI R1, 26
- Here move the binary equivalent of 26 to the register R1 immediately.

Advantages-

- The operand is available in the instruction as soon as the instruction fatch is over.

4. Stack addressing-

- In this mode the addressing of the operand is specified by stack pointer.
- The length of the instruction is shortest because of it does not include any address of the memory location.
- The content of the stack pointer are automatically incremented or decree mented after each stack operation.
- PUSH instruction is used to sense to the content of Register pair.
- POP is used to transfer content from stack to register pair.
-

5. Register addressing-

- In this mode the operands are content of a processor register.
- The name (address) is given to the instruction.
- **Ex- ADD R1, R2**
  Here R1 and R2 are the register present in the CPU.

6. Register indirect addressing-

- In this mode the address of the operand is given directly.
- The contents of the register or register pair are the address of an operand.
- **Ex- LXI HL 2400H**
  Here load the HL pair in adress 2400H.

7. Index addressing-

- The effective address of the operand is generated for adding a constant value to the contents of the register.
- The index register is a special CPU register that contain an index value.
- The distance between the beginning address and the address of an operand is the index value stored in the index register.
- **Ex- X(Ri)**
  Where 'X ' denotes the constant value in the instruction and Ri is the name of the register available.

8. Relative addressing-

- The effective address is determined by the index more and using the program counter in case of general purpose register(Ri)
- **Ex- ADD 100(PC) ,R2**

Here program counter is used to calculate the effective address which is obtained by adding the offset bit with the content of program counter.

9. Implied addressing-

- In this case the operand specified immediately in the instruction.
- **Ex- ADD R1**
  Here add the content of R1 with the content of accumulator.

10. Base register addressing-

- It is used for relocation of the program in the memory.
- In this mode the content of the base register is added to the address part of the instruction to obtain the effective address.
- This is similar to index addressing mode except the register is now call base register in instead of index register.
- It is used for multiprogramming system.
- **Ex- ADD 20(R1) ,R2**

Here content of R2 is adding to the base register R1 with offset 20.

11.Auto increment-

- The effective address of the operand is the contents of Register specified in the instruction after assessing the operand the contents of this register are automatically incremented to point to the next item in a list.
- This is denoted by putting the specified register in parentheses.
- **Ex- (R1) +**

12.Auto decrement-

- The contents of registers specified in the instruction are fast automatically decremented and are then used as the effective address of the operand.
- **Ex- -(R1)**

Short question

1. **What do you mean by instruction format and its types ? [2013 S]**

   Ans- • The format of an instruction is usually represented in a bits of instruction as they appear in memory records or in registers.

- There are four types of instruction format

  Three address instruction
  Two address instruction

  One address instruction

  Zero address instruction

2. **What is the function of program counter ? [2019 W]**

- **Ans-** The contents of Program Counter transfer to memory address register (MAR) and read the control signal is send to the memory.
- It is one of the specialized register which contains the memory address of the next instruction to be executed.

3. **What do you mean by instruction ? [2019 S]**

Ans- Instructions are the commands given to a computer processor buy a computer program to perform certain task searches adding two numbers ,testing for particular condition, reading a character from keyboard for sending a character to be displayed on a display screen.

4. **Define operand and give an example of an operand ?**
   Ans-

- Operands are the variables at which the values are stored.
- Opcode perform their operation by the help of operands.
  Ex-ADD A, B
  A, B are the operand

5. **Define addressing mode and its types ? [2015 W]**
   Ans- • The different ways in which the location of an operand is specified is an instruction are referred to as addressing mode.

- The technique of specifying the address of the operands are known as addressing modes.
  There are various types of addressing modes.
  1. Direct addressing
  2. Indirect addressing
  3. Immediate addressing

  4.Stack addressing
5. Register addressing

6. Register indirect addressing
7. Index addressing
8. Relative addressing
9. Implied addressing
10. Base register addressing
11. Auto increment
12. Auto decrement

6. Define direct addressing mode with an example ?

Ans-

- In this mode the operand resides in the memory and its address is given directly in the address part of the instruction.

- Ex- LDA A => load address of the operand store of memory location A into the accumulator

7. Define indirect addressing mode with an example ?

Ans- • The effective address of the operand is the contents of Register or memory location.

- Whose address appear in the instructions.

- Ex-MOV R1, (5000)
- Here 5000 is the address specified in the instruction which contain the address of the data.

Long question

1. **Explain the various addressing modes available in basic computer system ? [2011 SW, 2012S,W,2018W,S,2019 W, S, 2020 W]**

   Hints- article 2.5
2. **State and explain various types of instruction format ? [2011 SW, 2012S,W,2018W,S,2019 W, S, 2020 W]**
   Hints- article 2.4

Chapter-3

Processer System

3.1 Register file

3.2 Complete instruction execution

Fetch,decorde,execution

3.3 Hard wared control

3.4 Microprogrammed control

Introduction of Processing Unit-

- Processing Unit is the unit in computing system which executes the instructions and coordinates the activities of other units of the system .
- So this unit is called instruction set processor ISP or processor .
- Processing system usually called as CPU.
- Instructions is executed by a sequence of elementary operations.

3.1 Register file-

- Register file is an array of processor register in CPU.
- In Computer Architecture ,a processor register is a small amount of available part of a CPU or other digital processor.
- Such registered are typically address by mechanism other than main memory it can be accessed more quickly.
- Register files are usually implemented by way of fast static RAM with multi parts.
- The instruction set architecture of CPU will almost always define a set of registers which are used to store data between the memory and the functional unit of the chip.

3.2 Complete instruction execution-

Fetch decode execute cycle-

- Instruction Fetch in Pulse reading of an instruction from a memory location to the CPU register.
- The instruction cycle is the cycle which the CPU follows from boot of until the computer has shut down in order to process instruction.

- It is composed of three main stages for change the stage the decode stage and the execute stage.
- In simplest CPU the instruction cycle in executed sequentially instruction being process before the next one is started.

This is a simple diagram illustrating the individual stages of the fetch-decode-execute cycle.

Fetch stage-

- The Galaxy is a special register that holds the memory address of the next instruction to be executed.
- In this case the address store in the PC is copied into the MAR and then the PC is incremented and point to next instruction to be executed.
- CPU then takes the instruction at the memory at described by the MAR and copies it into the MDR.
- The instruction in the MDR is copied into which acts as a temporary holding ground for the instruction that has fetched from memory.

Decode stage-

- During this stage the control unit(CU) will decode the instruction in the instruction register(IR) .

Execution stage-

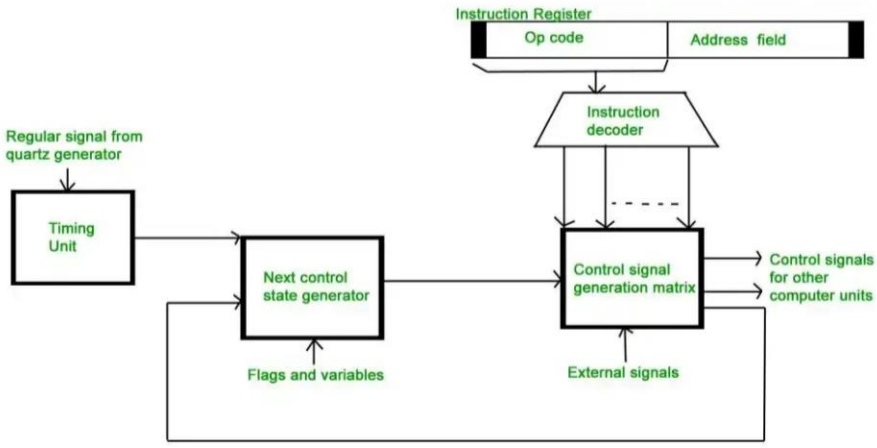
- The control unit then sends signal to other components within the CPU such as ALU.
- ALU perform on arithmetic and logic operation.

Technique for generating control signal-

- To execute instructions the processor must have some means of generating the control signals needed in the proper sequence.
- Computer designer use a wide variety of techniques to solve this problem.
  a. Hardware control
  b. Microprogram control

3.3 Hardwared control-

- Hardware control is a control mechanism that generates control signals by using an appropriate finite state machine (FSM).
- The sequence of the operation carried out by this machine is determined by the wiring of the logic elements and hence named as hardwared.



- In the above figure timing units generate a clock signal to the next control state register.

- By inputting charge and variables that controls Ltd generator generates one control signal to the input of control signal generator matrix.

- An instruction register contains two field and off code and address field. It gives the instruction to instruction decoder.

- Instruction Decoder generates a number of instructions to the control signal generation metrics. It provides a separate signal lines for each step in a control sequence.

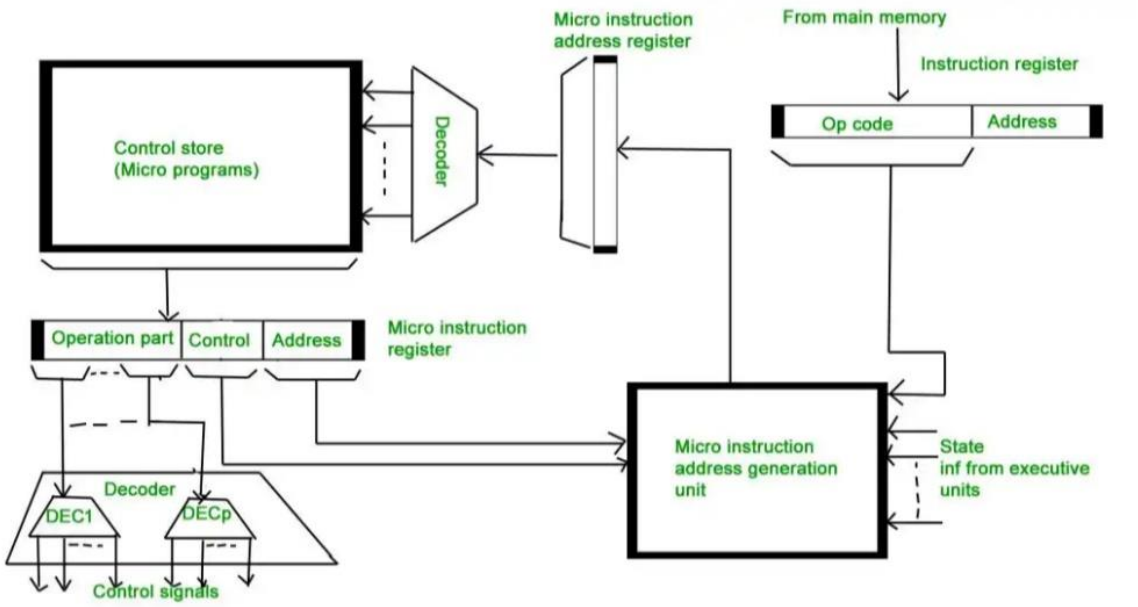
- By combining all the signal the control signal generation Matrix generate a number of control signals.

- A feedback cycle is again go to as next control state registers.

3.4 Microprogrammed control-

- Microprogram control is a control mechanism that generates control signals by reading a memory called control storage(CS) that contains control signals.
- The control signals associated with operations are stored in special memory units assessable by the programmer as control word.
- Control signal are generated by a program are similar to machine language programs.
- It is slower in speed because of time to page microinstruction from the control memory.

- Here the instruction register generates an instruction to the micro adress



generation unit again this unit is gives a signal to the decoder.

- The Decoder generates a numbers of instruction to control Store or microprogram and give signal to micro instruction register.
- Micro instruction register has three part operation part control and address. Operation part generate the signal for decoder and control and address part generate the signal for micro instruction address generation unit.
- After that the decode generate the control signals.

Difference between Hardwired control and Microprogrammed control

Hardwired Control Unit	Microprogrammed Control Unit
• Hardwired control unit generates the control signals needed for the processor using logic circuits	• Micrprogrammed control unit generates the control signals with the help of micro instructions stored in control memory
• Hardwired control unit is faster when compared to microprogrammed control unit as the required control signals are generated with the help of hardwares	• This is slower than the other as micro instructions are used for generating signals here
• Difficult to modify as the control signals that need to be generated are hard wired	• Easy to modify as the modification need to be done only at the instruction level
• More costlier as everything has to be realized in terms of logic gates	• Less costlier than hardwired control as only micro instructions are used for generating control signals
• It cannot handle complex instructions as the circuit design for it becomes complex	• It can handle complex instructions
• Only limited number of instructions are used due to the hardware implementation	• Control signals for many instructions can be generated
• Used in computer that makes use of Reduced Instruction Set Computers(RISC)	• Used in computer that makes use of Complex Instruction Set Computers(CISC)

Short Question-

1. **Define instruction set processor or ISP ?**
   Ans- • Processing Unit is the unit in computing system which executes the instructions and coordinates the activities of other units of the system .

- So this unit is called instruction set processor ISP or processor .

2. **Define register file ? [S-2019]**
   Ans-
   Register file is an array of processor register in CPU.
   In Computer Architecture ,a processor register is a small amount of available part of a CPU or other digital processor.
3. **What is the function of fetch cycle ?**

- **Ans-** the address store in the PC is copied into the MAR and then the PC is incremented and point to next instruction to be executed.
- CPU then takes the instruction at the memory at described by the MAR and copies it into the MDR.

4. **What is the function of decode cycle ?**
   Ans-

- During this stage the control unit(CU) will decode the instruction in the instruction register(IR) .

5. **What is the function of execute cycle ?**
   Ans-

- The control unit then sends signal to other components within the CPU such as ALU.
- ALU perform on arithmetic and logic operation.

6. **Define hardware control ? [S-2019]**
   Ans-

- Hardware control is a control mechanism that generates control signals by using an appropriate finite state machine (FSM).
- The sequence of the operation carried out by this machine is determined by the wiring of the logic elements and hence named as hardwared.

7. **Define microprogram control ?**
   Ans-

- Microprogram control is a control mechanism that generates control signals by reading a memory called control storage(CS) that contains control signals.
- The control signals associated with operations are stored in special memory units assessable by the programmer as control word.

Long question-

1. **Explain the complete instruction execution ? [S-2016]**
   Hints- article 3.2

2. **Explain the function of hardwared control ? [W-2014,]**
   Hints- article 3.3

3. **Explain the function of microprogram control ? [W-2015]**
   Hints- article 3.4

4. **Differentiate between microprogram control and Hardwared control ? [W-2016,W-2017,S-2018,W-2020]**
   Hints- article 3.3 & 3.4

Chapter- 4

Memory System

4.1 Memory characteristic

4.2 Memory hierarchy

4.3 Semiconductor RAM Organisation

Semiconductor ROM Organisation

4.4 Interleaved memory

4.5 Cache memory

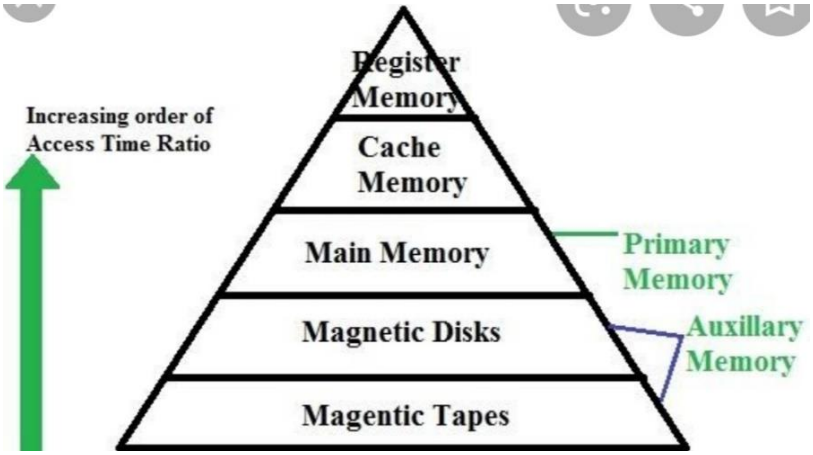
4.6 Virtual memory

4.1 Memory characteristic-

Primary memory	**Secondary memory**
1. It is very closely connected to the processor	**1.** It is outside the processor.
2. It hold program and data that the processor is actually working with.	**2** it does not hold the program and data that the processor is actively working with.
3. It is used for short time storage.	**3.** It is used for long time storage.
4. Program execution is faster.	**4.** Program execution is slower.
5. The contents is easily changed.	**5.** The contents is easily changed.
6. Relative low capacity	**6.** Relative high capacity.
7. Fast access.	**7** . Low access.
8. It is called as main memory.	**8.** It is called as auxiliary memory.
9.Its content are not organized into file.	**9.**Its content are organized into file.

4.2 Memory hierarchy-

- Memory hierarchy consists of total memory system of any computer.
- The hierarchy mainly depends upon the three parameters
  1.Access time
  2.storage capacity
  3.cost
- Primary reason that a memory system is considered as a direct she is that the cost for bait of memory .
- Technology is generally proportional to the speed of the technology.
- Computer memory can be viewed as the hierarchy.



(memory hierarchy)

1.Register memory-

- Registered memory are allocated located inside the processor and are therefore directly accessed by the CPU.
- Each registers store a word of data.
- CPU instructions instruct the Arithmetic and logic unit to perform various calculation over the data.
- Register are the fastest among all type of Computer memory.

2. Catch memory-

- Cache memory is an intermediate form of storage between the ultrafast register and the RAM.
- The CPU uses cache memory to store instructions and data that are repeatedly required to execute program.
- It improves the overall system speed and increases the performance of the computer.
- It is widely used for memory caching.

3.Main memory-(Primary memory)

- Primary memory is the type of memory that is directly accessed by the CPU.
- The CPU continuously read the instructions stored in the primary memory and execute them.
- Any data that has to be operated by the CPU is also stored there.
- Primary memory is two types one is RAM (Random Access Memory(and other one is ROM (Read Only Memory).

RAM-

- RAM is a volatile Storage Area within the computer that is typically used to store the data temporarily.
- It is of two types Static RAM(SRAM) and Dynamic RAM (DRAM) .

ROM-

- ROM is a non volatile memory which refers to computer chips containing permanent or semi permanent data.
- The types of ROM are PROM, EPROM, EEPROM.

3. Auxiliary memory-

- This memory differs from main memory is that it is not directly accessible by the CPU.
- The secondary storage device hold data even when the computer is switched off.
- Accessing speed is slow as compared to main memory.
- It has high storage space.
- Ex- magnetic disk,Magnetic tape,optical disk,magnetic Core, floppy disk, hard disk,CD ROM, USB flash devices.

4.3 Semiconductor RAM Organisation-

- The user's program in data are entered into the RAM at the time of execution.
- It has Random Access property hence any memory location can be accessed in a random way without the memory location.
- Information can be read from and written into a during normal operation.
- RAM is volatile in nature that is it contents are erased when power is turned off.
- It can be of two types static RAM and dynamic RAM.

Static RAM-

- It consists of internal flip flop that store the binary information. It is of higher cost as compared to dynamic RAM**.**
- Speed of s RAM is faster**.**
- In Islam the store information remains valid as long as the processor is on.

Dynamic RAM-

- The dynamic Ram consists of internal capacitor to store the binary information. It is a lower caste.
- The speed of the RAM is slower.
- The DRAM information is lost in a very short time even if the power supply is on.
- So there are certain mechanism to recharge the capacitor periodically.
- Capacitor must be periodically exchanged by refreshing the dynamic memory.

Semiconductor ROM Organisation-

- Read Only Memory is a nonvolatile memory is used extensively in embedded system.
- **Types of ROM**
  It is of three types
  1. PROM
  2. EPROM
  3. EEPROM

1.PROM-

- PROM starnds for Programmable read only memory.
- It can be programmed by the user only once.
- PROM provide faster and considerable less extensive the approach because they can be programmed directly by the user.

2.EPROM-

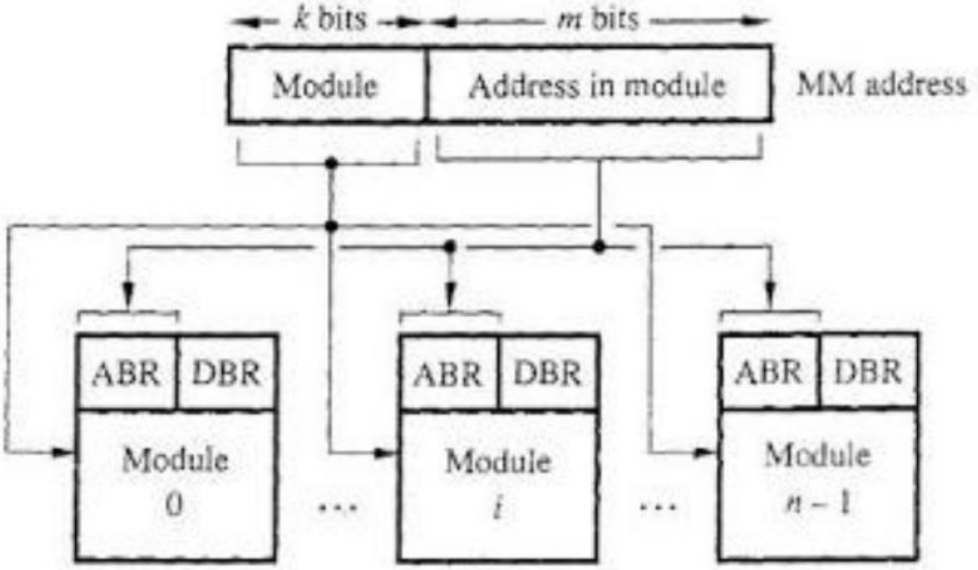
- EPROM stands for Erasable Programmable Read Only Memory.
- It provides considerable flexibility during the development phase of digital system.
- EPROM are capable of retaining store information for a large time they can be used in place of from where software is to be developed.
- In PROM we can write program only once but in EPROM the program can be erased and number of program can be rewritten number of times.
- The content of EPROM can be erased using **ultraviolet rays.**

3.EEPROM-

- EEPROM stands for Electrically Erasable Programmable Read Only Memory.
- A significant disadvantages of epidermal is that it must be physically removed from the circuit for reprogramming and that its entire contents are erased by the ultraviolet Ray.
- It is possible to implement another person of erasable proms that it can be both program and **erase electrically.**

4.4 Interleaved memory-

- The main memory of a computer is structure is a collection of physical separate models each with own Address Buffer Register(ABR) and Data Buffer Register(DBR) .
- Memory access operation may occure in more than one module at the same time.
- Does the rate of transmission of words to and from the main memory system can be increased.
- The technique in which to address the module in a more effective way is called Memory interleaving or interleaved memory.
- In this method the lower order k bits of the memory address select a module and the higher order m bits name at the address of the module.
- In this way a consecutive address located in successive module.
- Does any component of the system that generates request for easy two consecutive memory location can keep several models by at any one time. .



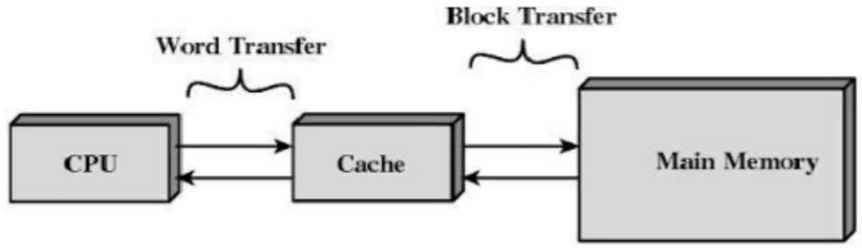
(a) Consecutive words in a module

- It is a technique for compensating the relative links Slow speed of the RAM.
- Main memory is compressed of collection of D RAM memory chief. A number of chip can be grouped together form a memory bank.
- it is possible to organise the memory banks in a way is known as interleaved memory.

4.5 Cache memory-

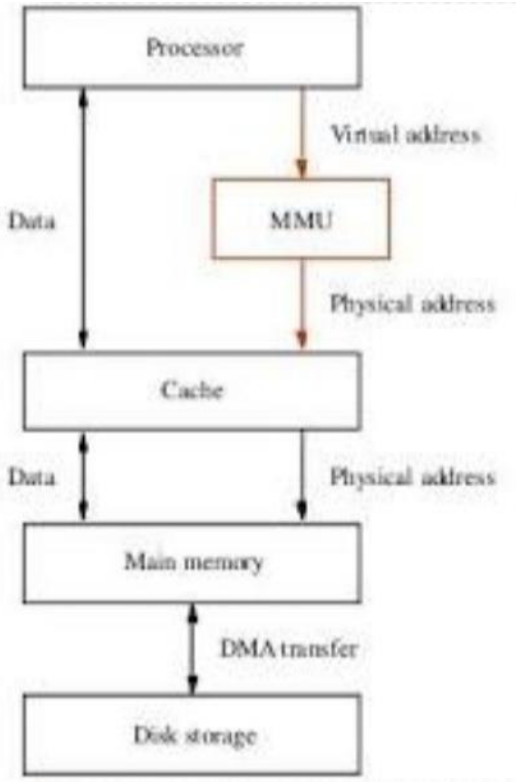
- The main purpose of cache memory is to increase the throughput of the CPU that is to increase the data transfer rate from main memory to CPU.
- If the active person of the program and the data are placed in a small memory the average memory access time can be reduced.

- Such a fast small memory is referred to as a cache memory.



- It is placed in between CPU and main memory.
- Its size is small as compared to main memory size and it is faster than main memory.
- It is made of **static RAM.**

4.6 Virtual Memory-



- The techniques that automatically move program and data blocks into the physical main memory when they are required to execution are called virtual memory technique.
- In virtual memory organisation the Memory Management Unit(MMU) translate virtual address into physical addresses.
- If the desired data or instruction are in main memory they are kept as described.
- If the desired data or instruction are not in the main memory the most be translated from secondary storage to the main memory.

- MMU causes the operating system to bring the data from the secondary storage into the main memory.
- Virtual addresses will be translated into physical addresses.
- The virtual memory mechanism bridges the size and speed gap between the main memory and secondary storage similar to catch.
- In memory hierarchy system programs and data storage store in auxiliary memory.
- The program and data are brought into main memory as they are needed by the CPU.
- Virtual memory is a concept used in same large computer system that permit the user to construct programs is through a large memory space where available equal to the totality of auxiliary memory.

Short questions-

1. **Define memory and what are the various types of it ?**
   Ans-
   Memory is **the process of taking in information from the world around us, processing it, storing it and later recalling that information**, sometimes many years later. Additionally, related to both navigation and autobiographical memory is the ability to think about events that might happen in the future.
   - Primery memory
   - Auxiliary memory
   - Resisted memory
   - Cache memory

2. **Define primary memory and its types ? [S-2015]**
   Ans-

- Primary memory is the type of memory that is directly accessed by the CPU.
- The CPU continuously read the instructions stored in the primary memory and execute them.
- Any data that has to be operated by the CPU is also stored there.
- Primary memory is two types one is RAM (Random Access Memory(and other one is ROM (Read Only Memory).

3. **Define auxiliary memory and its example?**
   Ans-

- This memory differs from main memory is that it is not directly accessible by the CPU.
- The secondary storage device hold data even when the computer is switched off.
  Example- magnetic disk, magnetic core, optical disk,floppy disk etc

4. **Differentiate between RAM and ROM ?**

Ans-

RAM-

- RAM is a volatile Storage Area within the computer that is typically used to store the data temporarily.
- It is of two types Static RAM(SRAM) and Dynamic RAM (DRAM) .

ROM-

- ROM is a non volatile memory which refers to computer chips containing permanent or semi permanent data.
- The types of ROM are PROM, EPROM, EEPROM.

5. **Differentiate between SRAM and DRAM ? [S-2013,S-2012,W-2018]**

Ans-

Static RAM-

- It consists of internal flip flop that store the binary information. It is of higher cost as compared to dynamic RAM**.**
- Speed of s RAM is faster**.**
- In Islam the store information remains valid as long as the processor is on.

Dynamic RAM-

- The dynamic Ram consists of internal capacitor to store the binary information. It is a lower caste.
- The speed of the RAM is slower.

6. **Define interleaved memory ? ? [S-2014,S-2011]**

Ans-

- The technique in which to address the module in a more effective way is called Memory interleaving or interleaved memory.
- In this method the lower order k bits of the memory address select a module and the higher order m bits name at the address of the module.

7. **What is the function of cache memory ? [S-2012,S-2014]**

Ans-

- The main purpose of cache memory is to increase the throughput of the CPU that is to increase the data transfer rate from main memory to CPU.
- If the active person of the program and the data are placed in a small memory the average memory access time can be reduced.

8. **Define virtual memory ? ? [S-2014, S-2018,W-2018,S-2019,W-2019,W-2020]**

- **Ans-** The techniques that automatically move program and data blocks into the physical main memory when they are required to execution are called virtual memory technique.

9. **Define hit rate and hit ratio ? ? [S-2015,S-2017, S-2016,W-2018,W-2019,W-2019]**

Ans-

- The no of hit started as a fraction of all attempts accessed is called hit rate.
- The performance of cache memory is frequently measured in term of a quantity called hit ratio.

Hit ratio = no. of hit / total no of CPU reference
= No of hits/ no of hit + no of miss

Long Question-

1. **Explain the characteristic of memory ? [S-2017,S-2018]**
   Hints- article 4.1

2. **Explain RAM and ROM organisation ? [S-2017,S-2018,S-2019,W-2019]**
   Hints- article 4.3

3. **Explain memory hierarchy by using suitable examples ? ? [S-2011, S-2018,W-2020]**
   Hints- article 4.2

4. **What is virtual memory and explain virtual memory organisation? [S-2011, S-2017,S-2018]**
   Hints- article 4.6

5. **Explain what is the importance of cache memory ? S-2017,S-2019]**
   Hints- article 4.5

6. **State and explain interleaved memory organisation ? [S-2014,S-2015,S-2017,S-2019,W-2020]**
   Hints- article 4.4

Chapter-5

Input output system

5.1 Input-Output Interface

5.2 Mode of data transfer

5.3 Programmed I/O transfer

5.4 Interrupt driven I/O

5.5 Direct memory access (DMA)

5.6 I/O channel architecture

5.1 Input-Output Interface-

- Interface provides a method for transferring transforming information between internal storage and external devices.
- Peripheral connected to a computer needs special communication links for interfacing them with the CPU.
- The purpose communication link is to reverse the difference that exist between the central computer and its peripherals.
- The major difference are the data transfer rate of peripheral is usually square then the transfer rate of CPU and consecutively a synchronisation mechanism may be needed.

5.2 Mode of data transfer-

- Data transfer between the central computer and the IO devices may be handled in a variety of modes.
- So mode use the CPU is a intermediate and Path,other transfer data directly to and from the memory unit.
- Data transfer to and from the Welfare and maybe handle in one of these following three possible modes
  1.programmed I/O
  2.interrupt initiated I/O
  3.Direct Memory Access(DMA)

5.3 Programmed I/O transfer –

- The program IO operation are the result of instructions written in the computer program.
- Each data transfer is initiated by an instruction in the program.
- Usually transfer is to and for CPU register and peripherals. Other instruction are needed to transfer the data to and from CPU and memory.
- Transferring data other program control required constant monitoring and peripheral by the CPU.
- Once a data transfer is initiated a CPU is required to monitor the interface transport can be again made.
- Here the CPU stays in a program loop untill the I/O unit indicate that it is ready for data transfer.
- This is a time consuming process since it keep the process busy.
- It can be avoided by using an interrupt facility and special commands to inform the interface to issue on interrupt request signal when that are available in device.

5.4 Interrupt driven I/O-

- When one program which done in a system and a new one we came for a time the interrupt is initiated.
- In this mean time the CPU can process to execute another program.
- The interfacing while keep monitor in the device.
- It is an alternative method to left CPU concentrate on some other programs and use and interrupt signal to inform CPU then I/O flag is set to 1.
- An interrupt driven IO system the device that is ready to transmit send a signal to CPU indicating that it requires data transmission.
- The CPU takes action according to the CPU response the interrupt signal by storing the return address from program counter in a memory stack and then control branches to a subroutine that processes the required IO transfer.
- The way that processor is the branch address of the subroutine there is from one unit to another.
- There are two methods :-
  a.Vector interrupt
  b.Non vectored interrupt

a. Vectored interrupt:

- In a vectored interrupt the source that interrupt supplies the branch information to the computer is called in interrupt vector.
- In some computers the interrupt vector is the first address of the service Routing.

- In other computers the interrupt vector is an address that pains to a location in memory where the beginning address of the service is stored.

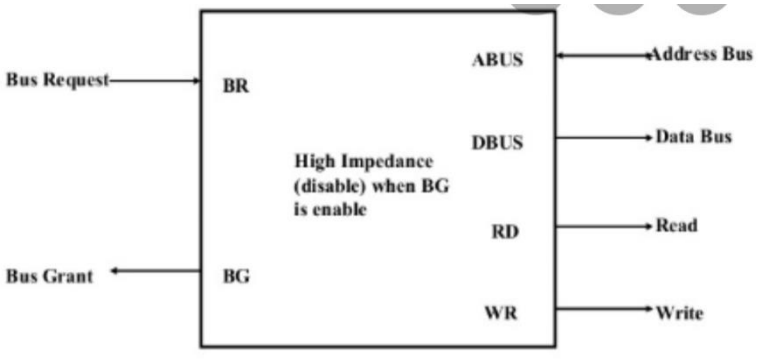
b. Non vectored interrupts:

- In a non vectored interrupt the branch address is assigned to a fixed location in memory.

5.5 Direct memory access (DMA)-

- DMA stands for Direct Memory Access.
- Direct Memory Access controller text over the buses to manage the transfer directly between the device and memory.
- In this method the I/O devices directly write or bit an information to or from the main memory without the interfacing of CPU.
- I/O devices write data or read data from main memory from memory bus.
- In this case DMA controller control the data transfer between memory and I/O devices.
- The transfer of data between a storage device such as magnetic disc and memory is often limited by speed of CPU.
- Removing the CPU from the path and the Peripheral device manage the memory process directly would improve the speed of the transfer. This is called Direct Memory Access.
- During DMA, the CPU is idle and has no control of memory buses.

DMA Controller:



CPU bus Signals for DMA Transfer

- The Bus Request(BR)input is used by the DMA input active the CPU terminate the execution of the current instruction and places the address bus,data Bus,read and write lines into a high independent state.
- The CPU activates the Bus Grand signal output to inform the external DMA and then the buses are in high independent state.

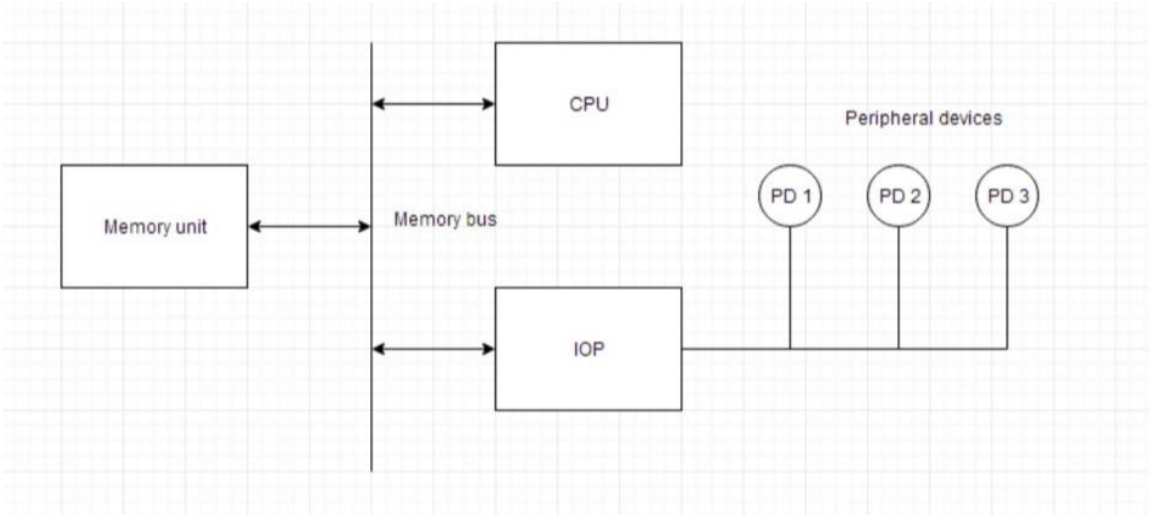
- The DMA that originate the Bus Request can now make control of the bus to conduct memory transfer without processor interference.
- When the DMA terminate the transfer it deserves the Bus request-line.
- When the DMA takes control of bus system it communicates directly with the memories.

5.6 I/O channel architecture-

- An input output processor is a processor that direct memory access the possibility to stop this the computer system is divided into a memory unit and number of processor.
- Each IOP control and manage the input output task to stop the op is similar to CPU except that it handles I/O processing.
- The IOP can fetch and execute its own instructions. This instruction are designed to manage I/O transfers only.

Block diagram of I/O processor-

- Below is a block diagram of a computer along with various processor. The memory Unit complies the central position and can communicate with each processor.
- The CPU processes that are required for solving the computational task.
- The IOP provides a path for transfer of data between peripherals and memory.
- The CPU assigns the task for installing the program. The IOP operates independent from CPU and transfer data between peripherals and memory.
- The communication between the IOP and the device is similar to the program control



method of transfer.

- And the communication with the memory is similar to the direct memory access method.
- Each processor is independent of other processor and any processor can initiate the operation in large scale computer.
- The CPU can act as master and the IOP act as slave processor.

- The CPU assigns the tasks of initiating operations but it is execute the instructions and not the CPU.
- The CPU instructions provide operations to start an I/O transfer.
- The IOP asks for CPU through interrupt.
- Instruction that are read from memory by an IOP are also called commands to distinguish them from instructions that are read by CPU.
- Commands are prepared by programmers and are stored in memory.
- Commands are make the program for IOP. CPU inform the IOP where to find the commands in memory.

Short questions:

1. Define I/O interface ?

Ans-

- Interface provides a method for transferring transforming information between internal storage and external devices.
- Peripheral connected to a computer needs special communication links for interfacing them with the CPU.

2. Define the modes of data transfer and its types ? [W-2019]

Ans-

- Data transfer between the central computer and the IO devices may be handled in a variety of modes.
- So mode use the CPU is a intermediate and Path,other transfer data directly to and from the memory unit.
- Data transfer to and from the Welfare and maybe handle in one of these following three possible modes
  1.programmed I/O
  2.interrupt initiated I/O
  3.Direct Memory Access(DMA)

3. What is programmed I/O? [S-2016,S-2018,W-2018]

Ans-

- The program IO operation are the result of instructions written in the computer program.
- Each data transfer is initiated by an instruction in the program.

4. Define interrupt driven I/O ?

Ans-

- An interrupt driven IO system the device that is ready to transmit send a signal to CPU indicating that it requires data transmission.

- The CPU takes action according to the CPU response the interrupt signal by storing the return address from program counter in a memory stack and then control branches to a subroutine that processes the required IO transfer.

5. **What is interrupt ? [S-2013,S-2014,S-2015,S-2017,W-2018]**

   Ans- An **interrupt** is a response by the processer to an event that needs attention from the software. An interrupt condition alerts the processor and serves as a request for the processor to interrupt the currently executing code when permitted, so that the event can be processed in a timely manner.

6. **Define DMA?**

   Ans-

- DMA stands for Direct Memory Access.
- Direct Memory Access controller text over the buses to manage the transfer directly between the device and memory.

7. **What is vector interrupt ? [S-2012]**

   Ans-

- In a vectored interrupt the source that interrupt supplies the branch information to the computer is called in interrupt vector.
- In some computers the interrupt vector is the first address of the service Routing.

8. **What is known non vector interrupt ?**

   Ans-

- In a non vectored interrupt the branch address is assigned to a fixed location in memory.

9. **Define I/O processor ?**

   Ans-

- An input output processor is a processor that direct memory access the possibility to stop this the computer system is divided into a memory unit and number of processor.
- Each IOP control and manage the input output task to stop the op is similar to CPU except that it handles I/O processing.

Long Question –

1. **Explain the modes of data transfer and its types ? [S-2011,S-2012,W-2015,W-2020]**

   Hints- article 5.2

2. **How interrupt initiated I/O is working ? [W-2017]**

   Hints- article 5.4

3. **Define DMA .Explain DMA method of data transfer by using suitable diagram ? [S-2016,S-2019,W-2019,W-2020]**

   Hints- article 5.5

4. **Explain working of input output processor ?**

   Hints- article 5.6

5. **Write short note on**
   a. **Programmed I/O** **Hints- article 5.3**
   b. **Vectored interrupt** **Hints- article 5.4**
   c. **DMA [S-2017]** **Hints- article 5.5**

Chapter 6

I/O interface and bus architecture

6.1 Bus and System bus

Bus-

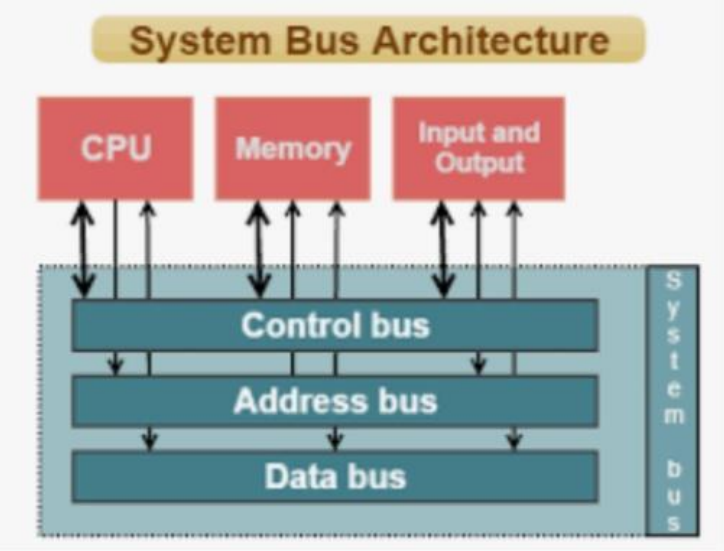
- The bus is nothing but a group of all lines responsible for data transfer.

Types of buses

- There are three types of buses
  1. System bus
     - **a.** Data bus
     - **b.** address bus
     - **c.** control bus
  2. Local bus
  3. Expansion bus

6.2 Types of System bus-

- It is a high-speed Bosch connecting high speed memory with iOS devices.
- Data transfer in system bus may be synchronous or asynchronous in nature.
- It is of three types data bus, address bus and control Bus.



a. Data bus-

- Data bus is used to transfer data.
- It is bidirectional in nature that is both input and output operation can be performed.
- It is there 8-bit bus that is 8 numbers of wires or lines are used.

b. Address Bus-

- Address bus is used to transfer the address.
- It is a unidirectional bus .
- Address bus is 18 bit bus that is it consists of 18 numbers of wires or lines.

c. Control bus-

- Control bus depends upon the status of data and address bus.
- It is a 4 bit bus.
- It is also uni-directional in nature.

2.Local bus-

- It is a high-speed bus which is used to transfer the data in general is synchronous order.

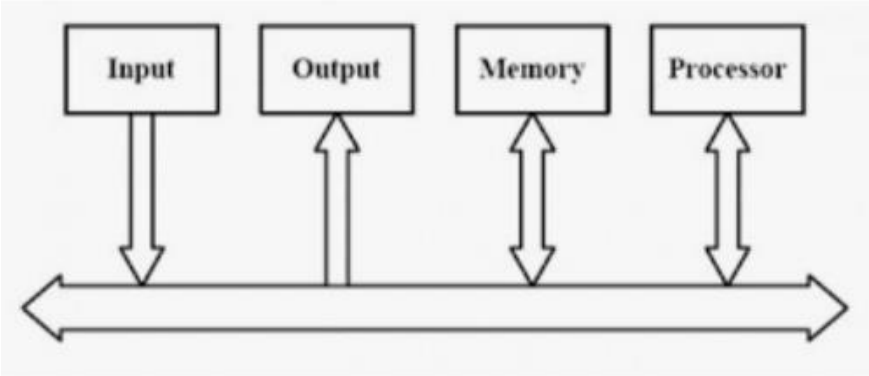
3.Expansion Bus-

- It is used to connect all kind of synchronous and asynchronous devices without interfering with the transfer between memory and processor.

6.3 Bus Structure-

- A group of lines connected to different devices for data exchange is known as Bus.
- Bus can carry that data and control signal.
- When a word of data is transferred between any two devices,all its bits are transferred in parallel manner that is the bits are transferred simultaneously over many lines one bits per line.

Single bus structure:



(Single bus stucture)

- In single bus structure the functional units are interconnected in a very simple ways.
- All units are connected to a single bus,so it provide the interconnection.

Advantages :

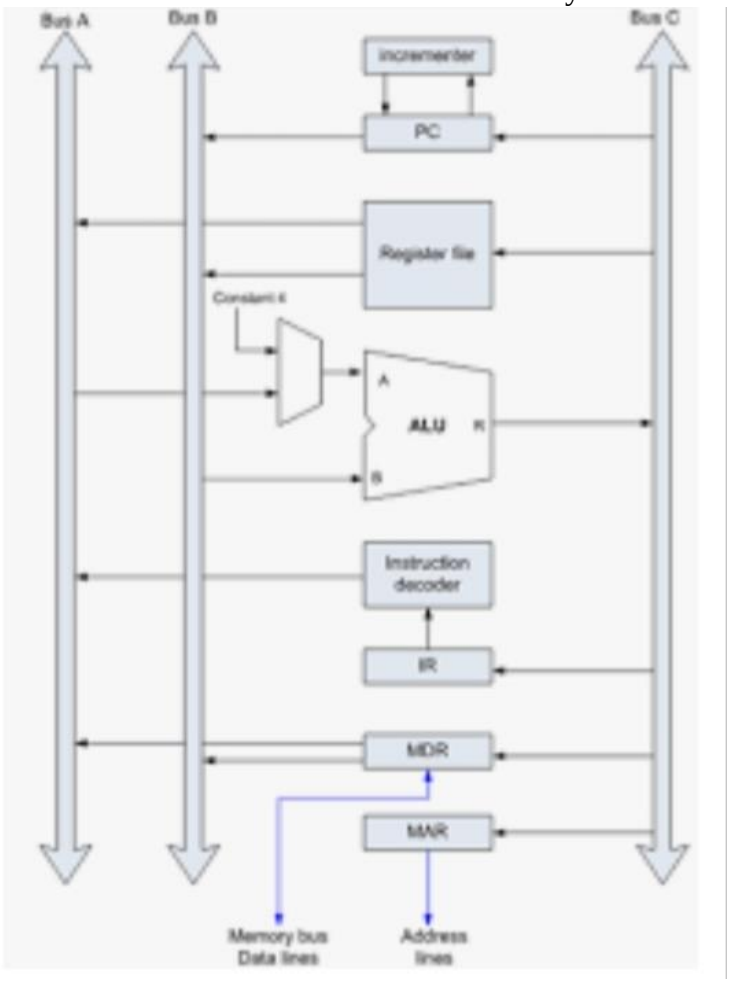
- It is of low cost and of simplicity. **Disadvantages :**
- It has limited speed. Since usually only two units can participate in a data transfer at any other time.
- Only two units can actively use the bus at any given time.
- Bus control lines are used multiple request for the use of the bus.
- Buffer register are used to hold information during transfer.

Multibus Structure-

- In multi bus Organisation all registers are combined into singing block called as register file with three ports two output line to register to be assessed simultaneously.
- Buses A and B are used to transfer source of grants to the A and B input of the ALU and result transfer to destination over bus C.

- Different unit in a system having different speed.
- Keyboard,printer are relatively slow.
- Some units are very fast all these devices communicate with each other over the same bus.

- In order to communicate at the unit simultaneously include buffer registers with the



devices to hold the data during transfer. Transfer of data between processor and printer.

- Processor sends data over the bus to print buffer.
- Once the buffer is loaded The Printer can start printing without the interaction of the processor.
- The bus and the processor are now free to do other type of work.

6.4 Basic parameters of Bus design-

- To design a bus parameters are the most essential requirement.
- The main parameter to design a bus are input,output,processor and memory.
- For a single bus structure used need only input unit, output unit, processor,memory and bus line.
- For a multibus structure used require some more parts then a single bus structure.
- In multibus structure other parameters are such as multiplexer, ALU,incrementer,register file etc with more than one bus line are required.

6.5 SCSI-

- The SCSI stands for Small Computer System Interface.
- SCSI is a set of stands for physical connecting and transforming data between computers and peripherals.
- SCSI stands define command protocols electrical and optical interface.

- It is most commonly used for hard disk and tape drives but it is it can connect a wide range of other device including scanner and CD drive.
- It is connected to the processor bus through a SCSI controller.
- This controller uses DMA to transfer data blocks from main memory to the device or vice versa.
- This may contain a block of data from the processor input device or status information from the device.
- SCSI is capable of supporting 8 device or 16 devices.

6.6 USB-

- USB stands for Universal Serial Bus.
- A modern computer system is likely to involve a wide variety of devices like keyboard,microphone, speaker and display devices.
- Most computers also have a wired or wireless connection to the internet.
- A key requirement in such an environment is the availability of a simple low cost mechanism to connect these devices to the computer and an important recent development in this regard is the introduction of the USB.
- Spread of operation called low-speed.
- It is quickly gaining acceptance in the Marketplace and with the addition of the high-speed capability it may well become the interconnection method of choice for most computer device.
- Provide a simple low cost and to use interconnection system that overcome the difficulties due to the Limited number of I/O path available on a computer.
- A wide range of data transfer characteristics for I/O devices including telephone and internet connection.

Short question:

1. **Define bus and what are the types of buses ?**
   Ans-
   - The bus is nothing but a group of all lines responsible for data transfer.
     Types of buses
   - There are three types of buses

   a. System bus
      Data bus
      address bus
      control bus
   b. Local bus
   c. Expansion bus

2. **Why the address bus is unidirectional ?**
   Ans- Address bus is Unidirectional because **the microprocessor is addressing a specific memory location**. No outside devices can not write into Microprocessor.

Data bus is Bidirectional because the Microprocessor can read data from memory or write data to the memory. Normally Control bus is unidirectional.

3. **Define system bus ? [S-2013]**
   Ans-
   - It is a high-speed Bosch connecting high speed memory with iOS devices.
   - Data transfer in system bus may be synchronous or asynchronous in nature.

4. **Differentiate between local Bus and control Bus ? [S-2012,S-2013]**
   Ans-

   Local bus-

   - It is a high-speed bus which is used to transfer the data in general is synchronous order.

   Control bus-

   - Control bus depends upon the status of data and address bus.
   - It is a 4 bit bus.
   - It is also uni-directional in nature.

5. **Define USB ? [W-2020,S-2018,W-2018]**
   Ans-
   - USB stands for Universal Serial Bus.
   - A modern computer system is likely to involve a wide variety of devices like keyboard,microphone, speaker and display devices.

6. **Define SCSI ? [S-2017,W-2020,S-2019,W-2019]**
   Ans-
   - The SCSI stands for Small Computer System Interface.
   - SCSI is a set of stands for physical connecting and transforming data between computers and peripherals.

7. **What are the types of bus structure?**
   Ans-
   Single bus structure
   Milti bus structure
8. **What is single bus structure ?**
   Ans-
   - In single bus structure the functional units are interconnected in a very simple ways.
   - All units are connected to a single bus,so it provide the interconnection.

9. **Define multibus structure ?**
   Ans-
- In multi bus Organisation all registers are combined into singing block called as register file with three ports two output line to register to be assessed simultaneously.

Long question:

1. **State and explain use of different types of buses used in computer ? ? [S-2011,S-2018,W-2018]**
   Hints- article 6.2
2. **Differentiate between single bus and multibus structure ? [W-2020]**

   Hints- article 6.3

3. **Explain about SCSI bus ? [W-2018]**

   Hints- article 6.5

4. **Write short note on:**
   a. **USB [S-2017] Hints- article 6.6**
   b. **SCSI [S-2013] Hints- article 6.5**
   c. **Bus structure [S-2012] Hints- article 6.3**

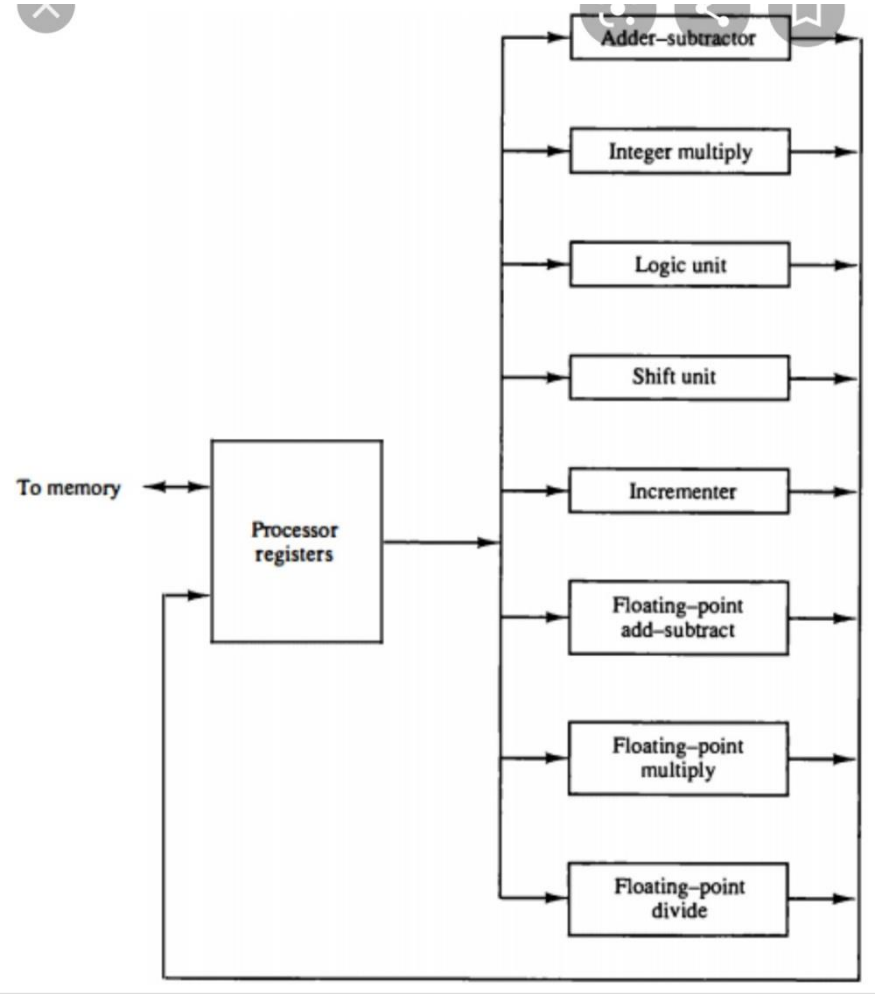
Chapter- 7

Parallel Processing

7.1 Parallel processing-

- Parallel processing is a technique that are used to provide simultaneous data Processing task for the purpose of increasing the computational speed up a computer system.
- It is able to perform concurrent data processing to active after execution time.
- For example while an instruction is being executed in the ALU, the next instruction can be read from the memory.
- The system may have two or more ALUs and be able to execute two or more instructions at the same time.
- The purpose of parallel processing is to speed up the computer processing capability and increased its throughput.
- This technique development have reduced hardware cost to the point where parallel processing technique are economically feasible.
- Parallel processing can be viewed from various level of complexity. At the lowest label registers are loaded parallel with all the bits of the word simultaneously.
- At the high level of complexity can be achieved by having a multiplicity of functional units that perform identical or different operations.

Processor with multiple functional units



7.2 linear pipelining-

- Pipeline is a technique of decomposing a sequential process into sub operations ,with each subprocess being executed in a special dedicated segment that operate operates on currently with all other segments.
- Linear pipelining are static pipeline because they are used to perform fixed functions. It allows only streamline connections.

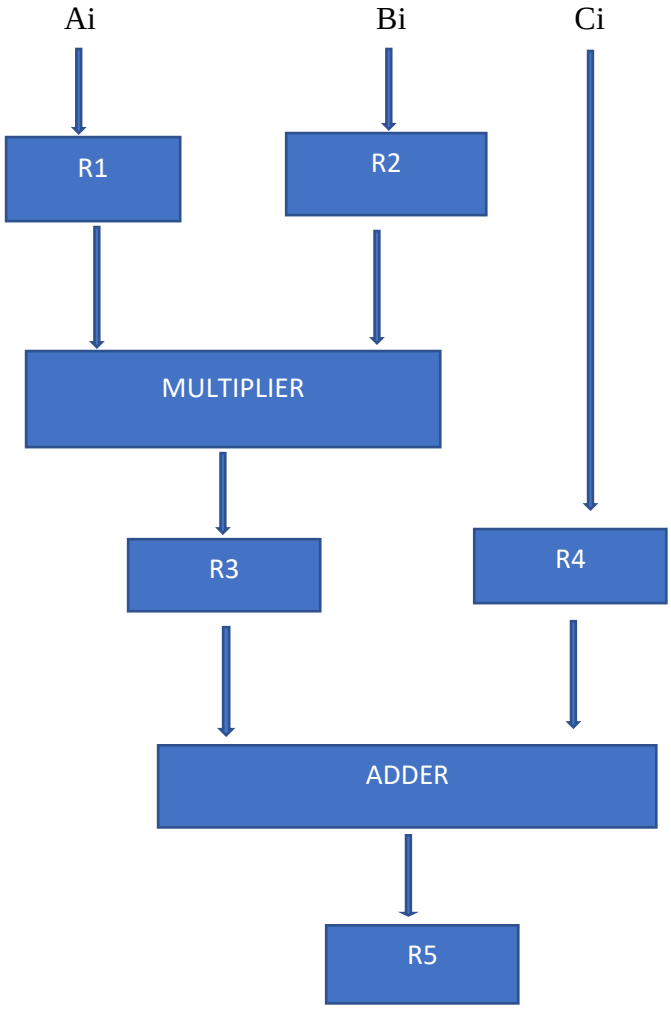
Example-

- The pipeline organisation will be demonstrated by means of a simple example.
- Suppose that we want to perform the combined multiply and add operations with a stream of numbers.

Ai *Bi+Ci for i= 1,2,……7

- Its operation is to be implemented in a segment within a pipeline.
- Each segment has one or two registers and a combinational circuit.

R1 ← Ai R2 ← Bi here Ai and Bi are input
R3← R1*R2 multiply
R4← Ci input Ci
R5← R3+R4 here add Ci to the product



- Here five registers are loaded with new data every clock pulses.

7.3 Multiprocessor-

- A multiprocessor system is an interconnection of two or more CPU with memory and input-output equipment.
- The term processor is is multiprocessor can mean either a CPU or an IO processor (IOP) .
- It improve the system performance.
- An overall function can be e partition into a number of task that each processor can handle individually.
  Example –
- In a computer where one processor perform high speed floating point mathematical computation and another takes care of routine data processing tasks.

7.4 Flynn's Classification –

- It depends on the distinction between the performance of the CU and the data Processing Unit.
- It devides computer into four major groups as follows:

1. Single Instruction stream, Single Data stream (SISD)
2. Single Instruction stream, Multiple Data stream (SIMD)
3. Multiple Instruction stream, Single Data stream (MISD)
4. Multiple Instruction stream, Multiple Data stream (MIMD)

1. SISD-

- It represents the organisation of a single computer containing a control unit, a processor unit and a memory unit.
- Instructions are executed sequentially and the system may or may not have internal parallel processing capabilities.

2. SIMD-

- It represents an organisation that includes many processing units under the supervision of a common control unit.
- All processors receive the same instruction from the control unit but operates on different items of data.
- The shared memory unit must contain multiple module so that it can communicate with all the processor simultaneously.

3. MISD-

- MISD structure is only of theoretical interest since no practical system has been constructed using this organisation.

4 .MIMD-

- This organisation refers to a computer system capable of processing several programs at the same time.

Short Questions:

1. **Define pipelining ? [W-2017]**
   Ans-

- Pipeline is a technique of decomposing a sequential process into sub operations ,with each subprocess being executed in a special dedicated segment that operate operates on currently with all other segments.

2. **Define parallel processing ? [W-2019]**
   Ans-

- Parallel processing is a technique that are used to provide simultaneous data Processing task for the purpose of increasing the computational speed up a computer system.
- It is able to perform concurrent data processing to active after execution time.
- For example while an instruction is being executed in the ALU, the next instruction can be read from the memory.

3. **Define multiprocessing system ?**
   Ans-

- A multiprocessor system is an interconnection of two or more CPU with memory and input-output equipment.
- The term processor is is multiprocessor can mean either a CPU or an IO processor (IOP) .

4. **What are the major groups of Flynn's classification ?**
   Ans-
   - Single Instruction stream, Single Data stream (SISD)
   - Single Instruction stream, Multiple Data stream (SIMD)
   - Multiple Instruction stream, Single Data stream (MISD)
   - Multiple Instruction stream, Multiple Data stream (MIMD)

5. **Define Linear pipelining ?**

Ans- Linear pipelining are static pipeline because they are used to perform fixed functions. It allows only streamline connections.

6. **What is clock cycle ? [W-2020]**
   Ans-
   The clock cycle is the amount of time between two pulses of an oscillator. It is a single increment of the central processing unit (CPU) clock during which the smallest unit of processor activity is carried out. The clock cycle helps in determining the speed of the CPU, as it is considered the basic unit of measuring how fast an instruction can be executed by the computer processor.

Long questions :

1. **State and explain the pipelining process ? ? [W-2020,S-2018,W-2019,S-2019]**
   Hints- Article 7.2
2. **Explain flynn's classification ? ? [W-2017,S-2019,W-2019]**
   Hints- Article 7.4

3. **Write short notes on**

   Pipelining [W-2018]
   Hints- Article 7.2