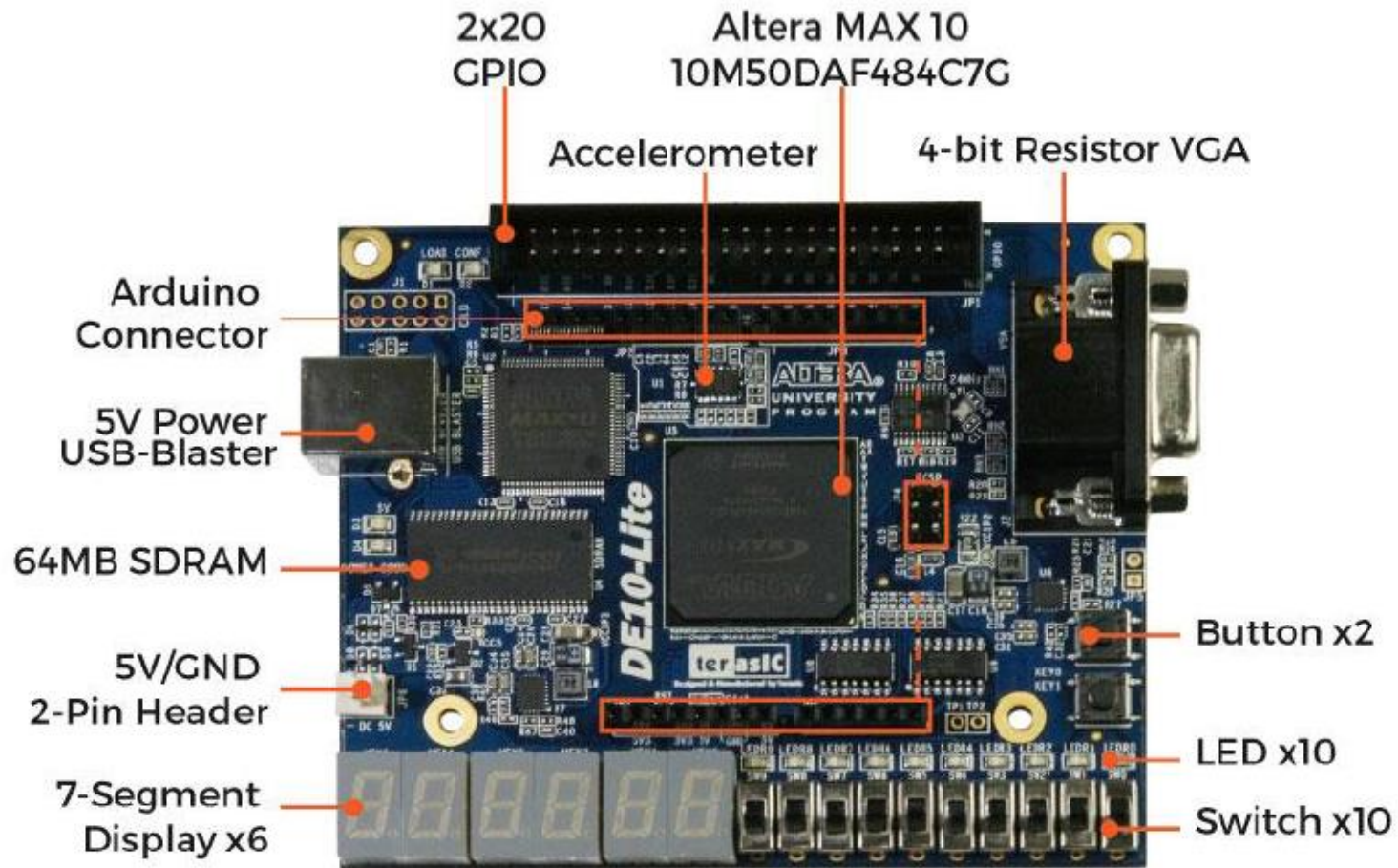


FPGA/CPLD發展環境簡介

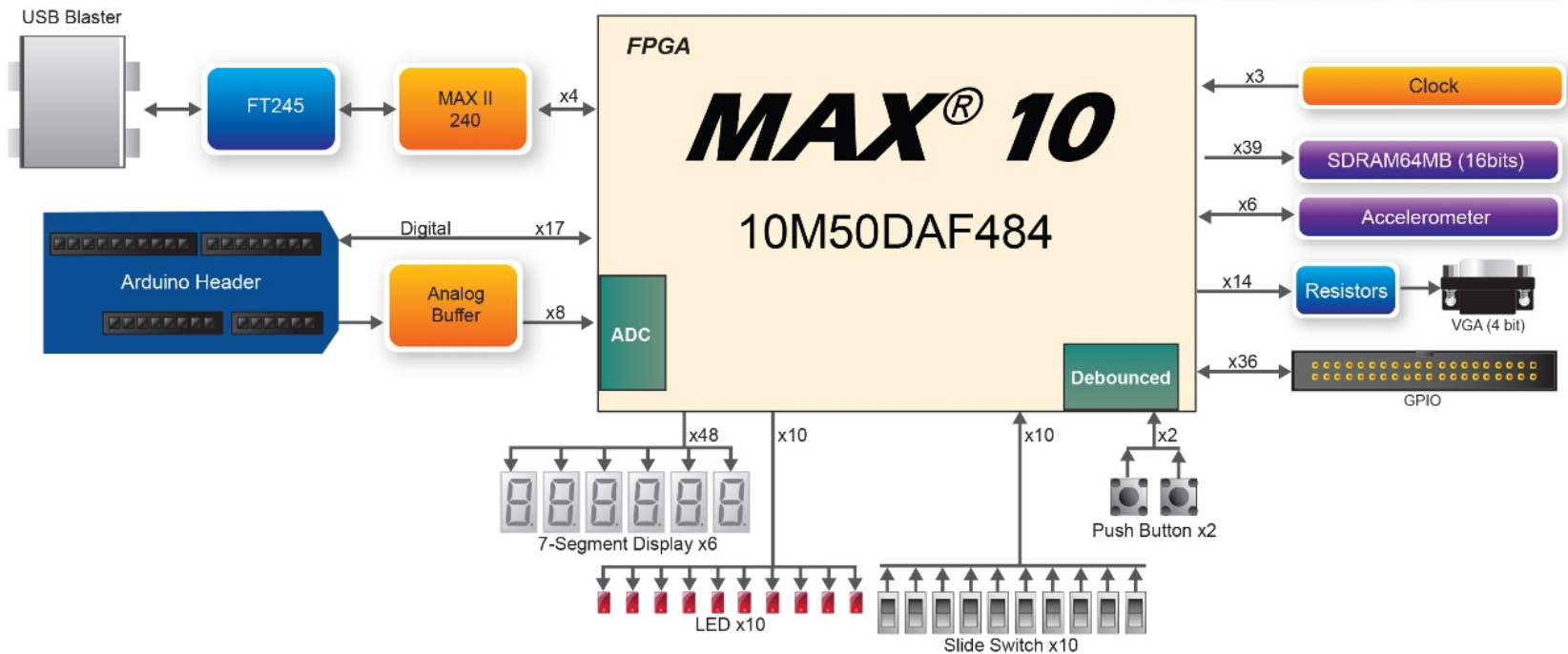
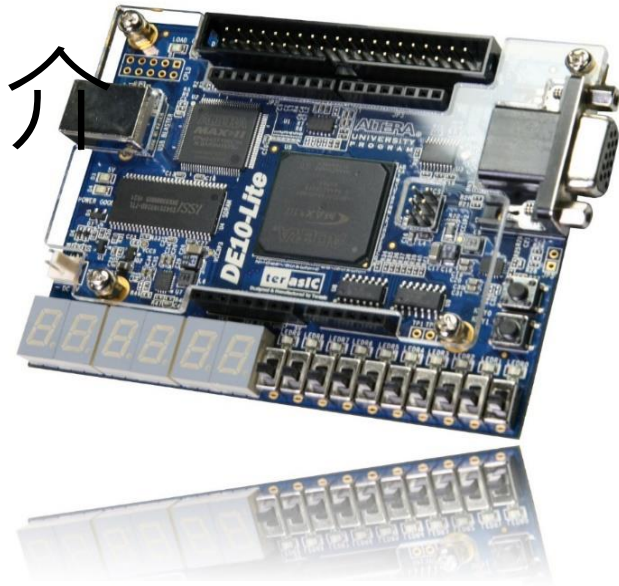
Outline

- Altera DE10 Lite實驗板簡介
（配合：如何配合使用電路文件）
- FPGA設計流程
- Quartus Prime介紹
- 課堂練習

Altera DE10實驗板簡介

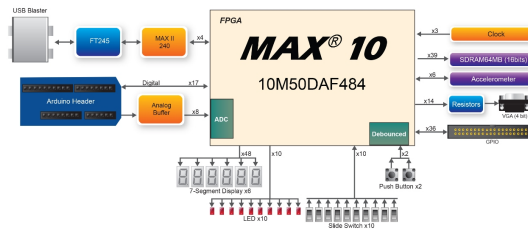
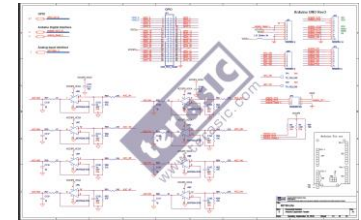
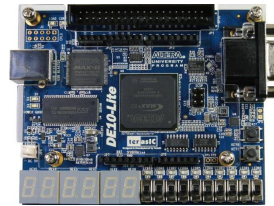


Altera DE10實驗板簡介



如何使用電路文件

- 電路板
- 電路圖
- 功能方塊圖
- 資料手冊

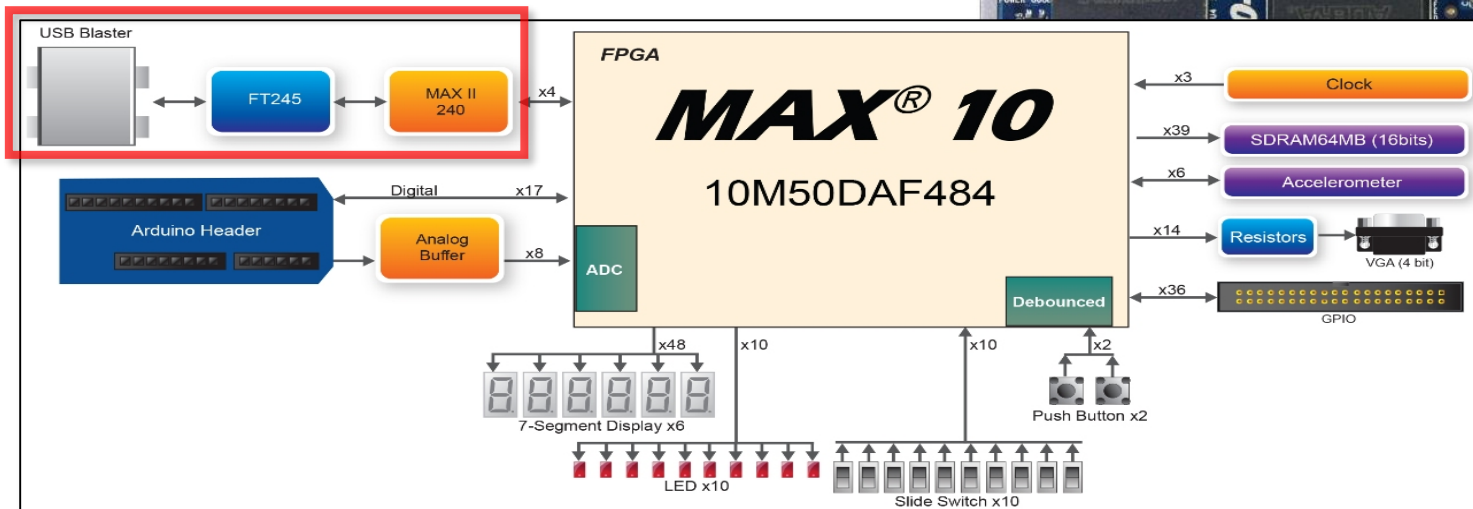
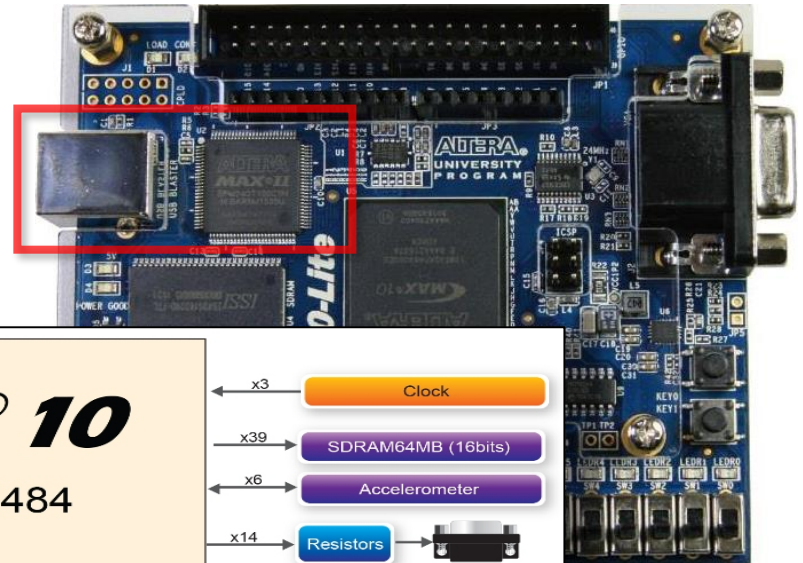


FPGA Device

- MAX 10 **10M50DAF484C7G** Device
- Integrated dual ADCs, each ADC supports 1 dedicated analog input and 8 dual function pins
- 50K programmable logic elements
- 1638 Kbits M9K Memory
- 5,888 Kbits user flash memory
- 144 18*18 Multiplier
- 4 PLLS

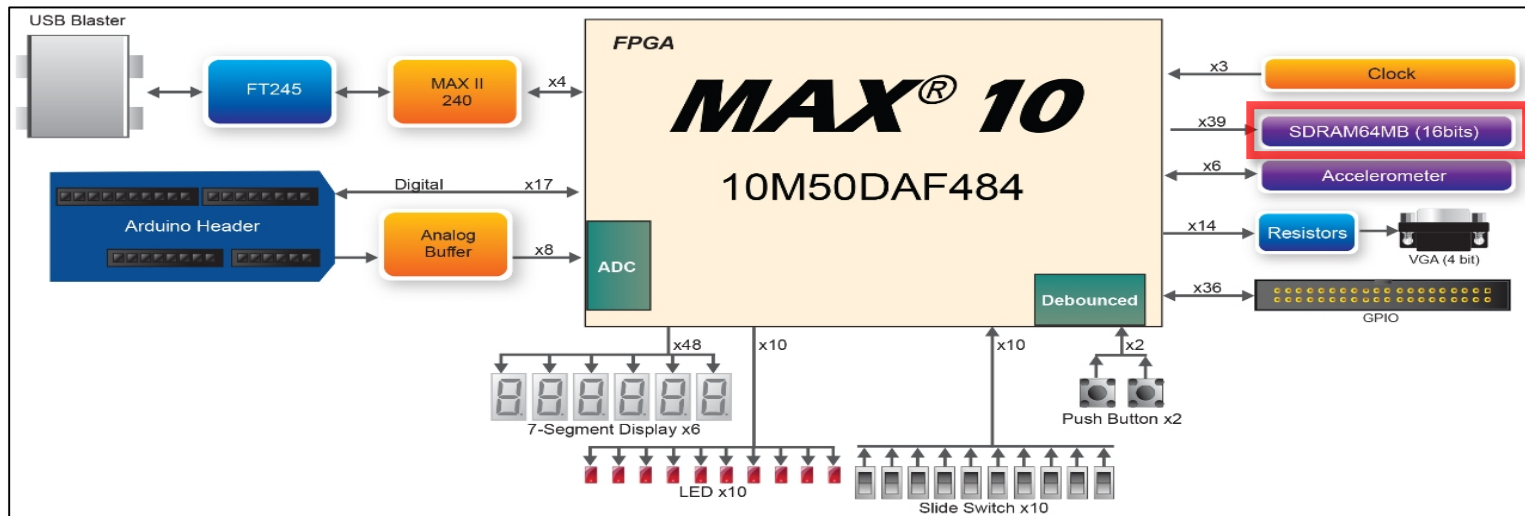
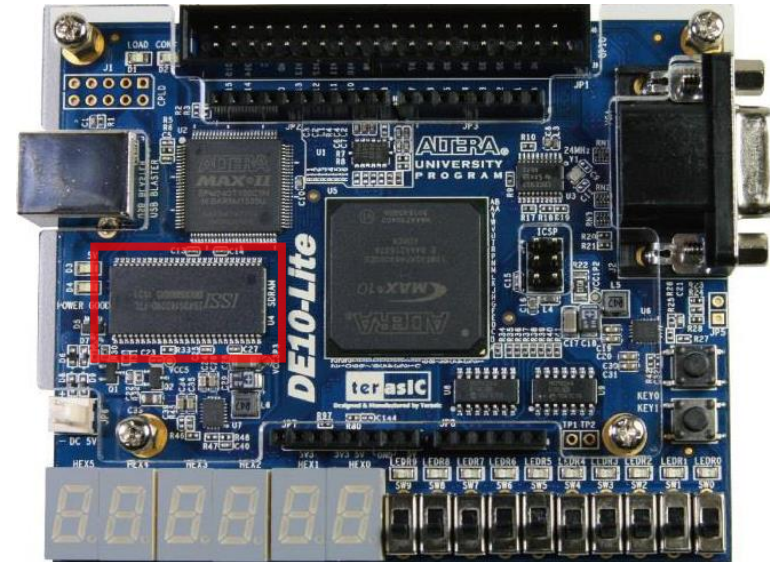
Programming and Configuration

- On-Board USB Blaster



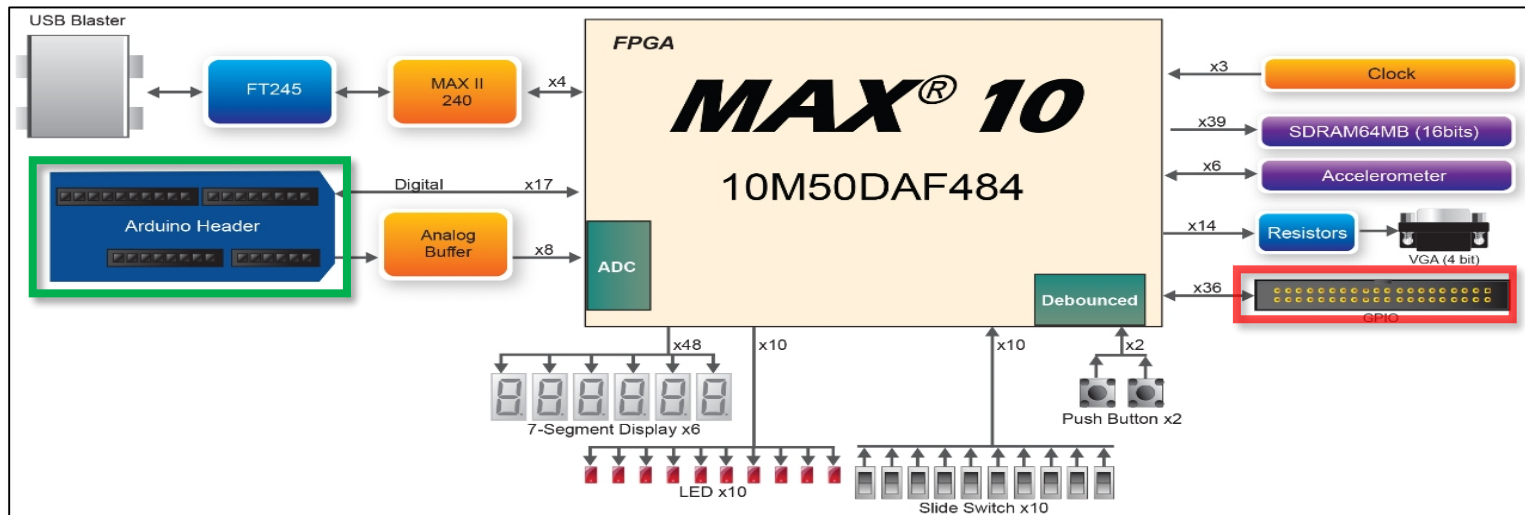
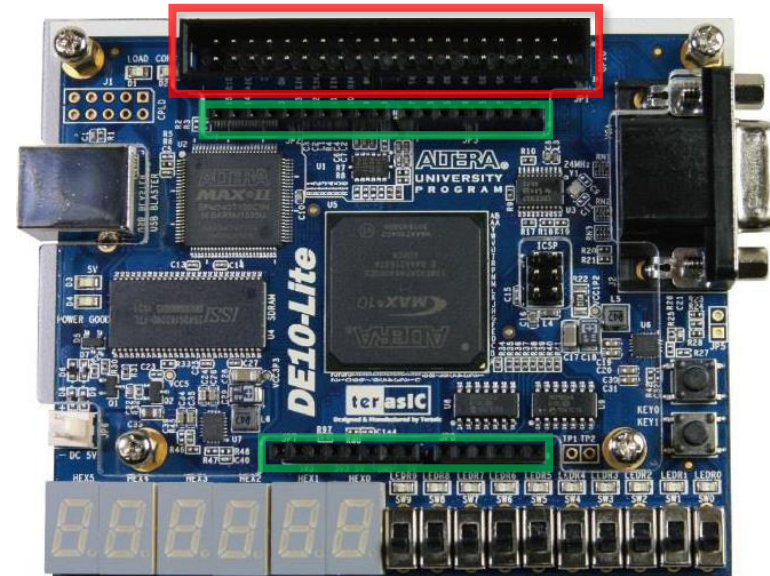
Memory Device

- 64MB SDRAM, x16 bits data bus



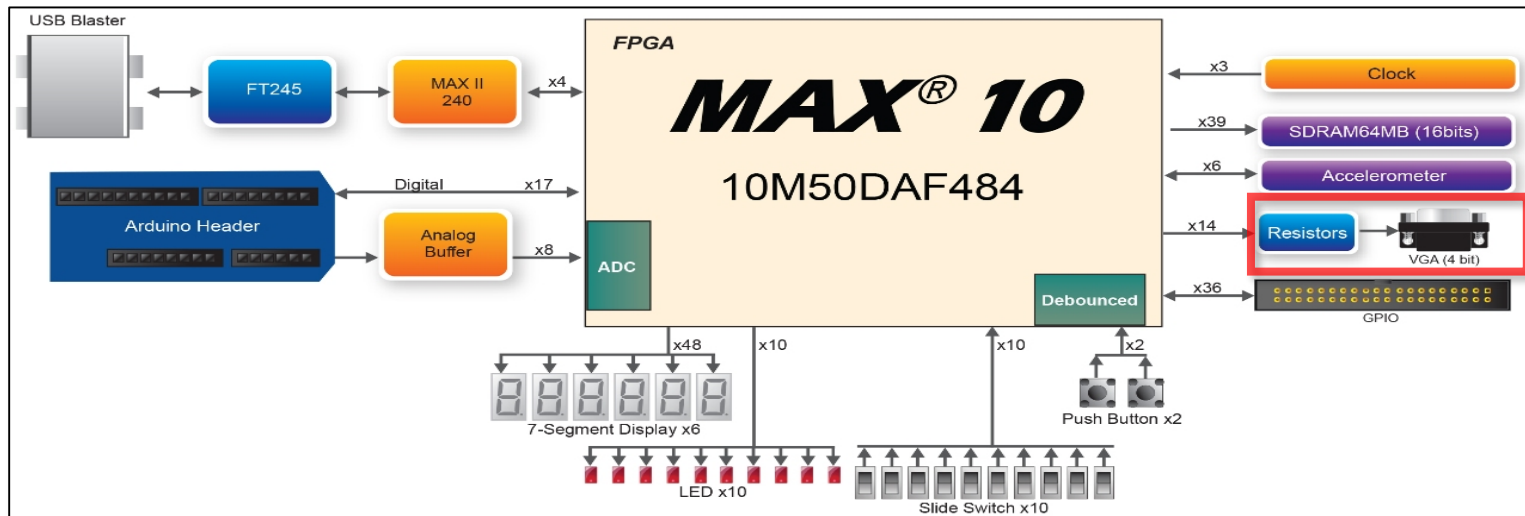
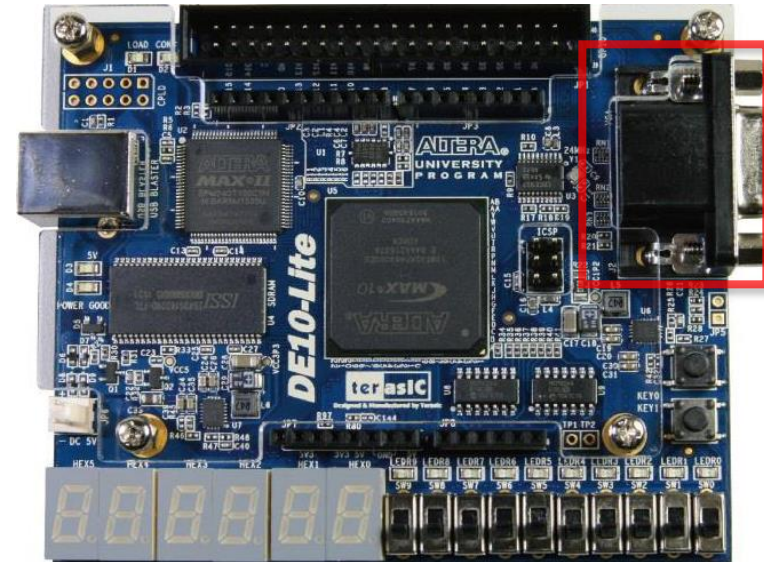
Connectors

- 2*20 GPIO Header
- Arduino Uno R3 Connector, including six ADC channels



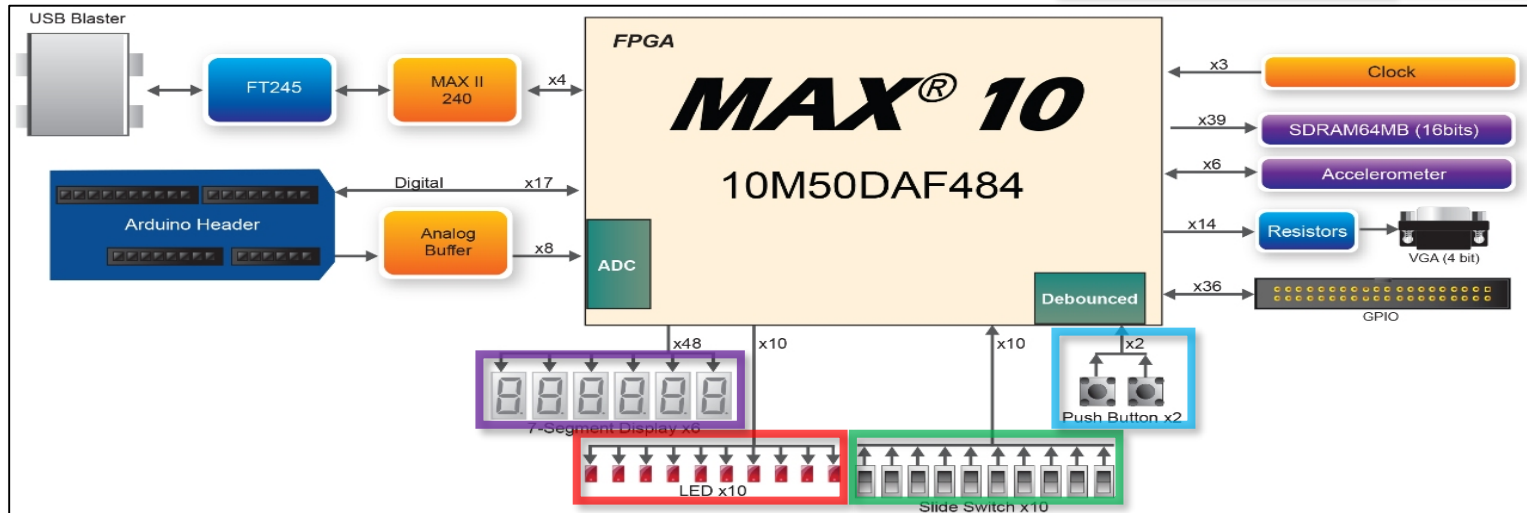
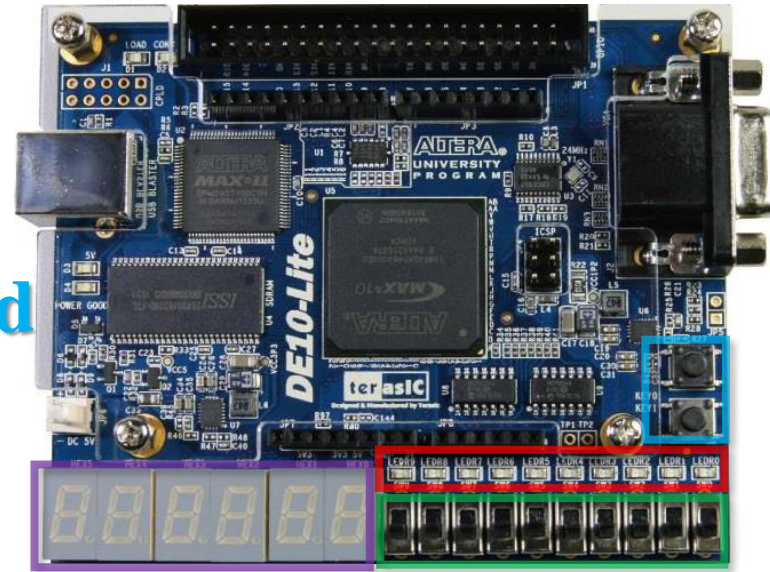
Display

- 4-bit resistor-network DAC for VGA

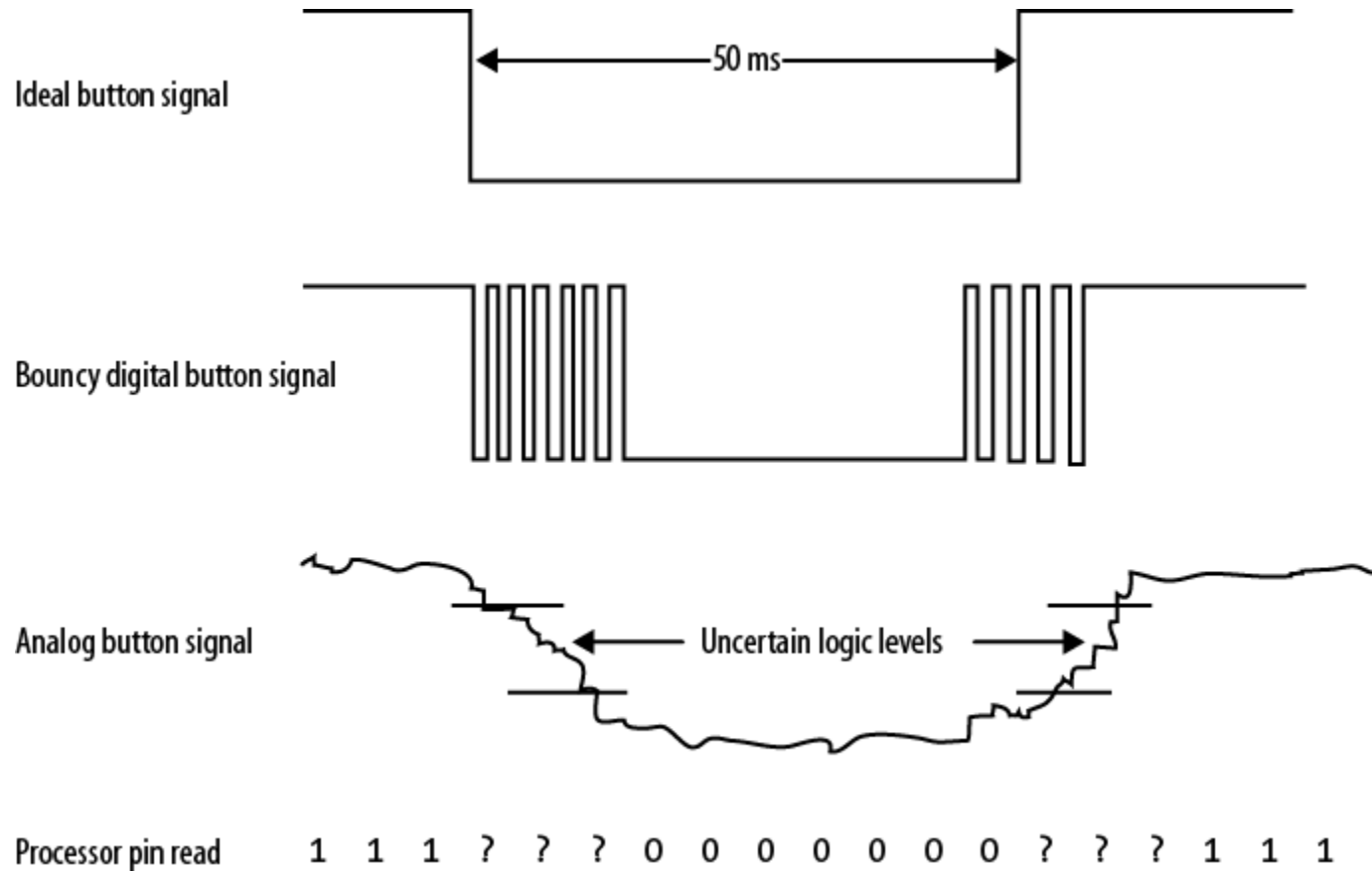


Switches, Buttons and LEDs

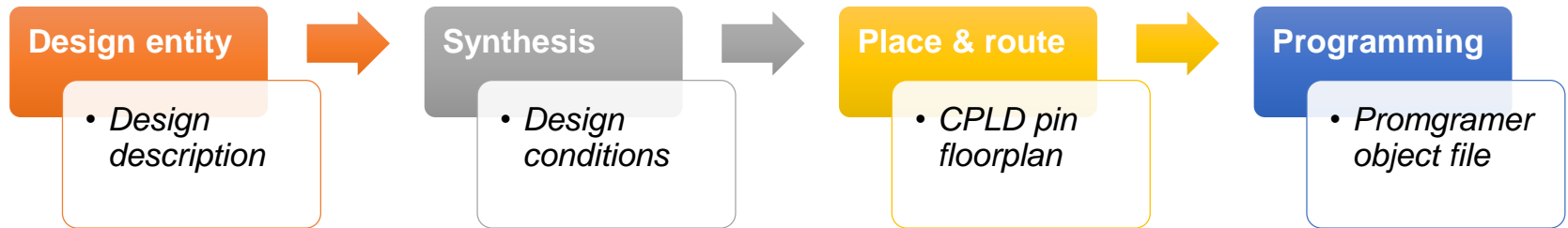
- 10 LEDs
- 10 Slide Switches
- 2 Push Buttons with Debounced
- Six 7-Segments



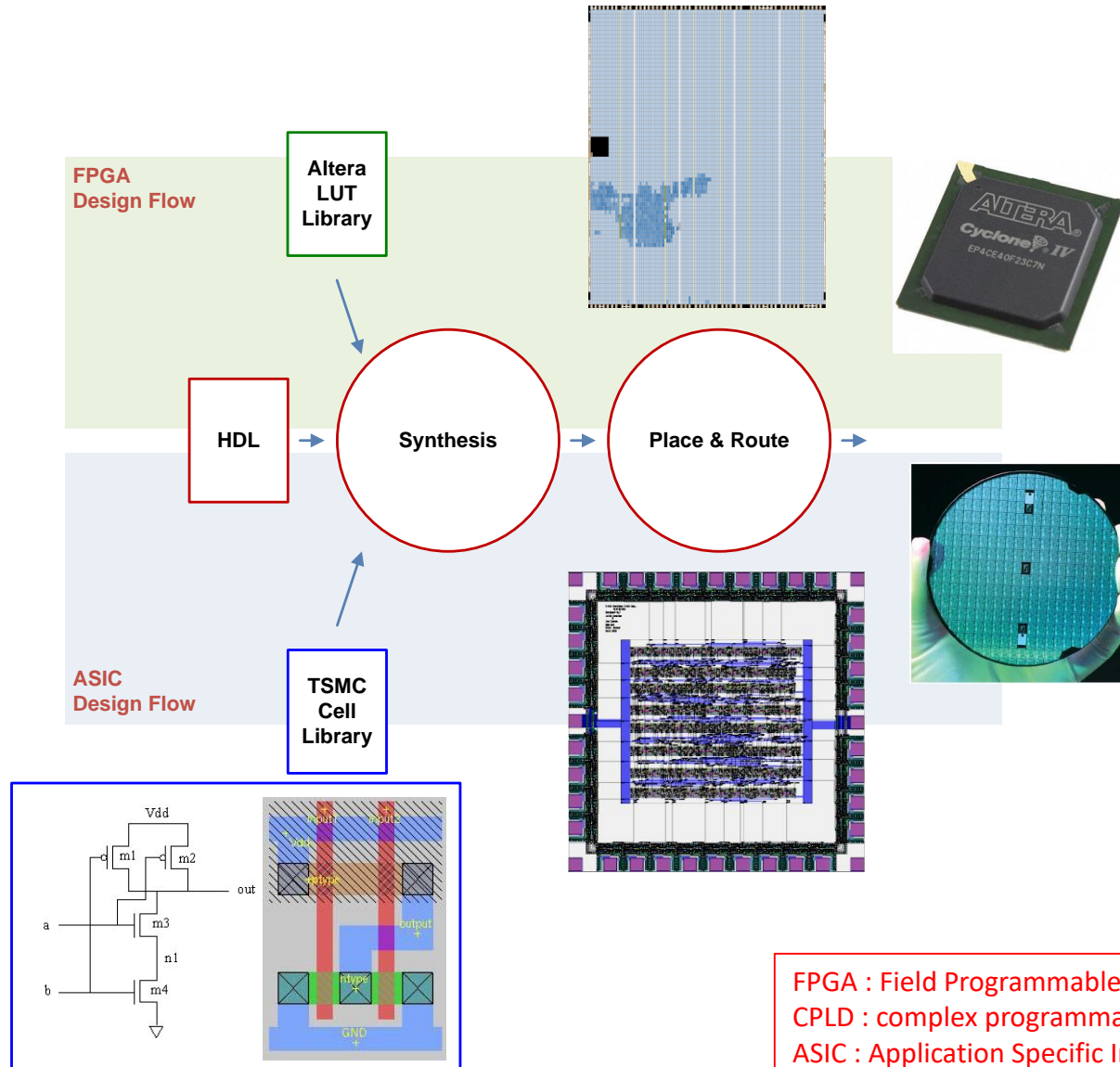
補充：**Bouncy** digital button Signal



FPGA設計流程



Design Flow of FPGA and ASIC



Quartus Prime



Quartus Prime Lite Edition

File Edit View Project Assignments Processing Tools Window Help

Project Navigator Hierarchy

Compilation Hierarchy

Recent Projects

- HaltAdd.qpf (F:/Quartus_Project/ex1/HaltAdd.qpf)
- TEST01.qpf (F:/Quartus_Project/TEST01.qpf)

New Project Wizard Open Project

Compare Editions Buy Software Documentation Training Support What's New Notifications

Tasks

Compilation

Task	Time
Compile Design	
> Analysis & Synthesis	
> Fitter (Place & Route)	
> Assembler (Generate programming files)	
> Timing Analysis	
> EDA Netlist Writer	
Edit Settings	
Program Device (Open Programmer)	

Close page after project load
Don't show this screen again

IP Catalog

Device Family Cyclone 10 LP

Installed IP

- Project Directory
- Library
 - Basic Functions
 - DSP
 - Interface Protocols
 - Memory Interfaces and Controllers
 - Processors and Peripherals
 - University Program
- Search for Partner IP

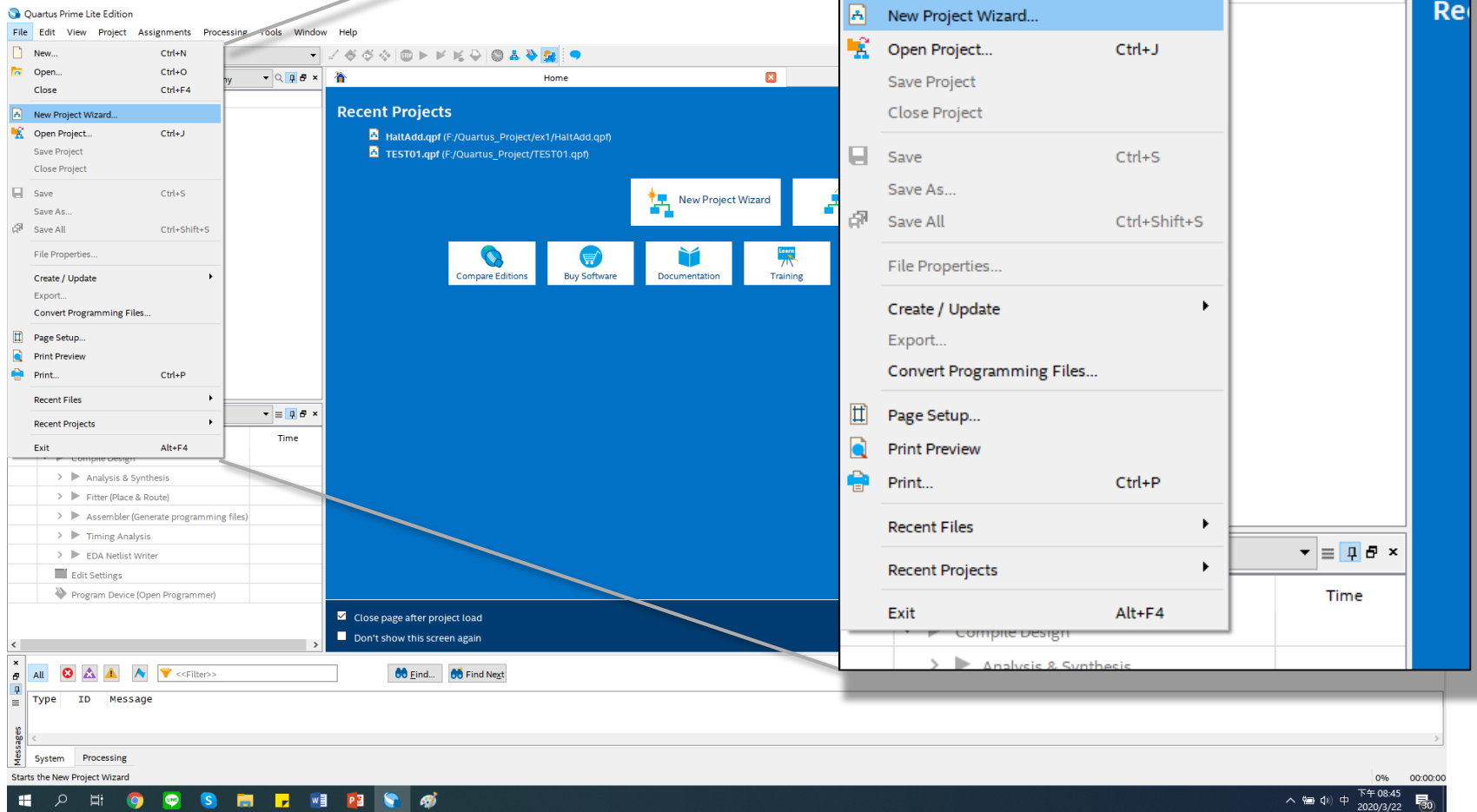
Messages

System Processing

0% 00:00:00

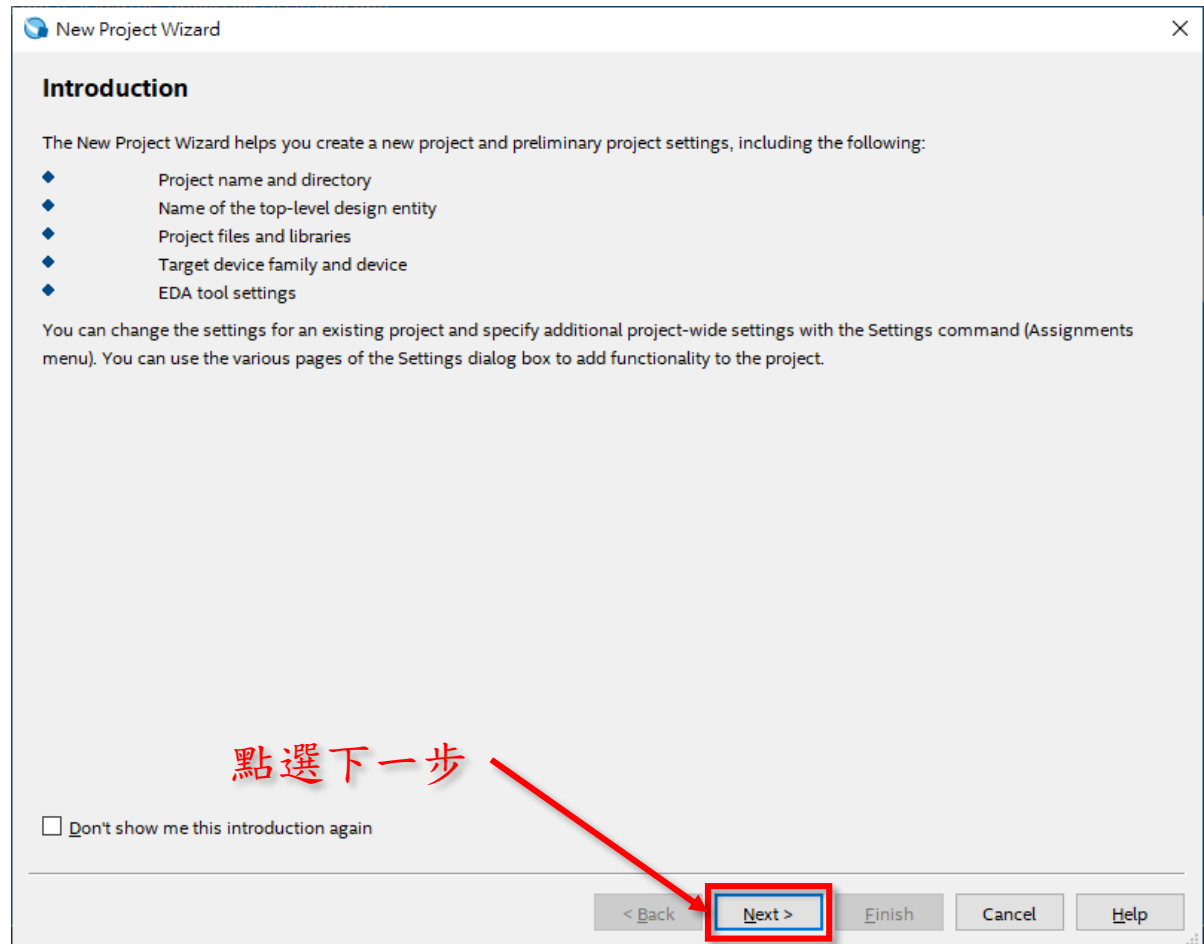
Quartus Prime

• 建立新專案(1/9)



Quartus Prime

- 建立新專案(2/9)



Quartus Prime

- 建立新專案(3/9)

The screenshot shows the 'New Project Wizard' dialog box with the title 'New Project Wizard'. The main section is titled 'Directory, Name, Top-Level Entity'. It contains three text input fields, each with a red border and a red arrow pointing to it from a Chinese annotation on the left. The first field is labeled 'What is the working directory for this project?' and contains the path 'F:\IntelFPGA_Project\DSE_EX\EX03_1'. The second field is labeled 'What is the name of this project?' and contains 'EX03_1'. The third field is labeled 'What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.' and also contains 'EX03_1'. Below these fields is a button labeled 'Use Existing Project Settings...'. At the bottom right, there are four buttons: '< Back', 'Next >', 'Finish', and 'Help'. A red arrow points from the annotation '點選下一步' to the 'Next >' button.

路徑與檔名
不可有中文

專案名稱

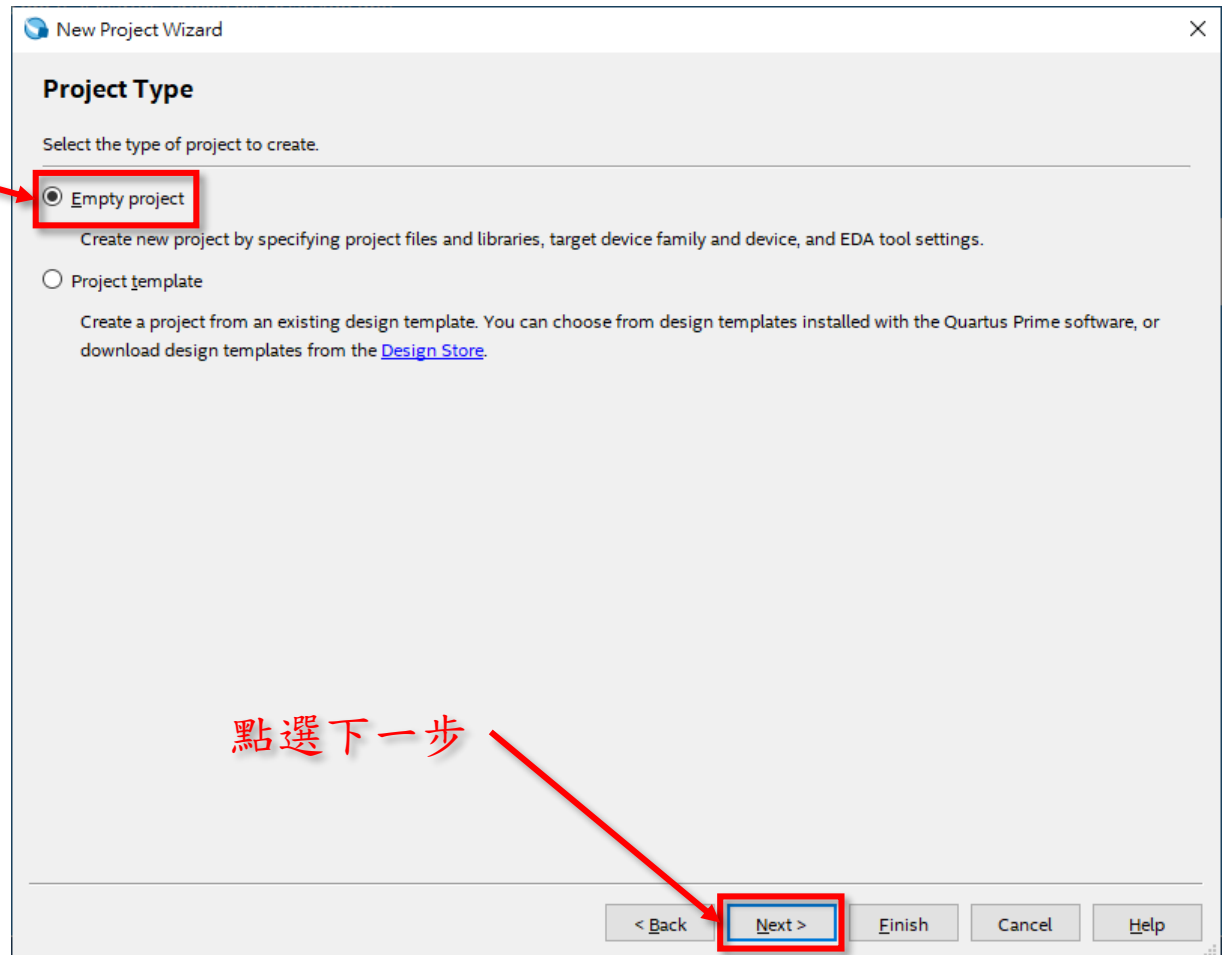
與專案名稱相同

點選下一步

Quartus Prime

- 建立新專案(4/9)

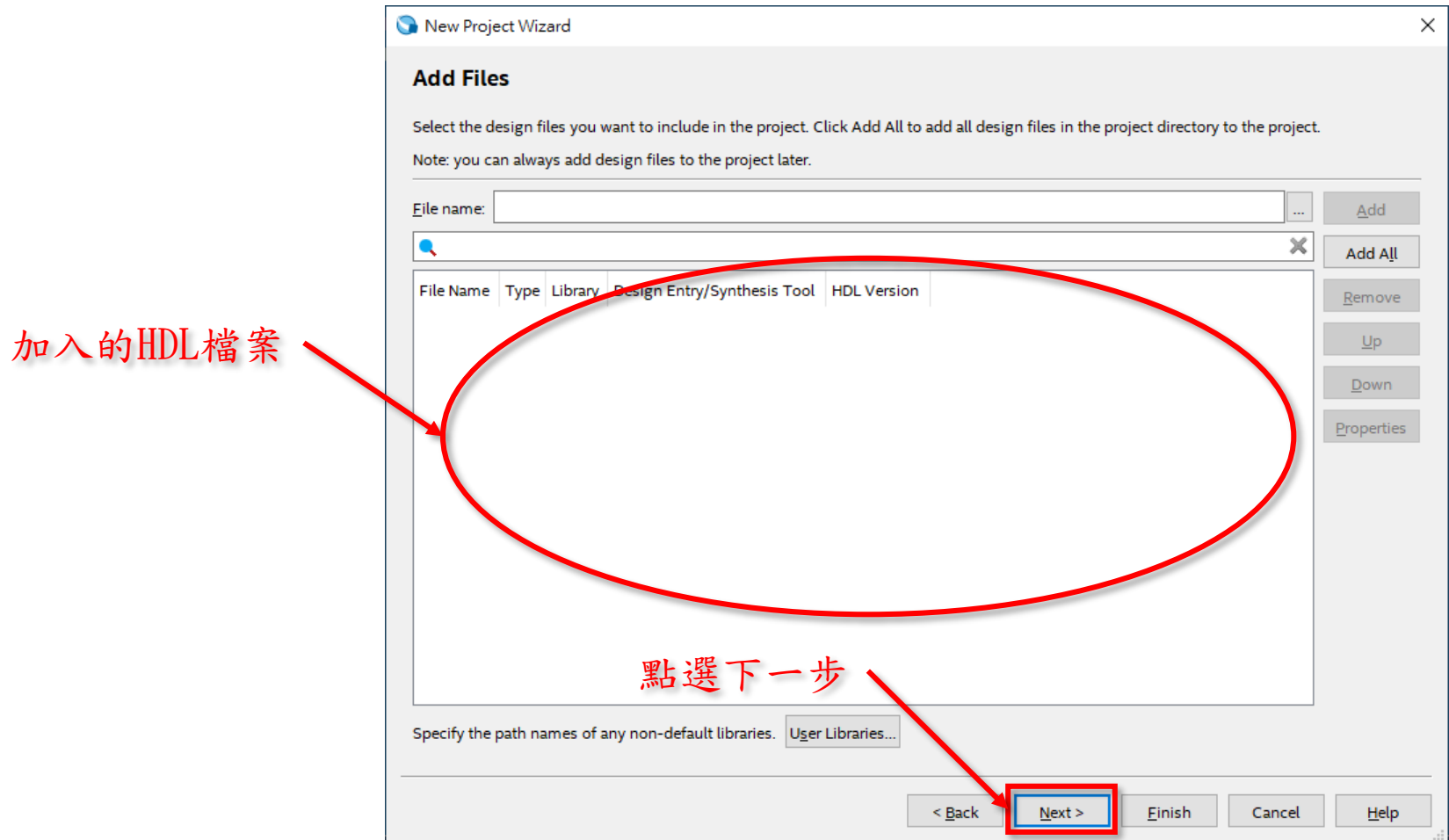
選擇空白專案



點選下一步

Quartus Prime

- 建立新專案(5/9)



Quartus Prime

- 建立新專案
(6/9)

利用參數濾出適當的晶片

Family : MAX 10 (DA/DF/DC/SA/SC)
Device : MAX 10 DA
Package : FBGA
Pin count : 484
Core speed grade : 7

選擇10M50DAF484C7G

New Project Wizard

Family, Device & Board Settings

Device Board

Select the family and device you want to target for compilation.
You can install additional device support with the Install Devices command on the Tools menu.

To determine the version of the Quartus Prime software in which your target device is supported, refer to the [Device Support List](#) webpage.

Device family

Family: MAX 10 (DA/DF/DC/SA/SC)
Device: MAX 10 DA

Target device

☐ Auto device selected by the Fitter
☒ Specific device selected in 'Available devices' list
☐ Other: n/a

Show in 'Available devices' list

Package: FBGA
Pin count: 484
Core speed grade: 7
Name filter:
☒ Show advanced devices

Available devices:

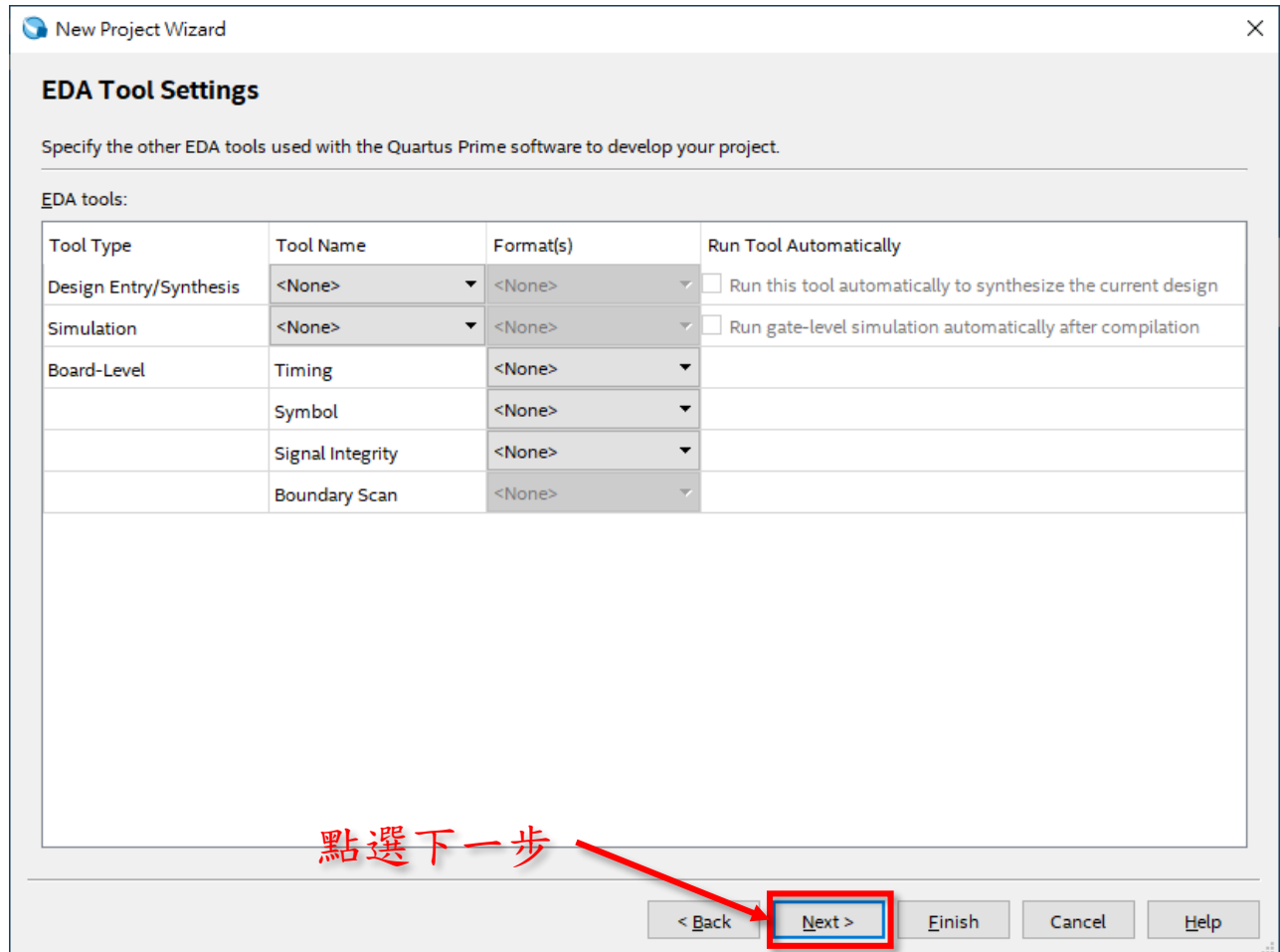
Name	Core Voltage	LEs	Total I/Os	GPIOs	Memory Bits	Embedded multiplier 9
10M40DAF484C7G	1.2V	40368	360	360	1290240	250
10M40DAF484I7G	1.2V	40368	360	360	1290240	250
10M50DAF484C7G	1.2V	49760	360	360	1677312	288
10M50DAF484I7G	1.2V	49760	360	360	1677312	288
10M50DAF484I7B	1.2V	49760	360	360	1677312	288

< Back Next > Finish Cancel Help

點選下一步

Quartus Prime

- 建立新專案(7/9)



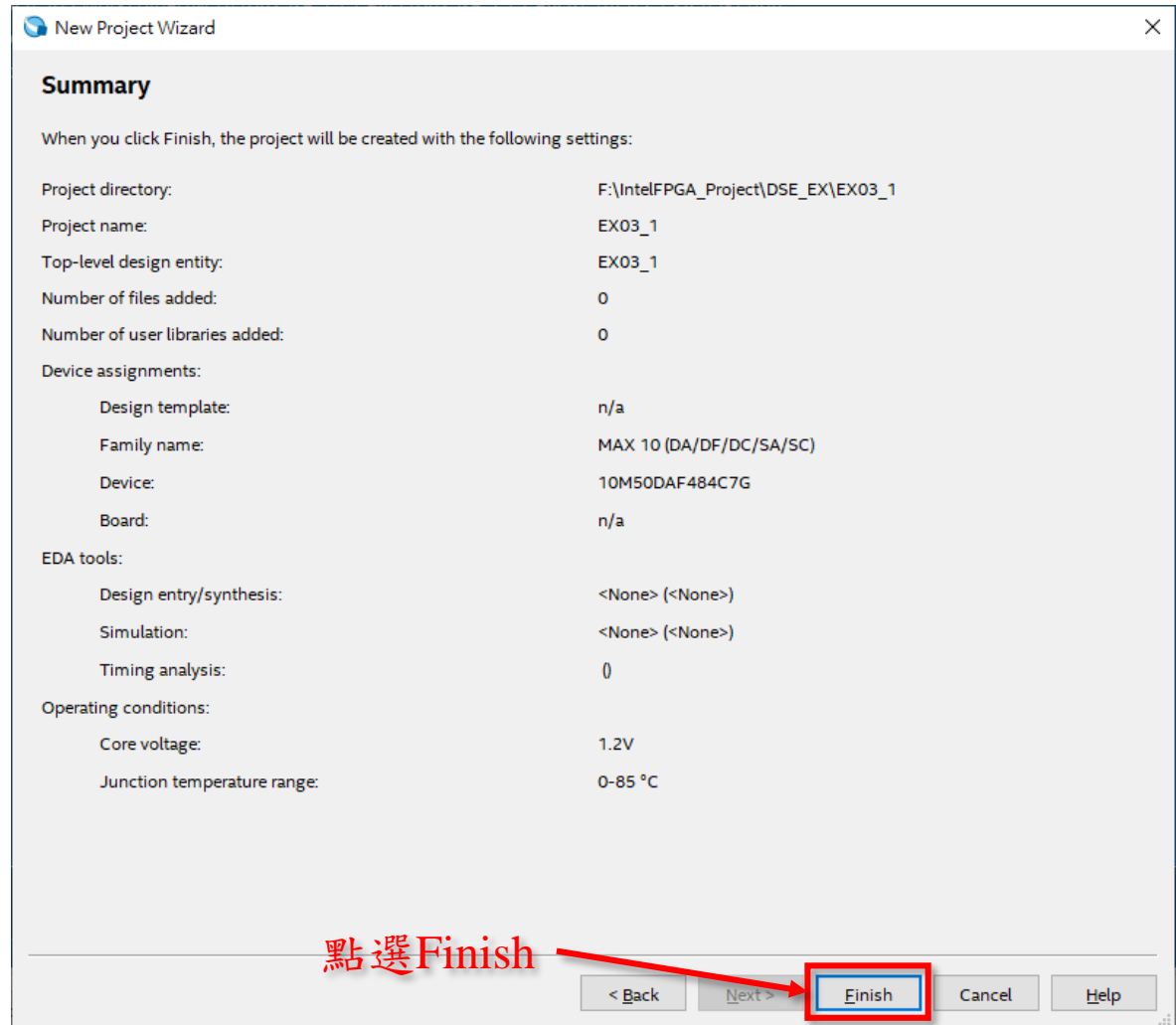
The screenshot shows the 'New Project Wizard' window in Quartus Prime, specifically the 'EDA Tool Settings' step. The window title is 'New Project Wizard'. The section is titled 'EDA Tool Settings' with a subtitle 'Specify the other EDA tools used with the Quartus Prime software to develop your project.' Below this, there is a table for 'EDA tools:'.

Tool Type	Tool Name	Format(s)	Run Tool Automatically
Design Entry/Synthesis	<None>	<None>	<input type="checkbox"/> Run this tool automatically to synthesize the current design
Simulation	<None>	<None>	<input type="checkbox"/> Run gate-level simulation automatically after compilation
Board-Level	Timing	<None>	
	Symbol	<None>	
	Signal Integrity	<None>	
	Boundary Scan	<None>	

At the bottom of the window, there are five buttons: '< Back', 'Next >', 'Finish', 'Cancel', and 'Help'. A red arrow points from the Chinese text '點選下一步' (Click Next Step) to the 'Next >' button, which is also highlighted with a red rectangle.

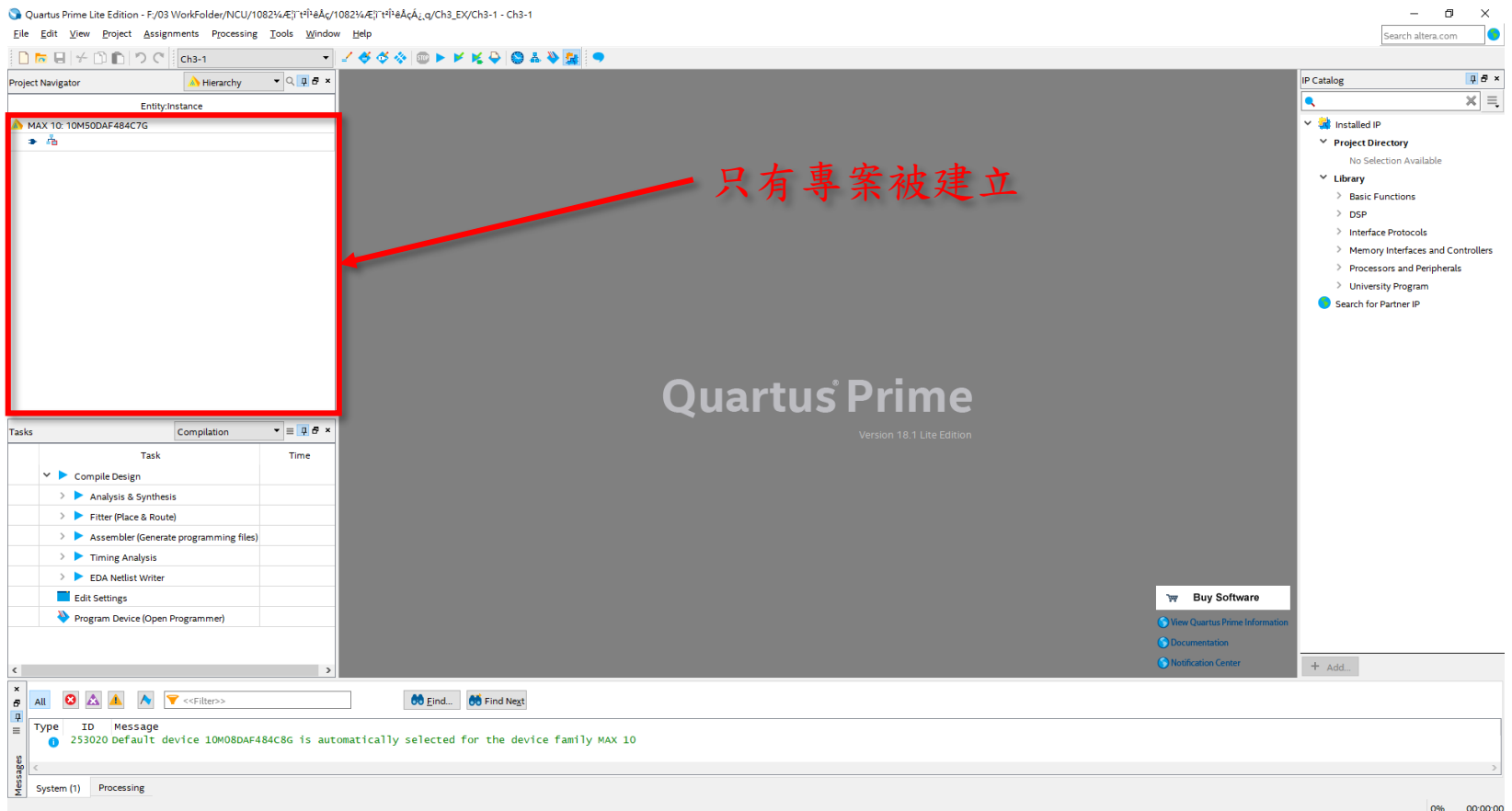
Quartus Prime

- 建立新專案
(8/9)



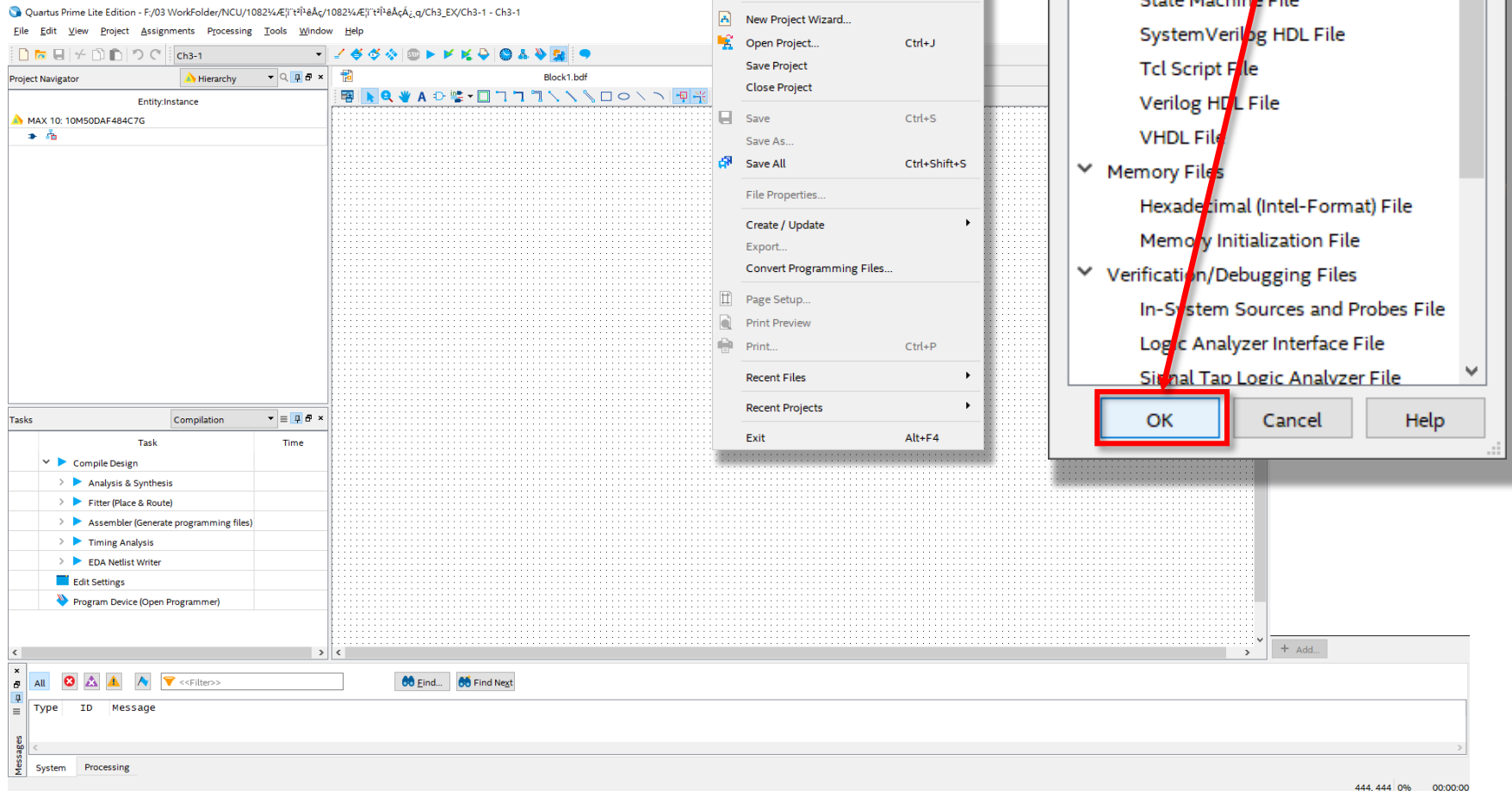
Quartus Prime

- 建立新專案(9/9)



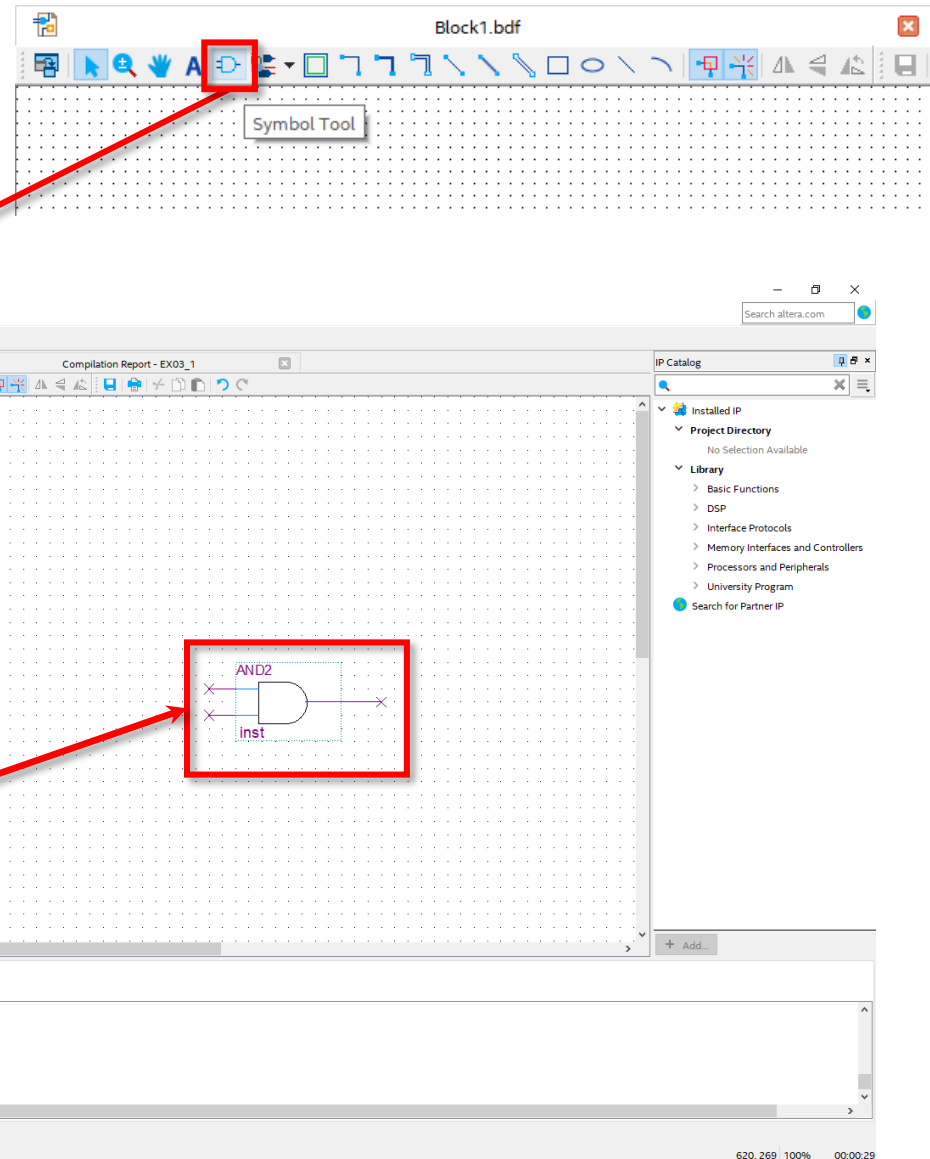
Quartus Prime

- Add a new entity



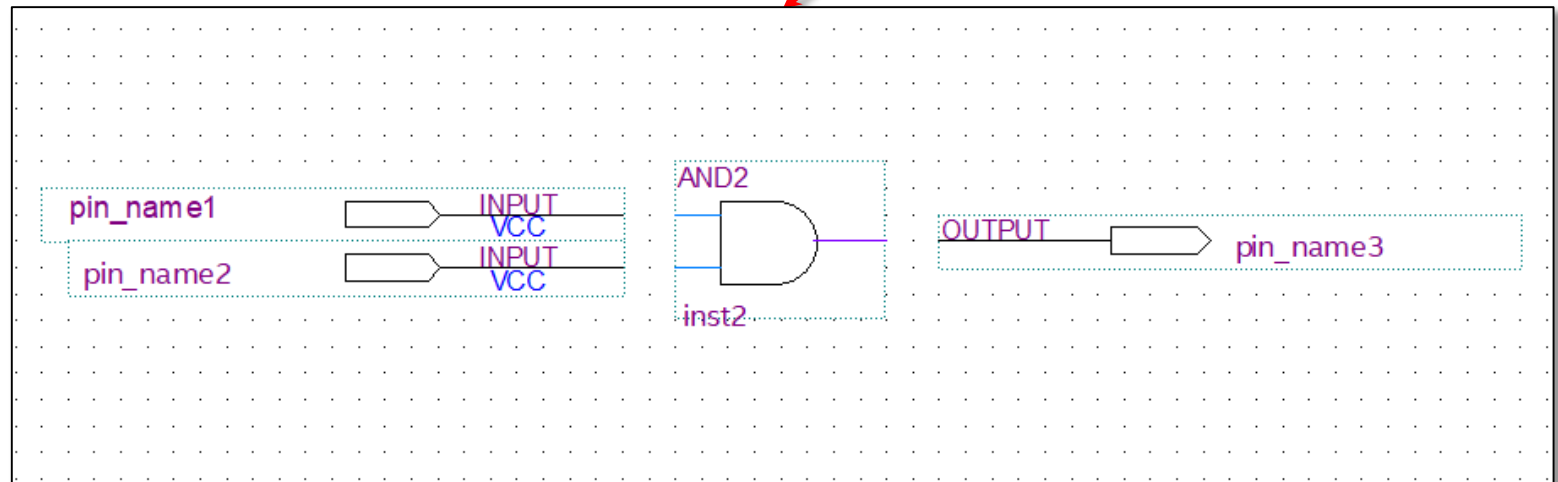
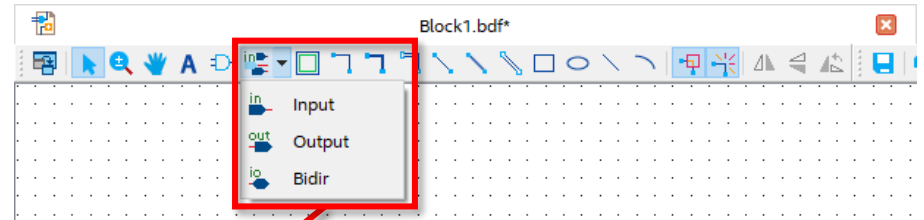
Quartus Prime

- 插入 2 input AND Gate
 - /primitives/logic/and2



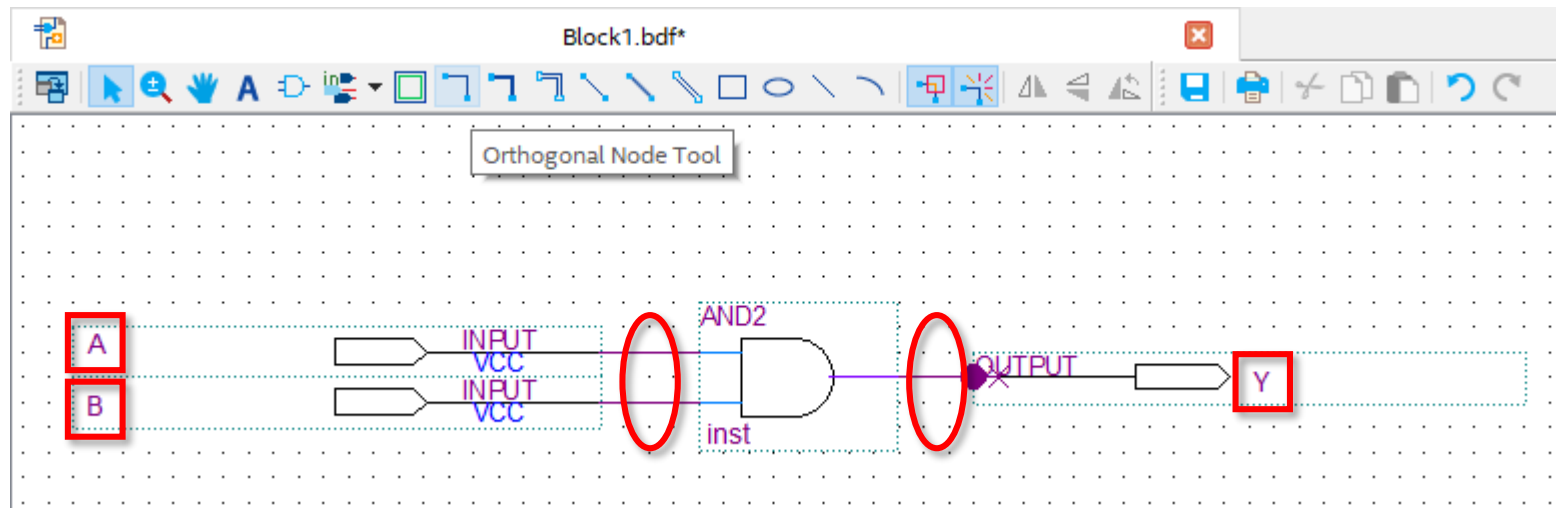
Quartus Prime

- 插入輸入輸出pin



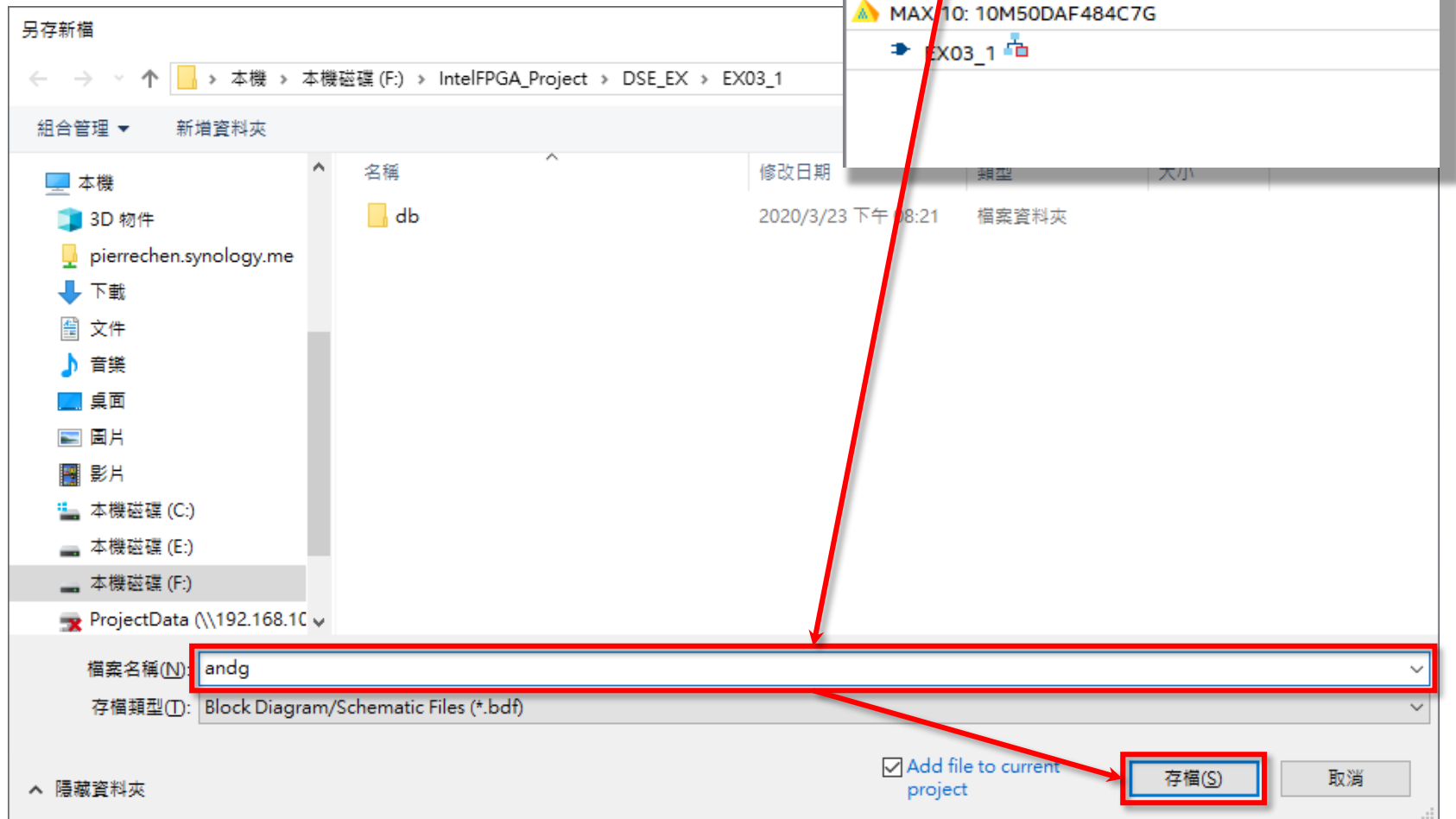
Quartus Prime

- 連接輸入輸出
- 修改pin name



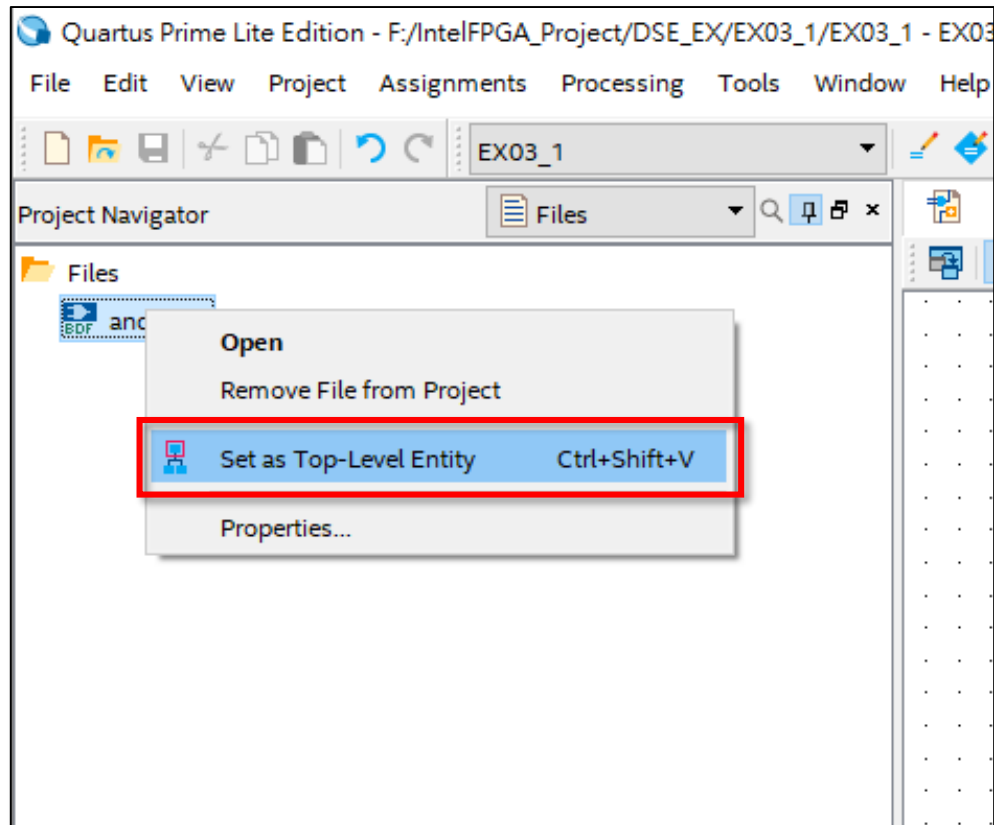
Quartus Prime

- 存檔



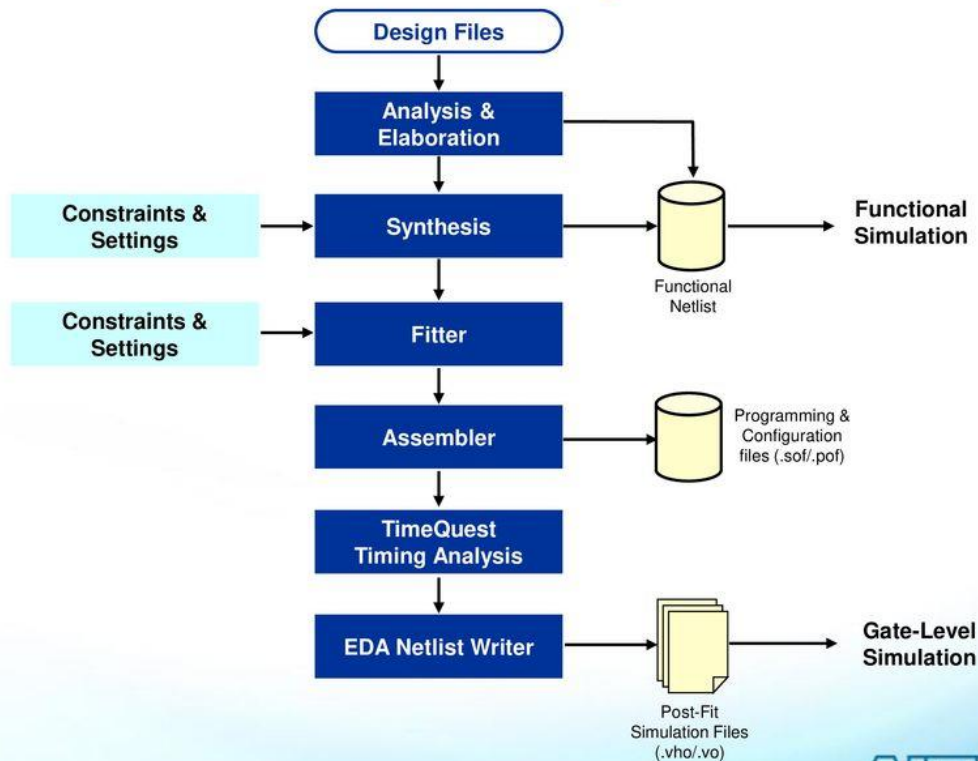
Quartus Prime

- 將Entity設定為Top-Level Entity



補充


Quartus II Full Compilation Flow*



- Start Compilation (Full)
- Start Hierarchy Elaboration
 - Checks syntax & build hierarchy
- Start Analysis & Elaboration
 - Checks syntax & builds hierarchy
 - Performs initial synthesis
- Start Analysis & Synthesis
 - Synthesizes & optimizes code
- Start Fitter
 - Places & routes design
 - Generates output netlists
- Start Assembler
 - Generates programming files
- Start EDA Netlist Writer
 - Dump Gate-level netlist file for simulation
- Analyzers
 - I/O Assignment
 - PowerPlay
 - Design Assistant

Quartus Prime

- Compile

 Start Analysis & Elaboration



Quartus Prime Lite Edition - F:/IntelFPGA/Project/DSE_EX/EX03_2/EX03_2 - EX03_2

File Edit View Project Assignments Processing Tools Window Help

EX03_2

Project Navigator Entity/Instance
MAX 10: 10M50DAF484C7G
EX03_2

Table of Contents
Flow Summary
Flow Settings
Flow Non-Default Global Settings
Flow Elapsed Time
Flow OS Summary
Flow Log
Analysis & Elaboration
Flow Messages
Flow Suppressed Messages

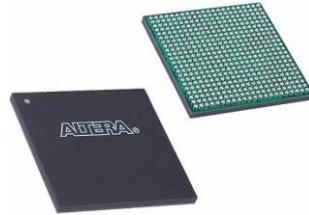
Flow Summary
Flow Status: Successful - Tue Mar 24 15:34:01 2020
Quartus Prime Version: 18.1.0 Build 625 09/12/2018 SJ Lite Edition
Project Name: EX03_2
Top-level Entity Name: EX03_2
Family: MAX10
Device: 10M50DAF484C7G
Timing Models: Final
Total logic elements: N/A until Partition Merge
Total registers: N/A until Partition Merge
Total pins: N/A until Partition Merge
Total virtual pins: N/A until Partition Merge
Total memory bits: N/A until Partition Merge
Embedded Multiplier 9-bit elements: N/A until Partition Merge
Total PLLs: N/A until Partition Merge
UFM blocks: N/A until Partition Merge
ADC blocks: N/A until Partition Merge

Tasks
Compilation
Task Time
Compile Design
Analysis & Synthesis
Edit Settings
View Report
Analysis & Elaboration 00:00:11
Partition Merge
Netlist Viewers
Design Assistant (Post-Mapping)
I/O Assignment Analysis
Fitter (Place & Route)
Assembler (Generate programming files)
Timing Analysis
EDA Netlist Writer
Edit Settings
Program Device (Open Programmer)

Messages
ID Message
18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL
20030 Parallel compilation is enabled and will use 4 of the 4 processors detected
System (1) Processing (8)

Quartus Prime

- Pin Planner (1/2)



Pin Planner - F:\IntelFPGA_Project\DSF_EX\EX03_1\EX03_1 - EX03_1

File Edit View Processing Tools Window Help

Groups

Named: +

Node Name Direction

<<new group>>

Groups Report

Tasks

- Early Pin Planning
 - Early Pin Planning...
 - Run I/O Assignment Analysis
 - Export Pin Assignments...
- Highlight Pins
 - I/O Banks
 - VREF Groups
 - Edges
- Clock Pins
 - Clock
 - PLL/DLL Input
 - PLL/DLL Output

Top View - Wire Bond
MAX 10 - 10M50DAF484C7G

Node Name Direction Location I/O Bank VREF Group Fitter Location I/O Standard Reserved Current Strength Slew Rate Differential Pair Strict Preservation

Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard	Reserved	Current Strength	Slew Rate	Differential Pair	Strict Preservation
in_A	Input				PIN_AB4	2.5 V (default)		12mA (default)			
in_B	Input				PIN_AA3	2.5 V (default)		12mA (default)			
out_Y	Output				PIN_W8	2.5 V (default)		12mA (default)	2 (default)		
<<new node>>											

Assignments

- Device...
- Settings... **Ctrl+Shift+E**
- Assignment Editor **Ctrl+Shift+A**
- Pin Planner **Ctrl+Shift+N****
- Remove Assignments...
- Back-Annotate Assignments...
- Import Assignments...
- Export Assignments...
- Assignment Groups...
- Logic Lock Regions Window **Alt+L**
- Design Partitions Window **Alt+D**

VREF

VCCP/VCCR/V...

VCCA

VCCINT

VCCIO

GND

No connect

Filter: Pins: all

Quartus Prime

從電路圖查詢
設定完成後直接關閉

- Pin Planner (2/2)

Pin Planner - F:\IntelFPGA_Project\DSE_EX\EX03_1\EX03_1 - EX03_1

File Edit View Processing Tools Window Help

Groups

Named: +

Node Name Direction

<<new group>>

Groups Report

Tasks

- Early Pin Planning
 - Early Pin Planning...
 - Run I/O Assignment Analysis
 - Export Pin Assignments...
- Highlight Pins
 - I/O Banks
 - VREF Groups
 - Edges
- Clock Pins
 - Clock
 - PLL/DLL Input
 - PLL/DLL Output

Top View - Wire Bond

MAX 10 - 10M50DAF484C7G

Pin Legend

Symbol Pin Type

- User I/O
- User assigned I...
- Fitter assigned I...
- Unbonded pad
- Reserved pin
- Other configura...
- DEV_OE
- DEV_CLR
- DIFF_n
- DIFF_p
- DQ
- DQS
- DQSB
- CLK_n
- CLK_p
- Other PLL
- Other dual purp...
- TDI
- TCK
- TMS
- TDO
- VREF
- VCCP/VCCR/V...
- VCCA
- VCCINT
- VCCIO
- GND
- No connect

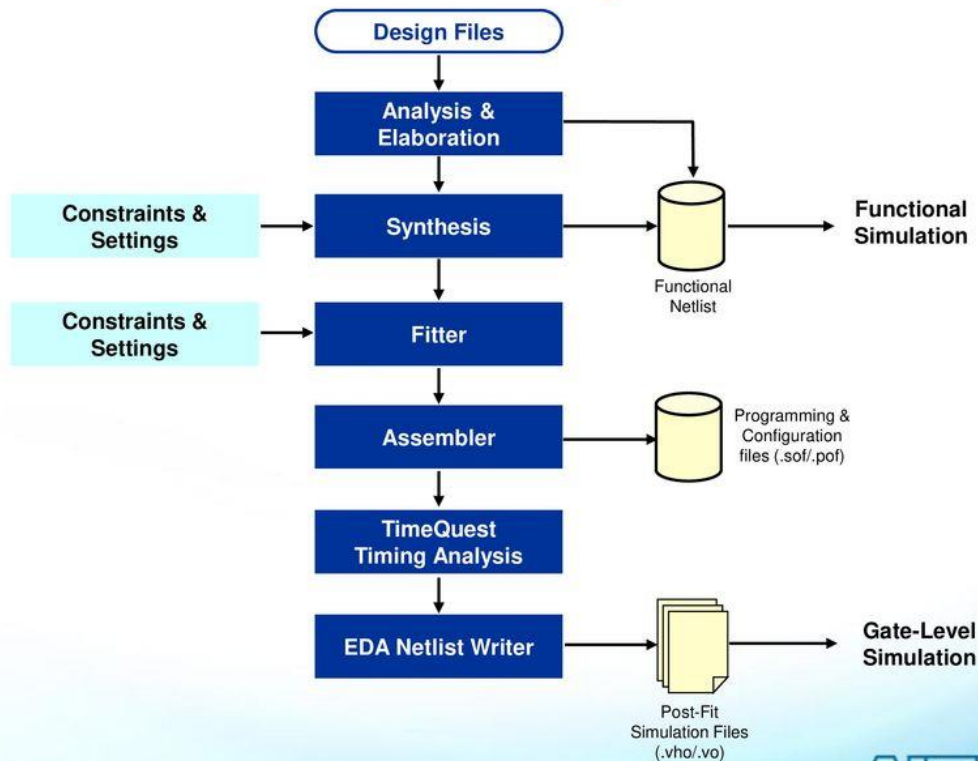
Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard	Reserved	Current Strength	Slew Rate	Differential Pair	Strict Preservation
A	Input	PIN_C10	7	B7_NO	PIN_C10	3.3-V LVTTTL		8mA (default)			
B	Input	PIN_C11	7	B7_NO	PIN_C11	3.3-V LVTTTL		8mA (default)			
Y	Output	PIN_A8	7	B7_NO	PIN_A8	3.3-V LVTTTL		8mA (default)	2 (default)		
<<new node>>											

Filter: Pins: all

0% 00:00:00

補充

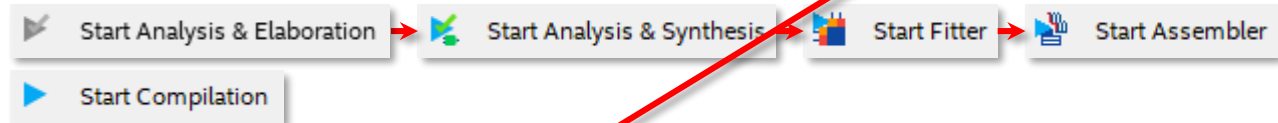
Quartus II Full Compilation Flow*



- Start Compilation (Full)
- Start Hierarchy Elaboration
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 - Generates programming files
- Start EDA Netlist Writer
 - Dump Gate-level netlist file for simulation
- Analyzers
 - I/O Assignment
 - PowerPlay
 - Design Assistant

Quartus Prime

- Compile



Quartus Prime Lite Edition - F:/IntelFPGA_Project/DSE_EX/EX03_1/EX03_1

File Edit View Project Assignments Processing Tools Window Help

EX03_1

Project Navigator Hierarchy Entity:Instance MAX 10: 10M50DAF484C7G andg

Table of Contents Flow Summary

Flow Status Successful - Tue Mar 24 09:40:55 2020

Quartus Prime Version 18.1.0 Build 625 09/12/2018 SJ Lite Edition

Revision Name EX03_1

Top-level Entity Name andg

Family MAX 10

Device 10M50DAF484C7G

Timing Models Final

Total logic elements 1

Total registers 0

Total pins 3

Total virtual pins 0

Total memory bits 0

Embedded Multiplier 9-bit elements 0

Total PLLs 0

UFM blocks 0

ADC blocks 0

Tasks Compilation

	Task	Time
25%	Compile Design	00:00:14
✓	Analysis & Synthesis	00:00:14
0%	Fitter (Place & Route)	00:00:00
0%	Assembler (Generate programming files)	00:00:00
0%	Timing Analysis	00:00:00
	EDA Netlist Writer	
	Edit Settings	
	Program Device (Open Programmer)	

Messages

Type ID Message

12127 Elaborating entity "andg" for the top level hierarchy

286030 Timing-Driven Synthesis is running

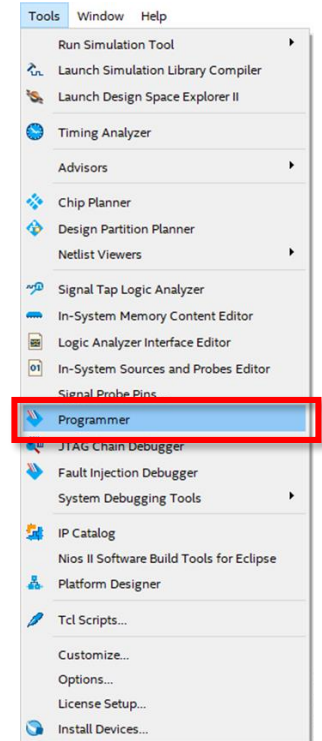
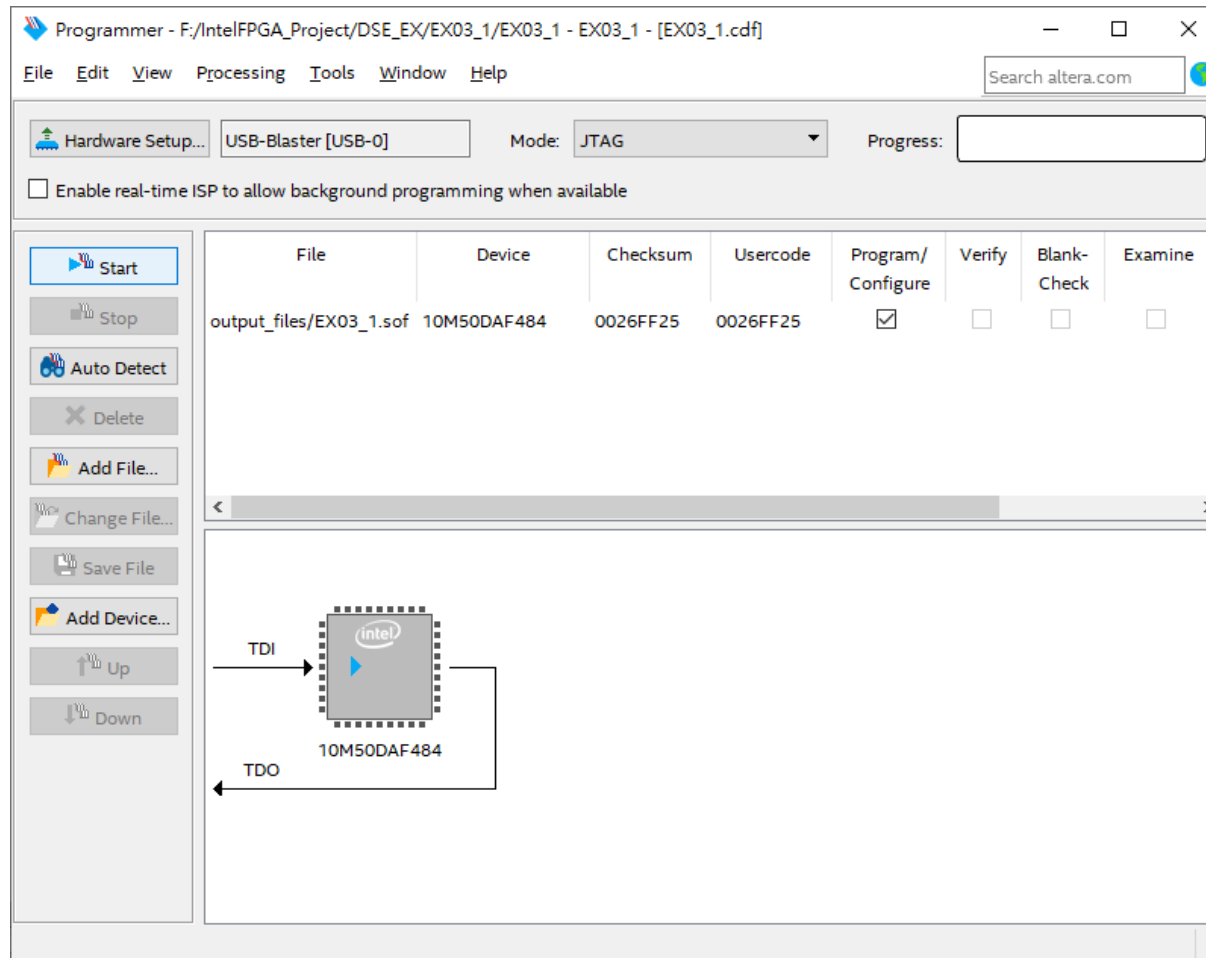
16010 Generating hard_block partition "hard_block:auto_generated_inst"

21057 Implemented 4 device resources after synthesis - the final resource count might be different

Quartus Prime Analysis & Synthesis was successful. 0 errors, 1 warning

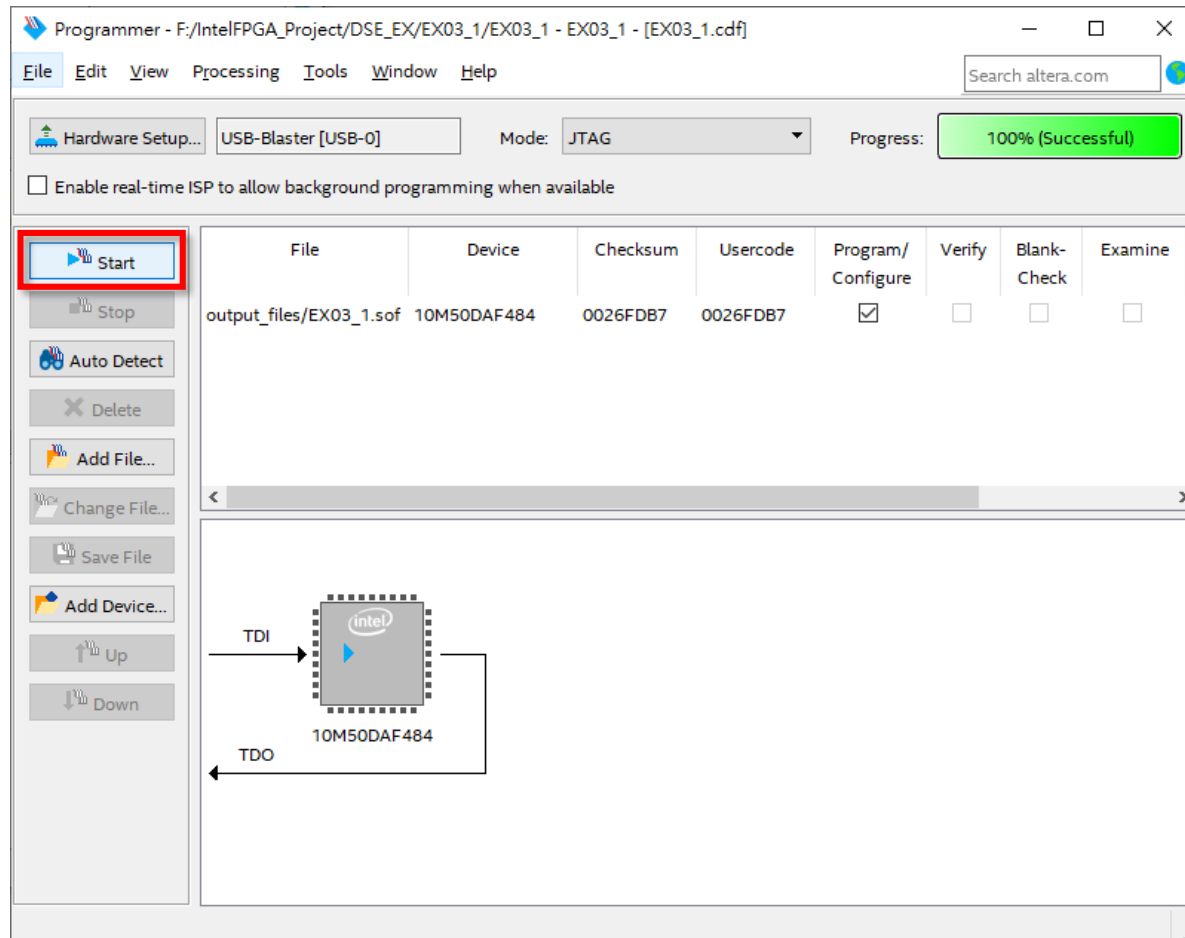
Quartus Prime

- Programming (1/2)



Quartus Prime

- Programming (2/2)



Quartus Prime

- 查看結果



實驗一：Quartus操作練習

- 參考講義流程，設計一數位邏輯電路，規格如下，
 - AND Gate : Input(SW0、SW1)，Output(LED0)
 - OR Gate : Input(SW2、SW3)，Output(LED2)
 - NOT Gate : Input(SW4)，Output(LED4)
 - XOR Gate : Input(SW5、SW6)，Output(LED5)
- 本次實驗需助教確認正確，並將專案壓縮上傳EE-Class。
- LectureX_組別XX.ZIP

- LE
- M9K Memory
- 18*18 Multiplier
- 4 PLLS