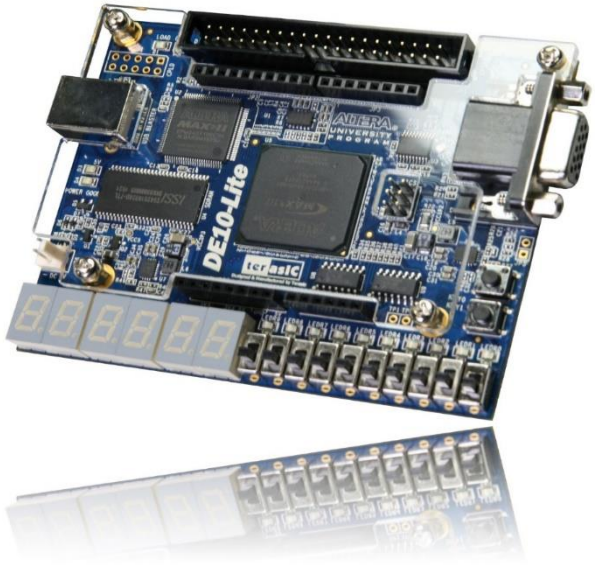


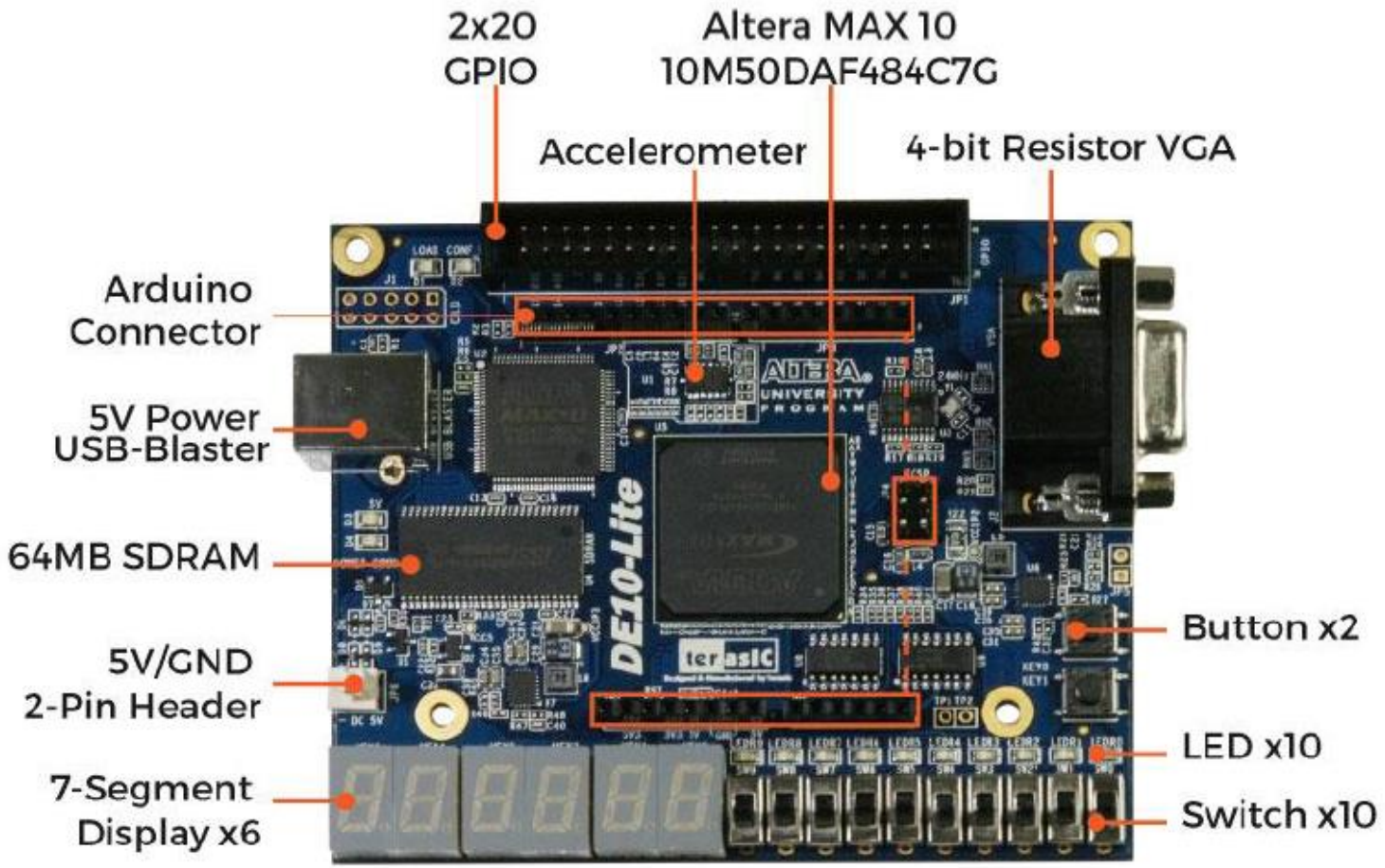
FPGA/CPLD發展環境簡介

CSIE MIAT Lab.

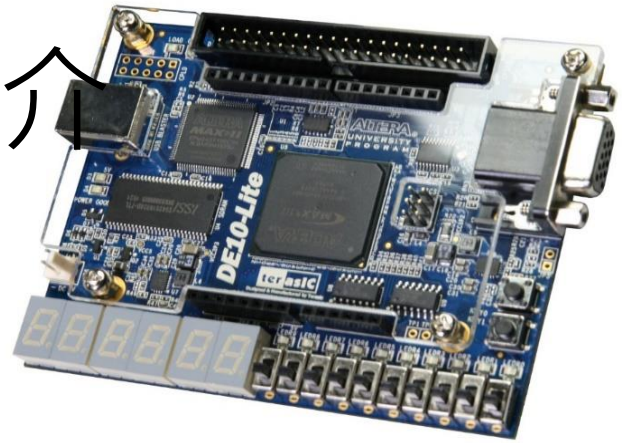
Outline

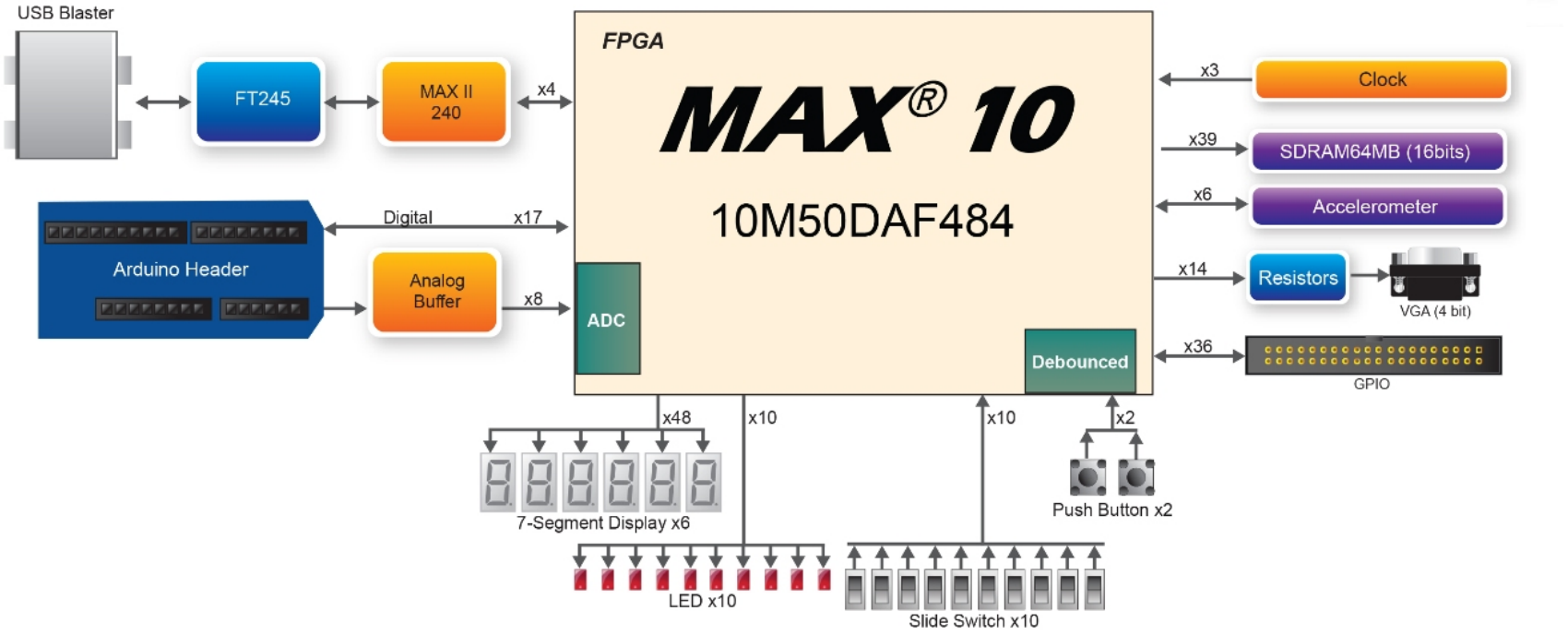
- Altera DE10 Lite實驗板簡介
  （配合:如何配合使用電路文件）
- FPGA設計流程
- Quartus Prime介紹
- 課堂練習

Altera DE10實驗板簡介



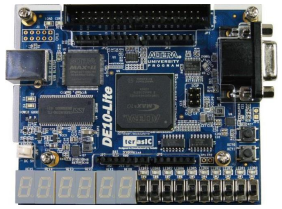
Altera DE10實驗板簡介

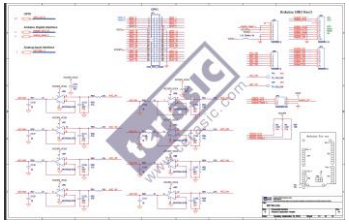


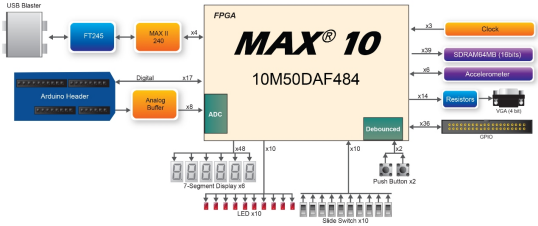


如何使用電路文件

- 電路板
- 電路圖
- 功能方塊圖
- 資料手冊





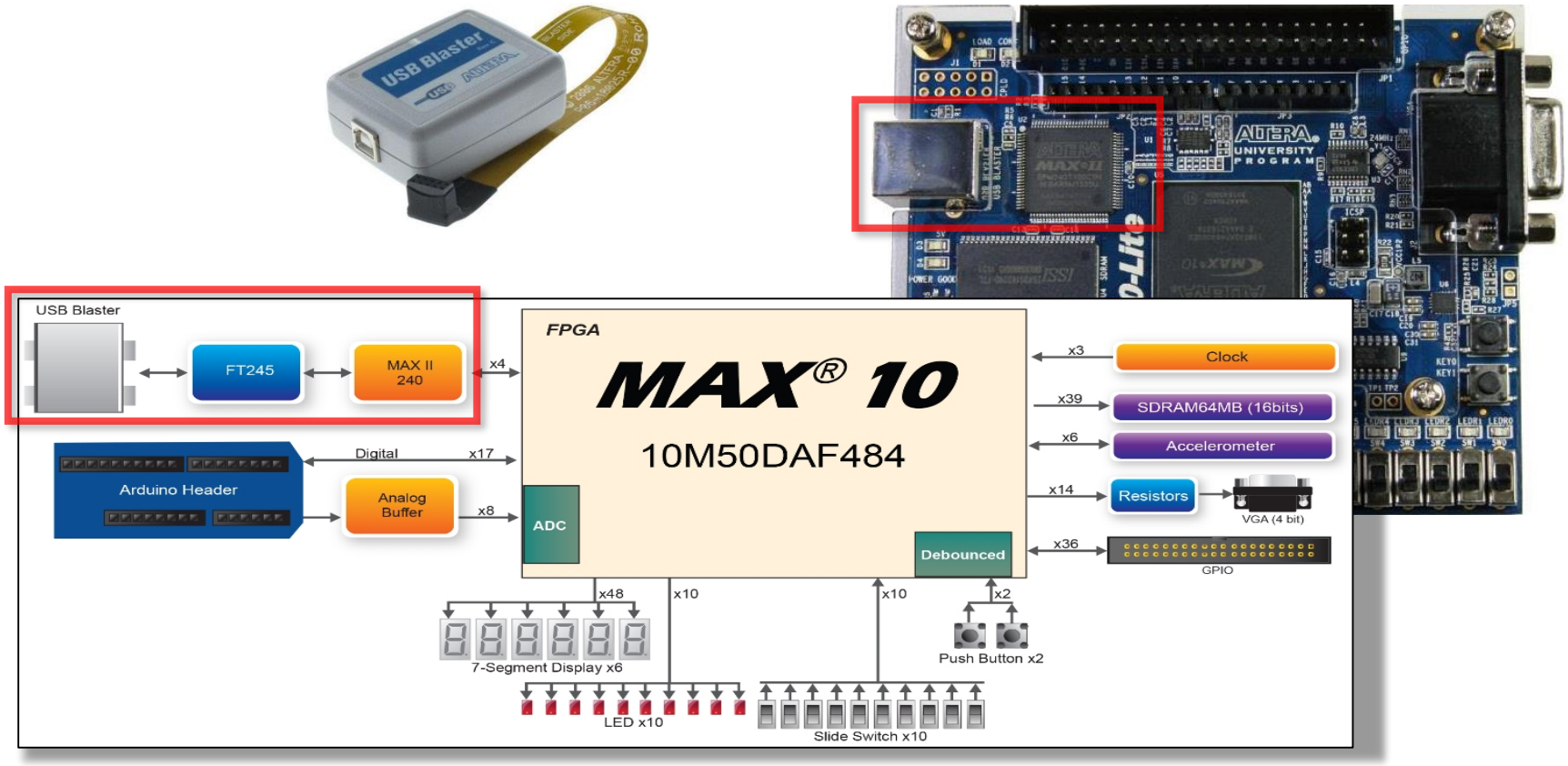


FPGA Device

- MAX 10 **10M50DAF484C7G** Device
- Integrated dual ADCs, each ADC supports1 dedicated analog input and 8 dual function pins
- 50K programmable logic elements
- 1638 Kbits M9K Memory
- 5,888 Kbits user flash memory
- 144 18*18 Multiplier
- 4 PLLS

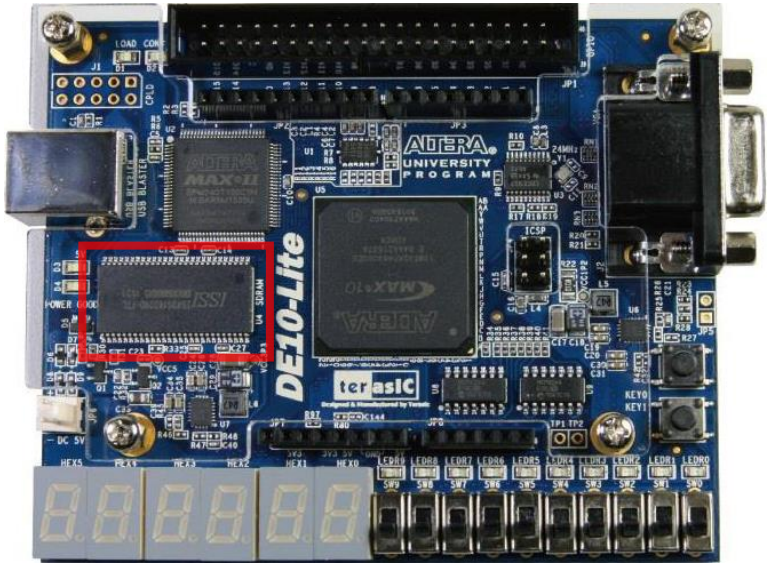
Programming and Configuration

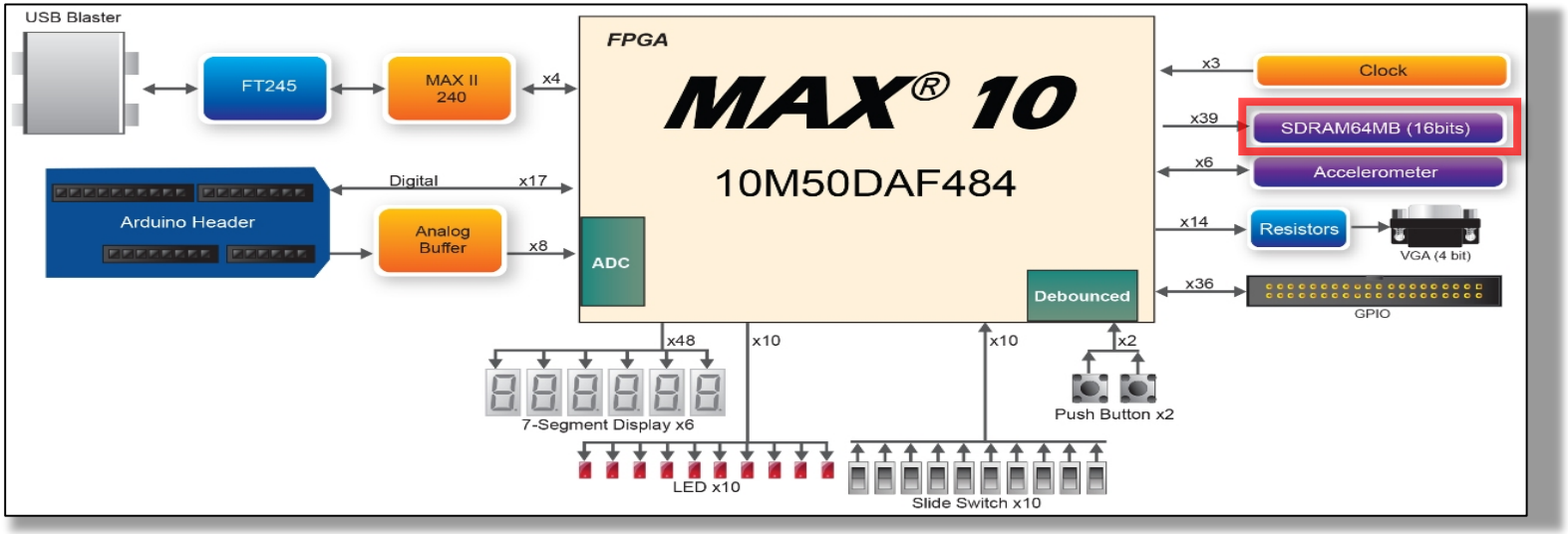
- On-Board USB Blaster



Memory Device

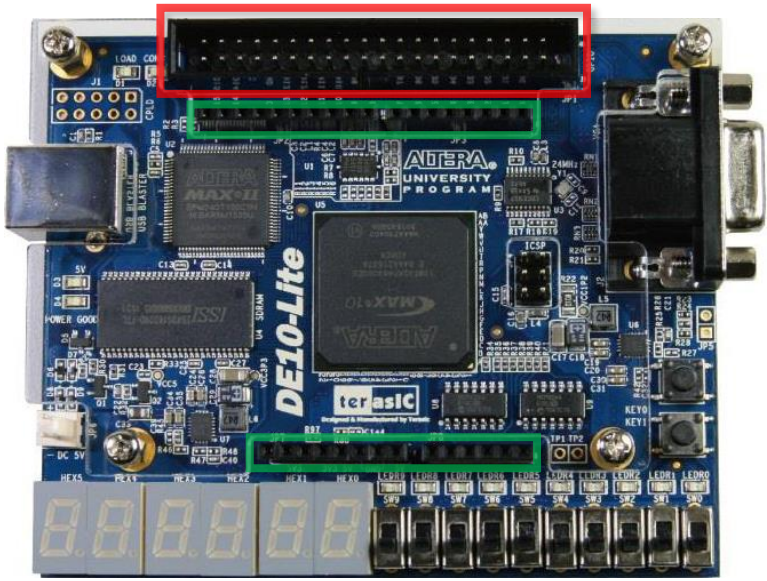
- 64MB SDRAM, x16 bits data bus

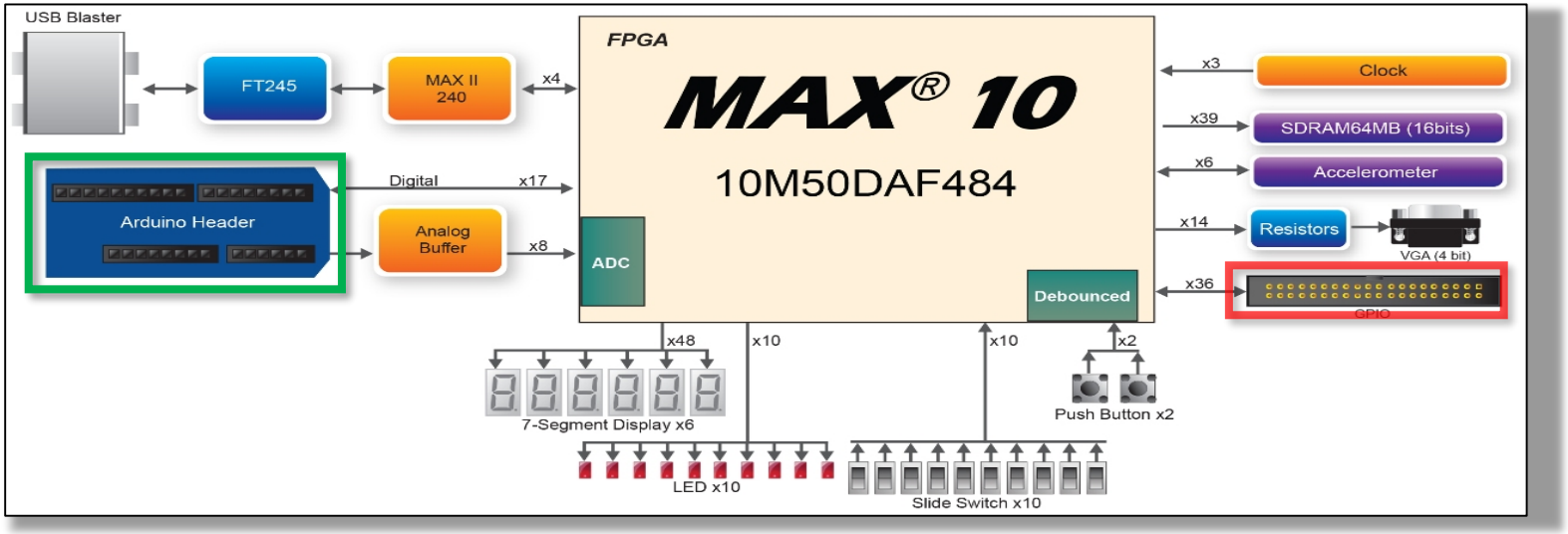




Connectors

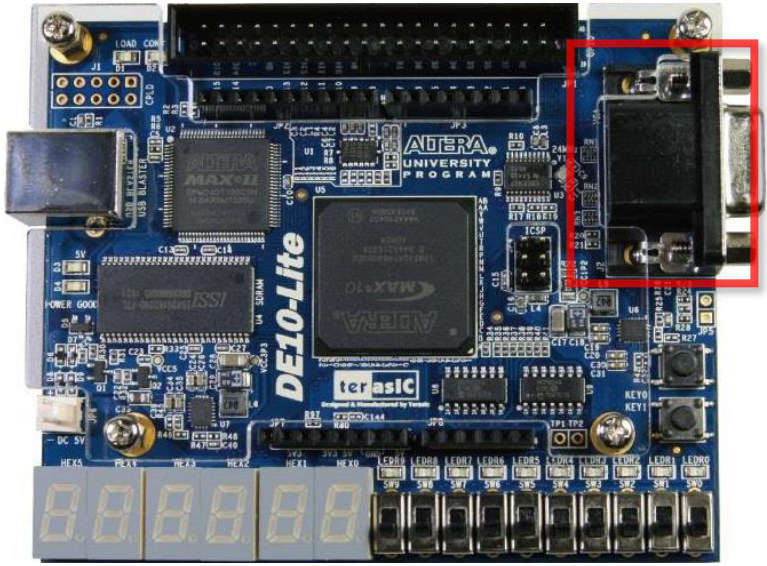
- 2*20 GPIO Header
- Arduino Uno R3 Connector, including six ADC channels

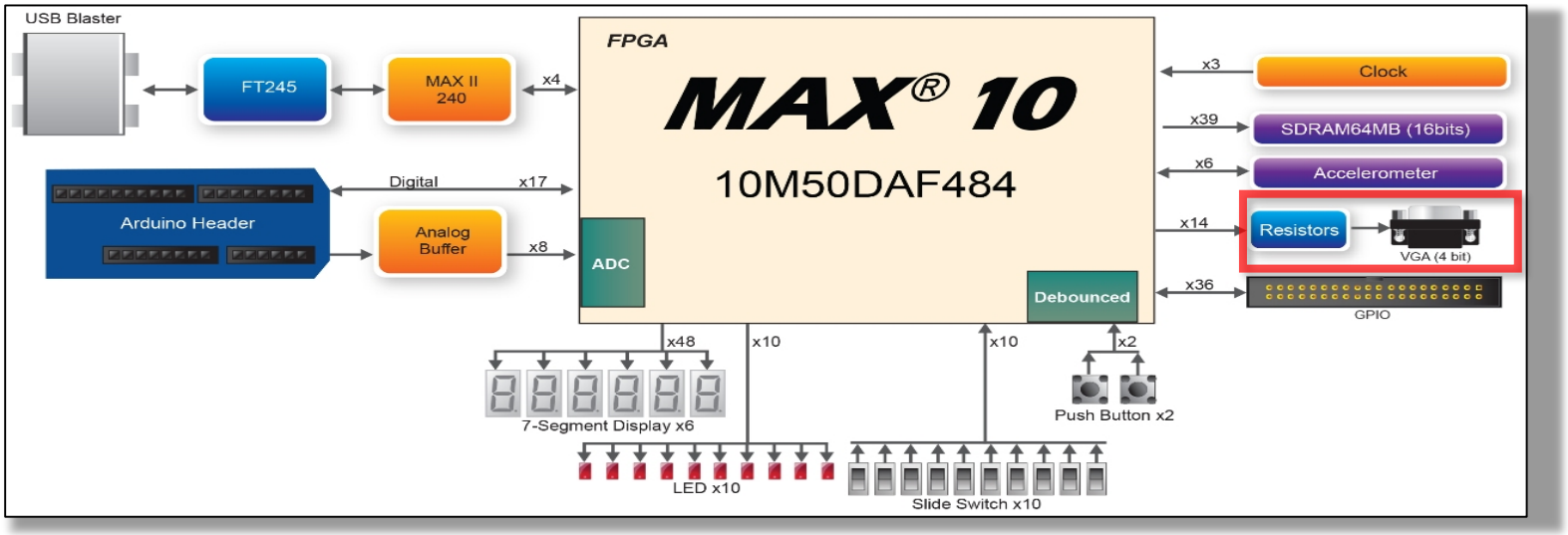




Display

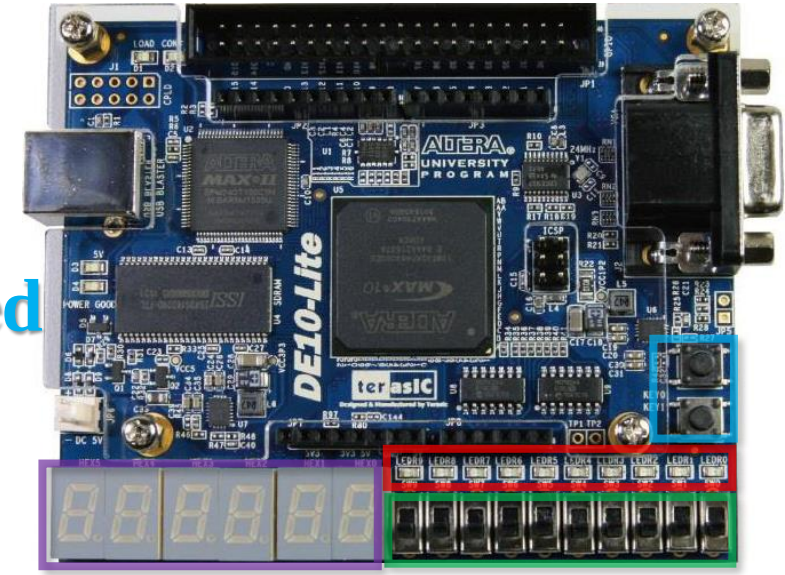
- 4-bit resistor-network DAC for VGA

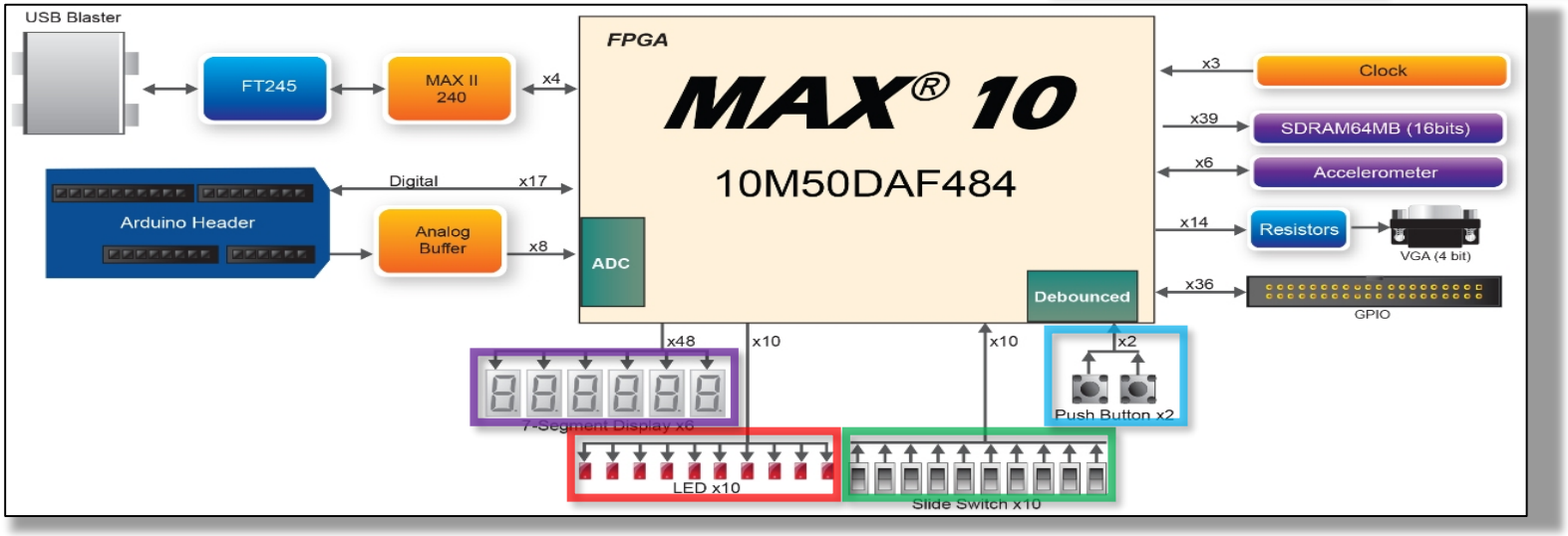




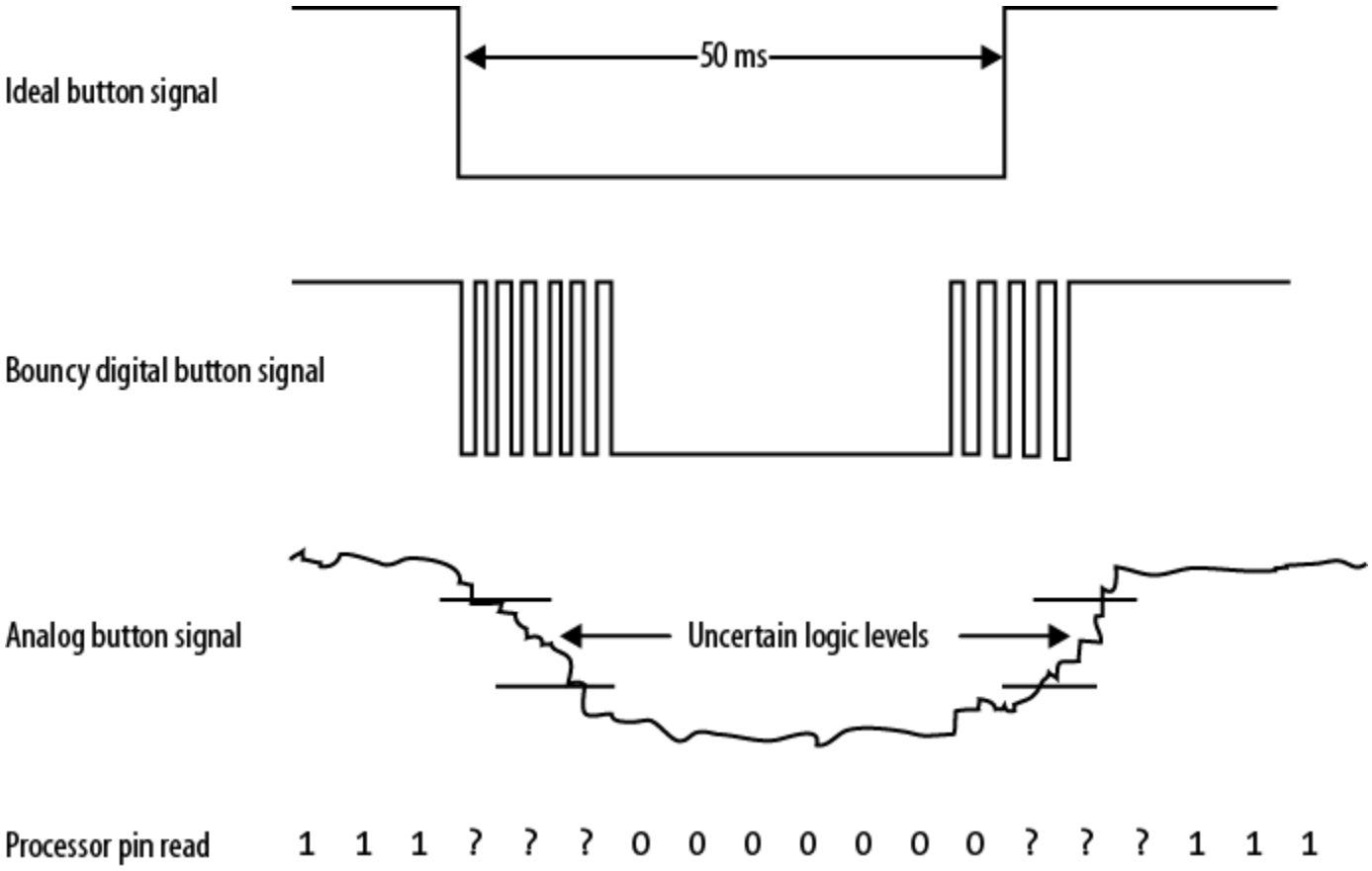
Switches,Buttons and LEDs

- 10 LEDs
- 10 Slide Switches
- 2 Push Buttons with **Debounced**
- Six 7-Segments

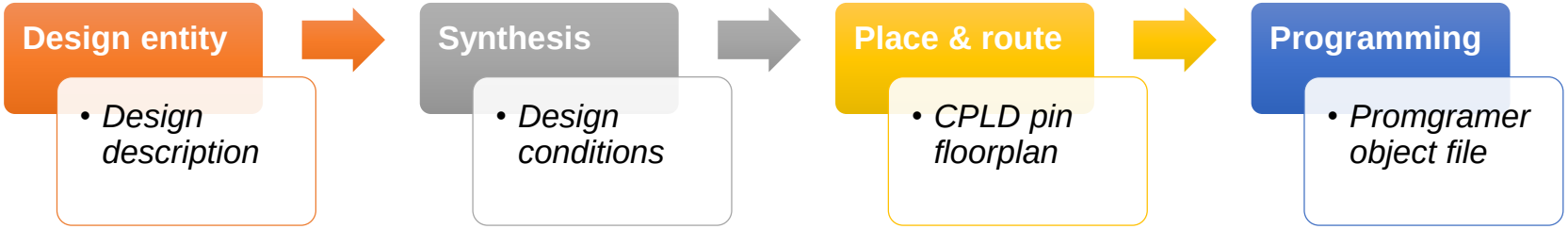




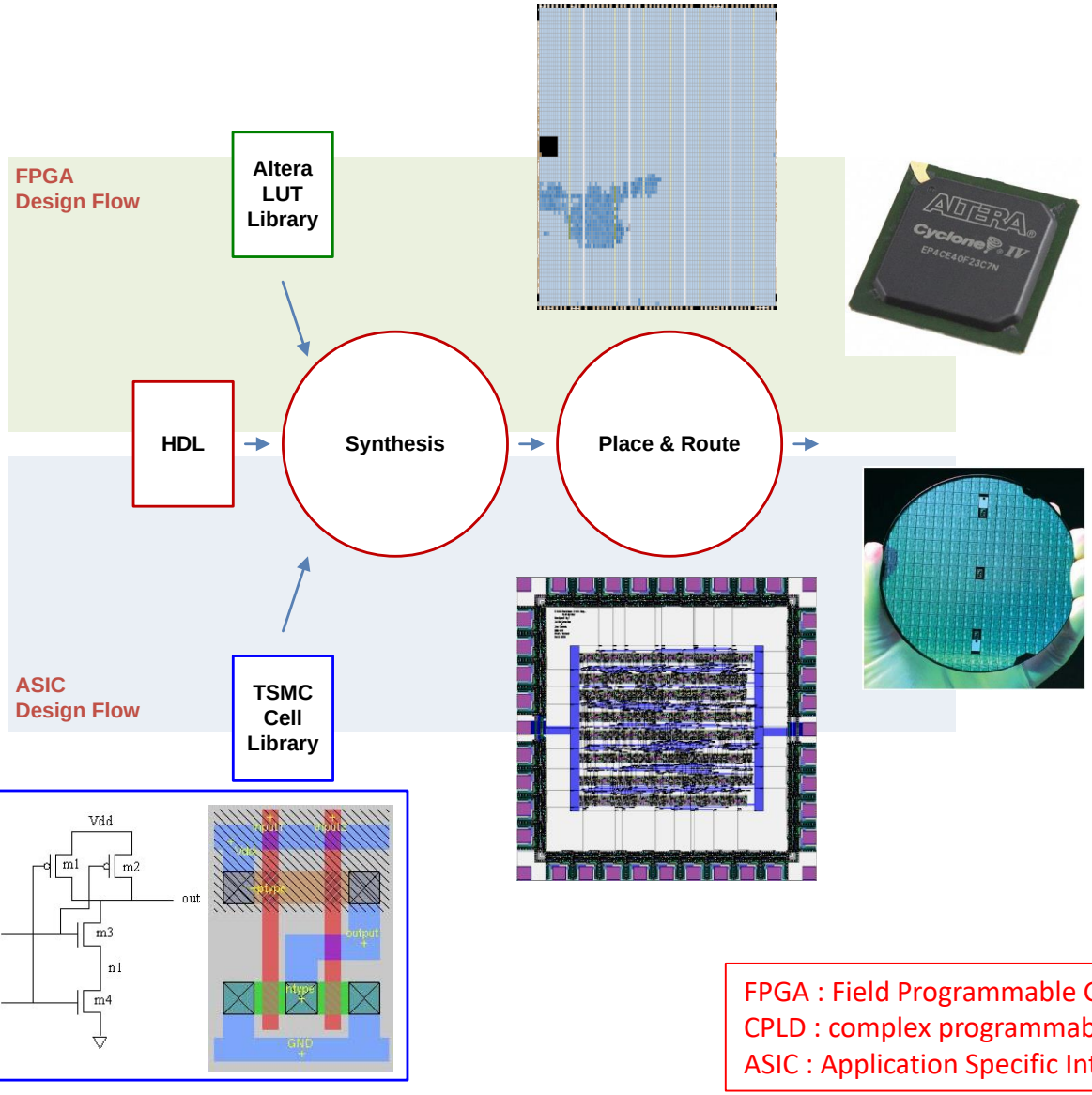
補充：**Bouncy** digital button Signal



FPGA設計流程

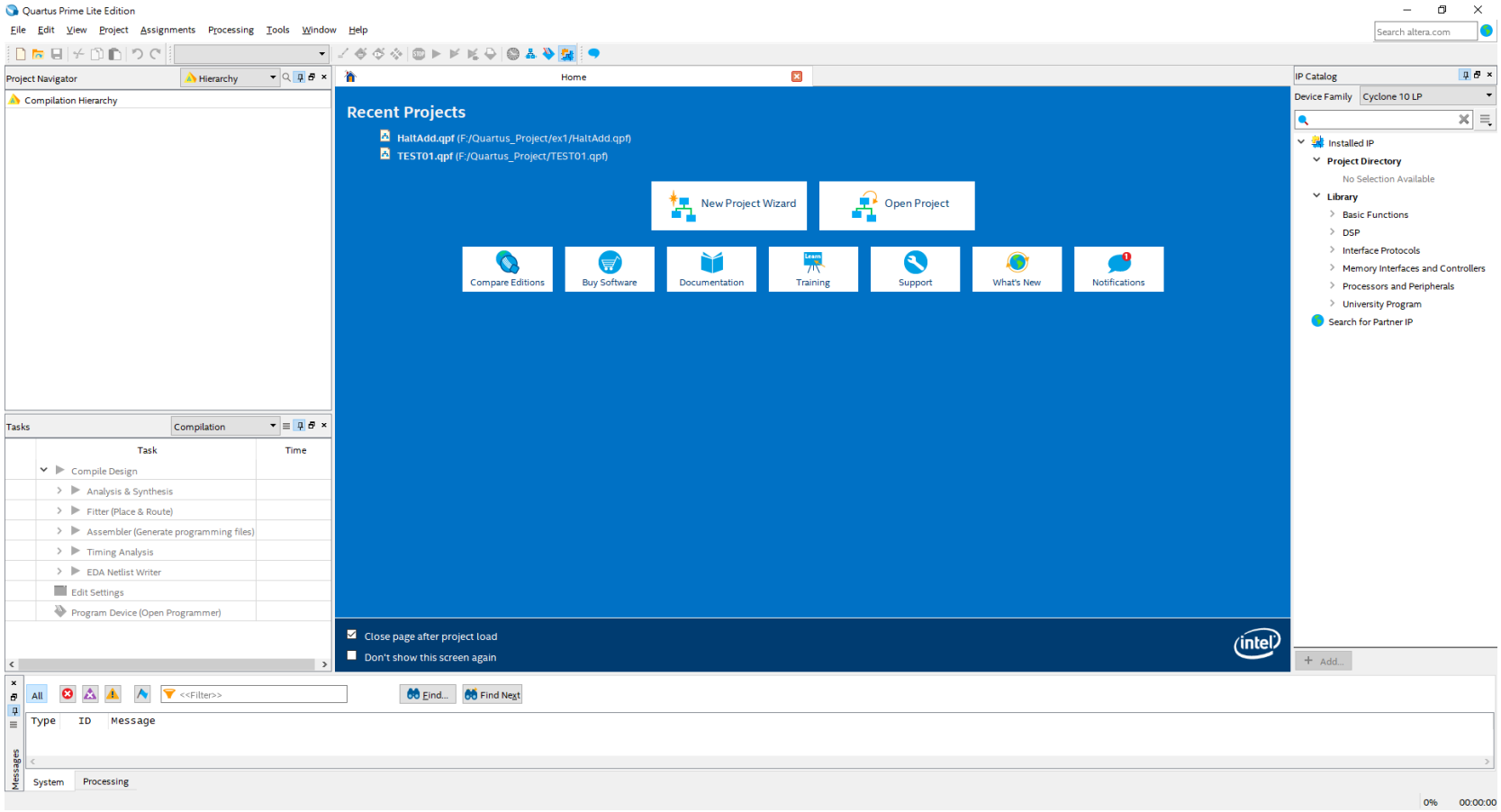

Design entity
• Design description
Synthesis
• Design conditions
Place & route
• CPLD pin floorplan
Programming
• Promgramer object file

Design Flow of FPGA and ASIC



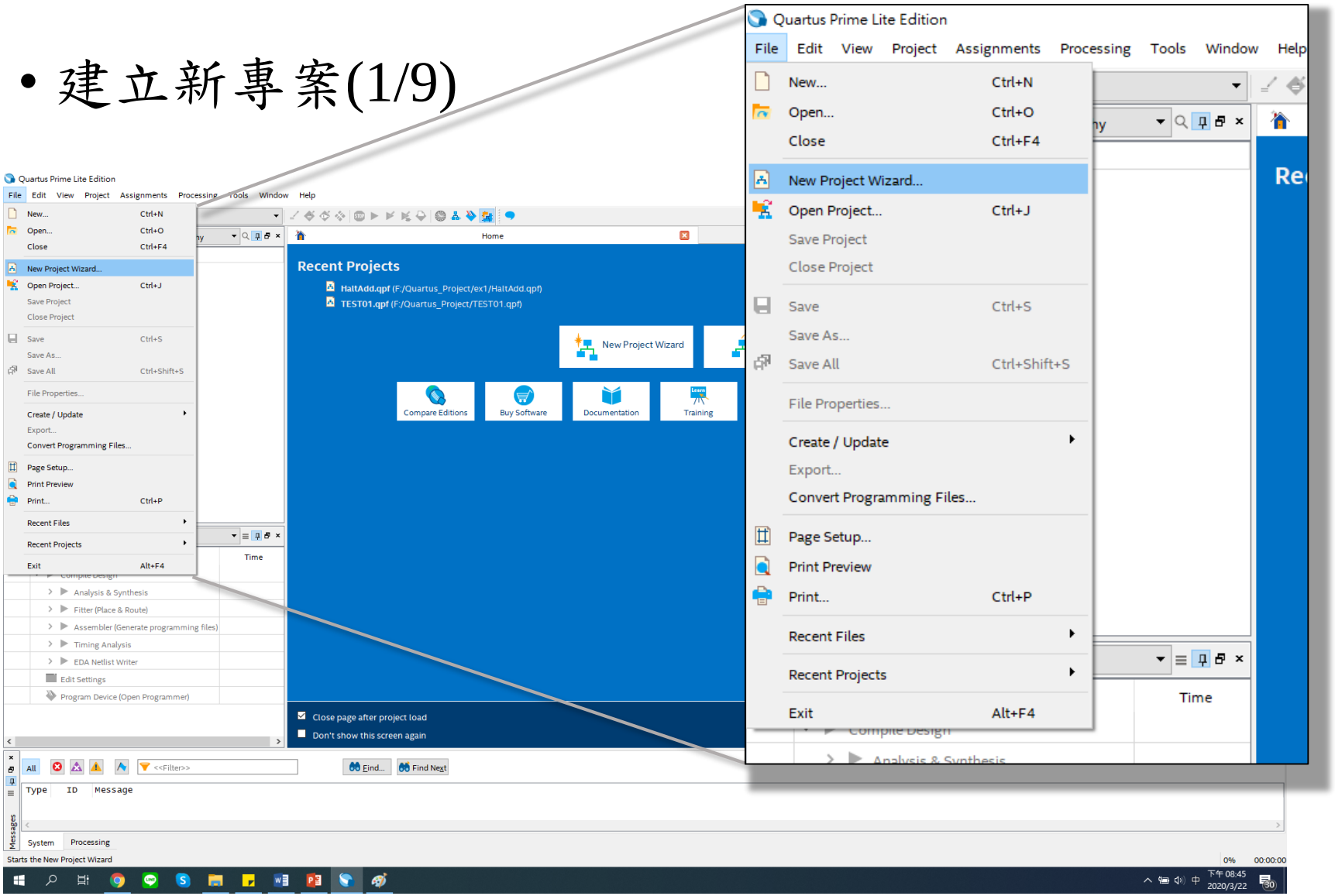
FPGA : Field Programmable Gate Array
CPLD : complex programmable logic device
ASIC : Application Specific Integrated Circuit

Quartus Prime



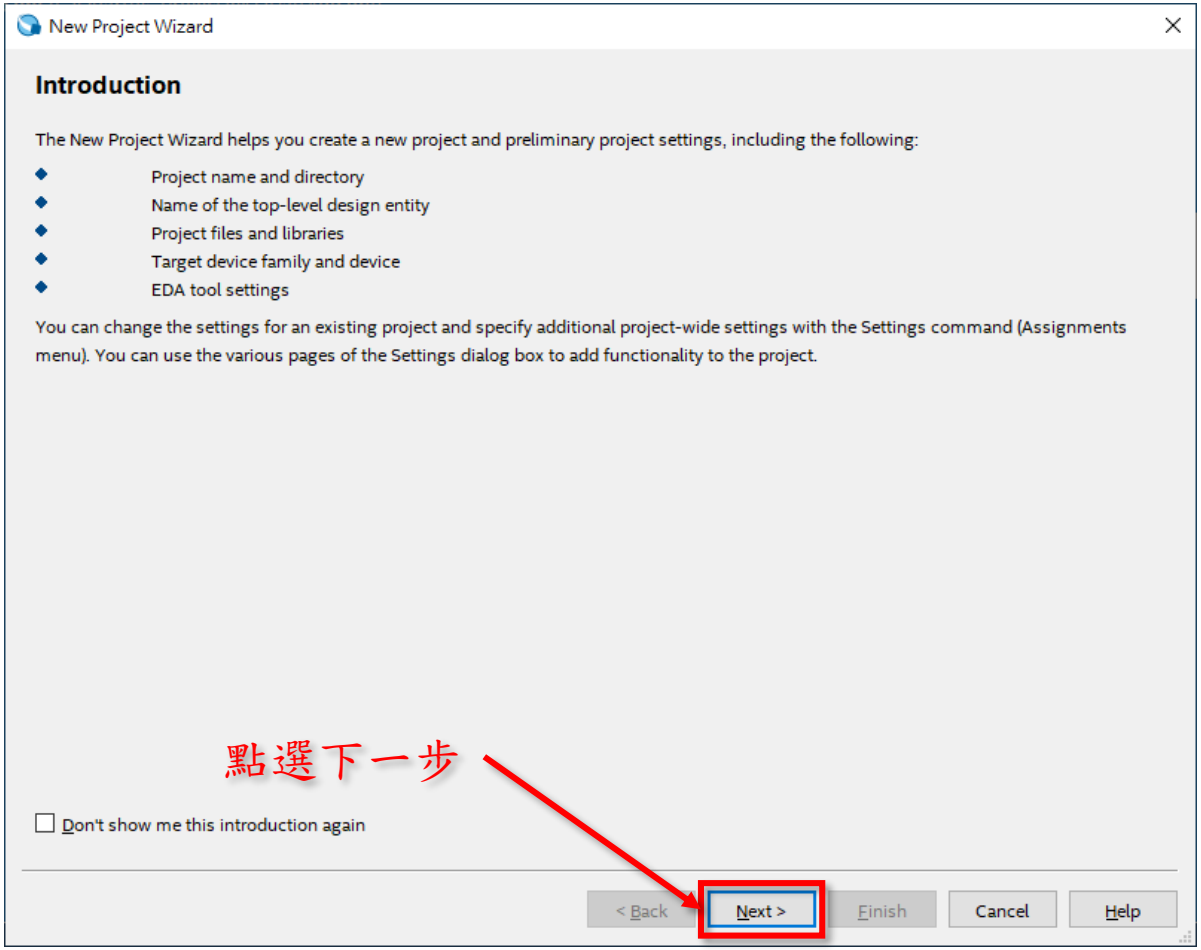
Quartus Prime

- 建立新專案(1/9)



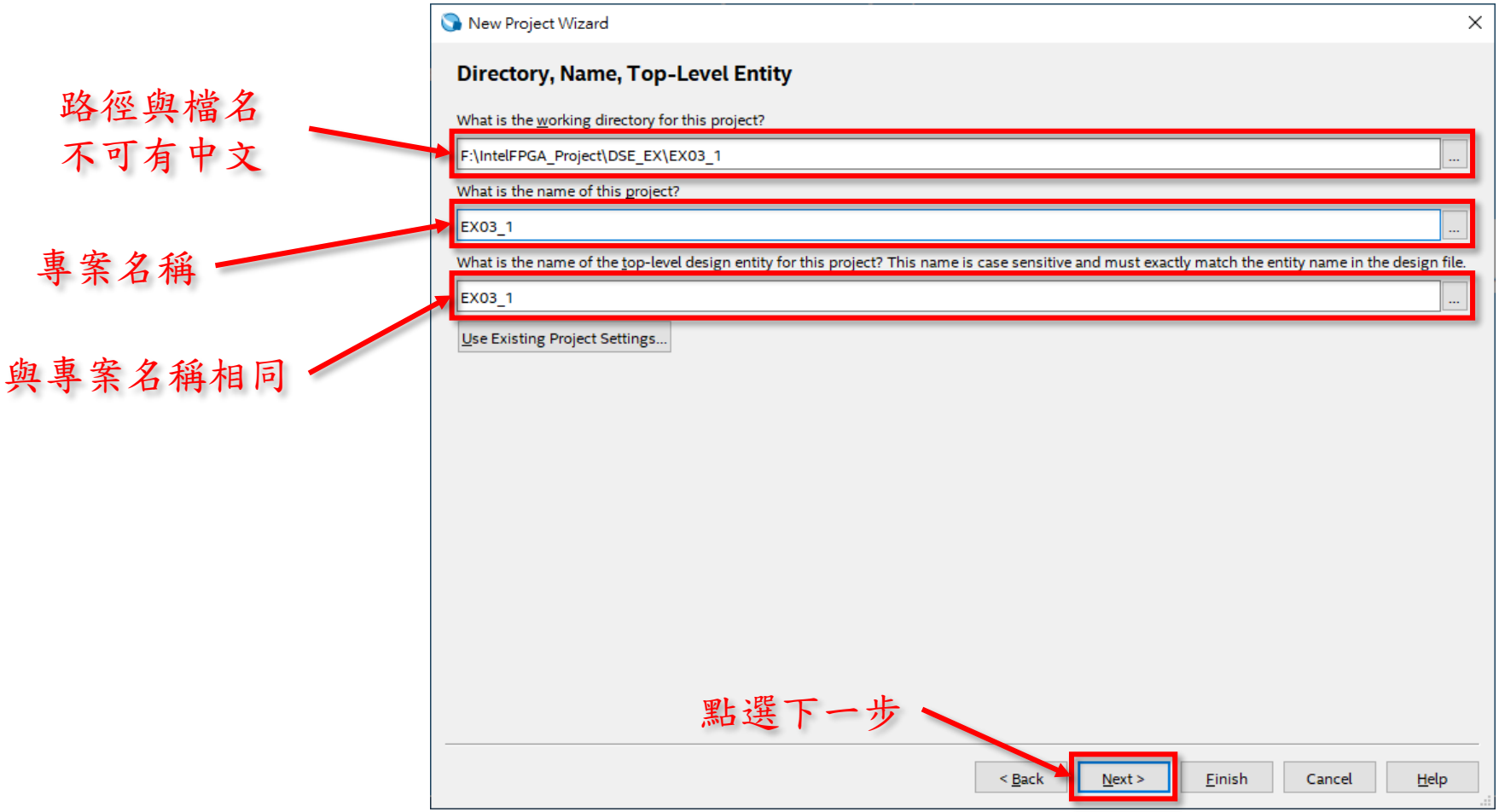
Quartus Prime

- 建立新專案(2/9)



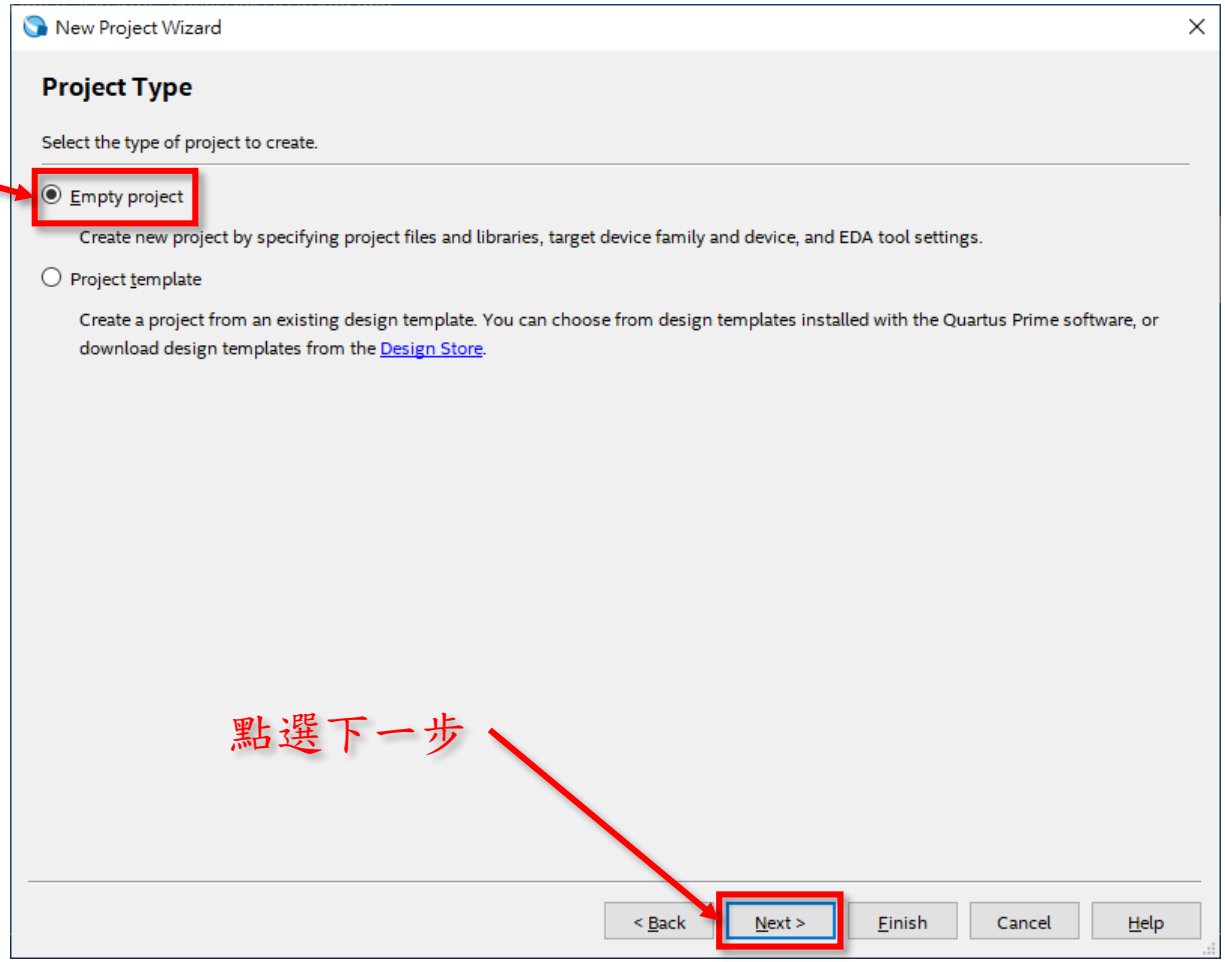
Quartus Prime

- 建立新專案(3/9)



Quartus Prime

- 建立新專案(4/9)

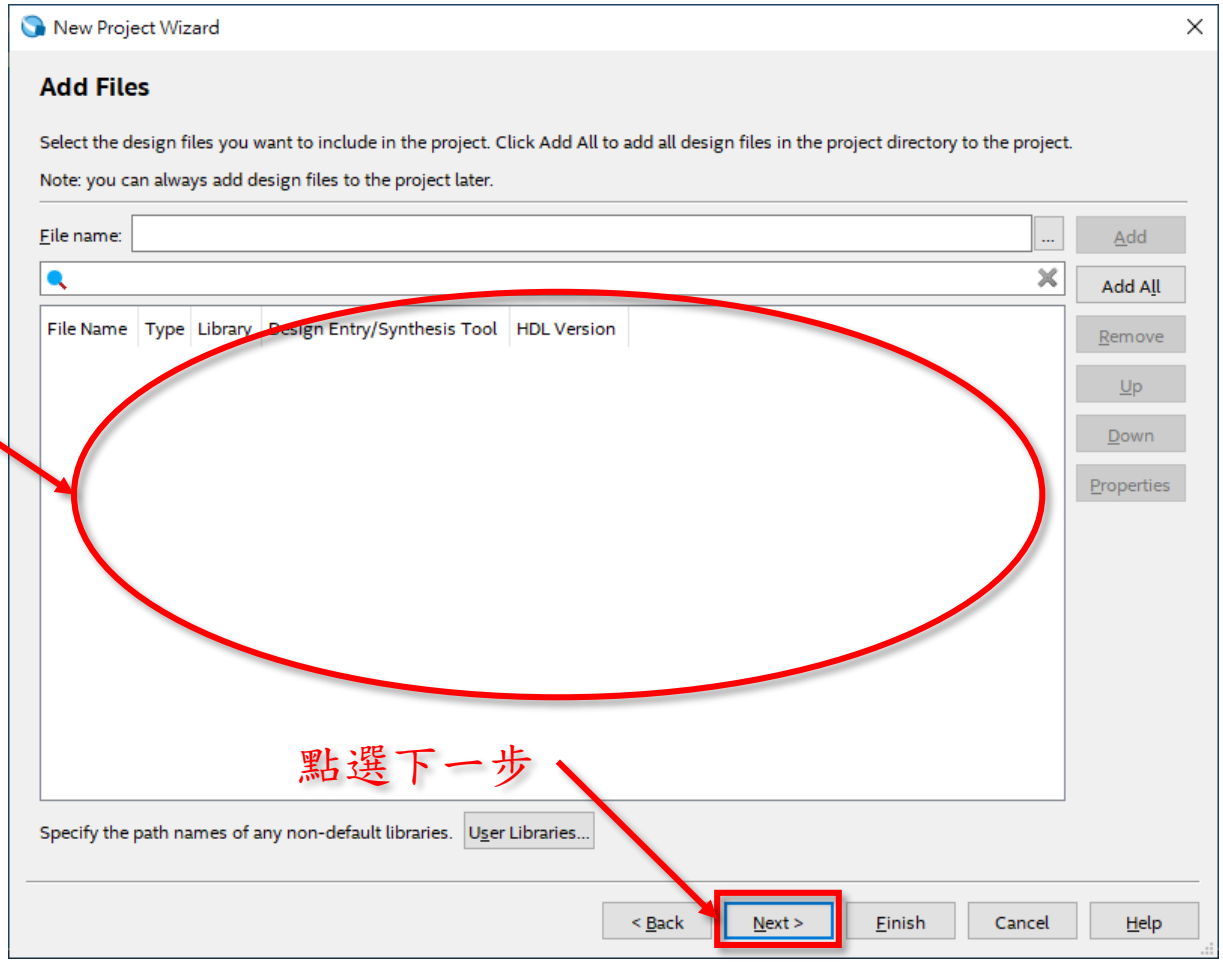


選擇空白專案

點選下一步

Quartus Prime

- 建立新專案(5/9)



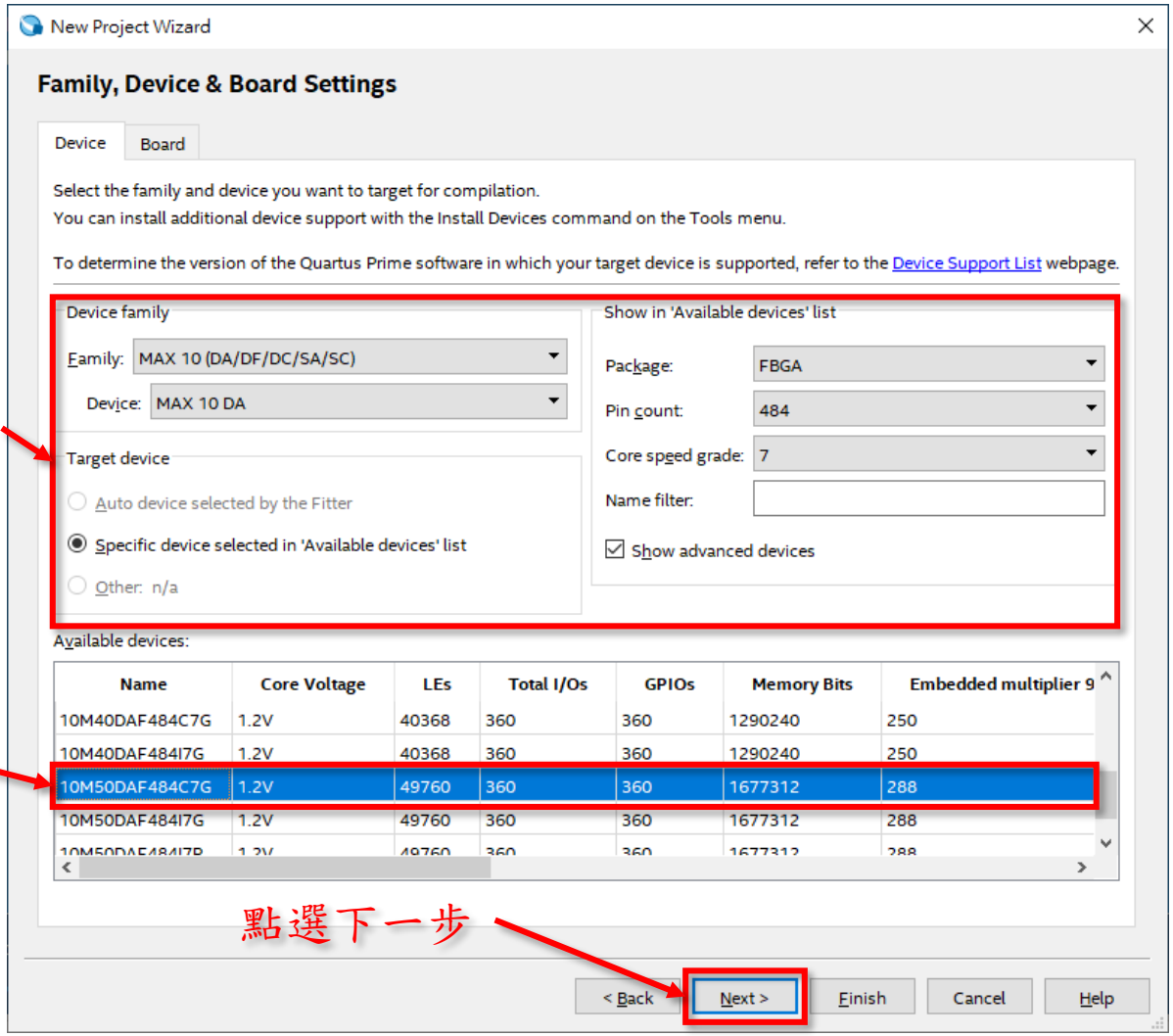
Quartus Prime

- 建立新專案 (6/9)

利用參數濾出適當的晶片

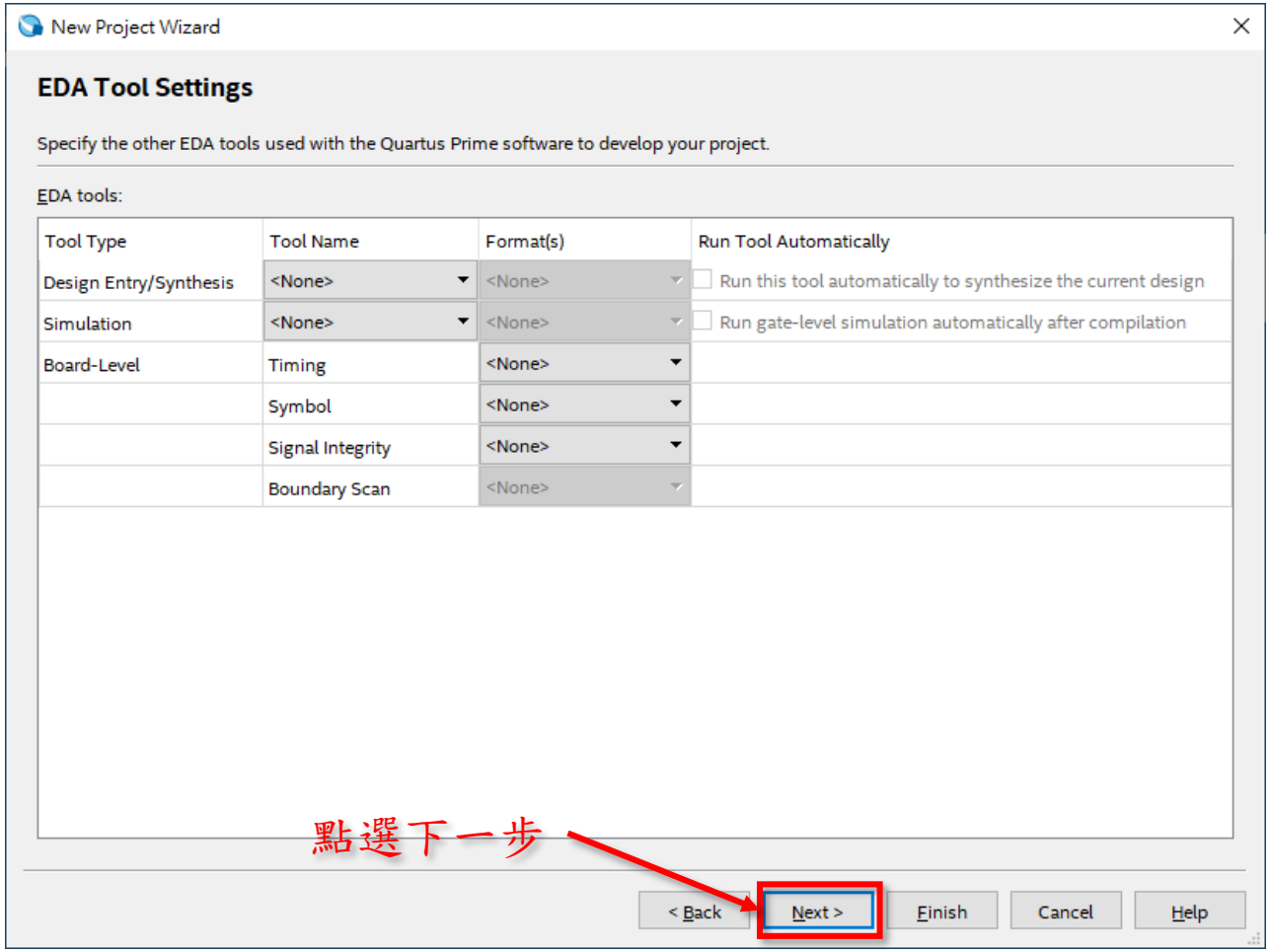
Family : MAX 10 (DA/DF/DC/SA/SC)
Device : MAX 10 DA
Package : FBGA
Pin xount : 484
Core speed grade : 7

選擇10M50DAF484C7G



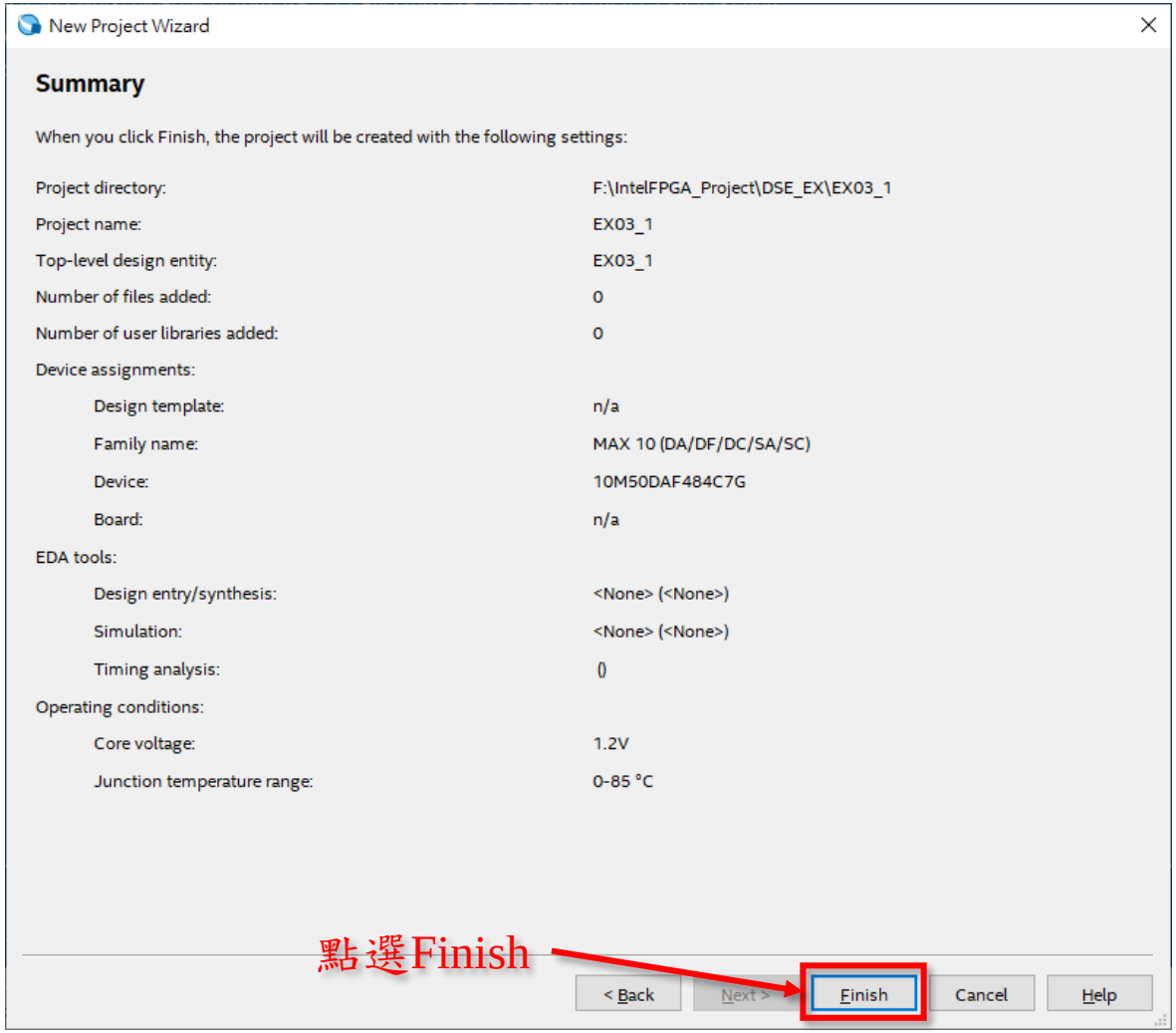
Quartus Prime

- 建立新專案(7/9)



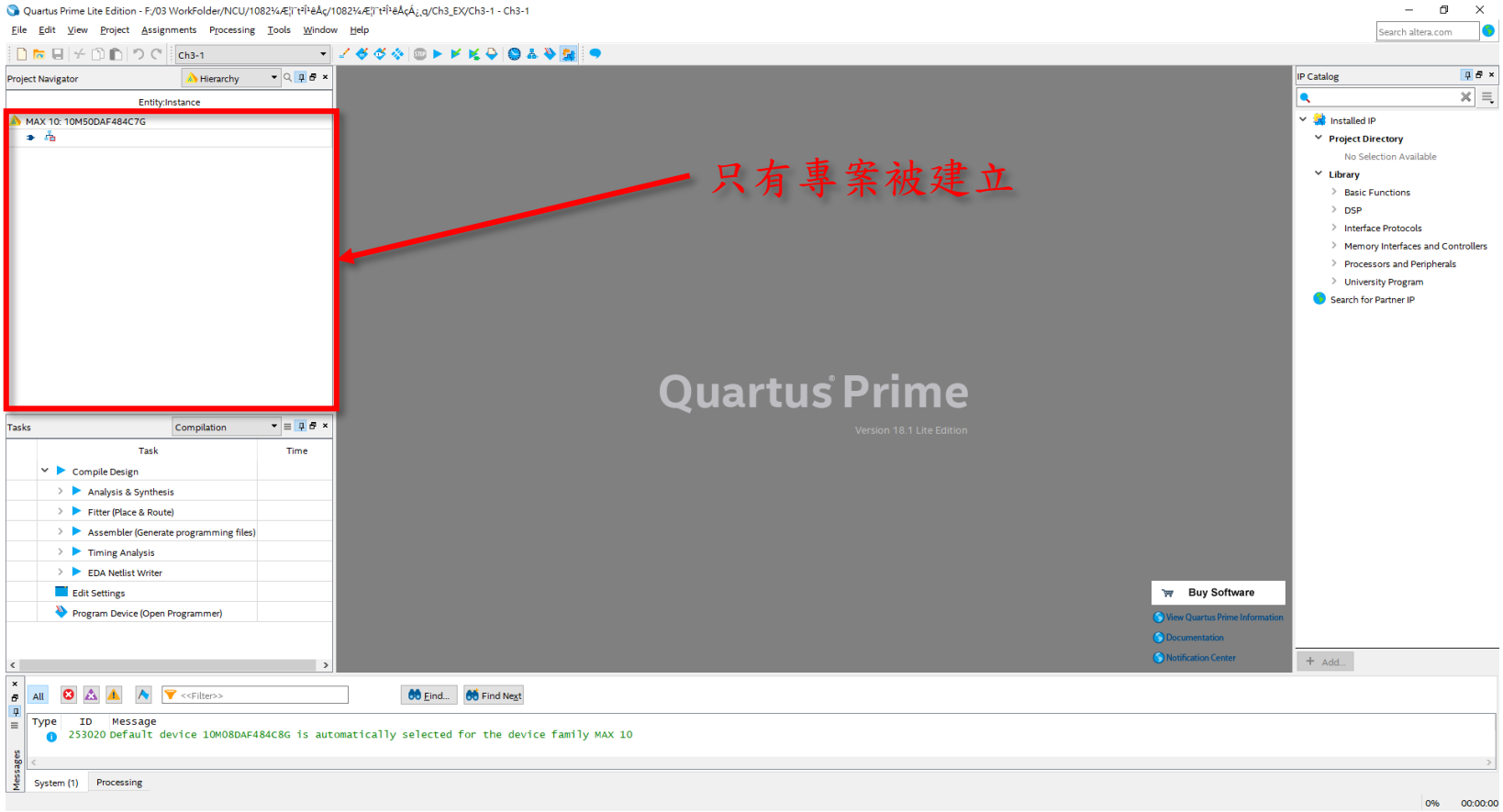
Quartus Prime

- 建立新專案 (8/9)



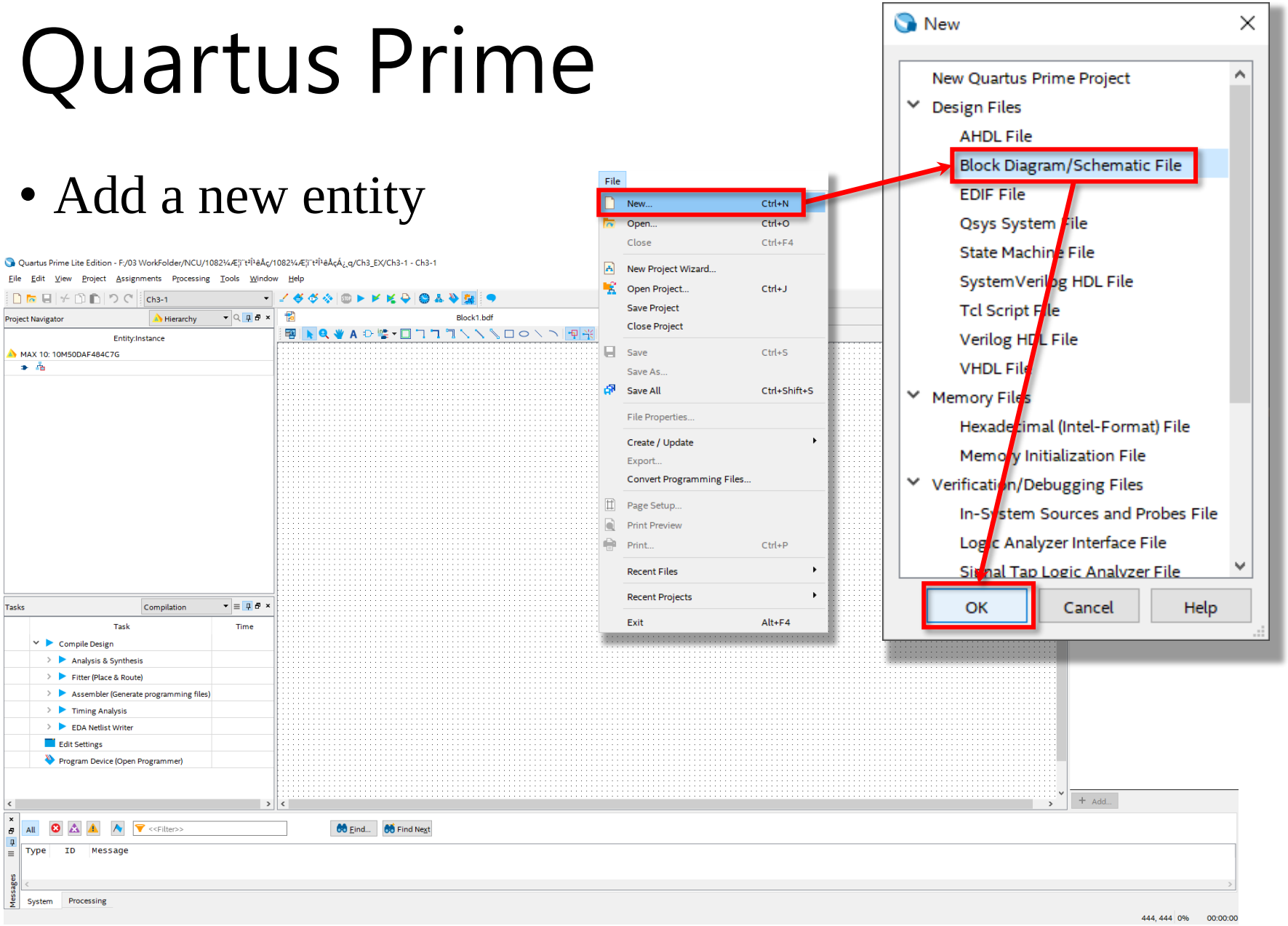
Quartus Prime

- 建立新專案(9/9)



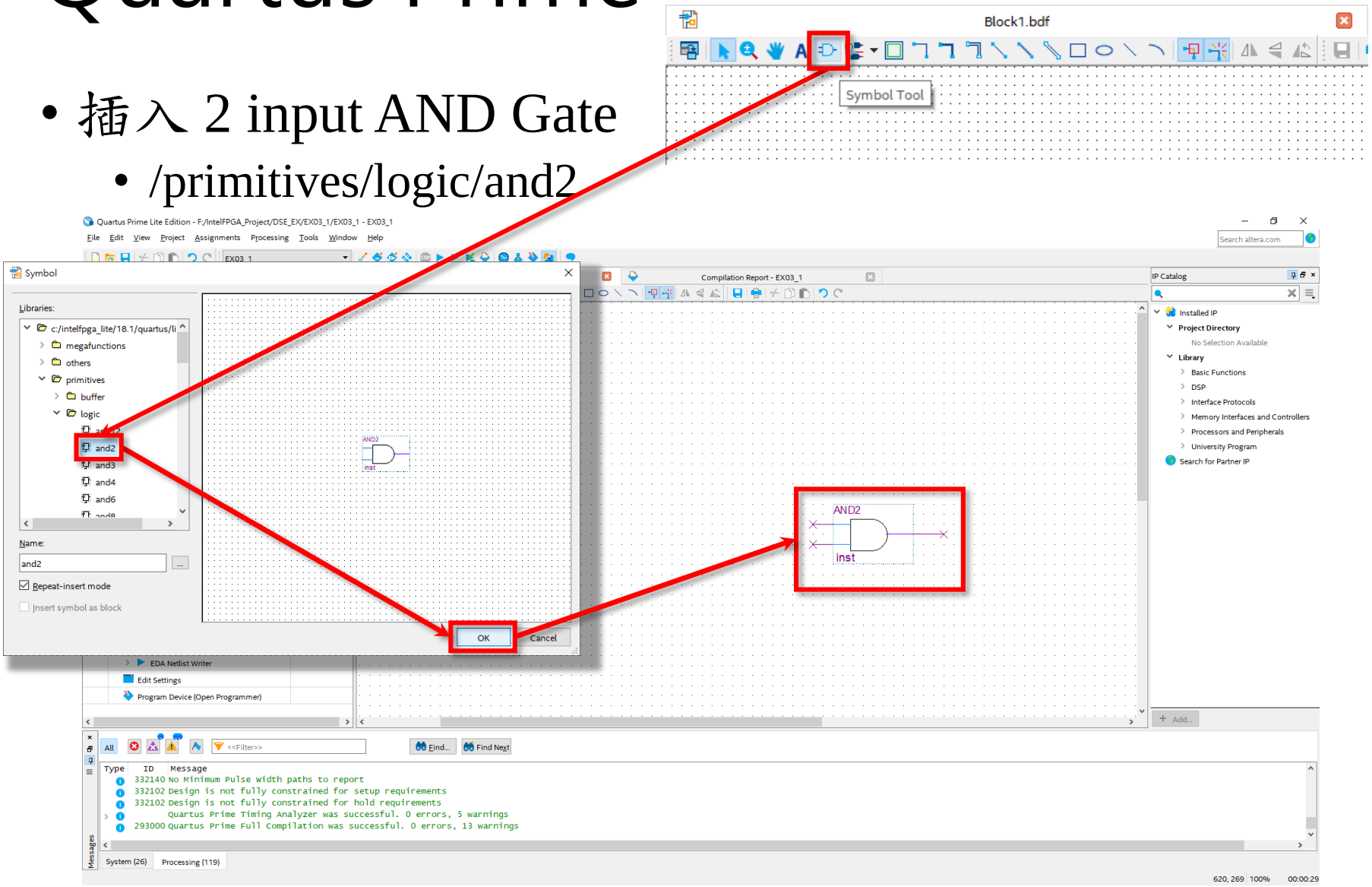
Quartus Prime

- Add a new entity



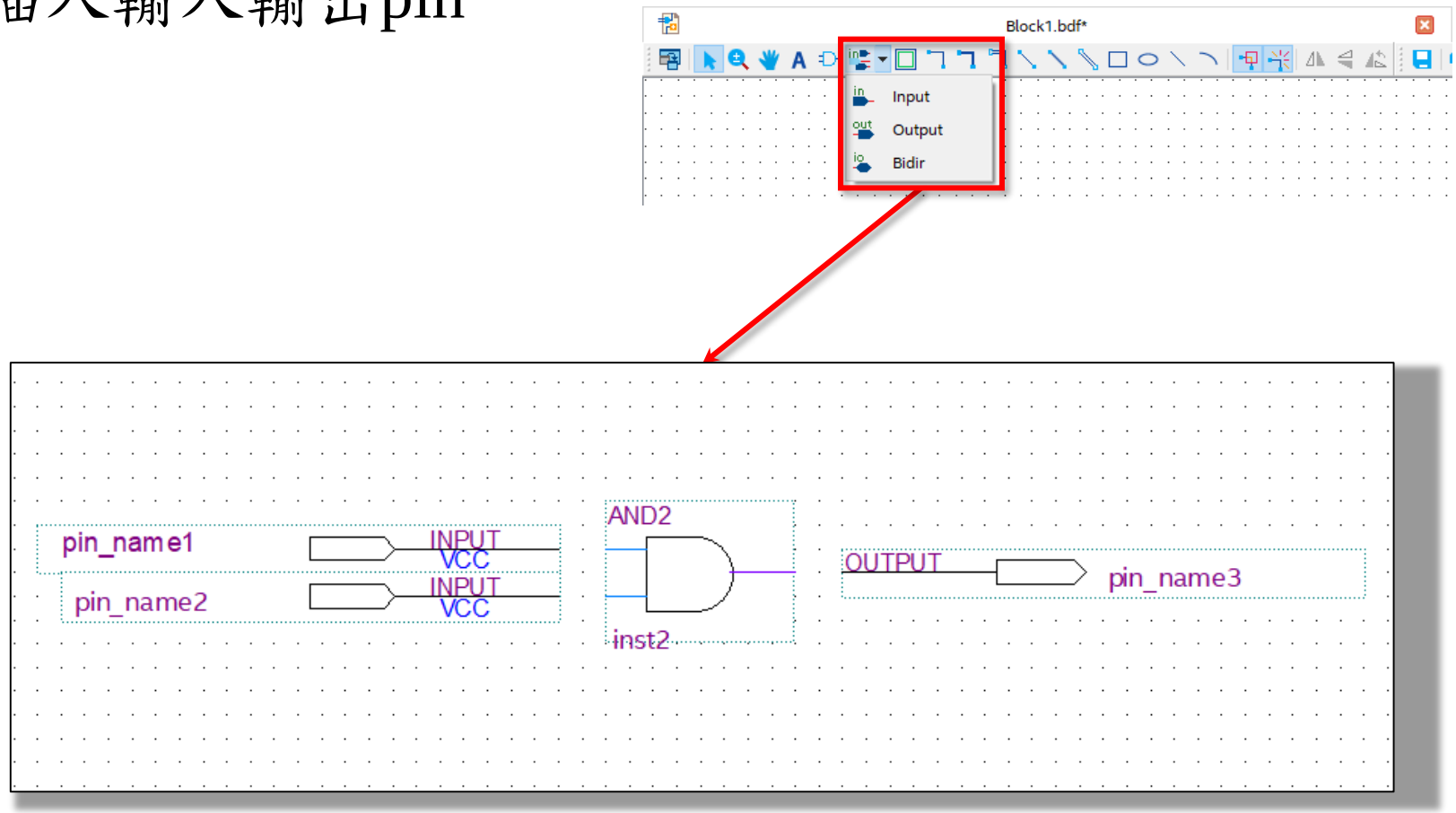
Quartus Prime

- 插入 2 input AND Gate
  - /primitives/logic/and2



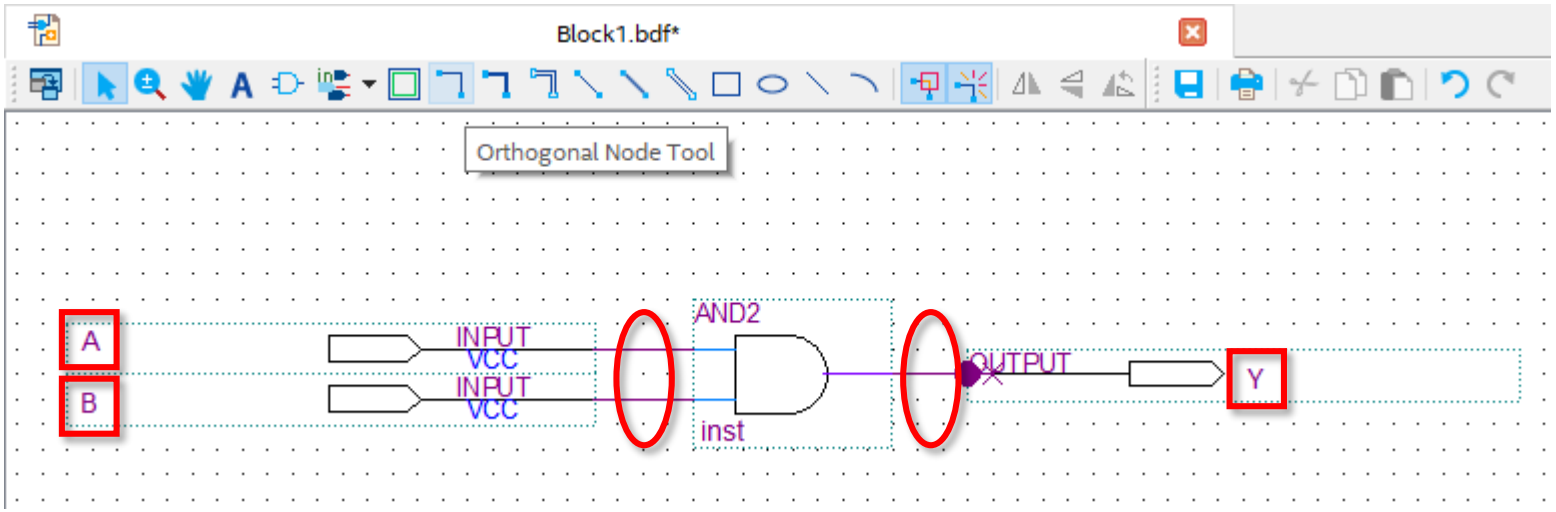
Quartus Prime

- 插入輸入輸出pin



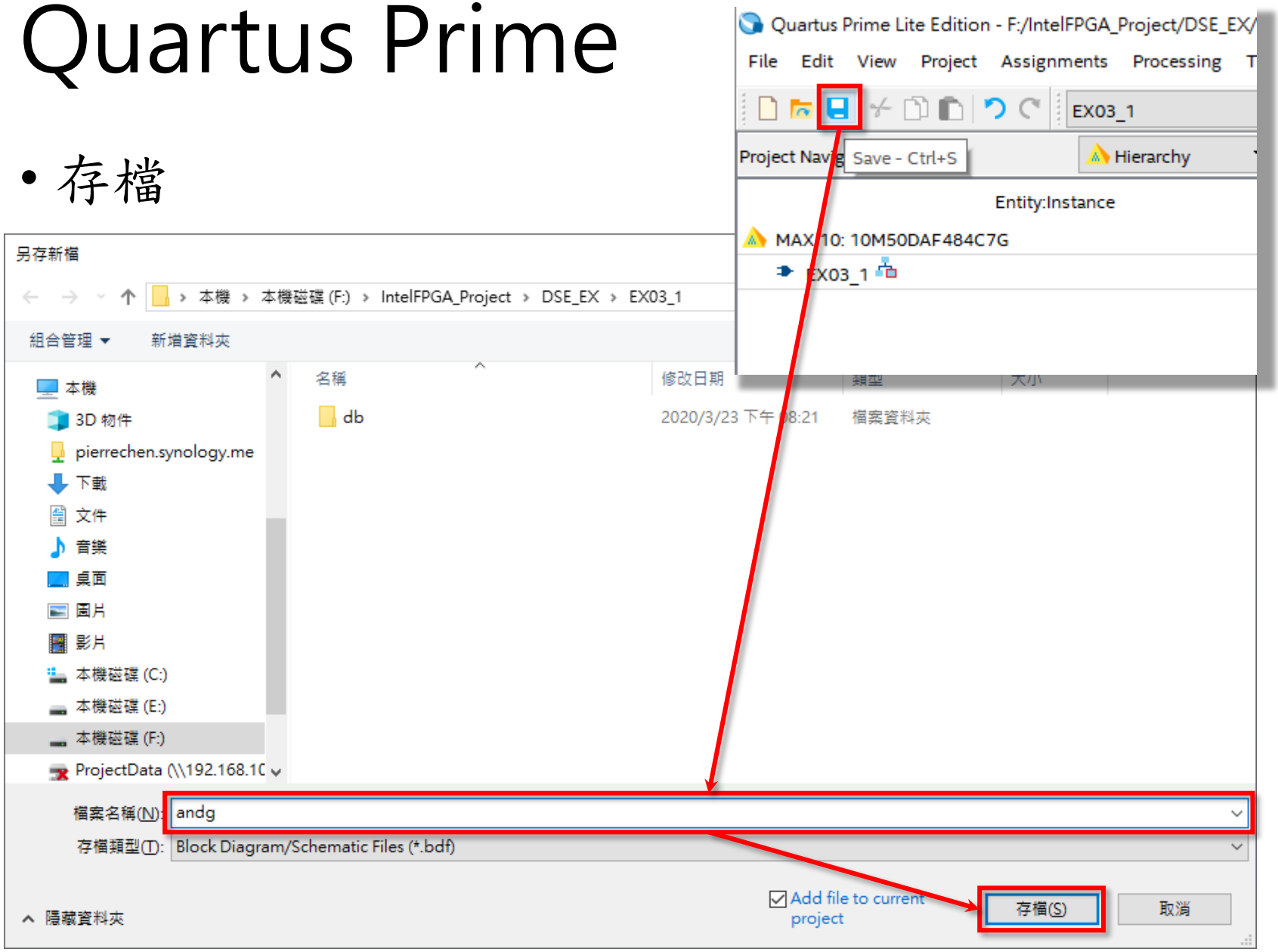
Quartus Prime

- 連接輸入輸出
- 修改pin name



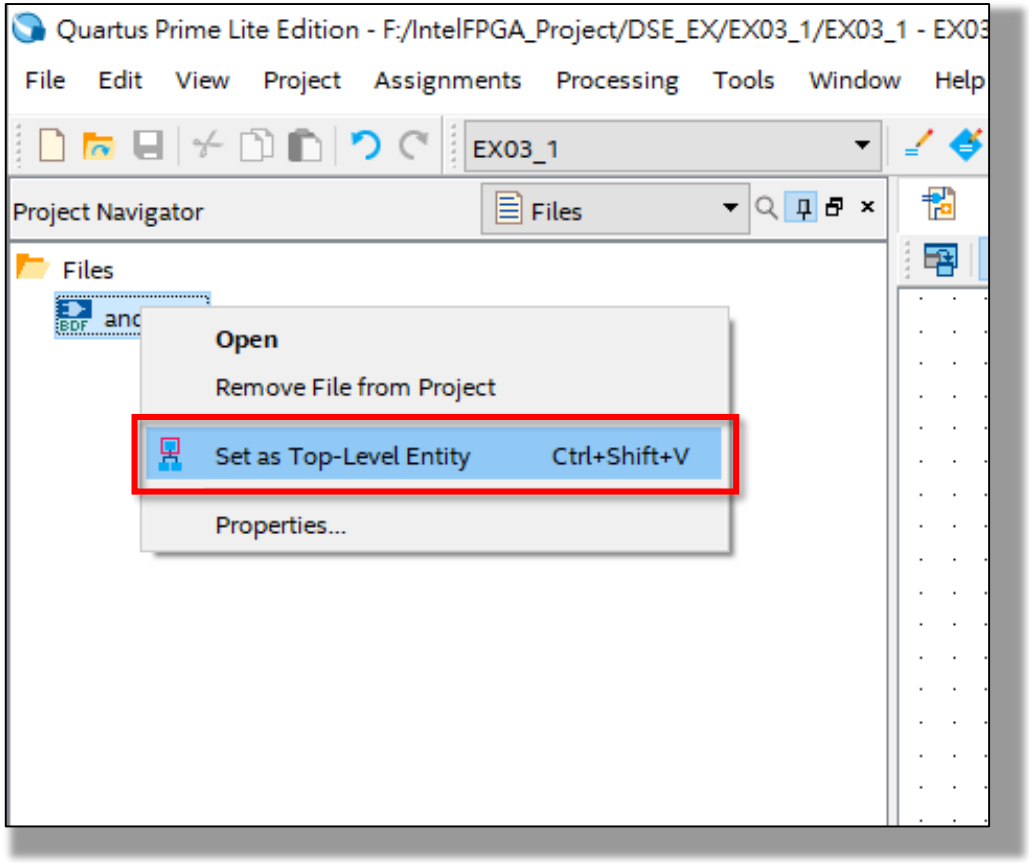
Quartus Prime

- 存檔

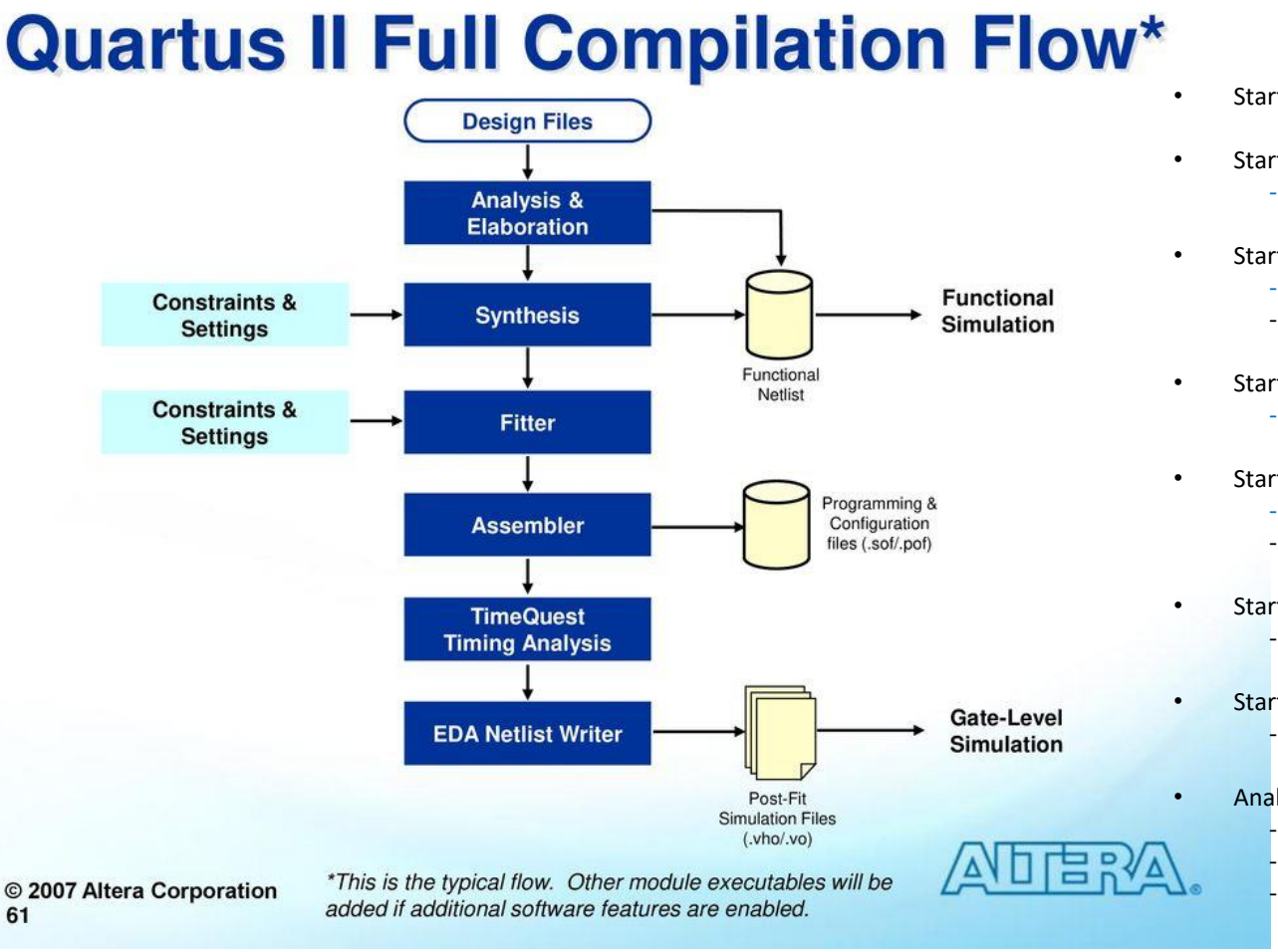


Quartus Prime

- 將Entity設定為Top-Level Entity

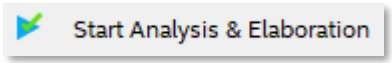


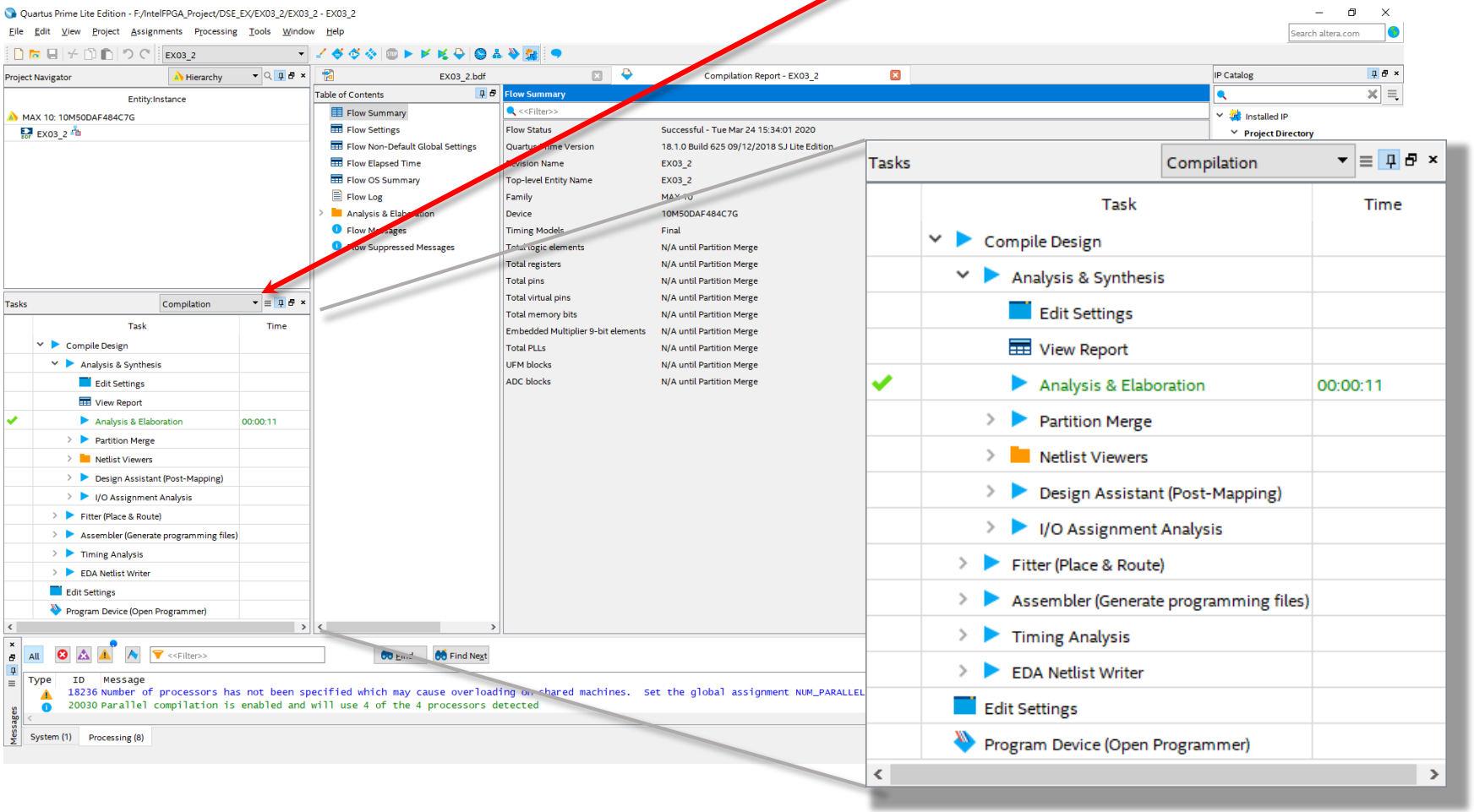
補充



- Start Compilation (Full)
- Start Hierarchy Elaboration
  - Checks syntax & build hierarchy
- Start Analysis & Elaboration
  - Checks syntax & builds hierarchy
  - Performs initial synthesis
- Start Analysis & Synthesis
  - Synthesizes & optimizes code
- Start Fitter
  - Places & routes design
  - Generates output netlists
- Start Assembler
  - Generates programming files
- Start EDA Netlist Writer
  - Dump Gate-level netlist file for simulation
- Analyzers
  - I/O Assignment
  - PowerPlay
  - Design Assistant

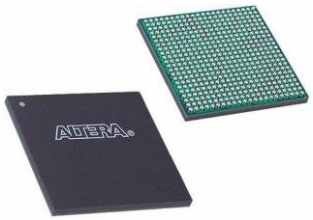
Quartus Prime

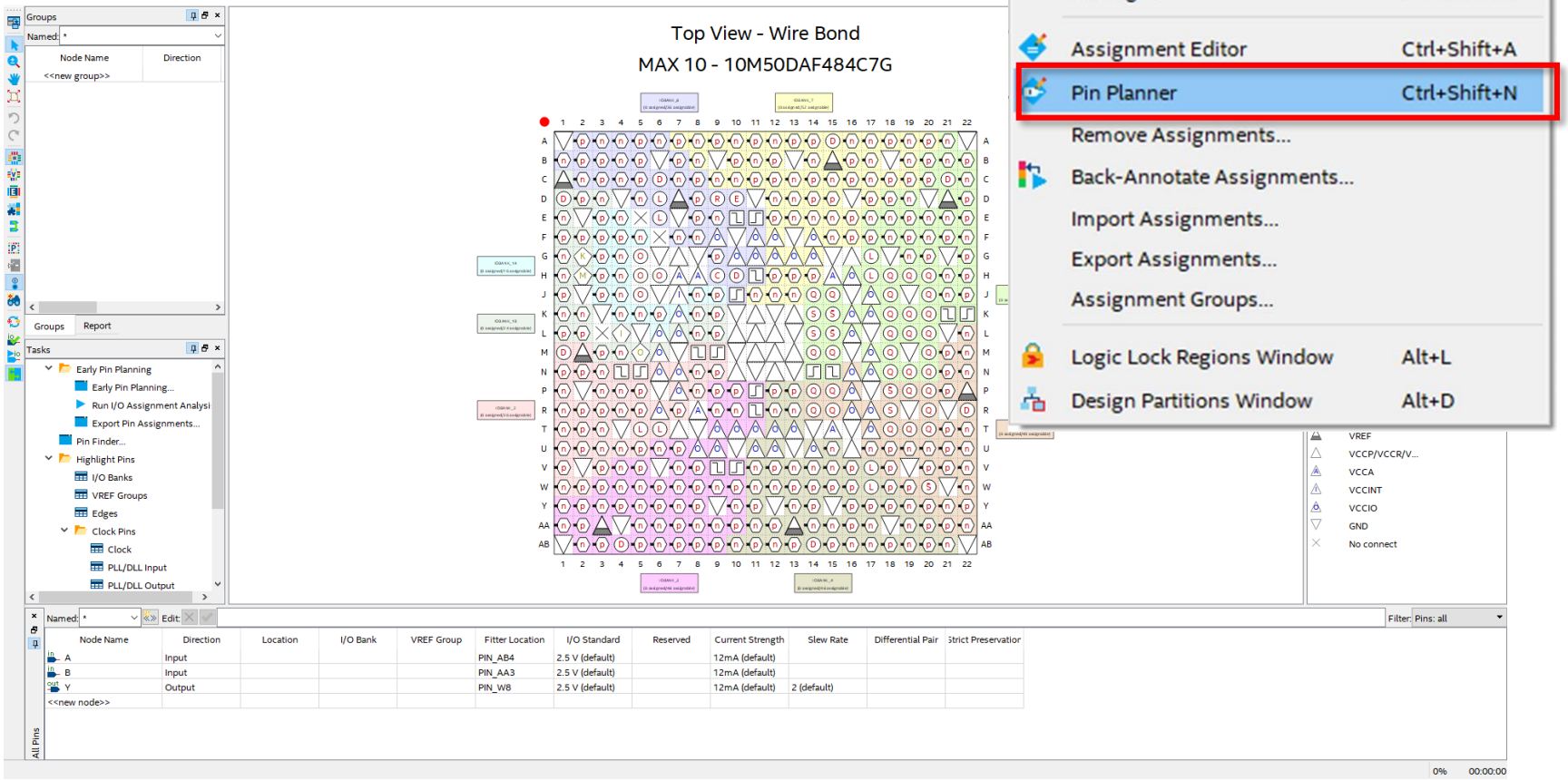
- Compile 



Quartus Prime

- Pin Planner (1/2)

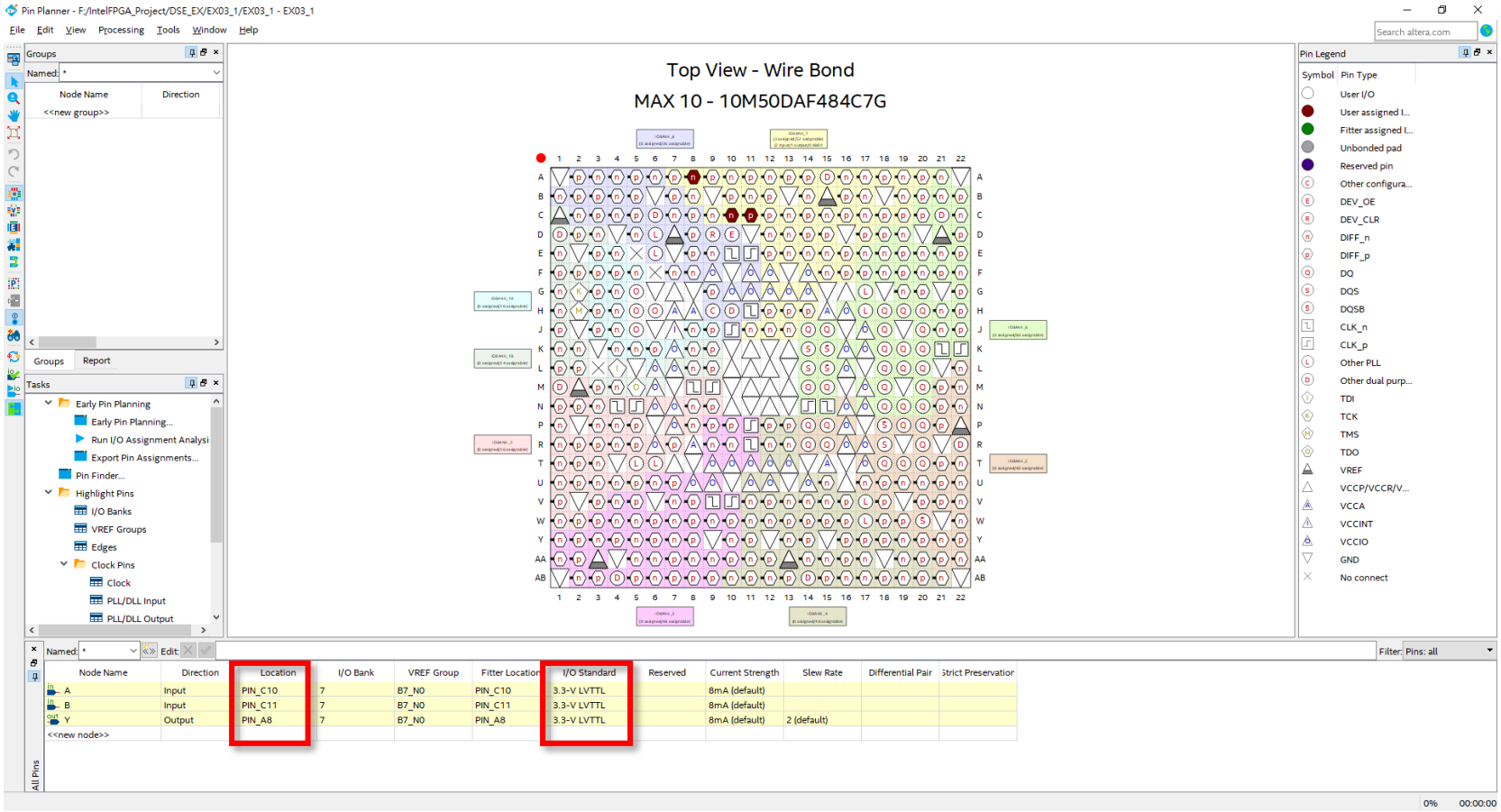




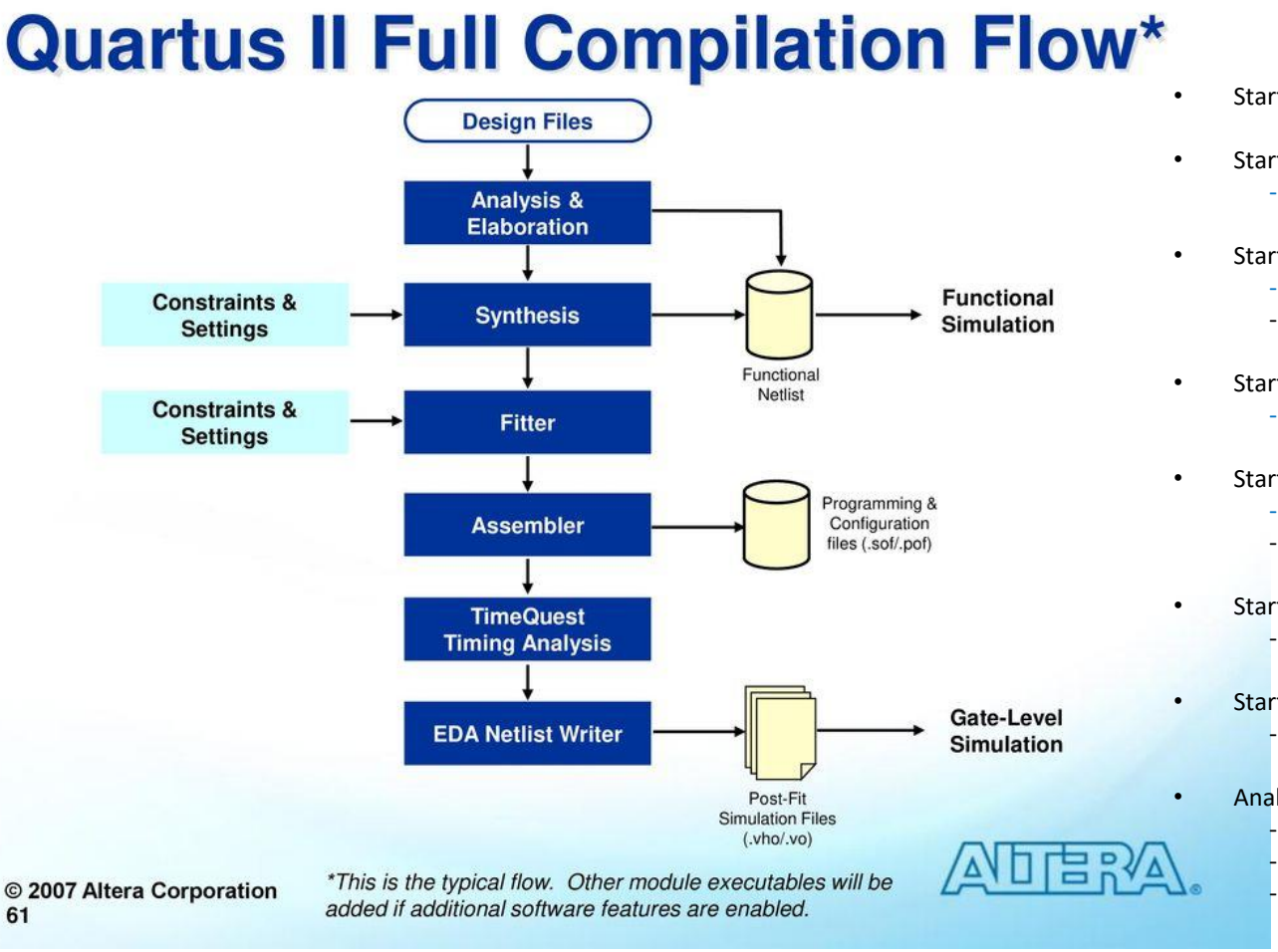
Quartus Prime

從電路圖查詢
設定完成後直接關閉

- Pin Planner (2/2)



補充



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  - Dump Gate-level netlist file for simulation
- Analyzers
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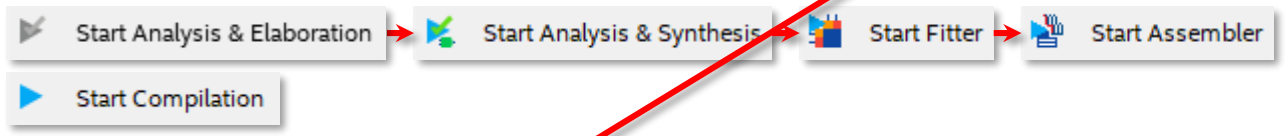
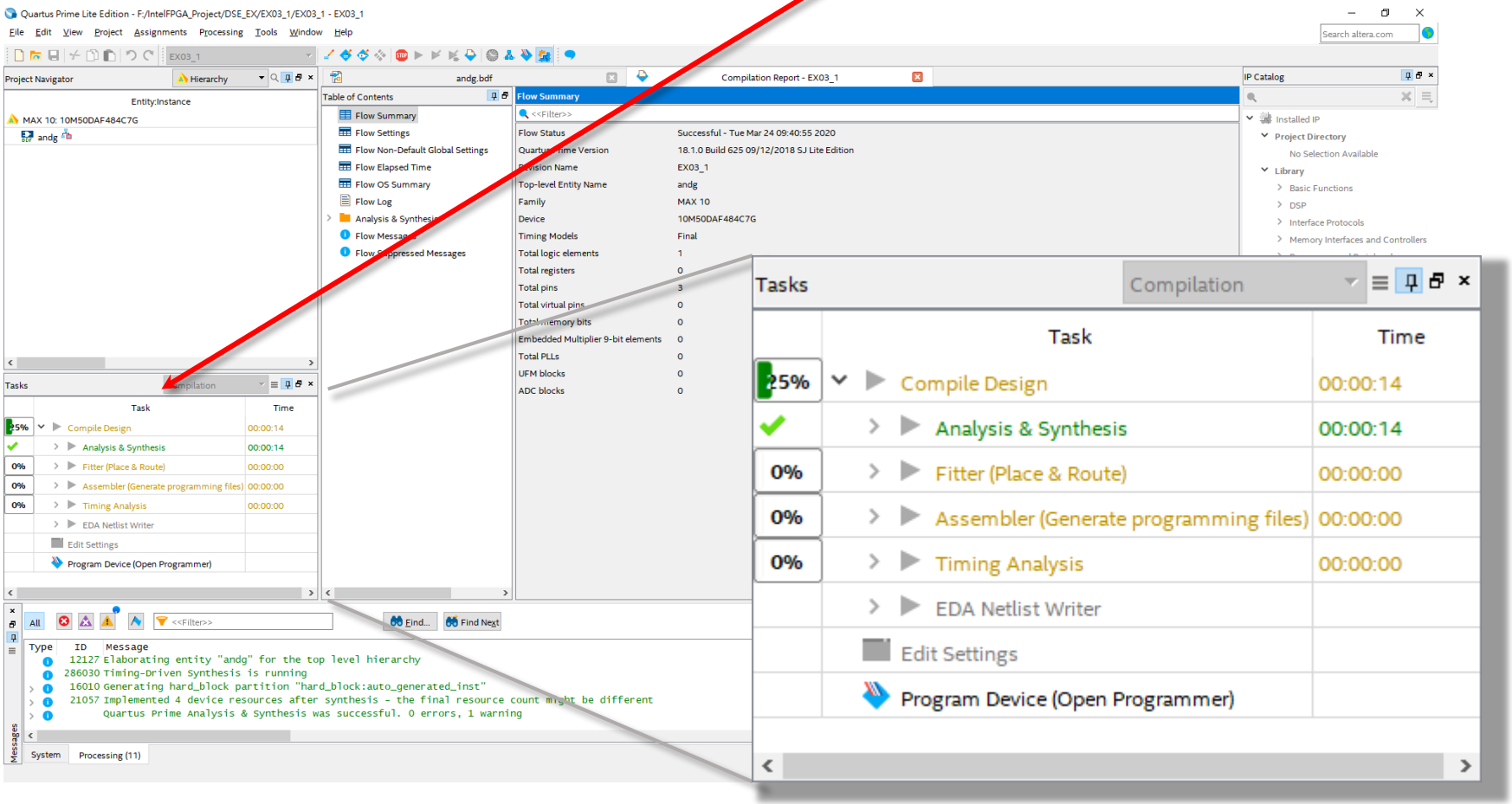
  - PowerPlay
  - Design Assistant

Quartus Prime

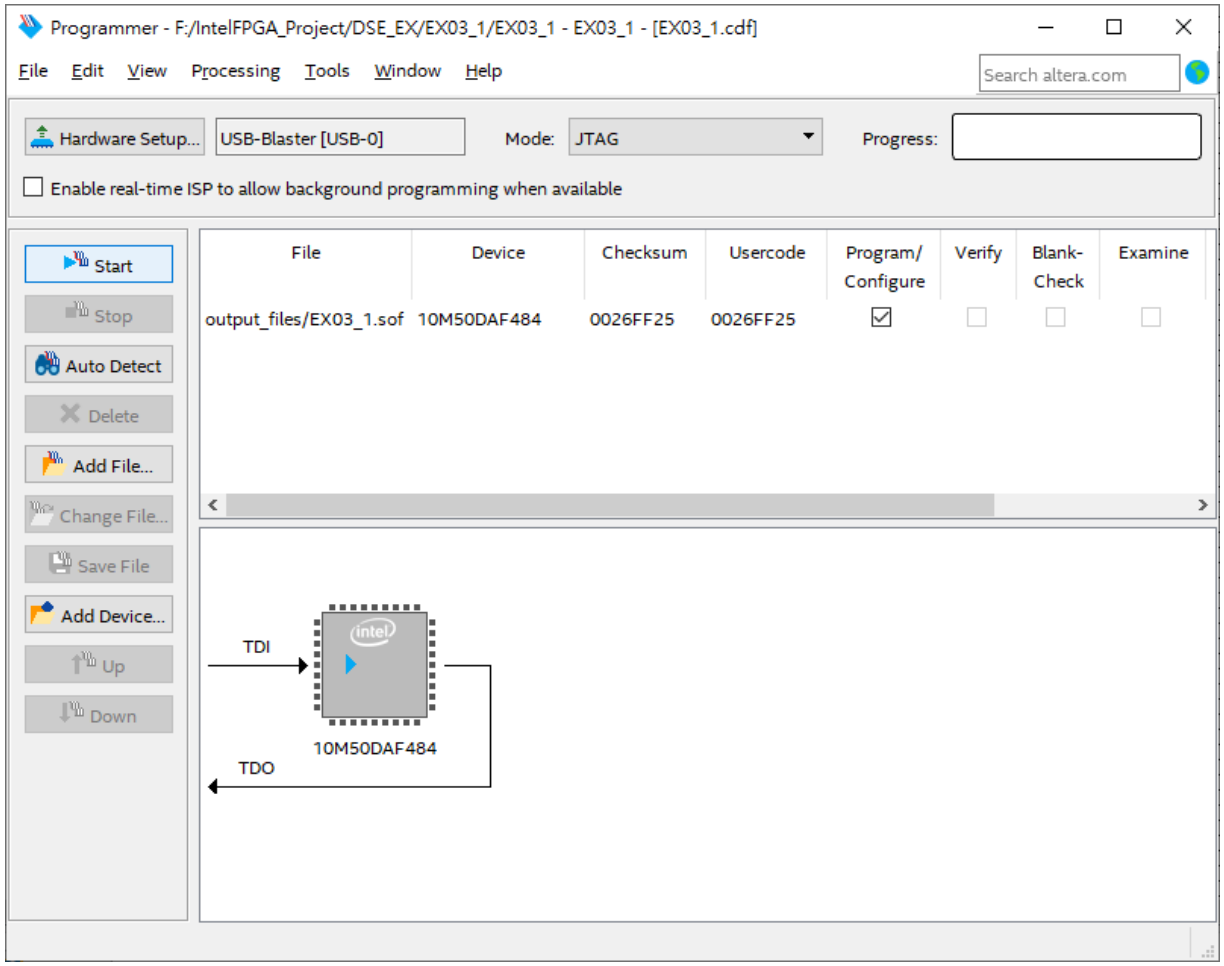
- Compile

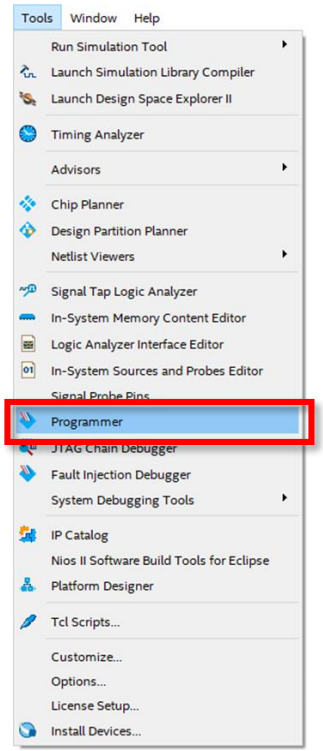




Quartus Prime

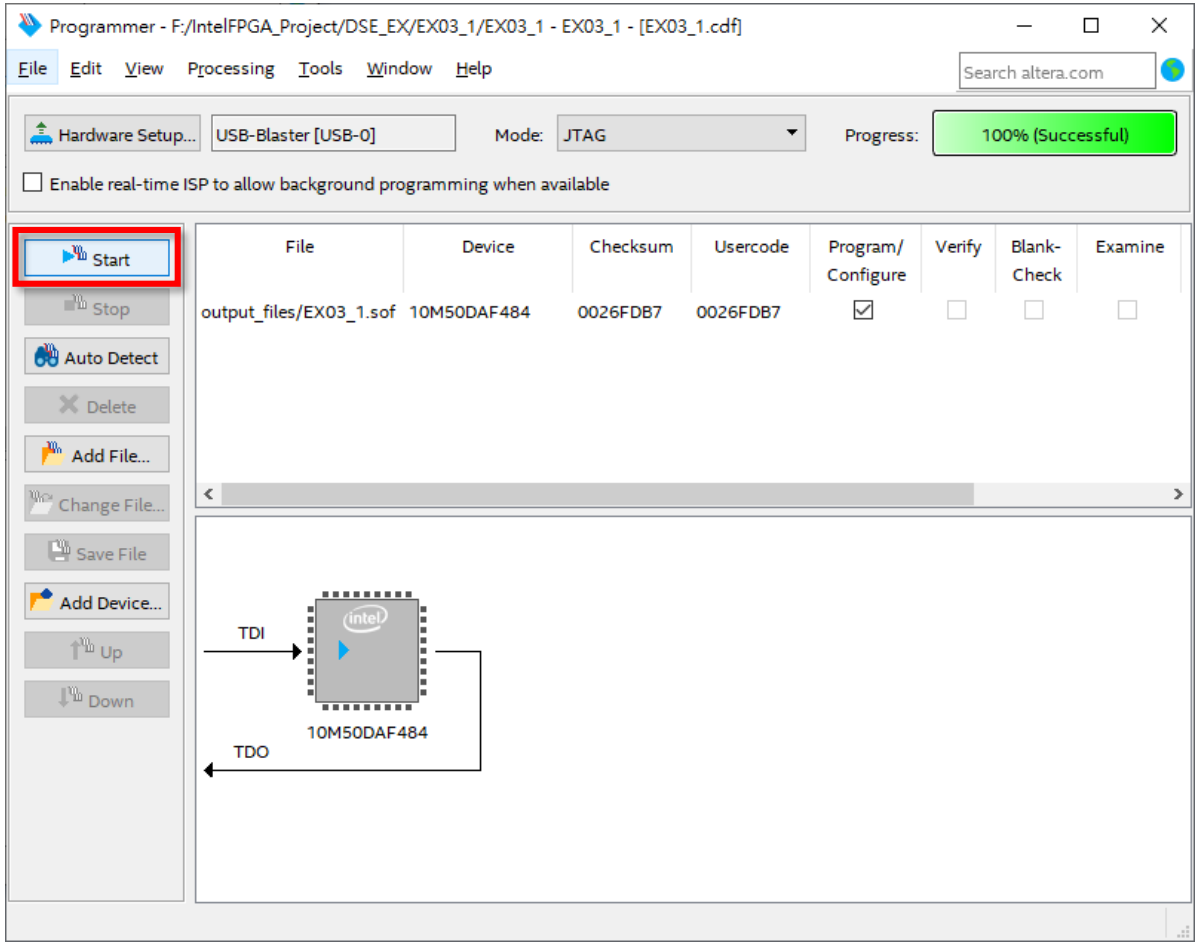
- Programming (1/2)





Quartus Prime

- Programming (2/2)



Quartus Prime

- 查看結果

實驗一 ：Quartus操作練習

- 參考講義流程，設計一數位邏輯電路，規格如下，
  - AND Gate : Input(SW0、SW1)，Output(LEDR0)
  - OR Gate : Input(SW2、SW3)，Output(LEDR2)
  - NOT Gate : Input(SW4)，Output(LEDR4)
  - XOR Gate : Input(SW5、SW6)，Output(LEDR5)
- 本次實驗需助教確認正確，並將專案壓縮上傳EE-Class。
- LectureX_組別XX.ZIP

- LE
- M9K Memory
- 18*18 Multiplier
- 4 PLLS