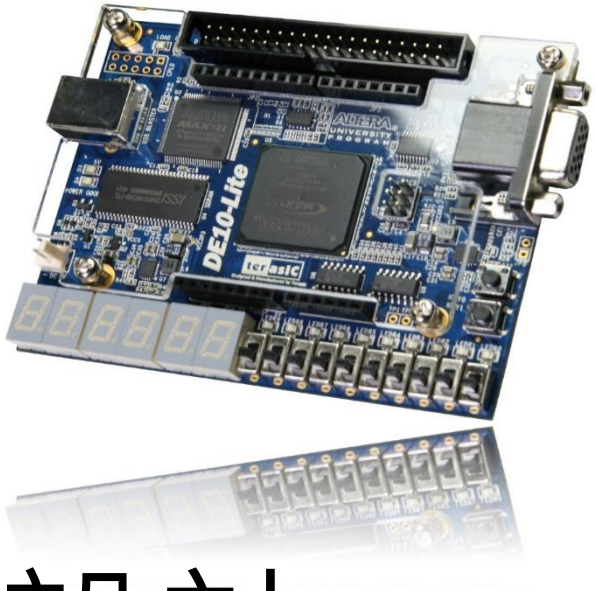


區塊圖形編輯設計

CSIE MIAT Lab.

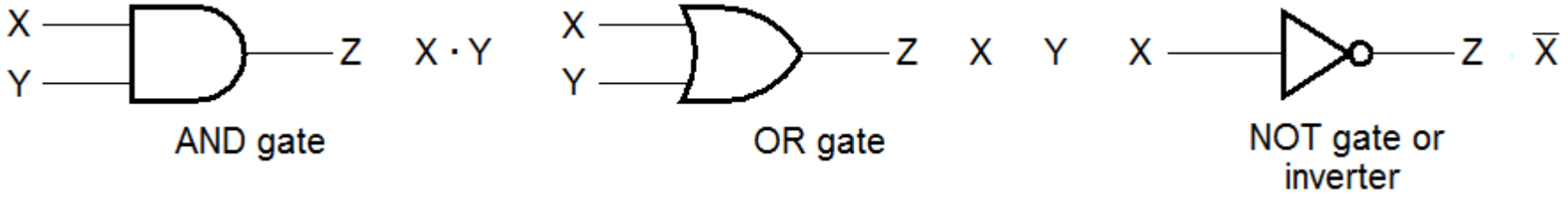
Outline

- 基本概念複習
- 區塊圖形編輯設計
- Quartus Prime補充
- 課堂練習

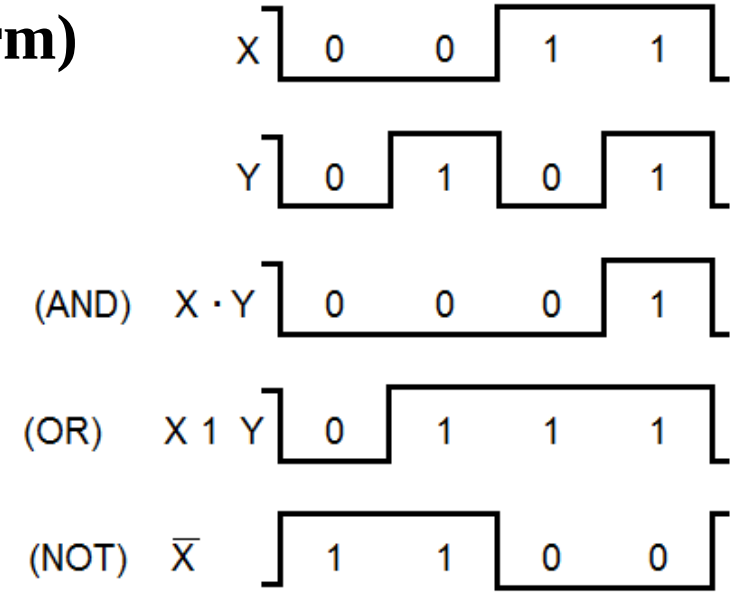
基本概念複習

Logic Gate Symbols and Behavior

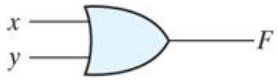
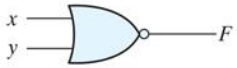
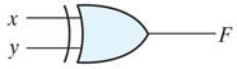
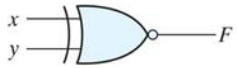
Logic gates symbols:



Timing diagram(waveform)



Logic Gates

Name	Graphic symbol	Algebraic function	Truth table
AND		$F = x \cdot y$	$x\ y \mid F$ $0\ 0 \mid 0$ $0\ 1 \mid 0$ $1\ 0 \mid 0$ $1\ 1 \mid 1$
OR		$F = x + y$	$x\ y \mid F$ $0\ 0 \mid 0$ $0\ 1 \mid 1$ $1\ 0 \mid 1$ $1\ 1 \mid 1$
Inverter		$F = x'$	$x \mid F$ $0 \mid 1$ $1 \mid 0$
Buffer		$F = x$	$x \mid F$ $0 \mid 0$ $1 \mid 1$
NAND		$F = (xy)'$	$x\ y \mid F$ $0\ 0 \mid 1$ $0\ 1 \mid 1$ $1\ 0 \mid 1$ $1\ 1 \mid 0$
NOR		$F = (x + y)'$	$x\ y \mid F$ $0\ 0 \mid 1$ $0\ 1 \mid 0$ $1\ 0 \mid 0$ $1\ 1 \mid 0$
Exclusive-OR (XOR)		$F = xy' + x'y$ $= x \oplus y$	$x\ y \mid F$ $0\ 0 \mid 0$ $0\ 1 \mid 1$ $1\ 0 \mid 1$ $1\ 1 \mid 0$
Exclusive-NOR or equivalence		$F = xy + x'y'$ $= (x \oplus y)'$	$x\ y \mid F$ $0\ 0 \mid 1$ $0\ 1 \mid 0$ $1\ 0 \mid 0$ $1\ 1 \mid 1$

Expressions of Logic Function

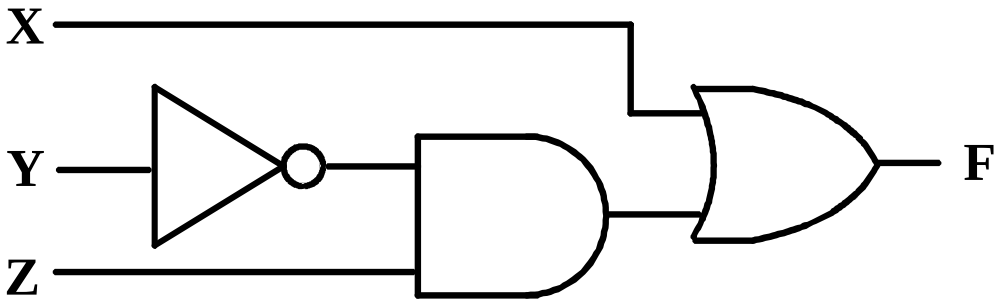
Truth Table

X Y Z	F = X + $\overline{Y}$ ×Z
0 0 0	0
0 0 1	1
0 1 0	0
0 1 1	0
1 0 0	1
1 0 1	1
1 1 0	1
1 1 1	1

Equation

$$F = X + \overline{Y}\,Z$$

Logic Diagram



- **Boolean equations, truth tables and logic diagrams describe the same function!**
- **Truth tables are unique; expressions and logic diagrams are not.**

Boolean Algebra

- **An algebraic structure defined on a set of at least two elements, B, together with three binary operators (denoted +, · and) that satisfies the following basic identities:**

1.	$X + 0 = X$	2.	$X \cdot 1 = X$
3.	$X + 1 = 1$	4.	$X \cdot 0 = 0$
5.	$X + X = X$	6.	$X \cdot X = X$
7.	$X + \overline{X} = 1$	8.	$X \cdot \overline{X} = 0$
9.	$\overline{\overline{X}} = X$		

10.	$X + Y = Y + X$	11.	$XY = YX$ Commutative
12.	$(X + Y) + Z = X + (Y + Z)$	13.	$(XY)Z = X(YZ)$ Associative
14.	$X(Y + Z) = XY + XZ$	15.	$X + YZ = (X + Y)(X + Z)$ Distributive
16.	$\overline{X + Y} = \overline{X} \cdot \overline{Y}$	17.	$\overline{X \cdot Y} = \overline{X} + \overline{Y}$ DeMorgan's

Boolean Operator Precedence

- **The order of evaluation in a Boolean expression is:**
  1. Parentheses
  2. NOT
  3. AND
  4. OR
- **Consequence: Parentheses appear around OR expressions**
- **Example:** $F = A(B + C)(C + \overline{D})$

- $F = A(B + C)(C + \overline{D})$
- $F = (AB + AC)(AC + A\overline{D})$
- $F = ABC + AB\overline{D} + AC + AC\overline{D}$

- $F = ABC + AB\overline{D} + AC(1 + \overline{D})$

- $F = ABC + AB\overline{D} + AC \rightarrow AC + ABC + AB\overline{D}$
- $F = AC(1 + B) + AB\overline{D}$
- $F = AC + AB\overline{D}$

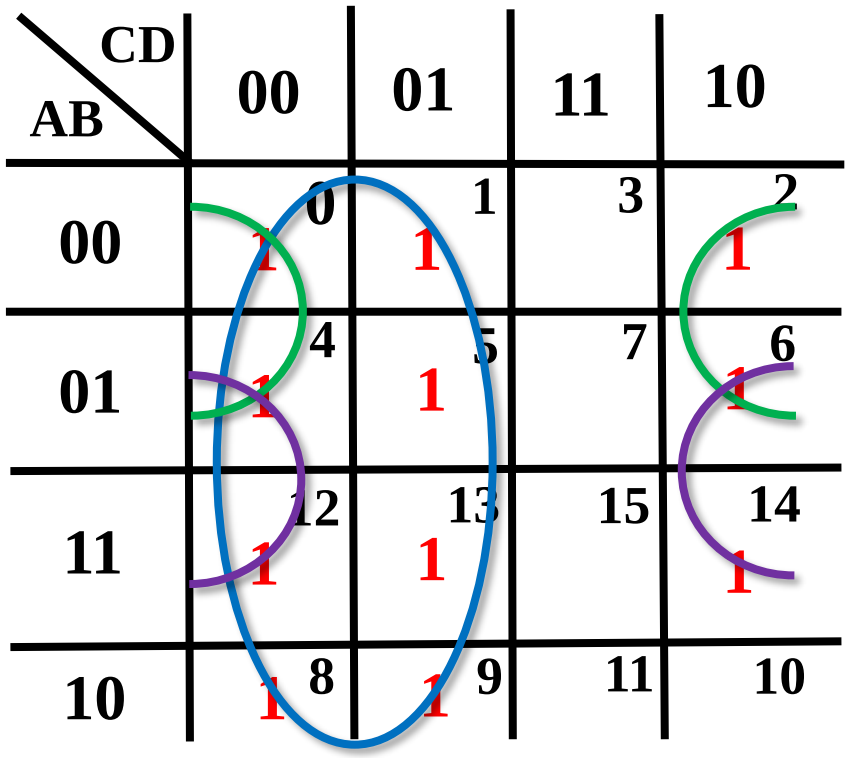
- $F = ABC + AB\overline{D} + AC + AC\overline{D}$

1

AB \ CD	00	01	11	10
00	0	1	3	2
01	4	5	7	6
11	12	13	15	14
10	8	9	11	10

K-Map

A	B	C	D	X
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0



F(w, x, y, z) = **C’**+**A’D’**+**BD’**

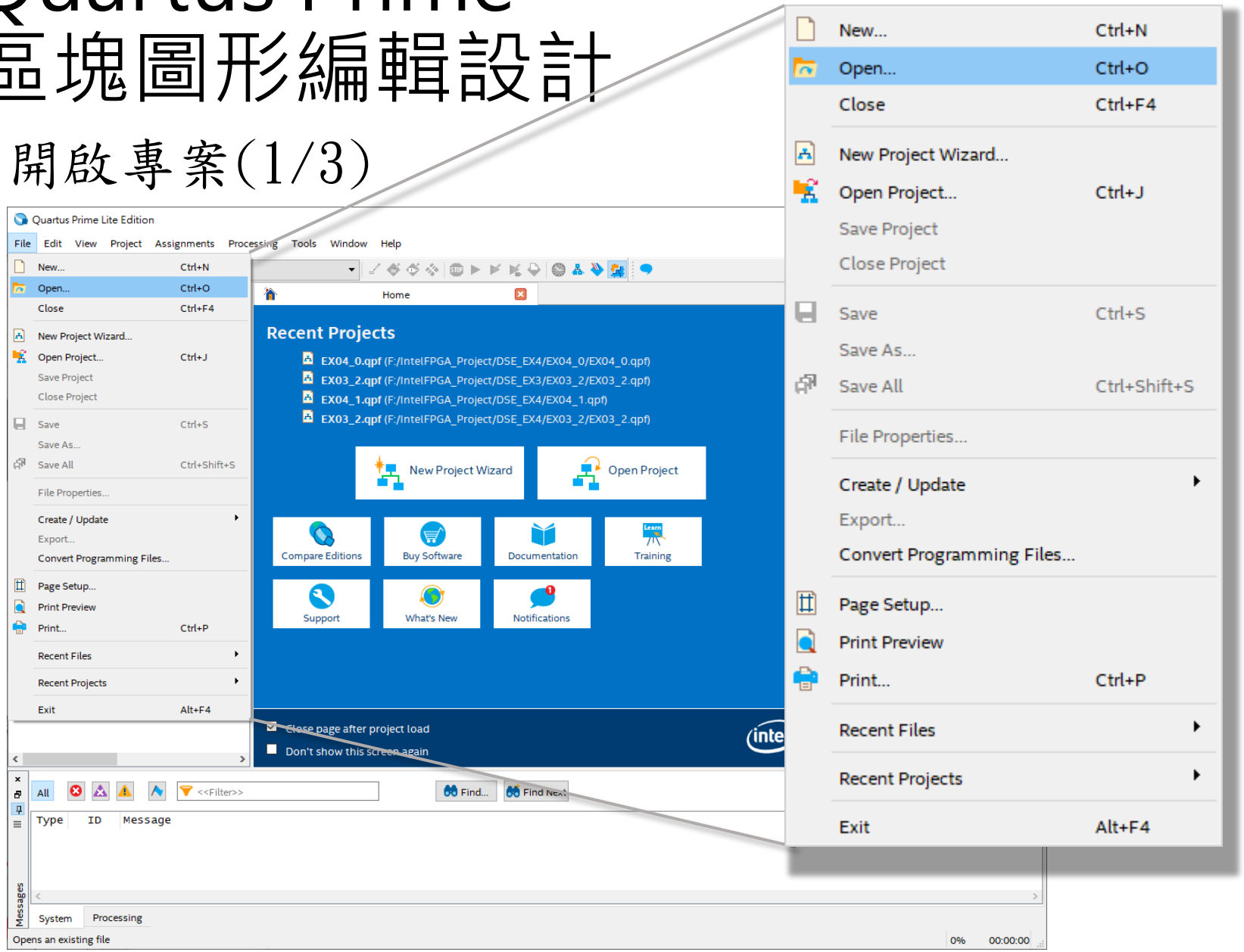
F(A, B, C, D) = ∑(0,1,2,4,5,6,8,9,12,13,14)

F(A, B, C, D) = A’B’C’D’+A’B’C’D+A’B’CD’+A’BC’D’+A’BC’D+A’BCD’+AB’C’D’+AB’C’D+ABC’D’+ABC’D+ABCD’

區塊圖形編輯設計

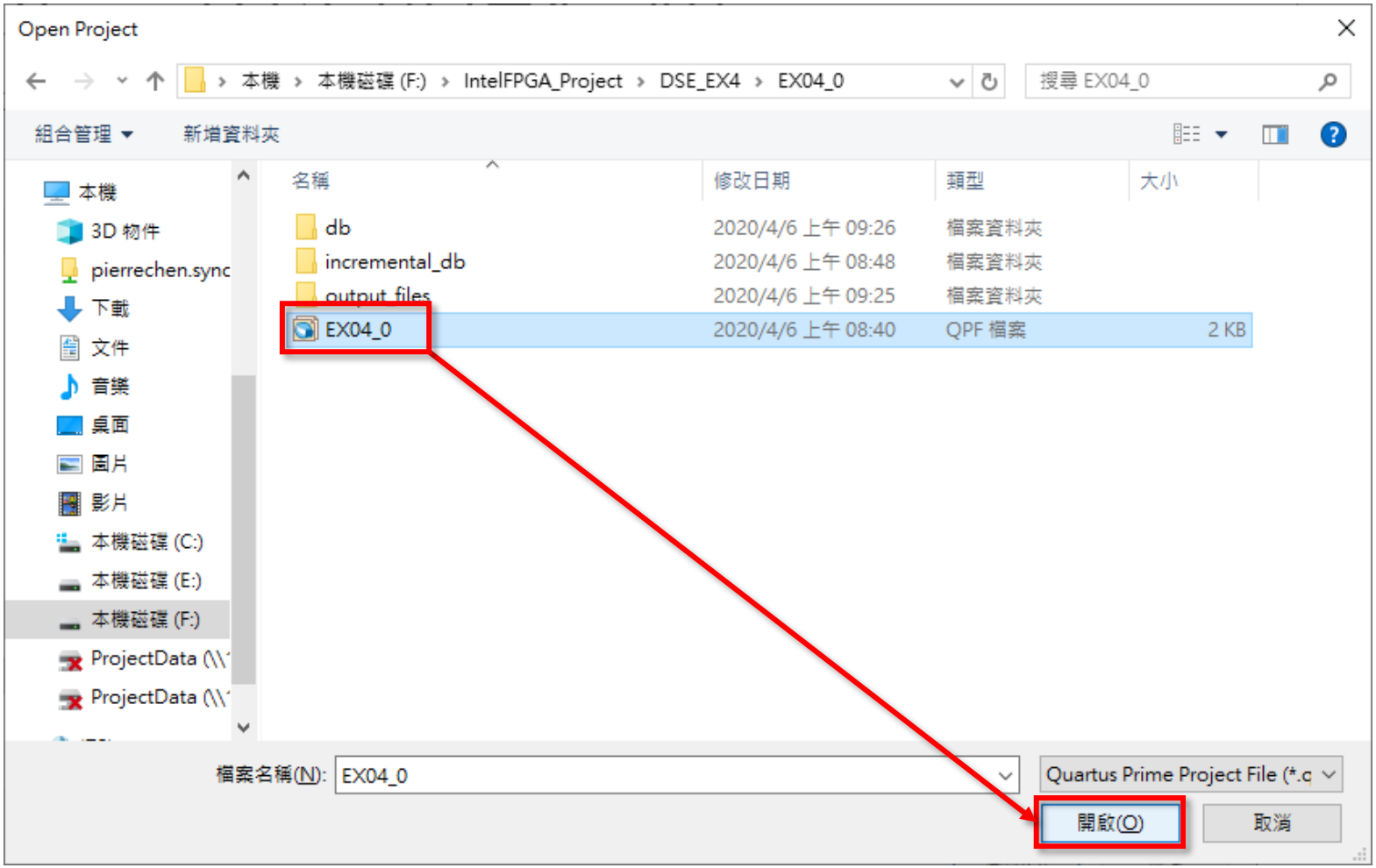
Quartus Prime
區塊圖形編輯設計

- 開啟專案(1/3)



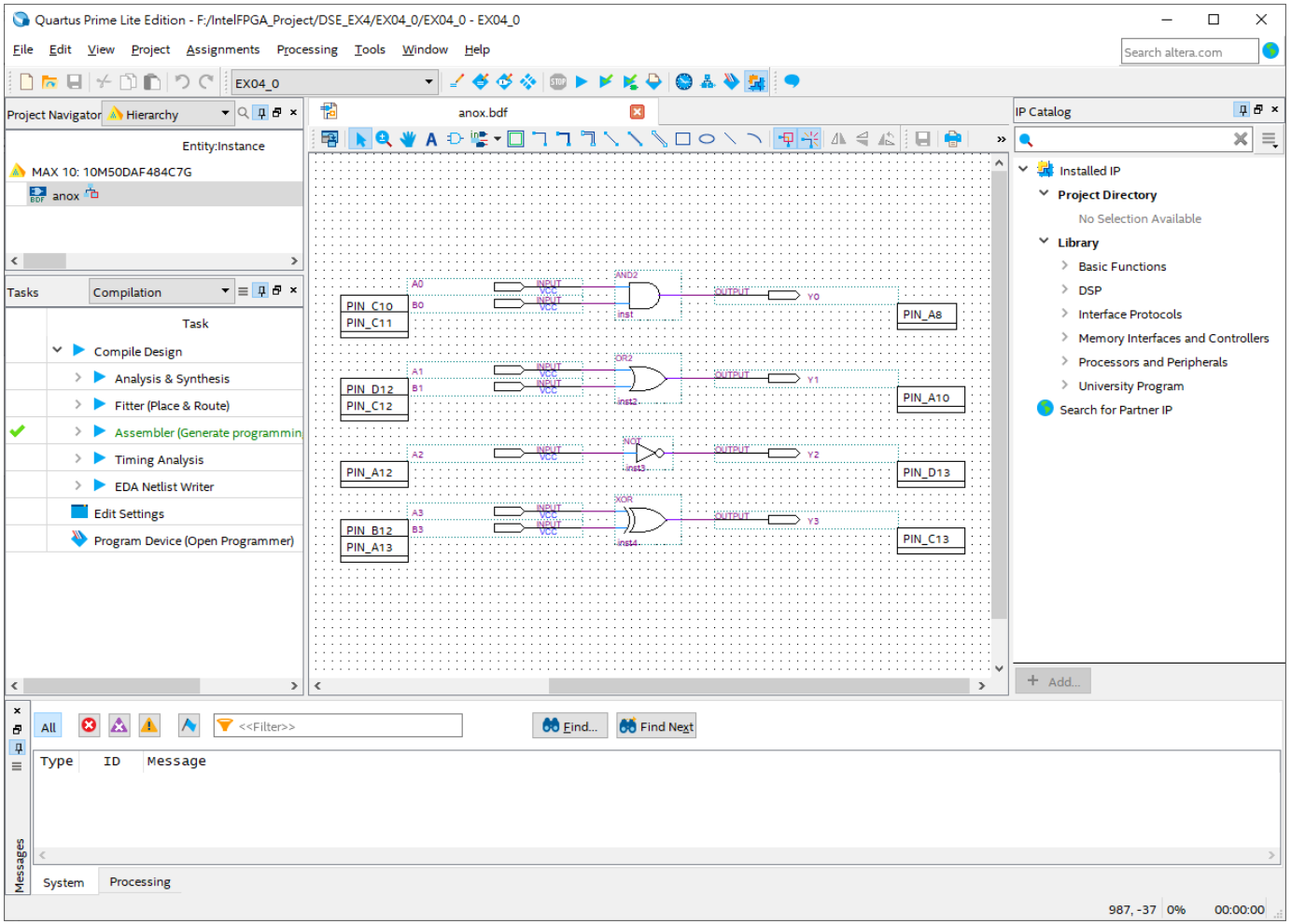
Quartus Prime
區塊圖形編輯設計

- 開啟專案(2/3)



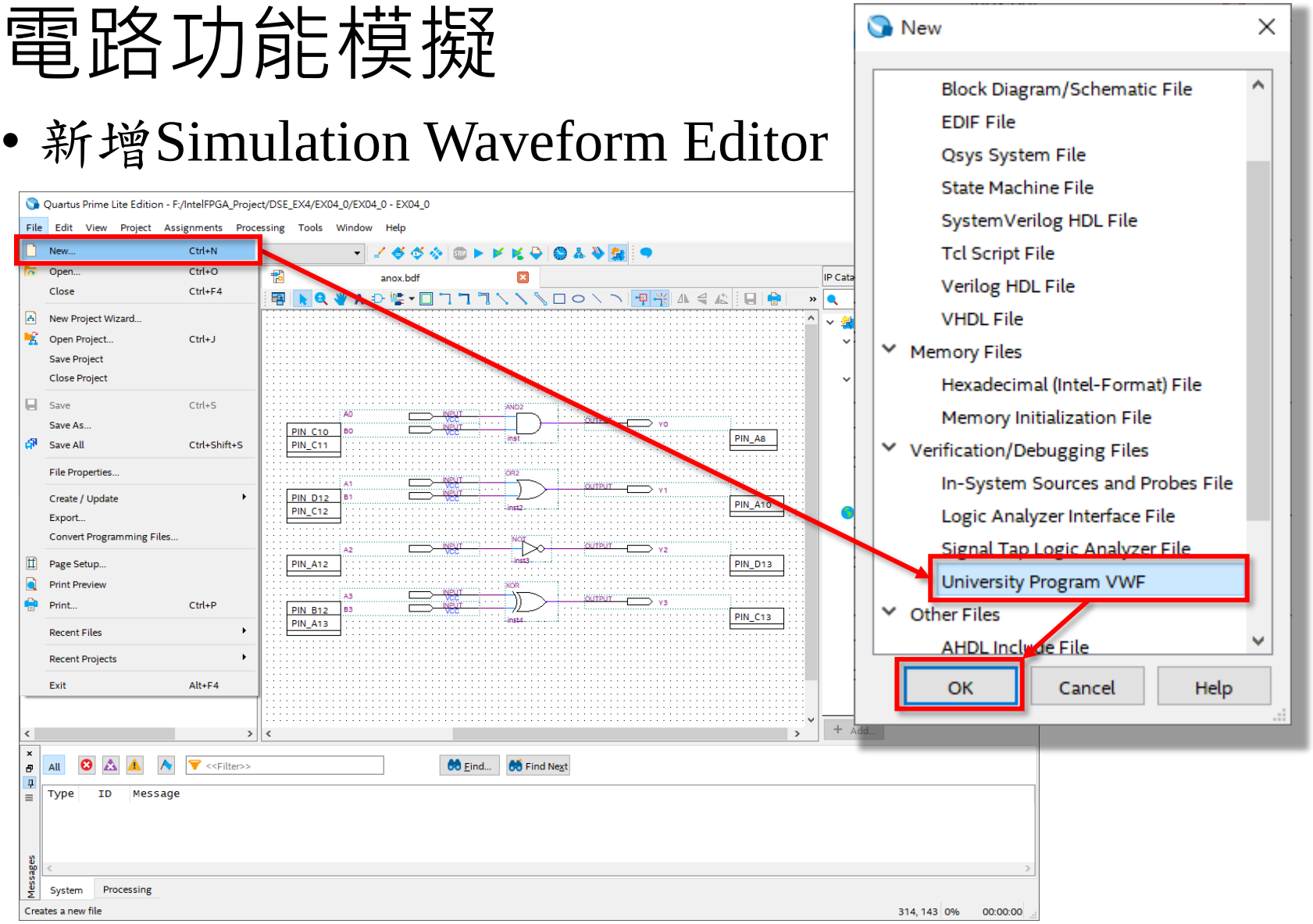
Quartus Prime
區塊圖形編輯設計

- 開啟專案(3/3)



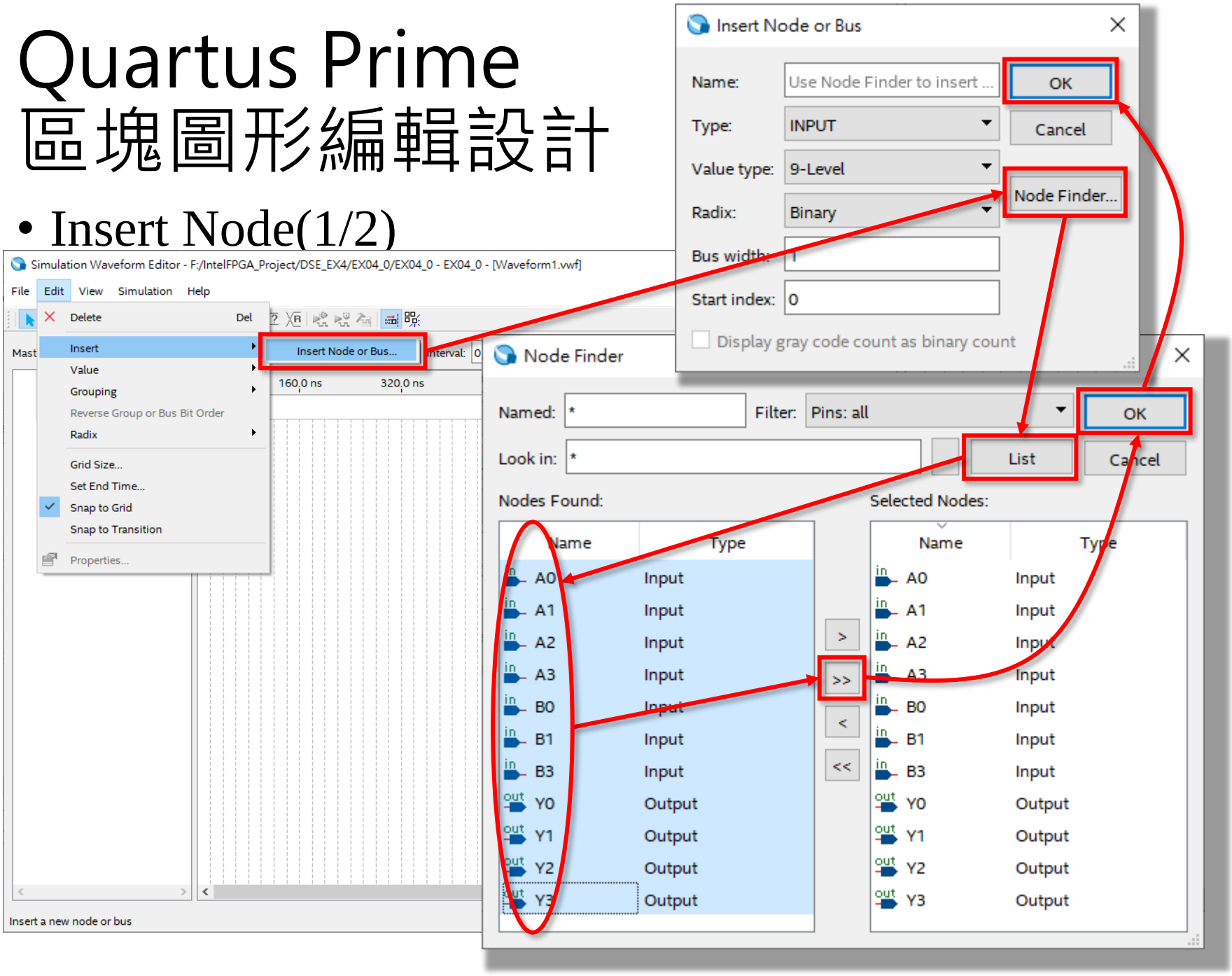
Quartus Prime
電路功能模擬

- 新增Simulation Waveform Editor



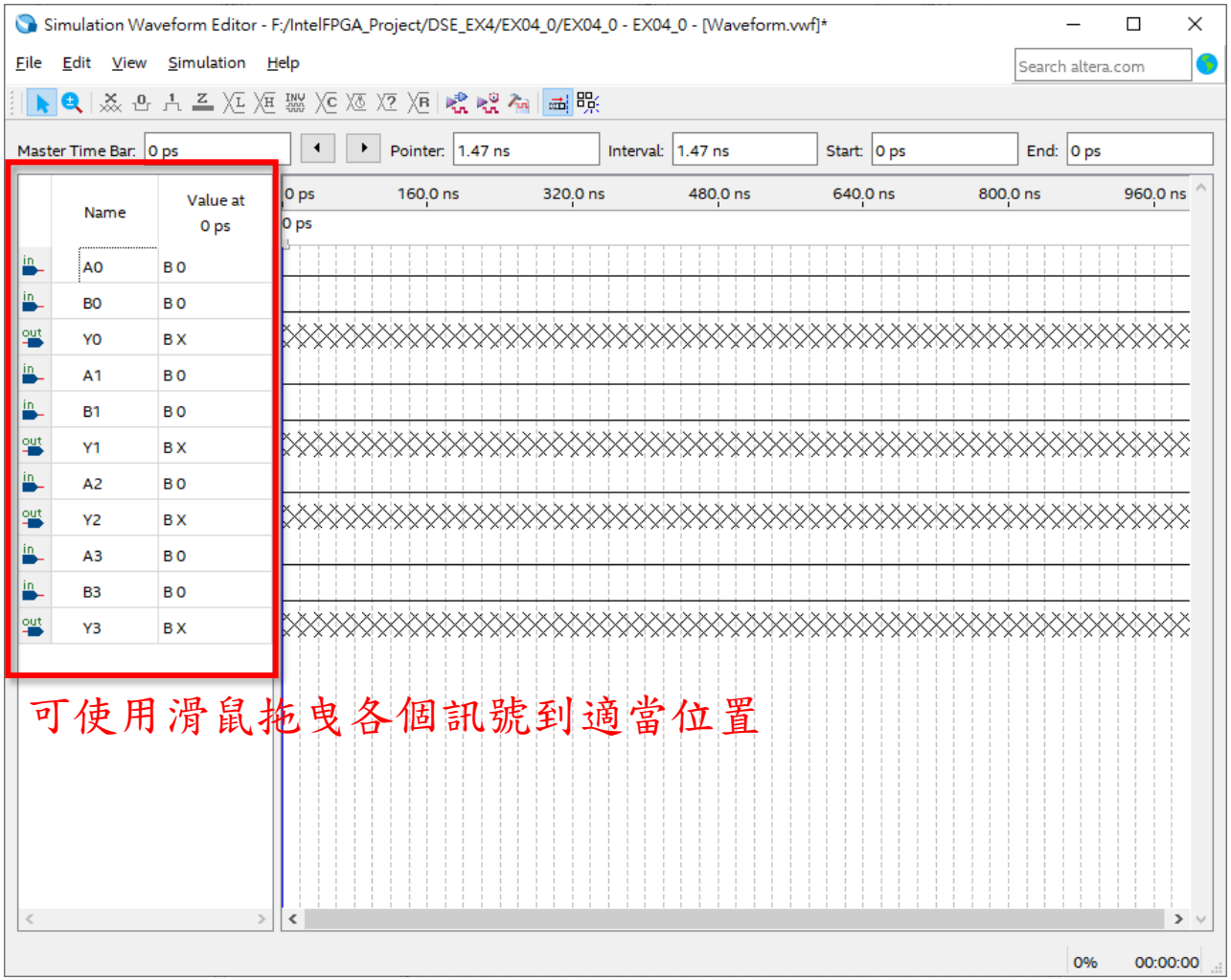
Quartus Prime
區塊圖形編輯設計

- Insert Node(1/2)



Quartus Prime
區塊圖形編輯設計

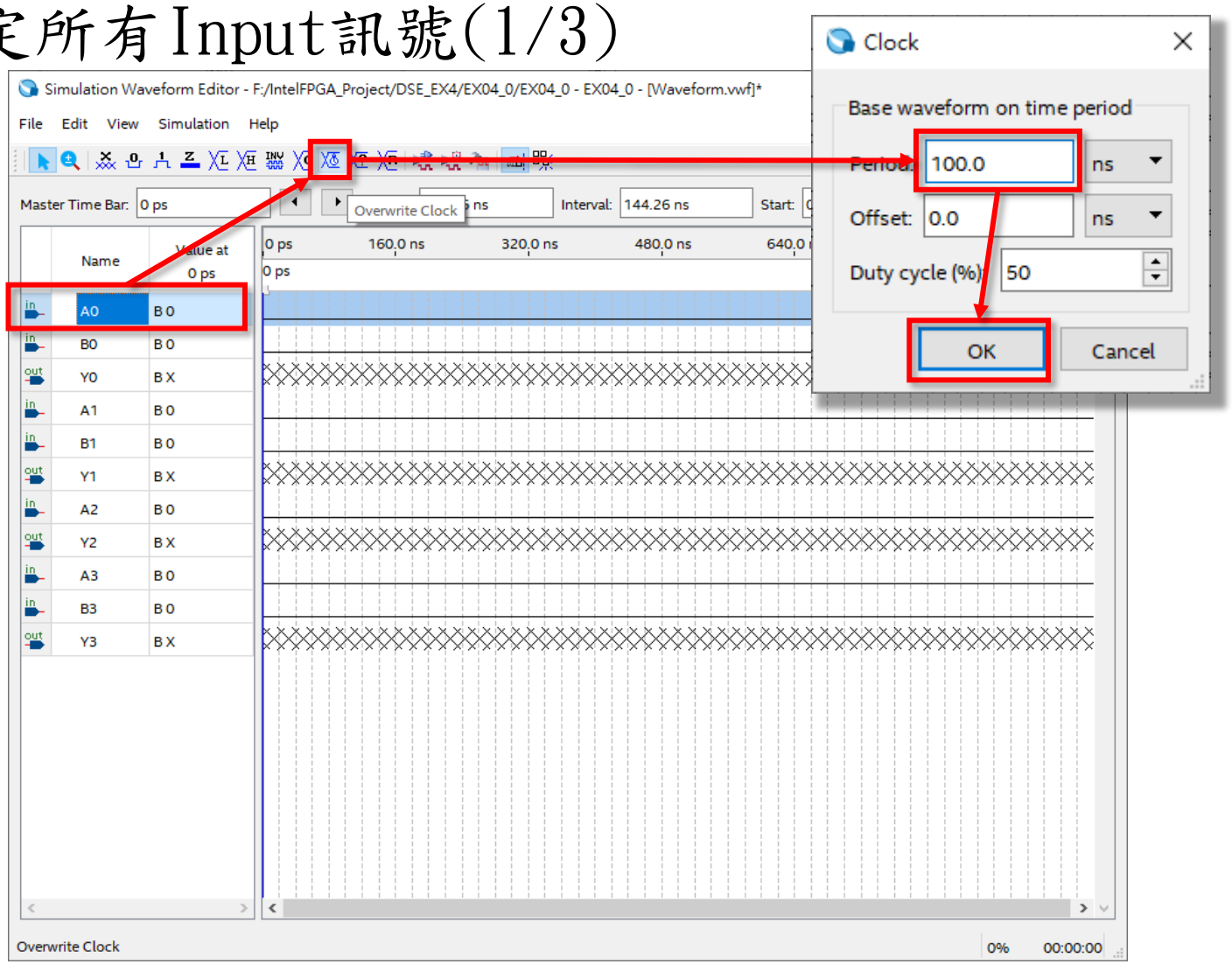
- Insert Node(2/2)



Quartus Prime
區塊圖形編輯設計

Name	Graphic symbol	Algebraic function	Truth table
AND	x, y → F	$F = x \cdot y$	x y | F: 0 0 | 0; 0 1 | 0; 1 0 | 0; 1 1 | 1

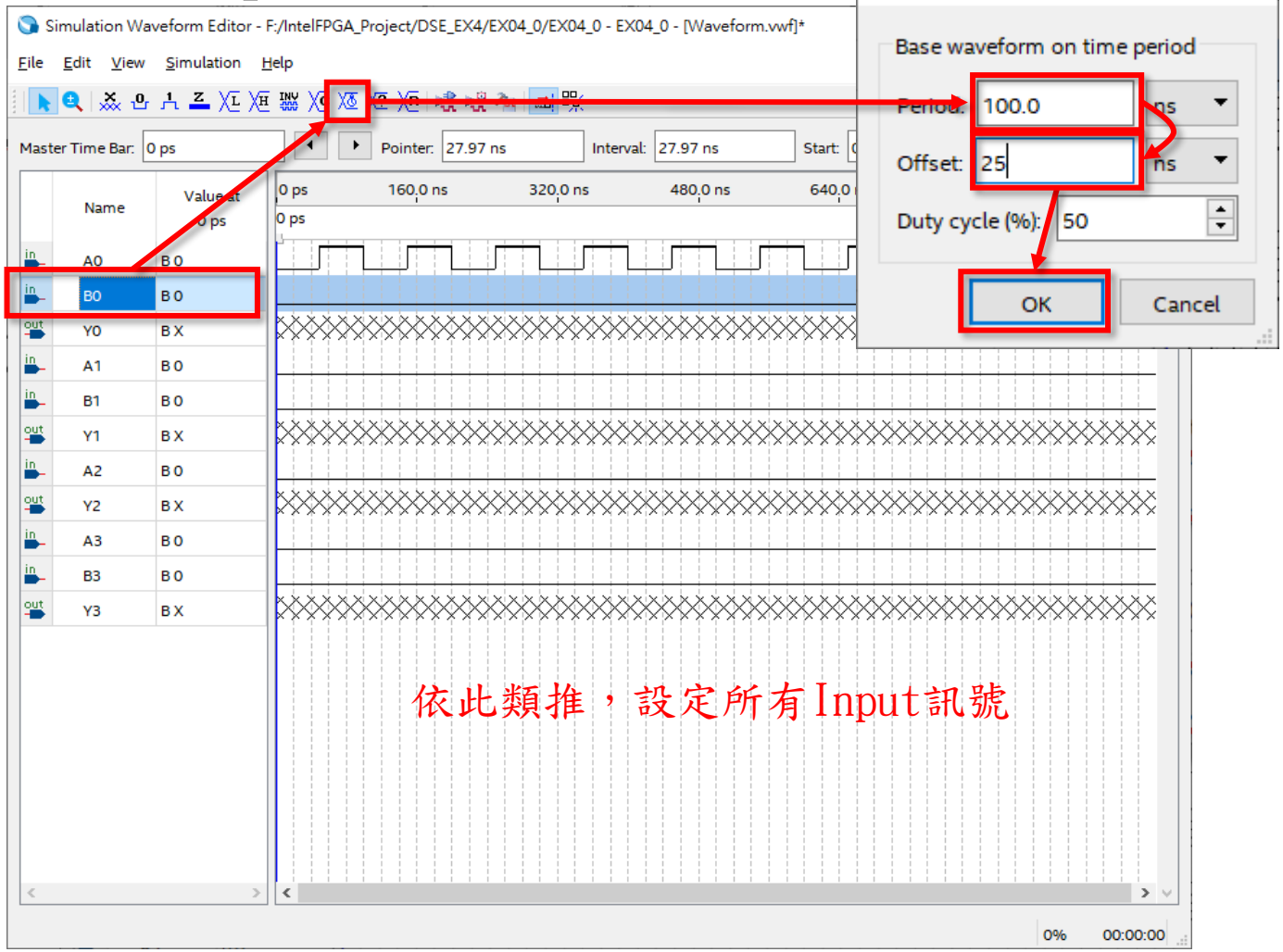
- 設定所有Input訊號(1/3)



Quartus Prime
區塊圖形編輯設計

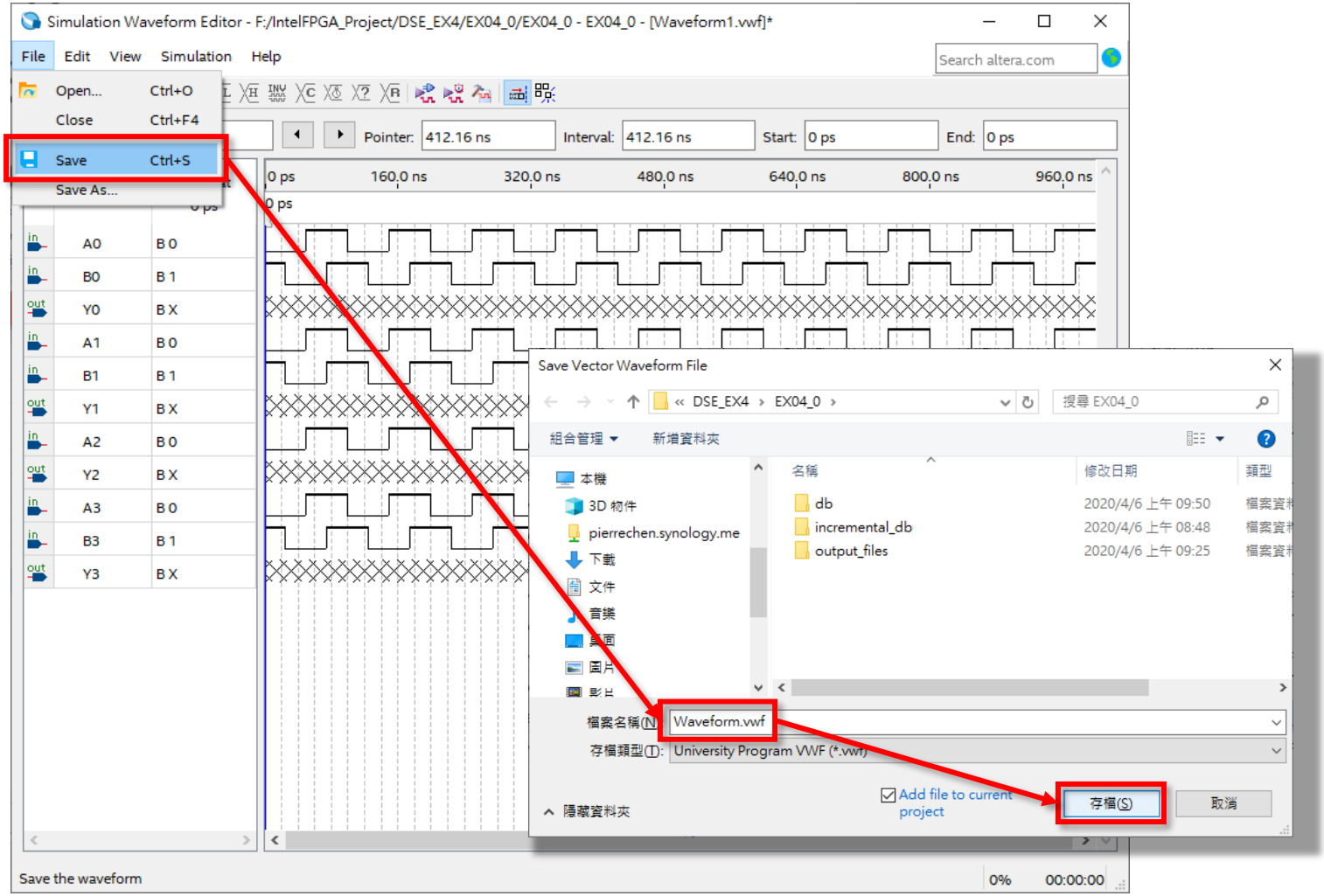
Name	Graphic symbol	Algebraic function	Truth table
AND		$F = x \cdot y$	x y | F 0 0 | 0 0 1 | 0 1 0 | 0 1 1 | 1

- 設定所有Input訊號(1/3)



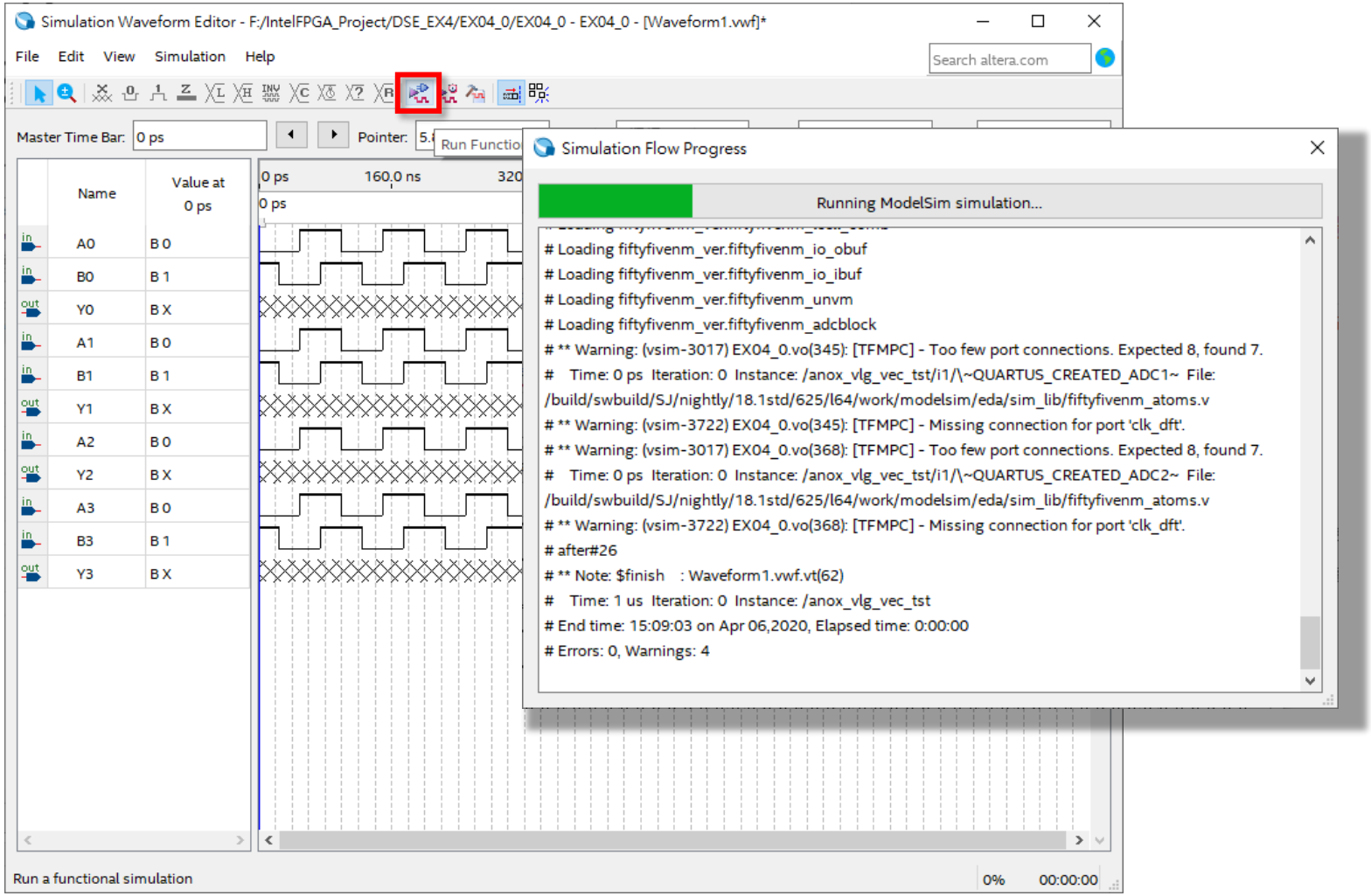
Quartus Prime
區塊圖形編輯設計

- 設定所有Input訊號(3/3)



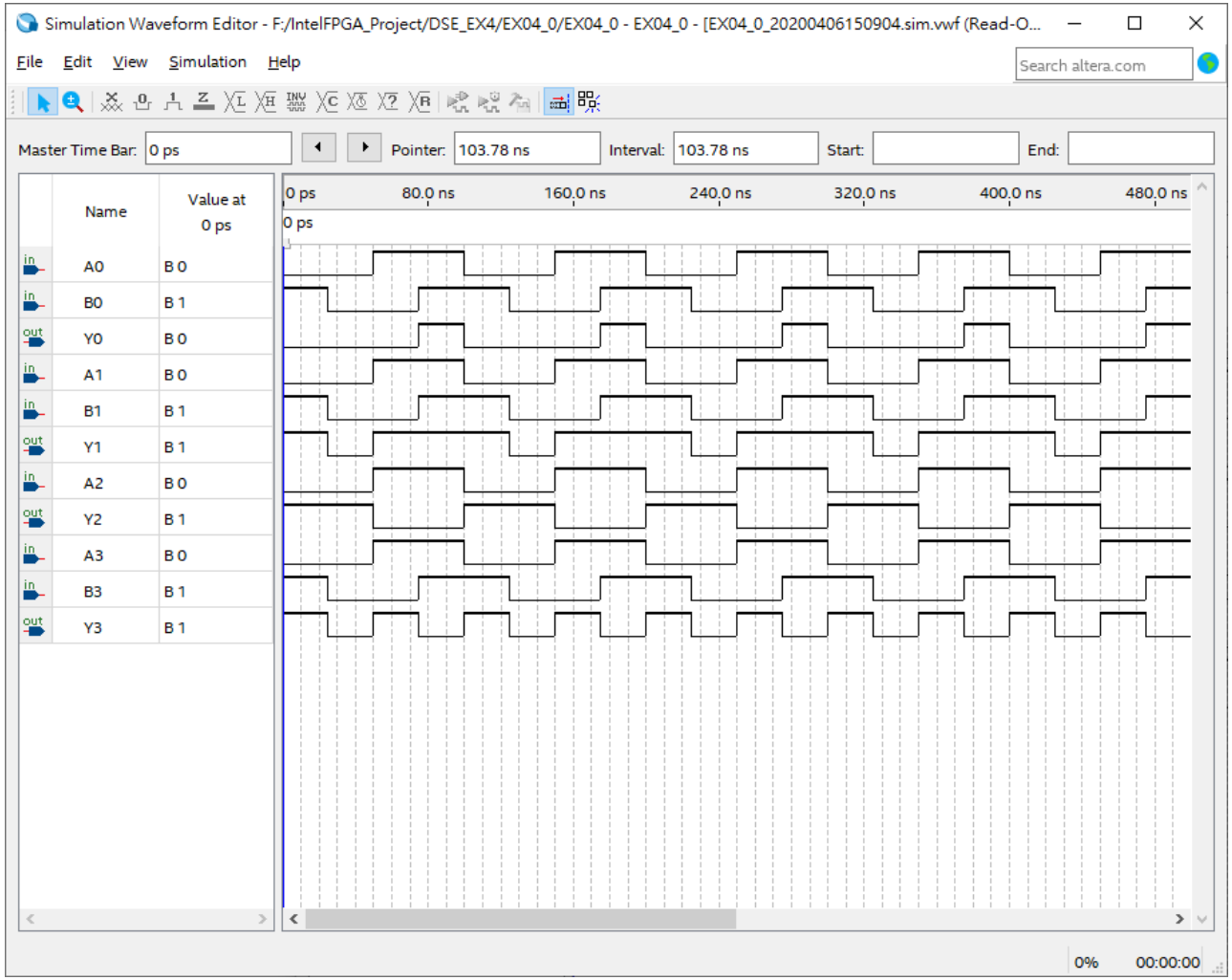
Quartus Prime
區塊圖形編輯設計

- 開始模擬



Quartus Prime
區塊圖形編輯設計

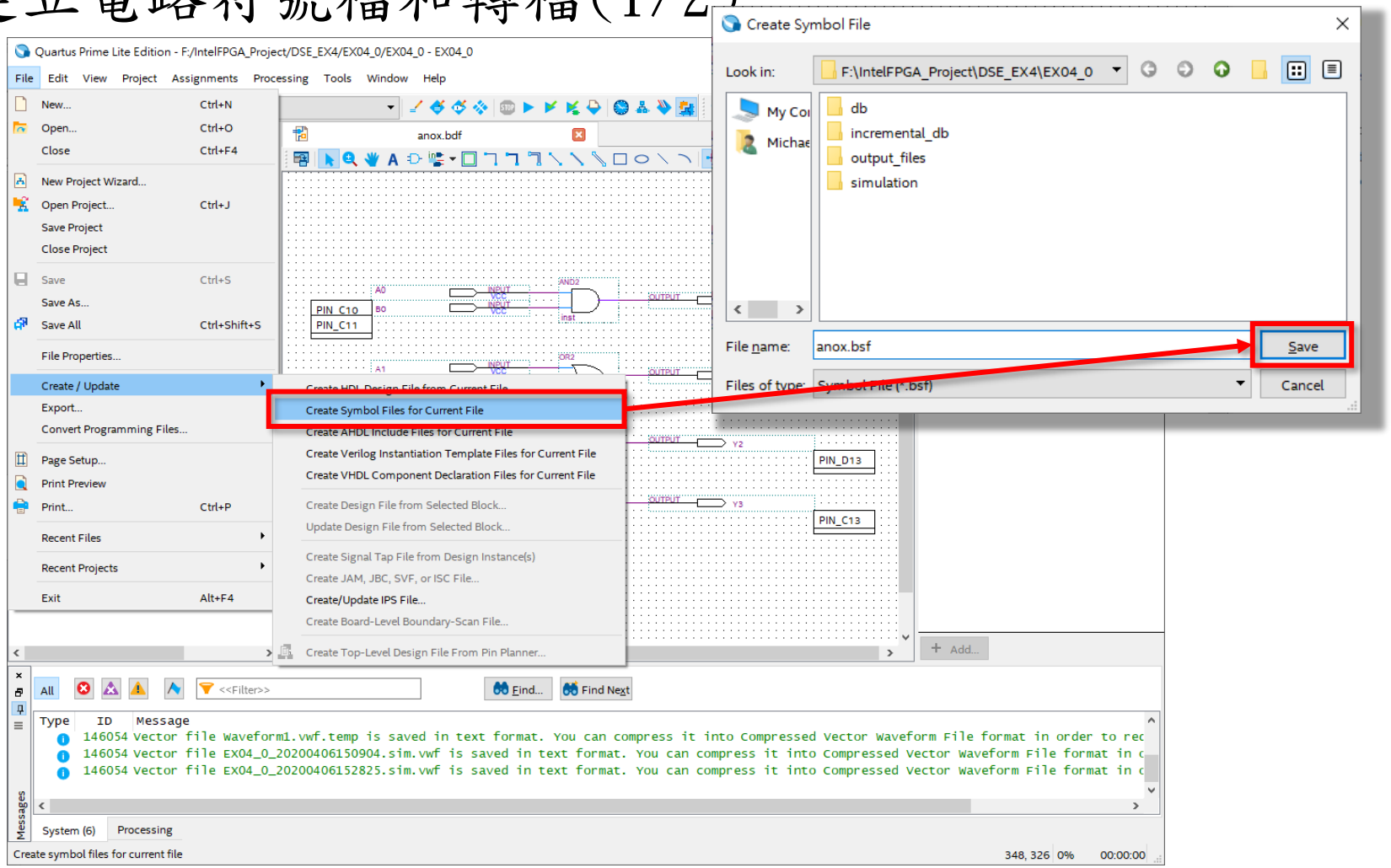
- 模擬結果



Quartus Prime 補充

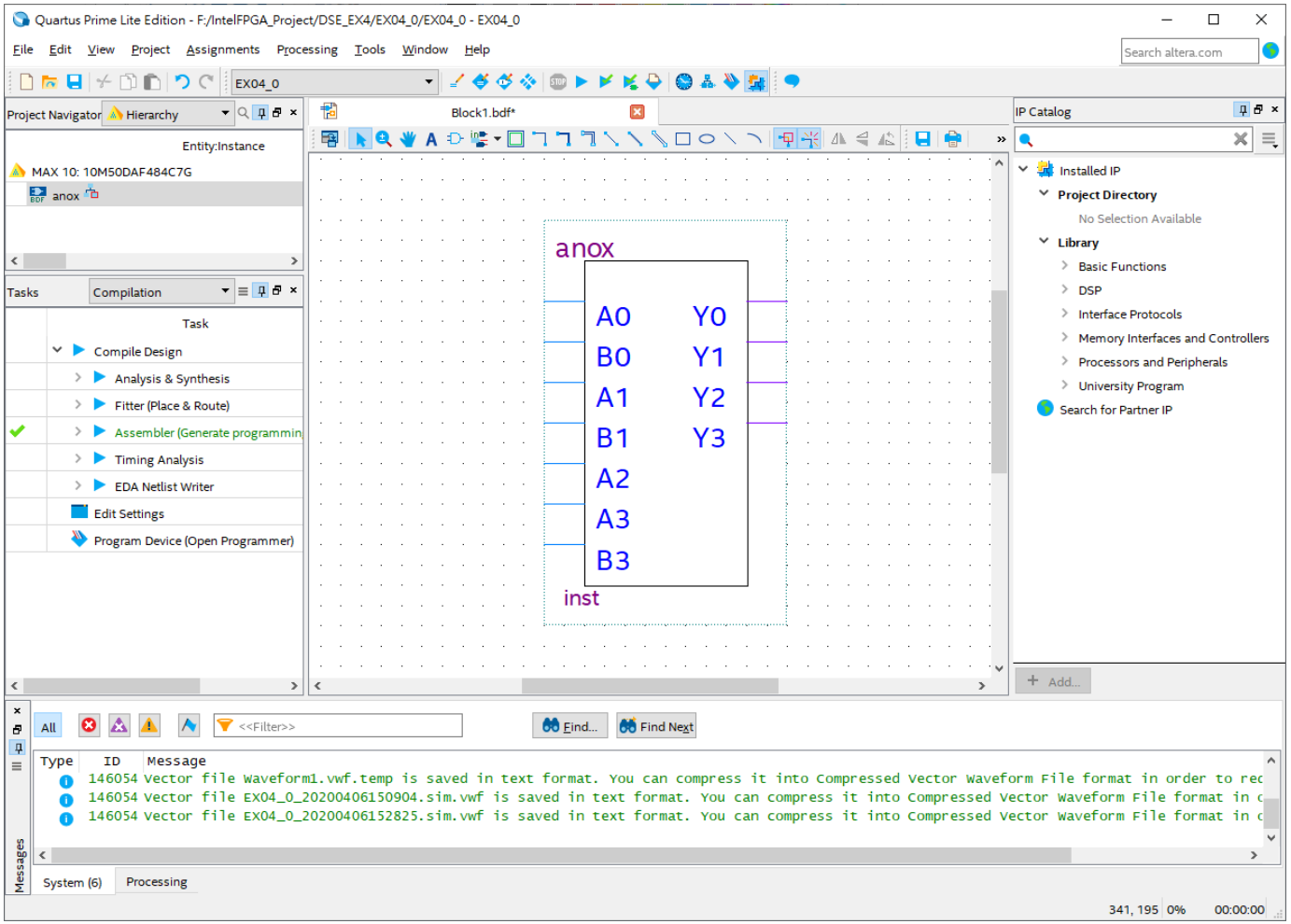
Quartus Prime 補充(一)

- 建立電路符號檔和轉檔(1/2)



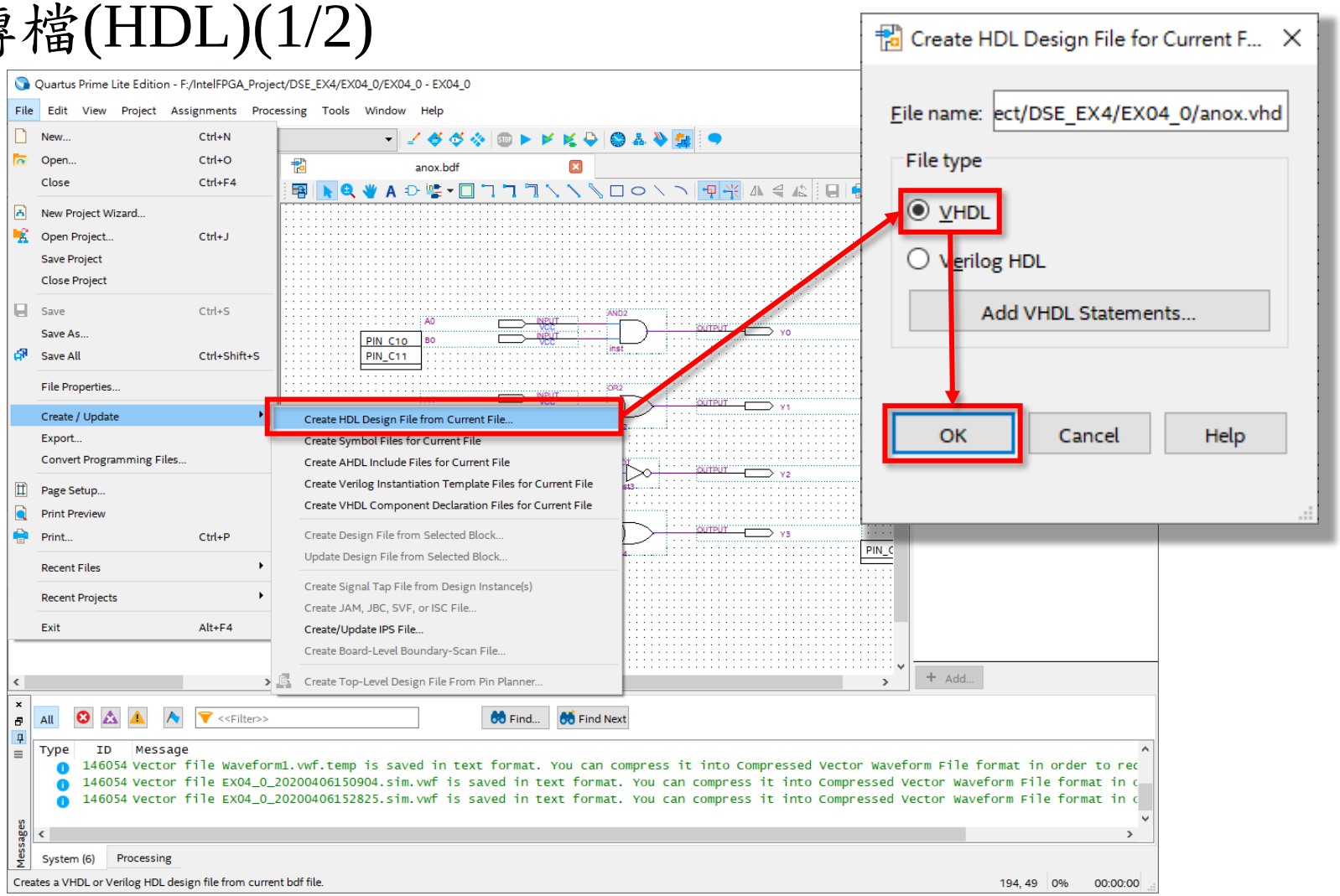
Quartus Prime 補充(一)

- 建立電路符號檔和轉檔(2/2)



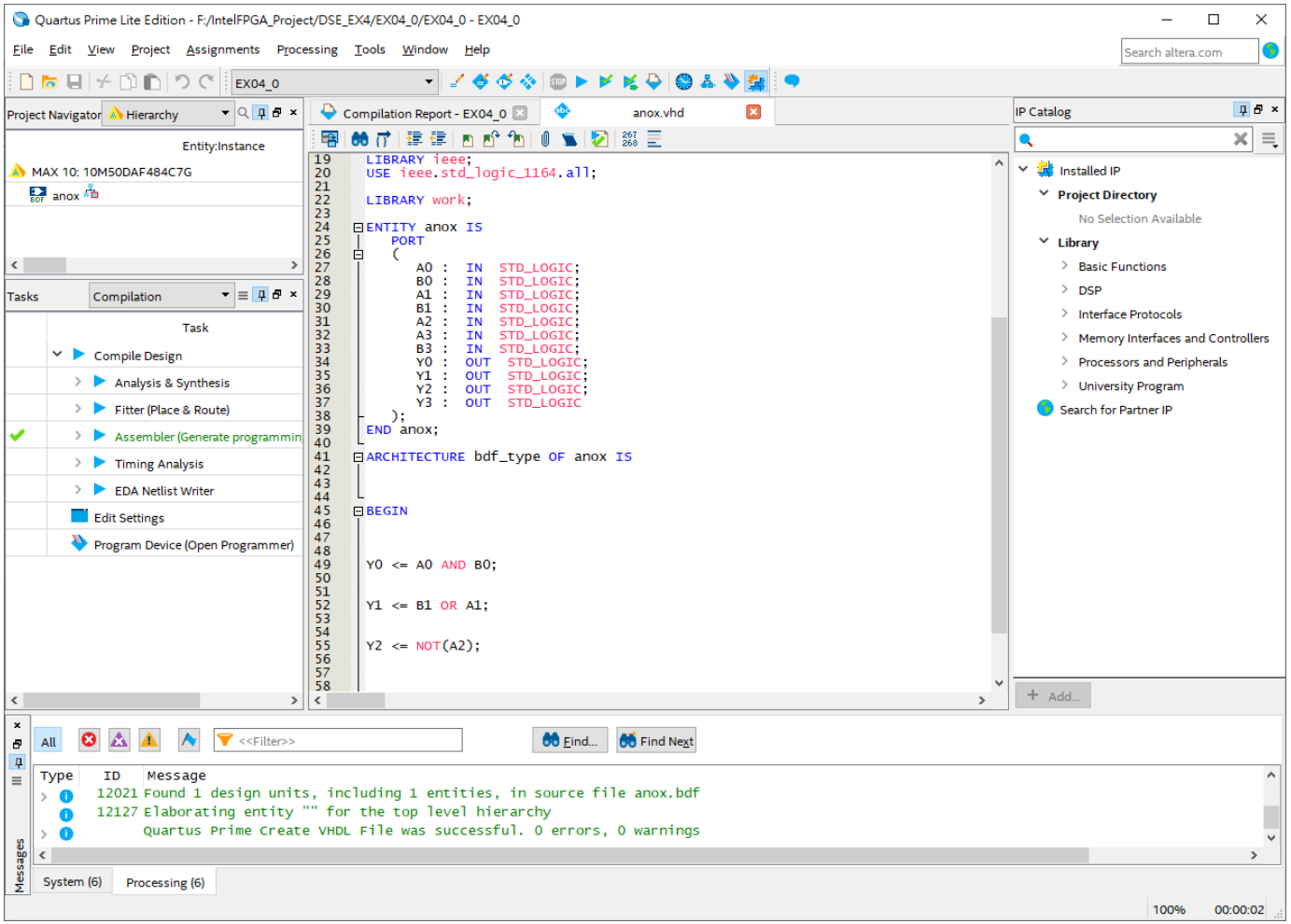
Quartus Prime 補充(二)

- 轉檔(HDL)(1/2)



Quartus Prime 補充(二)

- 轉檔(HDL)(2/2)



課堂練習

實驗一 ：Quartus操作練習

- 請完成下列邏輯表示式之:
  - a） 真值表
  - b） 最簡SOP
  - c） 電路設計並下載至DE10-Lite
  - d） 模擬波形圖

$Y(A, B, C, D) = \sum(0, 1, 4, 5, 6, 8, 9, 10, 12, 13, 14)$

- Pin Definition : A(C12)、B(D12)、 C(C11) 、 D(C10) 、 Y(A8) 、
- 本次實驗需助教確認正確，並將專案跟文件資料(真值表、最簡SOP …)壓縮上傳EE-Class。
- 作業x_第x組 例如:作業3_第一組