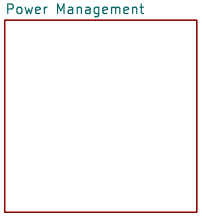
Power Management



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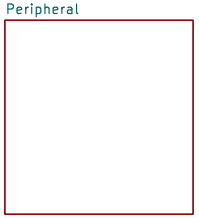
Peripheral



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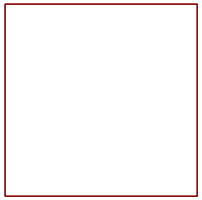
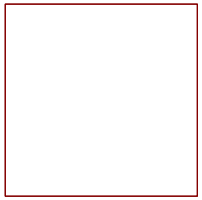
RAM



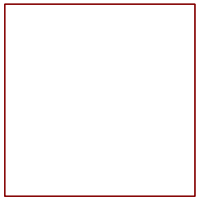
File: RAM.kicad_sch

WiFi_BLE



File: WiFi_BLE.kicad_sch

FPGA

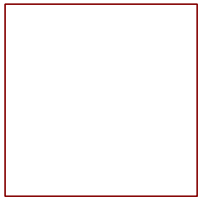


File: FPGA.kicad_sch

FPGA Power

File: FPGApwr.kicad_sch

FPGA MIO



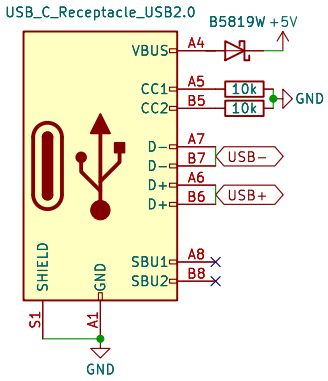
File: FPGA MIO.kicad_sch

Sheet: /
File: SYNC-VT.kicad_sch

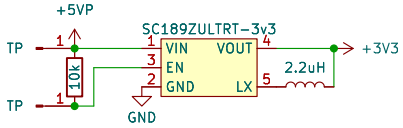
Title:

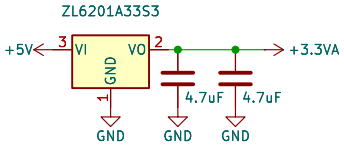
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.6		Id: 1/8

UART USB C



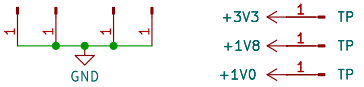
5v to 3v3 Switching Regulator



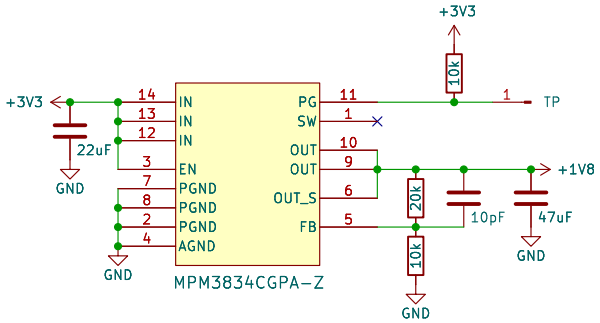


Two regulators:
1) For FPGA and else
2) For ESP32-C6 and its peripherals

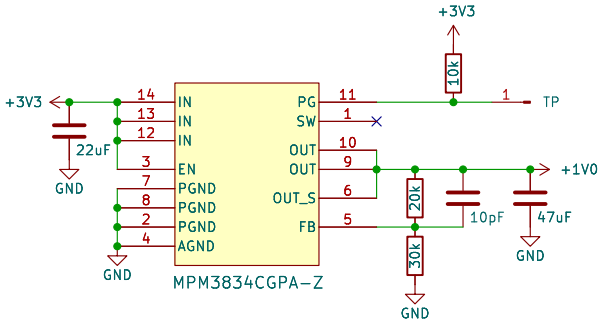
Test points and Mounting holes



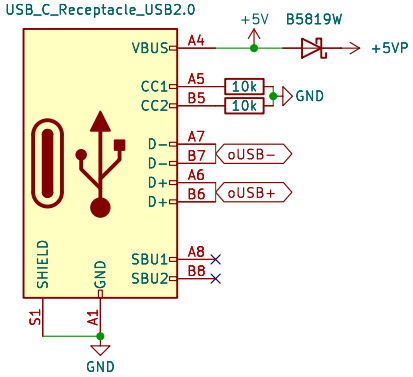
1V8 Regulator Circuit



1V0 Regulator Circuit

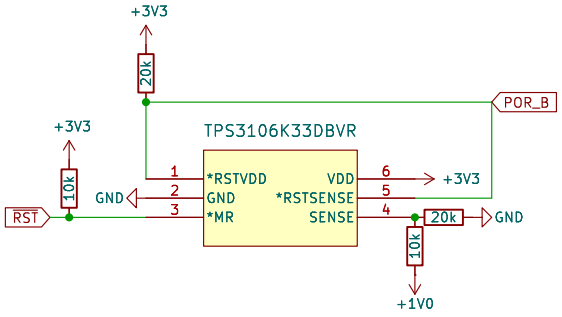


POWER USB C



The board could run on just the Power or the UART plug.
The reason there are two plugs, are to the make the board compliant with the RPI Zero form-factor and to allow the inclusion of the OTG function in the future.

Power-On Reset circuit



Sheet: /Power Management/
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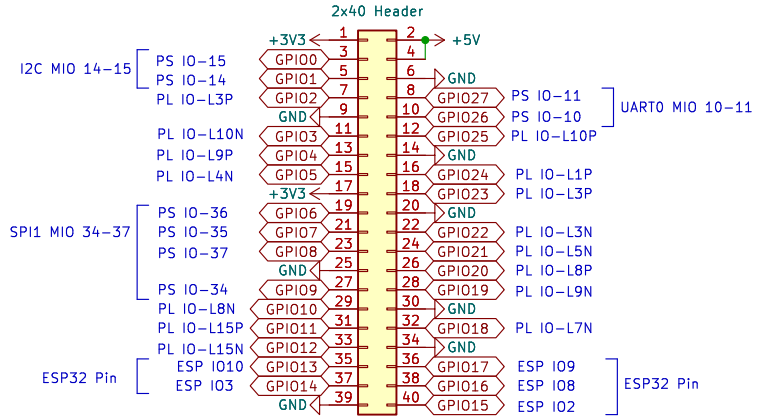
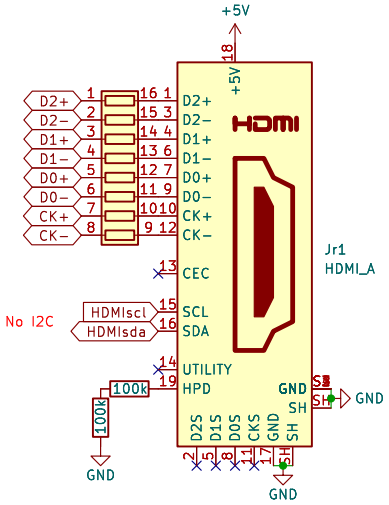
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.6		Id: 2/8

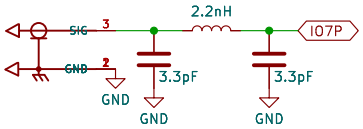
Pin Header/Expansion

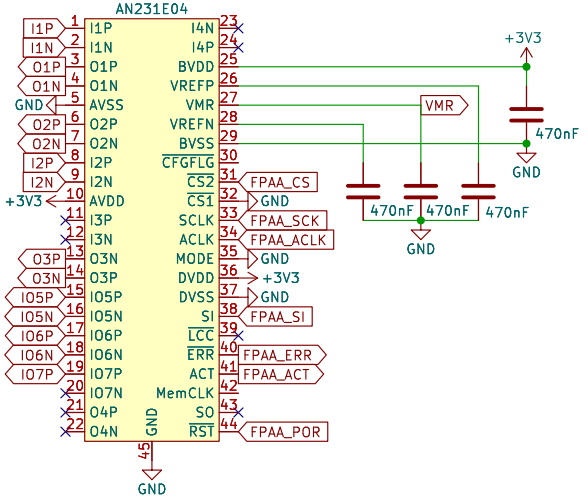


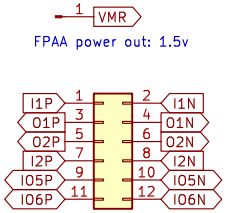
HDMI Plug



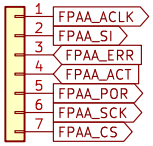
FPAA Experimental Circuit







FPAA header



Note: the FPAA is not connected to the FPGA or ESP32
The only way for user to use the FPAA is to connect this header to any IO of either of the FPGA or ESP32.
The system was designed this way as to completely seperate the FPGA and FPAA in any case that the FPAA don't work as intended.

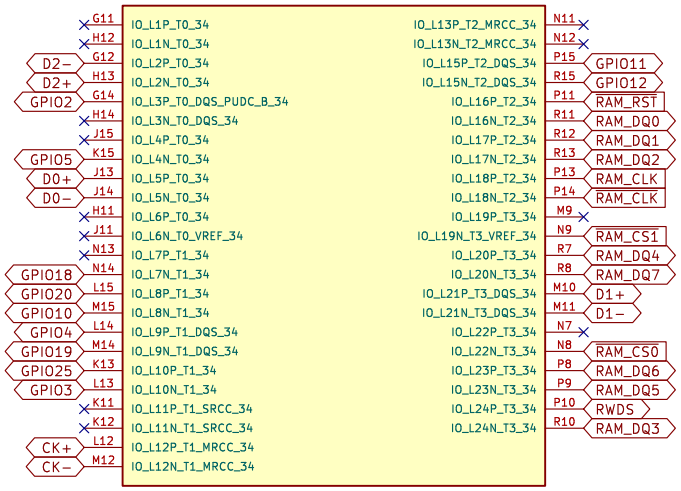
Sheet: /Peripheral/
File: Peripheral.kicad_sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.6		Id: 3/8

PL IO

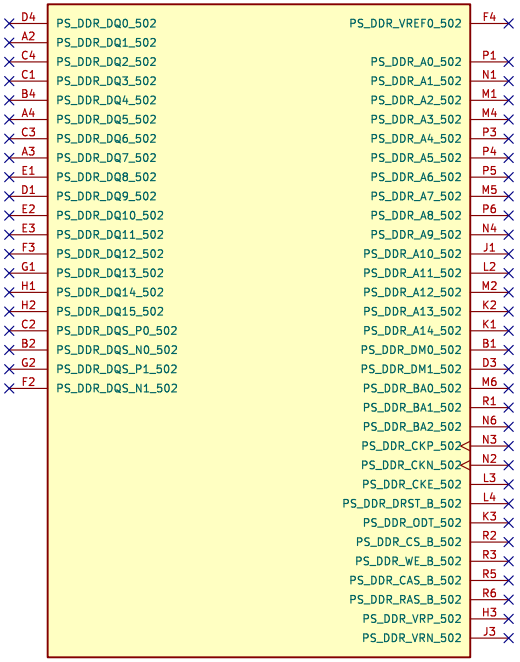
U3B
XC7Z010-1CLG225I



Some pins aren't useable due to its locations and or due to support capacitors over lapping it on the PCB.

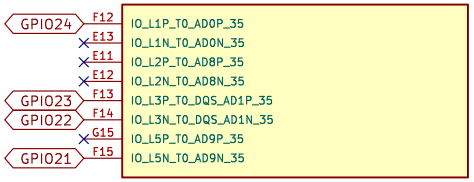
DDR RAM (not in use)

U3E
XC7Z010-1CLG225I



SYNC-VT plans to utilize DDR RAM in future revisions due to its higher speed and more memory dense architecture. However for this revision, the team wants to lower the IO pin counts and to test the usability of PSRAM technoclogies.

XADC PL IO



U3C
XC7Z010-1CLG225I

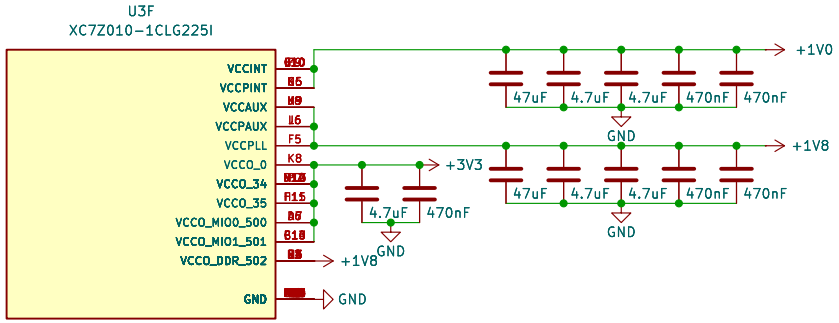
These pins could be use as digital IO, however they're input only for analog.

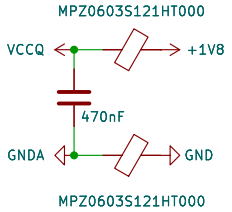
Sheet: /FPGA/
File: FPGA.kicad_sch

Title:

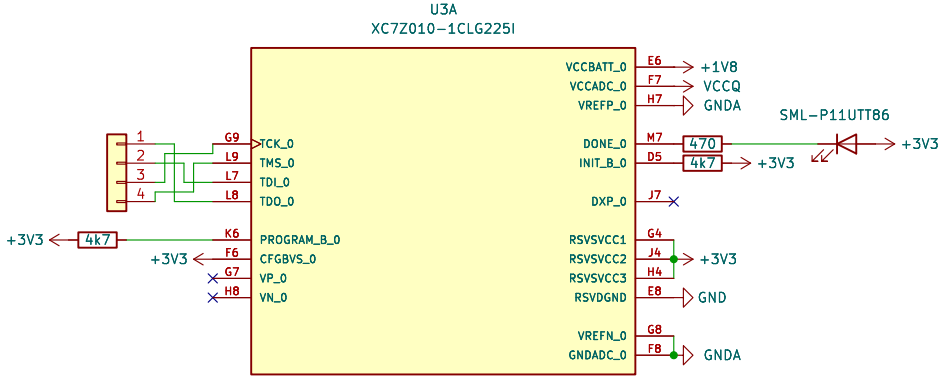
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.6		Id: 4/8

FPGA Power pins



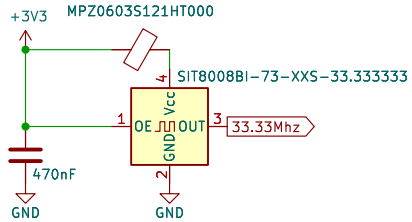


Programming pins

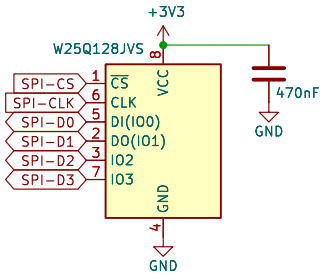


Sheet: /FPGA Power/	
File: FPGApwr.kicad_sch	
Title:	
Size: A4	Date:
KiCad E.D.A. 8.0.6	Id: 5/8

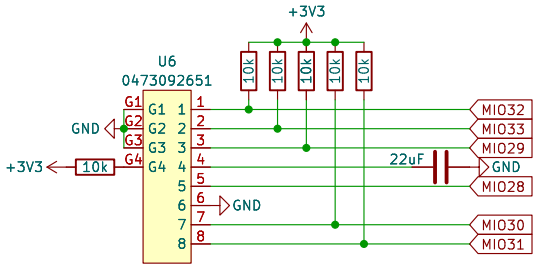
33.33MHz reference cock



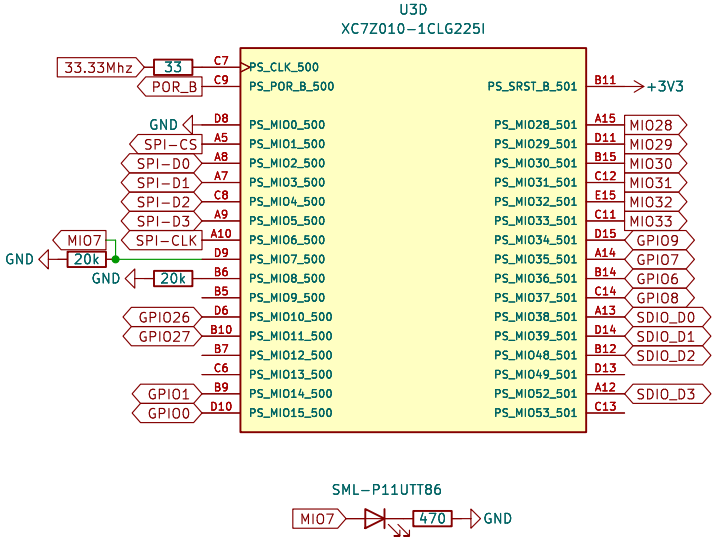
Octal SPI NOR FLash



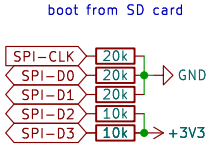
SD Card plug



PS IO pins



Hard wired Boot option

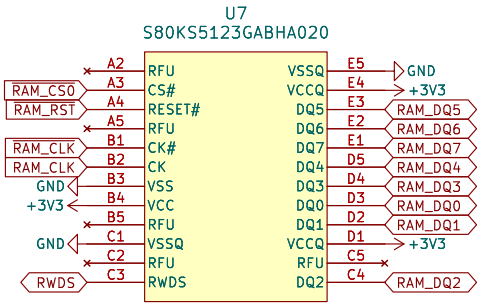


Sheet: /FPGA MIO/
File: FPGA MIO.kicad_sch

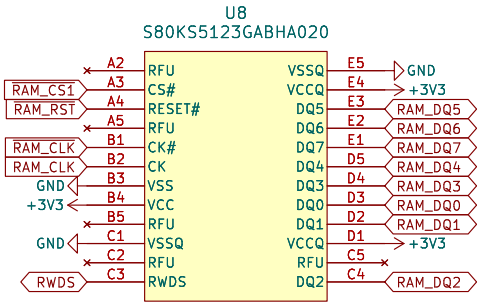
Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.6		Id: 6/8

PSRAM system



64MB of storage each



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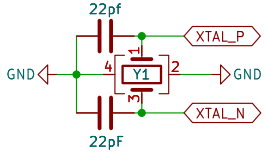
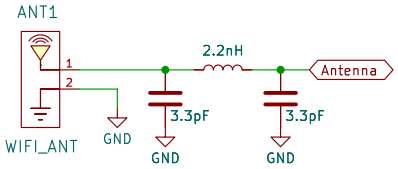
Title:

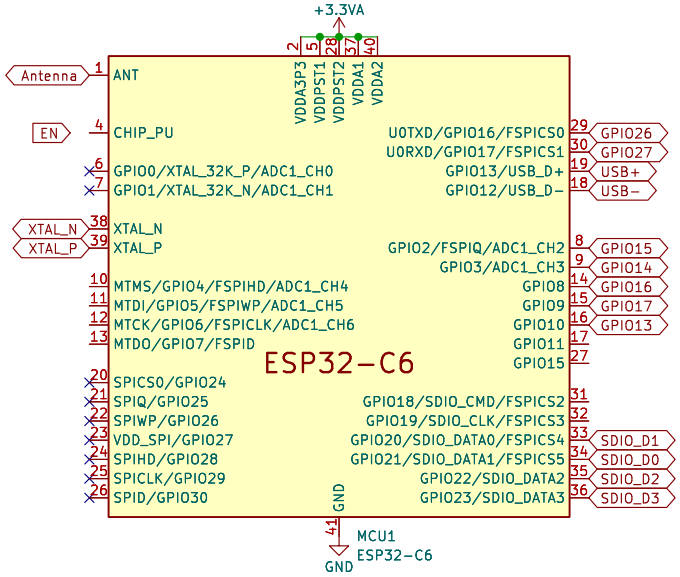
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.6		Id: 7/8



40 Mhz Oscillator



There are plans to switch the PCB antenna to a UFL connectore for a longer range antennas.



There might be plans to break out more IOs from the ESP32 and or give it more RAM so it could act on its own.

Sheet: /WiFi_BLE/		
File: WiFi_BLE.kicad_sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. 8.0.6		Id: 8/8