Name :- Chetan Singh
UnivRollNo:- 1918305
Roll No:- 19
Section:- K

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Assignment-4

1) 2^{21} words of main memory implies we have 21 bits in an address, Cache contains 2^6 blocks, but each set must have 2 blocks, so we have $\frac{2^6}{2} = 2^5$ sets

∴ our 21-bit address is divided into 14 bits for the tag field, 5 bits for the set field and 2 bits for the word field

2) Set associative cache combines the ideas of direct mapped and fully associative cache is as follows:
- An N-way Set associative cache mapping is like direct mapped cache in that a memory reference maps to a particular location in cache
- A memory reference maps to a set of several (N) cache blocks, similar to the way in which fully associative cache works unlike direct mapped cache
- A memory reference can map only to the subset of cache slots instead of mapping anywhere in the entire cache
- In set associative cache mapping a memory reference is divided into three fields those are tag, set and word

3) Main memory size = 16MB = 224B
Cache memory size = 64kB = 216B
Block size = 128B.
Number of lines (N) = $\frac{64K}{128} = \frac{2^{16}}{2^7} = 2^9$

Number of sets (S) = $\frac{N}{\text{P-ways}} = \frac{2^9}{2^2} = 2^7$

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A1 : (52(9A4)

52	1100 1000	1A4

A2 : (54698)

54	110010	108

A3 : (6A389C)

6A	1100100	09C

A4: (5E4699)

5E	1000110	099

A1, A2, A3 same cache set

4) Average access time = Hit time x Hit rate + Miss penalty * miss Rate

Cache Hit time 5ns
Hit rate 65%.
Miss penalty 50ns
Miss rate 35%.

∴ Average Access time = 0.65(5) + 0.35(50)
= 20.75

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5) main memory has 256K = $2^{?} \times 2^{10} = 2^{18}$
i e we need 18 bit to address main memory
cache memory has 4K = $2^2 \times 2^{10} = 2^{12}$
i.e we need 12 bits to address cache memory
Cache consists of indexs and tag which together are used to address main memory location
Here index is 12 bits and tag is 6 bits
(18 - 12 = 6)

Index is divided into block part and word part
Block part is used to address blocks in cache
and word part addresses individual word in block
Here a block size is 16 words i.e 2^4, we need 4 bits to address a word and 12-4 = 8 bits to address block in cache memory

Since cache is 4K words and block size is 16 words i e No of block in cache = $\frac{4K}{16} = 256$

6) The memory system for Pentium microprocessor is 4G Bytes in size just as in 8086 and 8088 microprocessor. Pentium uses a 64 bit data Bus to address memory organized in eight banks that each contains 512 m bytes of data

Most microprocessors including Pentium also supports virtual memory concept with the help of memory management unit. Virtual memory is used to manage the resource of physical memory

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By adding a paging unit and a new system in memory system the management of it has been improved upon.
The Paging mechanism work on 4KB memory pages or with a new extension available to the Pentium with 4MB memory pages.
The system memory management mode is in the equal levels such as the protected mode real mode, and virtual mode still the memory management mode function as a manager. High level system functions such as power management and security are taken care of by it

6) Address space = The set of address use by virtual memory is called address space
The address space is divided into pages

Memory space: The set of addresses use by main memory is called memory space
The address space divided into two blocks
No. of bits used for address space = 32
No. of word there in address space
$= 2^{32} = 16 \times 2^{28}$