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Ans (1) a) $2^8 = 256$ which is larger than 150 we take the next lower which is $2^7 = 128$ bits.
therefore operation code needs 8 bits.

b) $24 - 8 = 16$
There are 16 bits available for the address part of the instruction.

c) $2^{16} = 65536$, max number is
XXXXX = 65536. Ans

Ans (2) 2.4 Ghz is faster than 1.4 Ghz.
2.4 Ghz CPU performs 71.5% more computations than 1.4 Ghz CPU in the same time. Says you have 71.5% more productivity with 2.4 Ghz CPU.
1.4 and 2.4 Ghz are CPU clock speeds.
$\frac{1}{freq}$ = period so you can calculate the period or time of each clock cycle.

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Ans (3) A) Minimum bus cycle duration = 1 clock cycle.

maximum bus cycle rate = 8 MHz / 4
= 2 MHz where
1 MHz = 1000000/sec

maximum data transferred per bus cycle rate = 2 bytes.

data transferred rate per second
= data transfer per bus cycle * bus cycle rate
= 2 byte * 2 MHz
= 4 × 10^6 bytes/sec Ans

B) if we double the clock rate
its = 8 × 2 = 16 MHz / 4
= 4 MHz
1 MHz = 10^6 /sec
so data transfer = 2 byte * 4 MHz
= 8 × 10^6 byte/sec

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(C) Input clock cycle = 8/4 = 2MHz
width = 32 bus cycle = 2.

32* 2MHz = 64,000,000 bit/sec.
8,000,000
= 64000,000
8
= 8,000,000 byte/sec

(D) Input clock cycle = 8/4 = 2MHz
width = 16 bus cycle = 2 . 16* 2MHz 32 000,000
bit/sec
= 4000000
byte/sec
(1 byte = 8 bits)

to increase performance, it would be better to make the external bus 32 bits.
This would double the bit rate across the external bus.

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Ans (4)

a) $(0.1)_{10} = 0.0001100110011001100110011001100_2$

$0.0001100110011001100110011001100 =$
$1.1001100110011001100110011001100 \times 2^{-4}$

Exponent = $-4 + 127 = 123$ (01111011)
Sign bit = 0
mantissa = 10011001100110011001100

S (1 bit)	Exponent (8 bit)	mantissa (23 bits)
0	01111011	10011001100110011001100

Ans 1)

b) $(+40.52)_{10} \rightarrow = (40.52)_2$

$(+40.52)_{10} = 101000.1000\ 0101\ 0001\ 1110\ 1011\ 1000$
$= 1.0100010000101000111101011100 \times 2^5$

Exponent = $5 + 127 = 132$
Sign bit = 1
Mantissa = 01000010000101000111101010

S bit	Exponent (8 bit)	Mantissa (23 bit)
1	10000100	01000010000101000111101010

Ans 2)

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(?)

Rep = (0000 1100 1100 1100 1100 1100 1100 1100)
= S = 0   Max Exponent = 128 (01111011)$_2$
Mantissa = (1001100110011001100100)

123 - 1
123 - (-1)
= 127

= 1.0000 1100 1100 1100 1100 1100)
= 0000.1100 1100 1100 1100 1100 1100 $\times 2^4$
= 0. 1100 1100 1100 1100 1100 1100
0. 1100 1100 1100 1100 1100 1100
0.01 (Rough calculation).

Rough
0. 1×2^{-1}
1×2^{-2} +0x2
+ ; |||
= (001)

Ans (5)

R = 100 11100
Arithmetic shift right = 1100 1110
Arithmetic ~~left~~ shift left = 00111 000
overflow because a negative number changed to positive.

Ans (6)

-13 = 0011   7 = 0111
Q = Q_3 Q_2 Q_1 Q_0 | Q_{-1}
0 1 1 | 0

Step	A	Q	Q_{-1}	A=A-M
4	0000	0111	0	0000 1101 1101
	1101	0111	0	
	0110	1011	1	

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N	A	Q	Q-1	
3	0110	1011	1	
	0011	0101	1	
2	0011	0101	1	
	0001	1010	1	
1	0001	1010	1	A = A + M 0001
				0001
				0100
N=0	0100	1010	1	
	1010	0101	0	

Product 1010 0101

2's 1010 0101

1101 1010

2's 1 1

1101 1011 = (-91)

(-13 × 7) = -91

1 1 0 1 1 0 1 1 = (-91)

7 6 5 4 3 2 1 0

One = 1 1011011 → (-91)

Sign bit

One's

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Ans (6)

$S = 1/(1-P)$

$P = 1 - \text{Seq. Part}$
$= 1 - 0.08 \ (\text{or } 8\%)$
$= 0.92$

$S = 1/(1-0.92)$
$= 1/0.08$
$= 12.5$ Ans.

Ans (7)

Instruction type	freq	cycles
Load and stores	30%	6 cycles
Arithmetic Instruction	50%	4 cycles
All others	20%	3 cycles

$CPI = (30*6 + 50*4 + 20*3)/100$
$= (180 + 200 + 60)/100$
$= 440/100$
$= 4.4$ Ans.