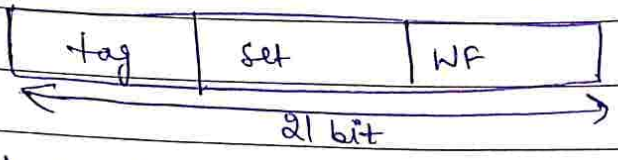
# Assignment = 04

Name = Aditi  Section-H  Univ Roll no = 1918143
Class Roll no = 16

Ans 1.) $2^{21}$ words = m/m , 64 blocks Cache. (each 4 words)
cache is 2 way set associative.




Total # of sets = $\frac{\text{cache total blocks}}{\text{no of block in each set}}$

$= \frac{64}{2} = \frac{2^6}{2} = 2^5$ sets.

∴ set field = 5

word field = $4 = 2^2$

∴ Word field = 2.

Tag + set + WF = 21
Tag + 5 + 2 = 21
Tag = 21 − 7
Tag = 14

∴ tag bit = 14, set = 5, WF = 2.

Ans 2.) Set associative cache is a combination of both Direct Associative and Fully Associative cache. The memory block in set associative is as same other two cache types but the cache in set associative is divided in the

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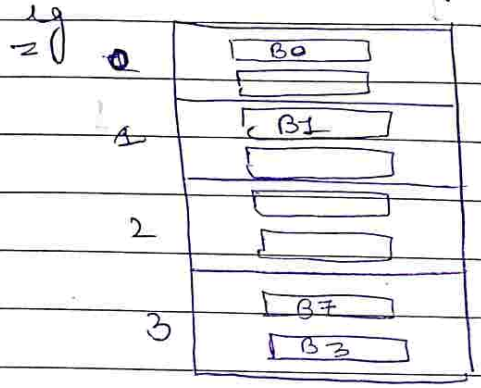
sets. Each block of cache contains the no. of sets in it. Hence, there are types of set Associate cache like 2 way set Associative and 4 way set Associative. So when the main memory in set Associative place the blocks of memory in cache lines, it uses the direct Memory cache technique there.




2 way cache.

M/m Blocks are
0 % 4 = 0
7 % 4 = 3
3 % 4 = 3
1 % 4 = 1

So the placing of blocks is as same as in DM cache. But if we get to place memory blocks in same cache line then the fully Associative cache technique is used. As in example B7 and B3 can be placed anywhere in set. Therefore it is concluded that the cache lines uses DM to place blocks and the set uses the FA to place blocks in it. This is how the combination works in the set Associative cache.

Ques 3)

Word length = 32 bits
Byte-addressable M/m = 16MB.
4 way cache = 64 KB.
Block size = 128 Bytes.

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A1 = 0X52C9AH = 01010010110010011010 0100
A2 = 0X54698
A3 = 0X6A3896
A4 = 0X5E4699.

Capacity of each set = 4 * 1280 bytes.
= bytes
= 512

Total set = 64 KBytes.
bytes.
= $2^6 \times 2^{10}$ B = $2^{16}$ B
$2^{10}$ B
= $2^6$ sets. = $2^9$ $2^7$ B.

∴ Set = 7
Word field = 128 = $2^7$
∴ WF = 7.

16 MB → bits.

(1) A1 = 52C9A4 = 01010010110010011010 0100
A1 = 0010011

(2) A2 = 54698 = 0101 0100 0110 1001 1000
A2 = 0001101

(3) A3 = 6A3896 = 011010100011100010010110
A3 = 1110001

(4) A4 = 5E4699 = 0101 1101 0100 0110 1001 1001
A4 = 0001101

A2 and A4 maps to the same cache.

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Ans 4)

Read Req = 55 ns (CM)

CH = 5 ns

CH = 65%, Cache miss = 100 − 65 = 35%

(a) For hierarchical memory access! −

EAT = 0.65 X 5 + 0.35 X (55+5)

= 3.25 + 21

= 24.25 n/s.

(b) for Simultaneous memory access! −

EAT = 0.65 X 5 + 0.35 X 55

= 3.25 + 19.25

= 22.5 n/s.

Ans 5)

m/m = 256 K, 16 words.

Cache = 1K words.

uses dM with a block size of 4 words.

(a) Main m/m has 256 K = $2^8 \times 2^{10} = 2^{18}$

∴ 18 bit address to m/m.

Cache m/m has 1K words = $1 \times 2^{10} = 2^{10}$

∴ 10 bits to address cache.

∴ 18 − 10 = 8.

∴ 8 tags are there.

16 words = $2^4$ ⇒ 4.

∴ Word field = 4.

Block = 10 − 4 = 6

Index = 12, Tag = 8, Block = 6, WF = 4.

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(b) Total bits = 27

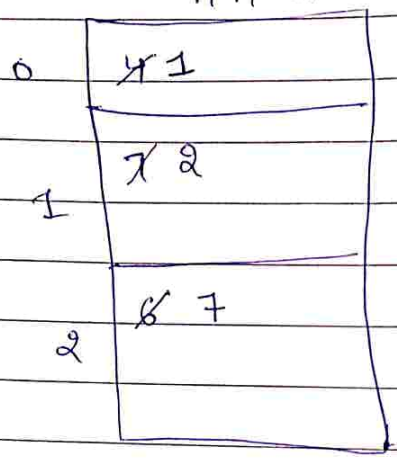
(c) no. of blocks = $\frac{1K}{16}$

$= \frac{2^{10}}{2^4} = 2^6$

= 64 blocks

Ans 7.)

4, 7, 6, 1, 7, 6, 1, 2, 7, 2.
H H H H

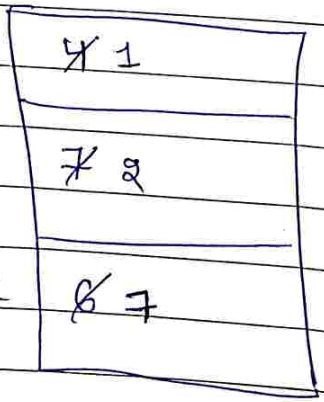



(a) FIFO. → Cache misses = ?

∴ no. of cache miss in FIFO is $\frac{6}{10} = 0.6$.

(B) For LRU replacement

4, 7, 6, 1, 7, 6, 1, 2, 7, 2.
H H H H




Cache Miss = $\frac{6}{10} = 0.6$.

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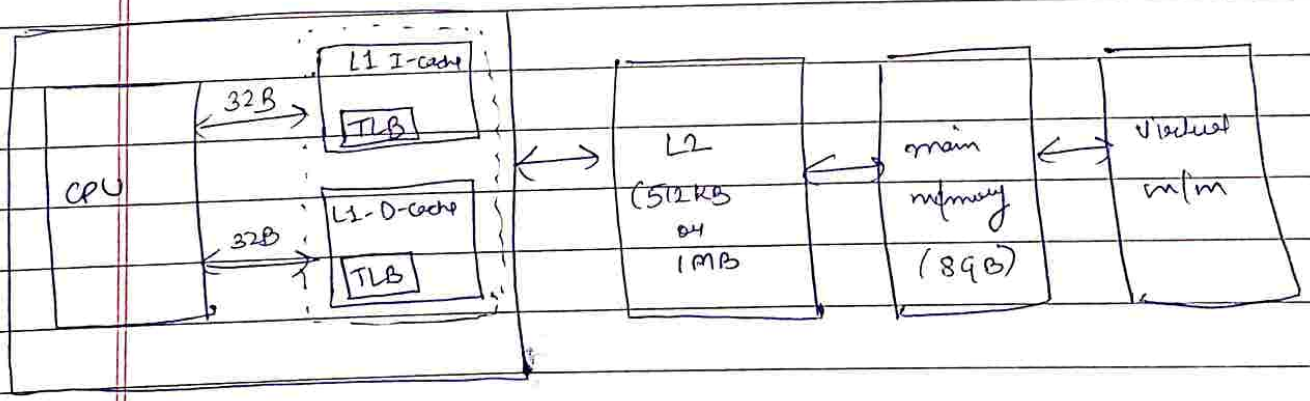
Ans 8) Memory Management of Pentium 4.

The Pentium architecture allows for 32-bit virtual addresses and 32-bit physical addresses. It uses either 4KB or 4MB page sizes, when using paging. Here both paging and segmentation can be applied in different combinations. The pentium has two caches, L1 and L2. The L1 cache is next is the processor and the L2 cache is between the processor and main memory. The L1 cache is further divided into two caches i.e cache I and cache D. L1 cache uses these caches two hold instruction and other cache to hold the data. Both the caches of L1 uses LRU bit for dealing with block replacement. Each L1 cache has a TLB. The entries in D cache is 64 and the entries in I-cache is 32. Both TLBs are 4-way set associative and use LRU replacement. Both D and I cache uses 2 way set associative maping. The L2 cache, like both L1 caches, uses 2-way set associative mapping. The L2 cache can be from 512 KB to 1MB. To manage access to memory, the Pentium I-cache and L2 cache both uses the MESI cache coherency protocol. MESI stands for modified, exclusive, shared and invalid.




Pentium Memory Hierarchy.