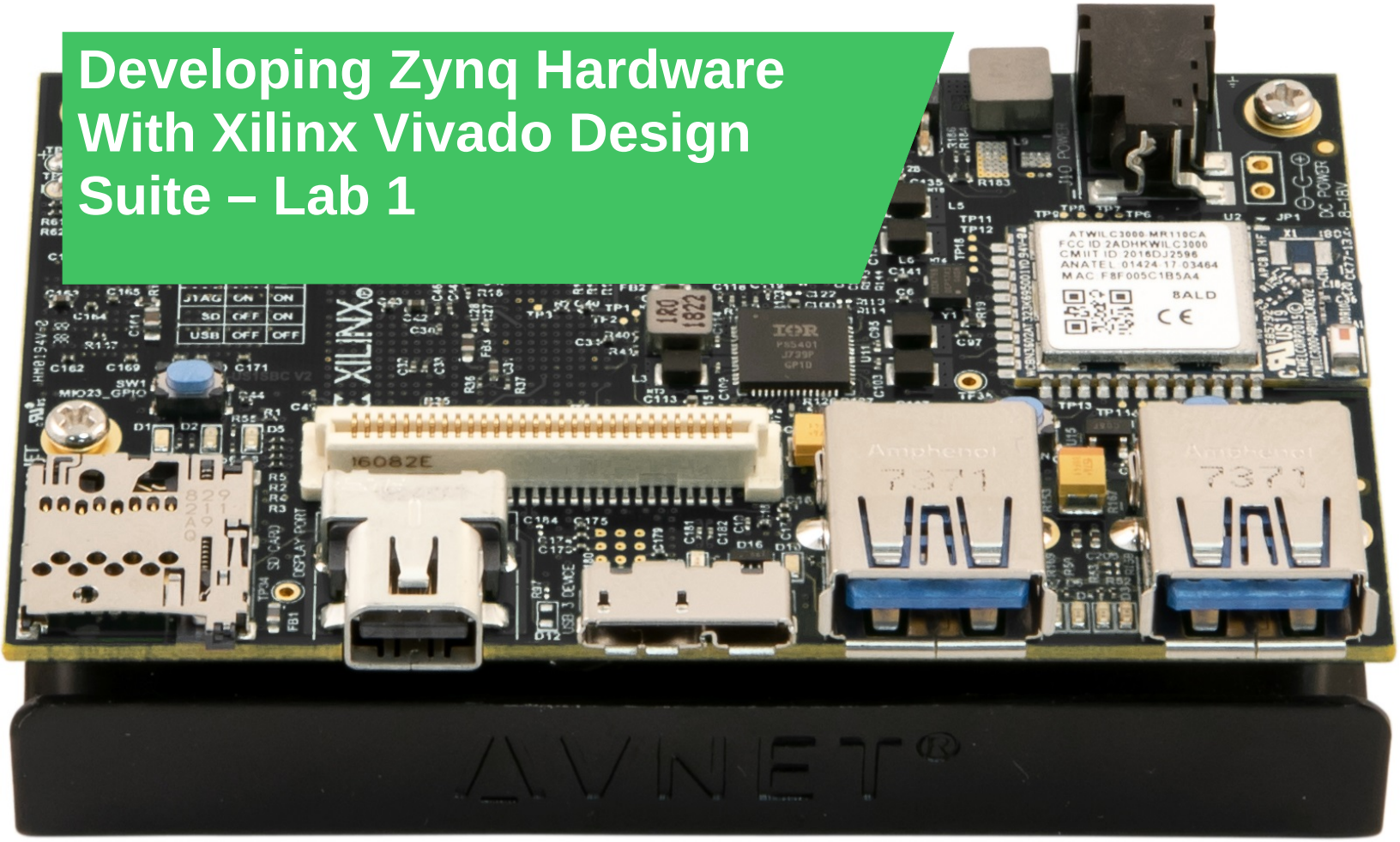
Avnet Technical Training Course

Developing Zynq Hardware With Xilinx Vivado Design Suite – Lab 1



Tools:	2019.1
Training Version:	v12
Date:	July 2019

Lab Setup

To complete all of the Avnet Technical Training Course labs, the following software and hardware setups are required.

Software

The recommended software for this Avnet Technical Training Course is:

- O/S supported by Xilinx Vivado® Design Suite 2019.1
  - See UG973 v2019.1 *Release Notes* for the supported list
  - Ubuntu Linux LTS 16.04.01 – Running in a Virtual Machine
- Xilinx Vivado Webpack 2019.1
  - With Vivado 2019.1

Hardware

The recommended target hardware consists of the following:

- Win-10 running a Ubuntu Virtual Machine PC with a minimum of 16 GB RAM and 200GB Storage, available for the Xilinx tools to complete a XC7Z007S design
  - https://www.xilinx.com/products/design-tools/vivado/memory.html
- Avnet MiniZed
- USB cable (Type A to Micro-USB Type B)

Lab Instruction Notes

Throughout all the Avnet Technical Training Course labs, a generalized instruction is given. If you're comfortable completing the task based on that instruction, feel free to do so. If not, step-by-step instructions are provided.

Technical Support

For technical support with any of the labs, please contact your local Avnet FAE or visit the Training Forum:

www.minized.org/forums/training

Additional technical support resources are listed below.

Evaluation Kit home pages with Documentation and Reference Designs

www.minized.org/product/minized

Xilinx technical support

You may contact your local Avnet FAE or Xilinx Online Technical Support at www.support.xilinx.com . On this site you will also find the following resources for assistance:

- Software, IP, and Documentation Updates
- Access to Technical Support Web Tools
- Searchable Answer Database with Over 4,000 Solutions
- User Forums
- Training - Select instructor-led classes and recorded e-learning options

Avnet technical support

Contact your Avnet FAE or the forums for any additional questions regarding the MiniZed reference designs, kit hardware, or if you are interested in designing any of the kit devices into your next design.

Lab 1 Overview

Vivado Design Suite WebPACK is free and includes all the required tools for creating new FPGA and SoC designs as well as the Software Development Kit (SDK) for developing software.

Unlike a traditional processor, the Zynq Processing System (PS) has a configurable set of built-in peripherals. Additionally it has direct access to Programmable Logic (PL) that can build virtually any custom IP. That said, the PS may be used without anything programmed in the PL. However, in order to use any soft IP in the PL, or to route PS dedicated peripherals to device pins in the PL, programming of the PL is required.

The hands-on labs for this Avnet Technical Training Course follow the Xilinx guidelines provided as part of UltraFast Design Methodology. For more information on the benefits of UltraFast Design Methodology, please refer to the Xilinx User Guide documents UG949 and UG1046. Links to these two documents are provided at the end of this lab.

This lab will illustrate an example of how to create a new Zynq project using UltraFast Design Methodology within Vivado Webpack.

Lab 1 Objectives

When you have completed Lab 1, you will know how to do the following:

- Create a new project in Vivado
- Target the Zynq 7Z007S device
- Create a new block design utilizing Vivado's IP Integrator design flow
- Add an Embedded ARM processor core to the project

Experiment 1: Create a new Zynq Project in Vivado

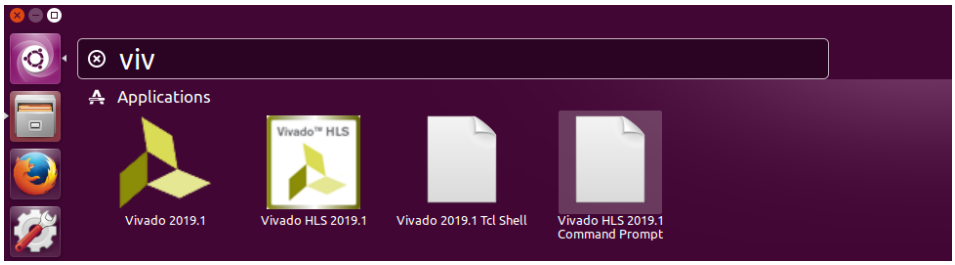
Vivado has awareness of several Xilinx development boards built-in, as well as the Avnet ZedBoard. However we will build this design from scratch, just as you would for your own custom Zynq design.

Experiment 1 General Instruction:

Launch Vivado 2019.1. Create a New project in the Avnet Technical Training Course directory. **/home/training/AvnetTTC/ZynqHW/2019_1/**

Experiment 1 Step-by-Step Instructions:

1. Launch Vivado 2019.1 from either the desktop icon or using the search your computer option and typing in vivado



2. Click on **Create Project**.

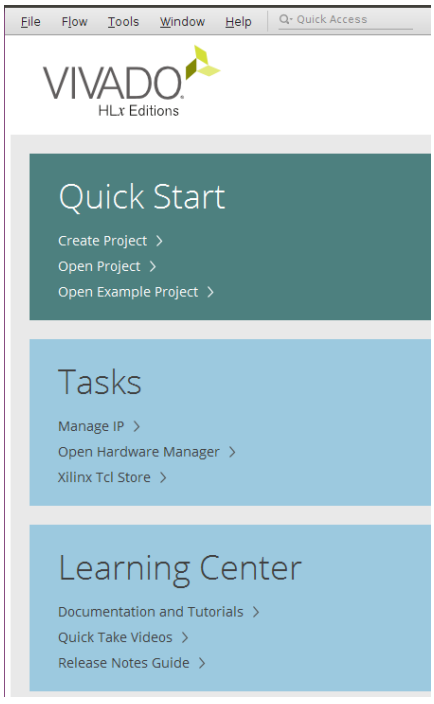


Figure 1 - Vivado Project Creation

3. Click **Next >** in the New Project window.

4. Set the *project name* to **ZynqDesign** and *project location* to the following directory: **/home/training/AvnetTTC/ZynqHW/2019_1**

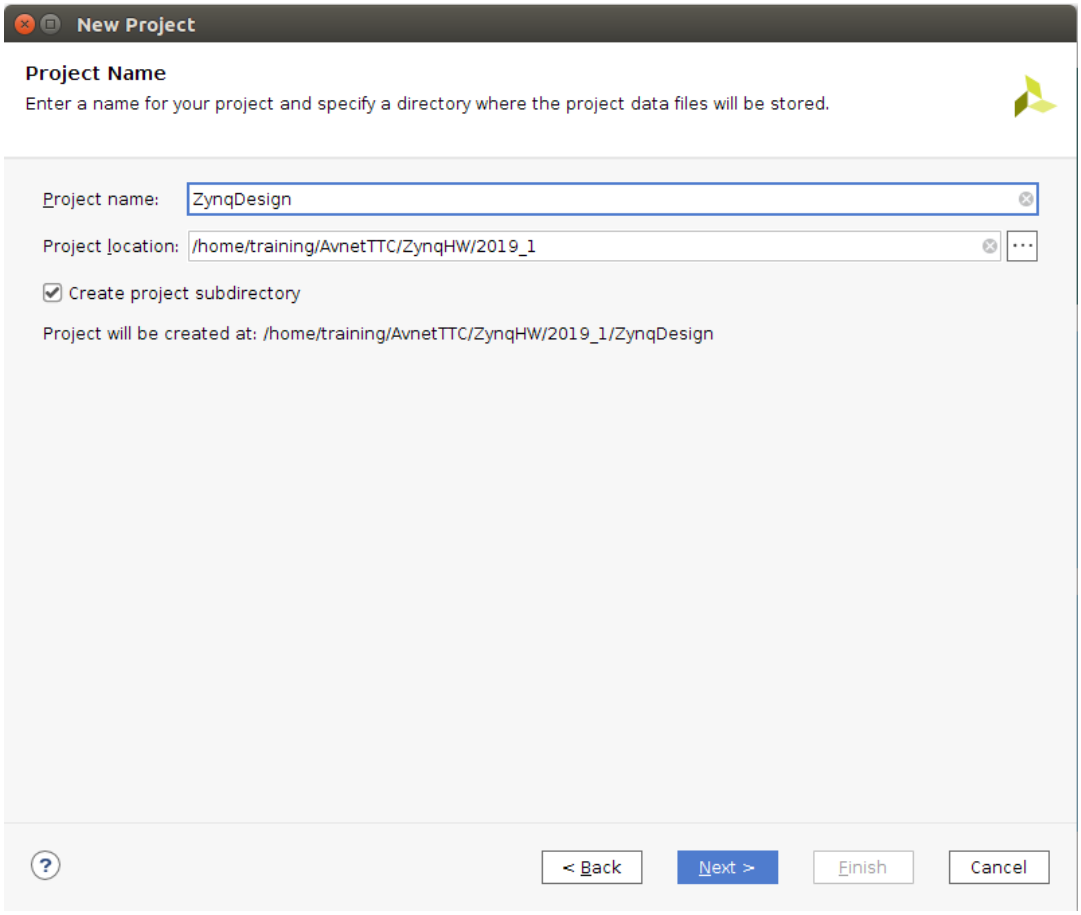


Figure 2 - New Project Name and Location

5. Click **Next >.**

6. For Project type, this will be a RTL-based project, thus leave the radio button for *RTL Project* selected and make sure Do not sepecify sources at this time is deslected. Click **Next >.**

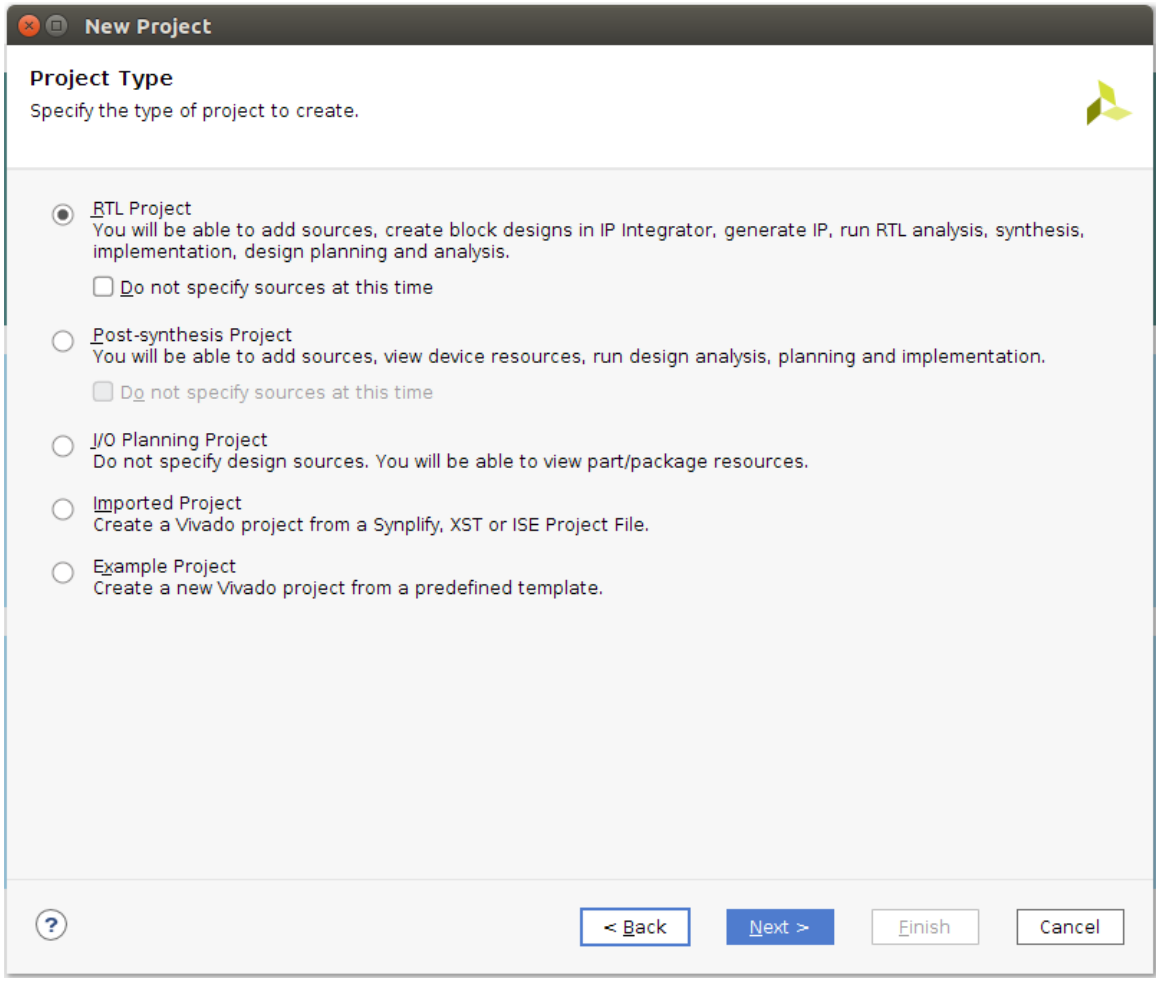


Figure 3 - Project Type Settings

7. Important : select **VHDL** as the Target language. Click **Next** 2 times.

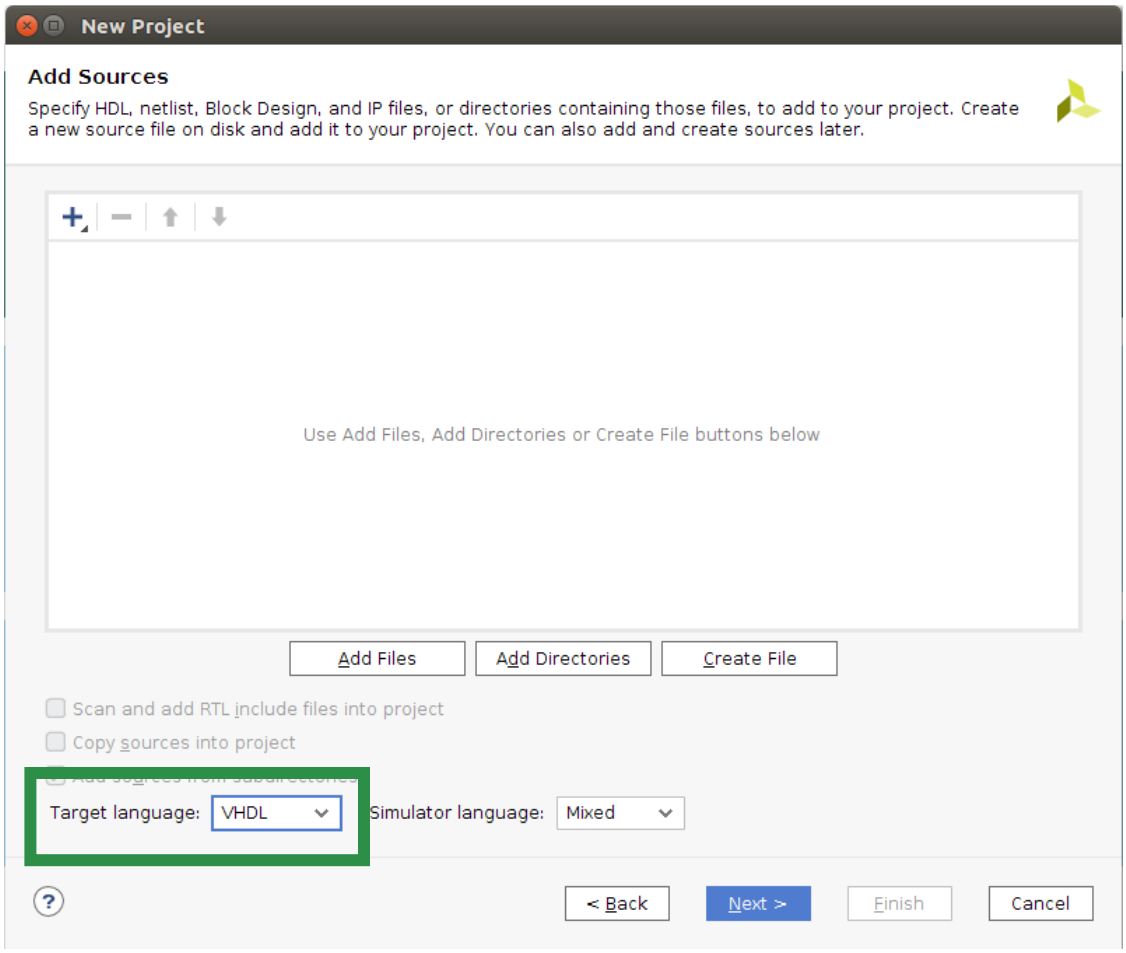


Figure 4 - Add Souces Settings

8. Next, select the target device for this design. This can be done by choosing a specific part or by selecting a board. While we can immediately target Zedboard here, we will not do so as the goal of this tutorial is to learn how to create a custom design for the MiniZed. Choose the *Parts* option next to *Select:*.

   Select the following:
   - Product category General Purpose
   - Family Zynq-7000
   - Package clg225 (MiniZed)

   - Speed grade -1
   - Temp grade Leave Alone

   This should minimize the part options:

   For MiniZed select the **xc7z007sclg225-1**

9. Click **Next >**.

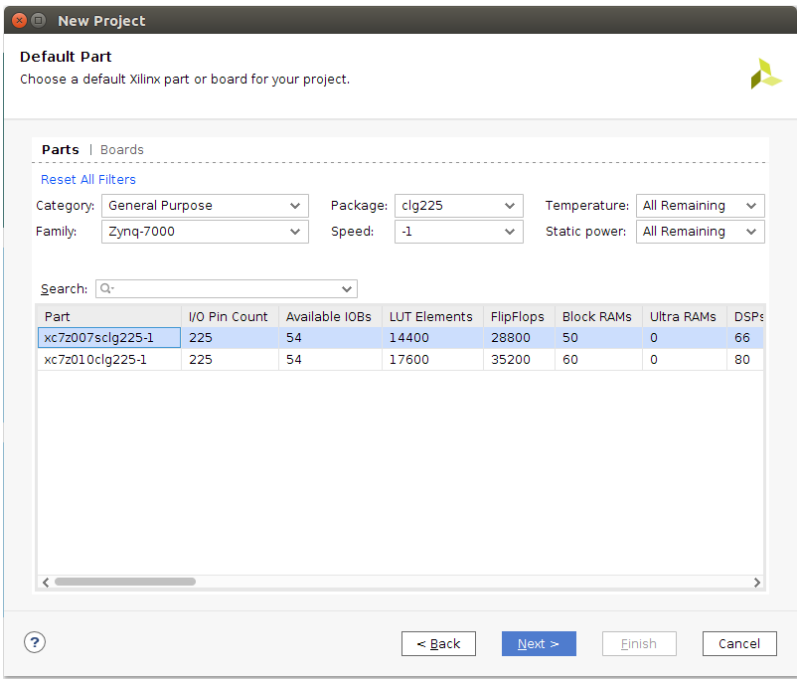


Figure 5 - Target Device - MiniZed Configuration

10. The following project summary is displayed. Click **Finish**.

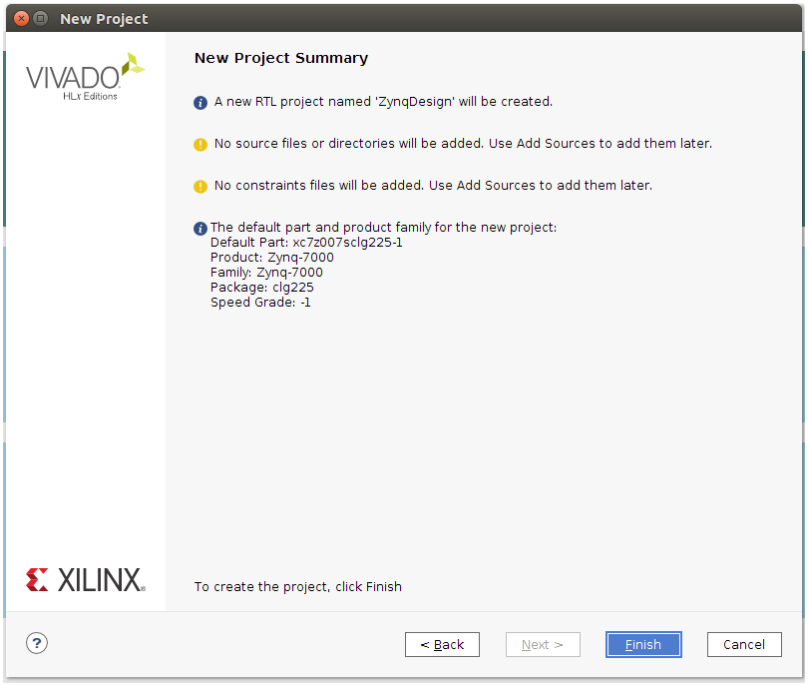


Figure 6 - New Project Summary (MiniZed)

The Vivado design cockpit will open. Take a minute to explore what's available and answer the questions below.

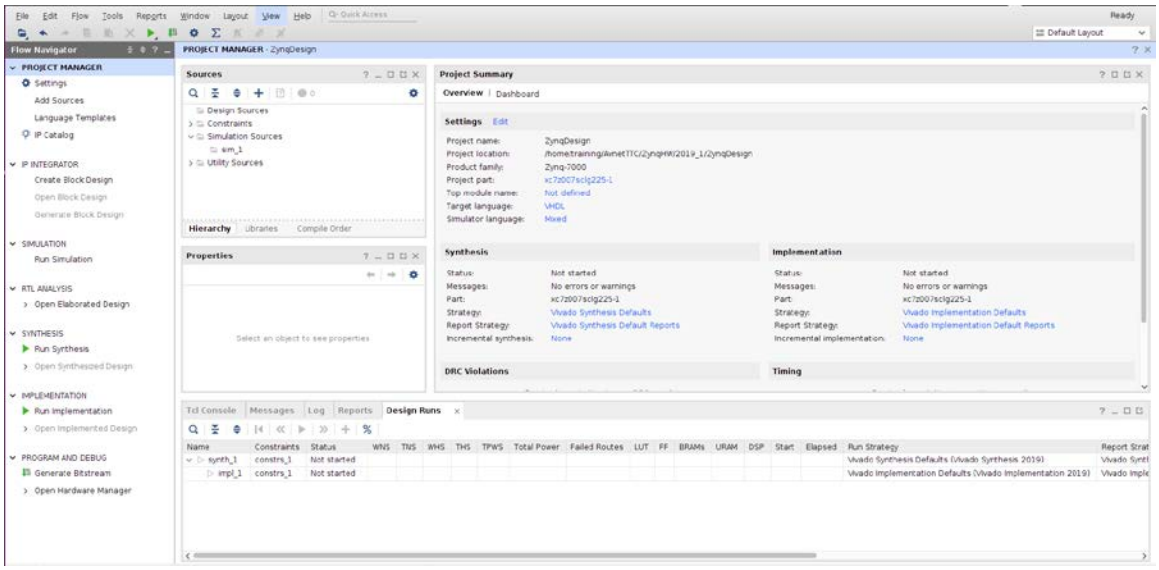


Figure 7 - Vivado Design Cockpit

Questions:

Answer the following questions:

- *What device is selected? Why is there no Top Module?*

_____

- *What are the Vivado Synthesis and Implementation Strategies?*

_____

- *What other information is available in the Project Summary?*

_____

Experiment 2: Create a new Block Design in Vivado

The current project is blank. To access the ARM processing system, we will add an embedded source to the Vivado Project by creating a block design using IP Integrator.

Experiment 1 General Instruction:

Create a block design and add a processor core.

Experiment 2 Step-by-Step Instructions:

1. Under IP Integrator, select **Create Block Design**.

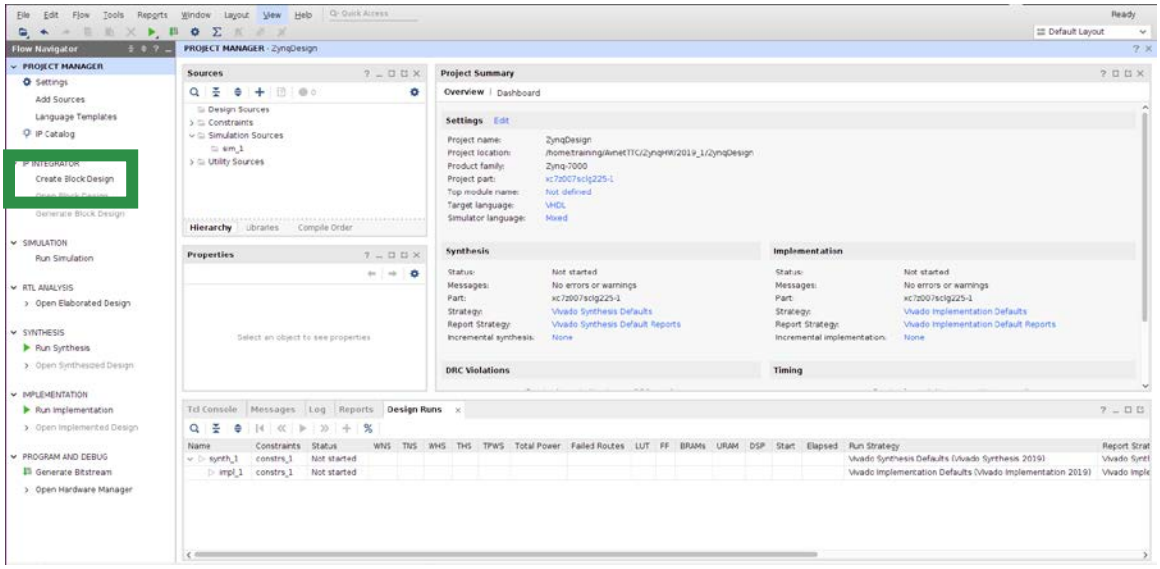


Figure 8 - Create Block Design

2. Enter the name, **Z_system**, for the block design name. Click **OK**.

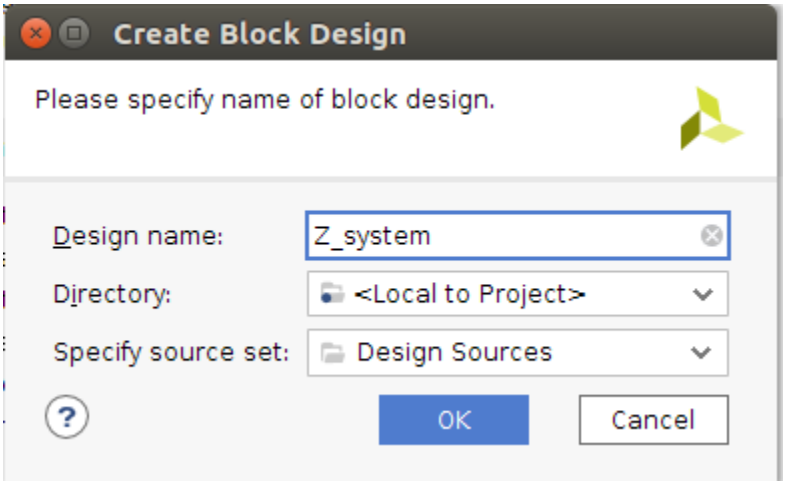


Figure 9 - Block Design Name

3. The Z_system Diagram window will open; select **Add IP** from the Design screen or from the vertical navigation bar shortcuts.

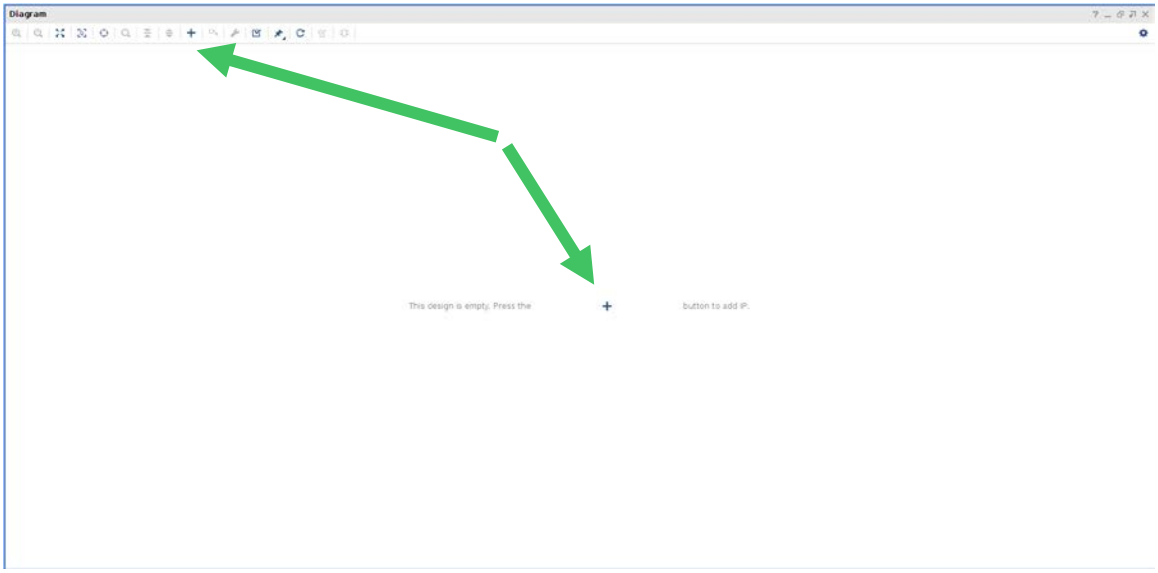


Figure 10 - Add IP

4. In the search window, type **zynq** to filter through the IP. Double-click **ZYNQ7 Processing System**.

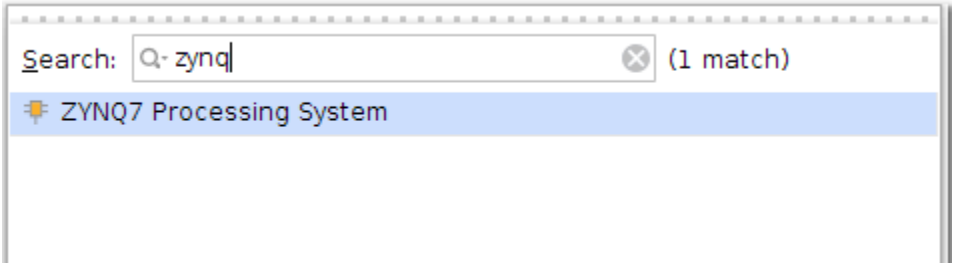


Figure 11 - Zynq Processing System IP

5. The block diagram will now show a *processing_system7_0* IP block. Notice a green navigation bar has reappeared offering *Designer Assistance*. Many of the IPs in a block design can be automatically connected by selecting Run Block Automation. Click on **Run Block Automation** to perform this task on the ARM processing core.

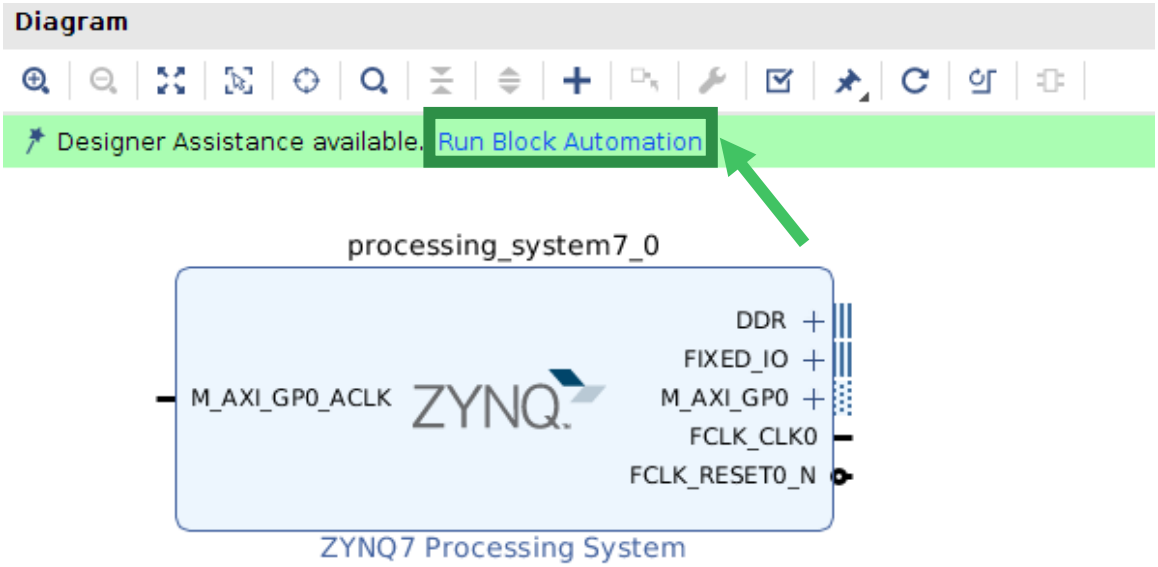


Figure 12 - Run Block Automation

6. The wizard automatically detects it needs to connect external interfaces for FIXED_IO and DDR interfaces. FIXED_IO are I/O dedicated to internal hardened peripherals in the Zynq processing subsystem. These include UARTs, Ethernet, USB and more IP. We'll cover this more later. For now, click **OK** to make these external connections. This simply defines these ports as external interfaces to the block design. Note, the block design may be a small piece of a larger design, thus its external interfaces must be defined.

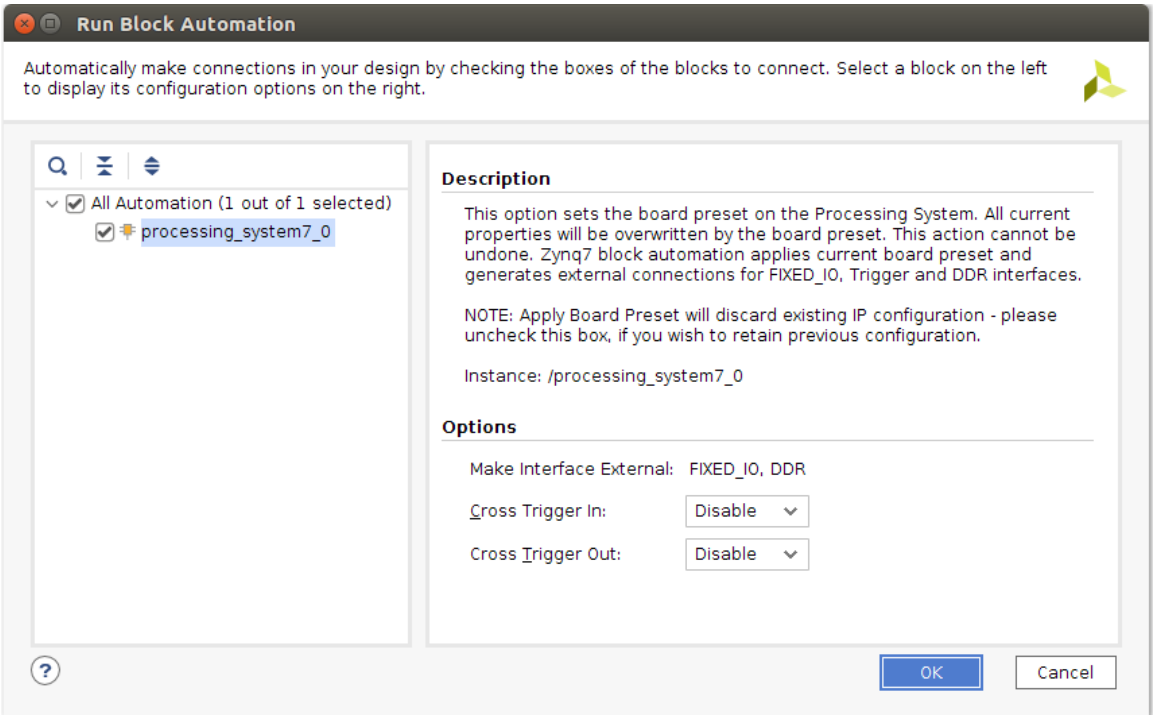


Figure 13 - Click OK to connect external interfaces

Two external ports are now connected to the IP core:

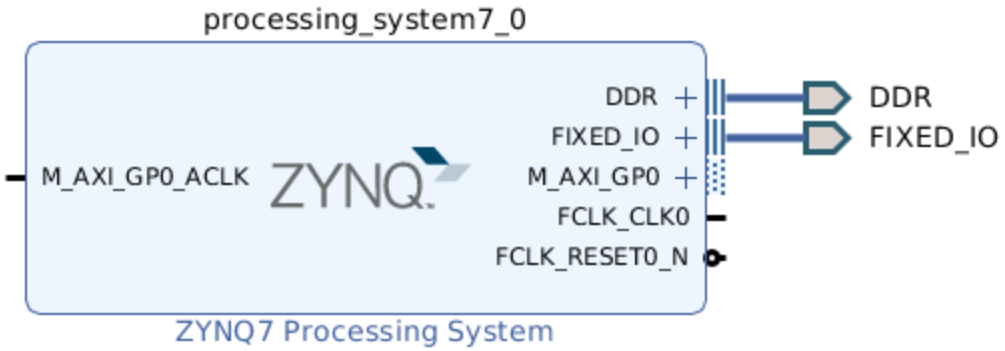


Figure 14 - External Port Connections

7. This is a good time to save the block design. Click the **Save Block Design** button to save the block design.

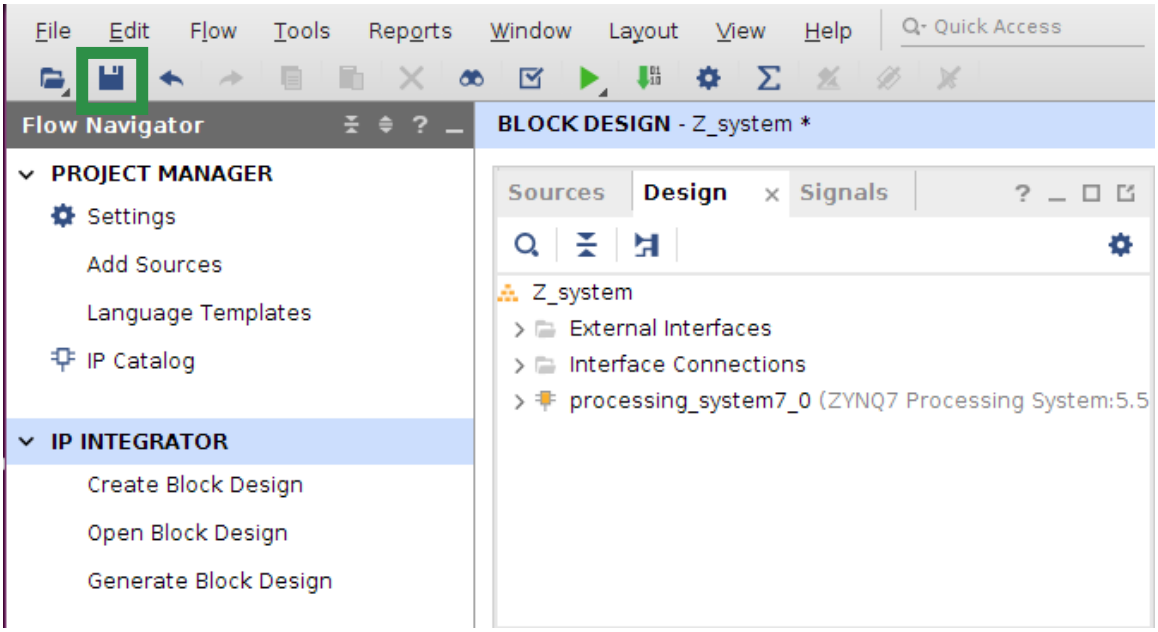


Figure 15 - Save Block Design

8. At this point, the ZYNQ7 Processing System (PS) is completely unconfigured. To start customizing our design, double-click on **the ZYNQ7 Processing System** IP block. Most IP can be customized this way.

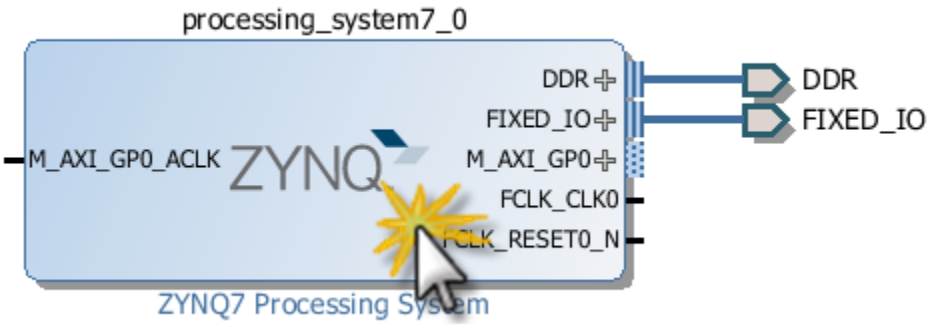


Figure 17 - Double-click on IP to customize the IP

The Zynq Recustomize IP window is now available. Here we can customize the Zynq processing core. All PS features are in their default state, ready to be customized, which is what we will do in the next two labs.

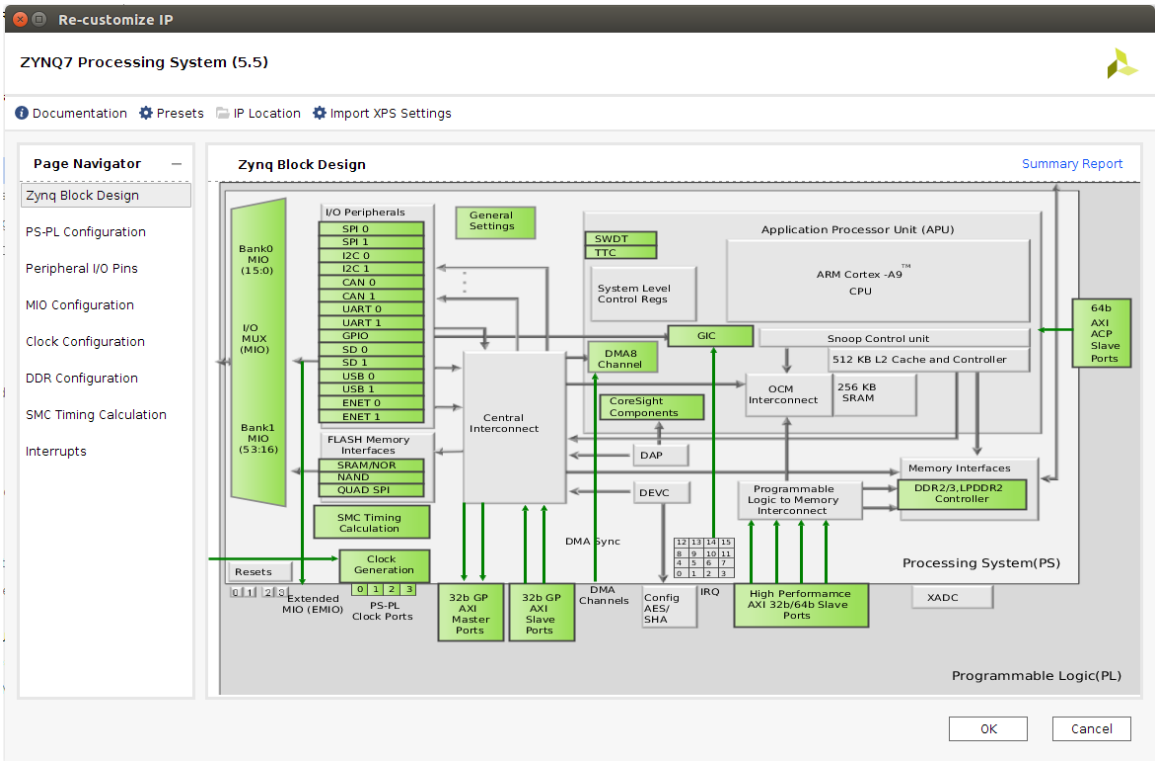


Figure 16 – Re-Customize IP window for the Zynq PS

We now have a new project created and we've added an embedded processing core! Leave the tools open as Lab 2 starts from this point.

Questions:

Answer the following questions:

- *List some configurable components (highlighted green boxes) in the Zynq PS:*

_____

- *The I/O Peripherals are connected to external I/O through the I/O Mux (MIO), how many I/O are available in the MIO?*

_____

Exploring Further

If you have more time and would like to investigate more…

- Explore some of the configurable PS blocks.
- Open the Zynq Technical Reference Manual (TRM) and view the available sections. This can be found in the Support Documents folder or online: http://www.xilinx.com/support/documentation/user_guides/ug585-Zynq-7000-TRM.pdf
- For ISE or PlanAhead users, open the Migration Methodology Guide. This document provides instruction for porting designs from ISE to Vivado. Also updating UCF constraints to XDC. This can be found in the Support Documents folder, or online: http://www.xilinx.com/support/documentation/sw_manuals/xilinx2016_2/ug911-vivado-migration.pdf
- For more information on the benefits of UltraFast Design Methodology, please refer to the Xilinx User Guide documents UG949 and UG1046. These can be found in the Support Documents folder or online: http://www.xilinx.com/support/documentation/sw_manuals/ug949-vivado-design-methodology.pdf http://www.xilinx.com/support/documentation/sw_manuals/ug1046-ultrafast-design-methodology-guide.pdf

This concludes Lab 1.

Revision History

Date	Version	Revision
6 Nov 2013	02	Initial Draft
30 Oct 2014	03	Updated to Vivado 2014.3
5 Jan 2015	04	Updated to Vivado 2014.4
06 Mar 2015	05	Final 2014.4 review
19 Mar 2015	06	Minor edits for release
Oct 2015	07	Updated to Vivado 2015.2
July 2016	08	Updated to Vivado 2016.2
May 2017	09	Updated to Vivado 2017.1
June 2017	10	Rebranded/Updated for MiniZed 2017.1
Jan 2018	11	Updated to 2018.1
July 2019	12	Updated to 2019.1

Resources

www.minized.org

www.xilinx.com/zynq

www.xilinx.com/sdk

www.xilinx.com/vivado

www.xilinx.com/support/documentation/sw_manuals/ug949-vivado-design-methodology.pdf

www.xilinx.com/support/documentation/sw_manuals/ug1046-ultrafast-design-methodology-guide.pdf

Answers

Experiment 1

- *What device is selected? Why is there no Top Module?*

For MiniZed it is xc7z007sclg225-1
This is a brand new project, so the top module has not been created yet. We will create it later, and it will appear under *Design Sources*.

- *What are the Vivado Synthesis and Implementation Strategies?*

Both are set to Default. See *Strategy* for each under the **Project Summary**.

Synthesis		Implementation	
Status:	Not started	Status:	Not started
Messages:	No errors or warnings	Messages:	No errors or warnings
Part:	xc7z007sclg225-1	Part:	xc7z007sclg225-1
Strategy:	Vivado Synthesis Defaults	Strategy:	Vivado Implementation Defaults
Report Strategy:	Vivado Synthesis Default Reports	Report Strategy:	Vivado Implementation Default Reports
		Incremental compile:	None

- *What other information is available in the Project Summary?*

Synthesis and Implementation status, DRC violations, timing results, device utilization statistics and power information.

Experiment 2

Answer the following questions:

- *List some configurable components (highlighted green boxes) in the Zynq PS:*

I/O Peripherals, General Settings, Flash Memory Interfaces, Clock Generation, AXI Ports, DDR Memory Controller, and more.

- *The I/O Peripherals are connected to external I/O through the I/O Mux (MIO), how many I/O are available in the MIO?*

32 Total in MiniZed