e-con Systems India Private Ltd

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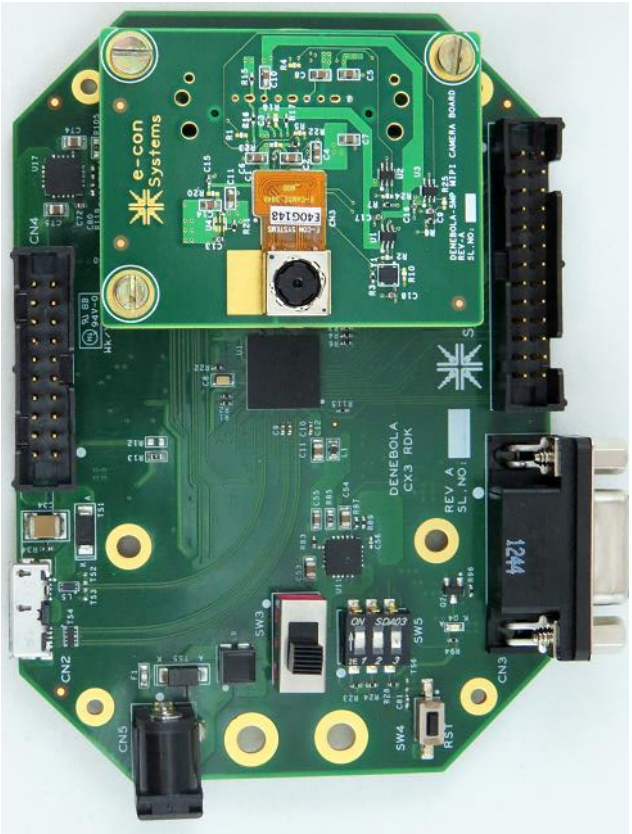
DENEBOLA (See3CAM_CX3RDK) - CX3 Reference Design Kit

Hardware User Manual

Revision 1.1

Oct 10, 2013



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1. INTRODUCTION

Denebola (See3CAM_CX3RDK) is a USB3.0 UVC Reference Design Kit (RDK) developed by e-con Systems using the EZ-USB® CX3 USB3.0 Peripheral controller from Cypress Semiconductors. The Cypress EZ-USB® CX3 is a USB 3.0 peripheral controller that enables developers to add USB 3.0 connectivity to any image sensors compliant with Mobile Industry Processor Interface (MIPI) Camera Serial Interface Type 2 (CSI-2) standard.
The Denebola Reference Design Kit developed using EZ-USB® CX3 is a complete Reference Design Kit and has OmniVision OV5640 CMOS image sensor interfaced to it through 2-lane MIPI CSI-2 interface. This is a fully functional camera reference design kit that can stream uncompressed 720p60, 1080p30 and 5MP@15fps.Denebola RDK is a two-board solution containing base board designed around Cypress CX3 USB3.0 Peripheral controller and the Camera daughter board designed using OmniVision OV5640 CMOS image sensor based Auto focus camera module.

2. SCOPE

This Hardware User Manual document details the hardware features of the Denebola RDK, electrical and mechanical specification and provides detailed information about interfaces available on CX3 RDK.

3. PRE-REQUISITES

This document details the hardware features and information about interfaces available on CX3 RDK. Please refer Cypress documentation for information on CX3 SDK and USB Control center.

4. FEATURES

- Two board solution containing baseboard, based on CX3 and camera daughter board, based on e-CAM52_MI5640_MOD
- Samtec High-speed connector for 4-lane MIPI to support Aptina demo3 image sensor board interface
- OmniVision OV5640 daughter board interfaced through 2-lane MIPI CSI-2 interface
- RS232 level UART port for debugging and other communication
- SPI Flash and I2C EEPROM for firmware storage
- User Configurable GPIOs from the GPIO header
- USB bus powered and also support for external 5V supply
- JTAG interface
- Maximum frame rates for Preview and Capture
  - VGA - 60fps
  - HD(720P) - 60fps
  - Full HD (1080p) - 30fps
  - 5MP (2592x1944) - 15fps
  - Preview format: YUV422 (16bits per pixel)

- Still Image Capture
  - 5MP (2592x1944) resolution
  - YUV422 (16 Bits per pixel) format

5. BLOCK DIAGRAM

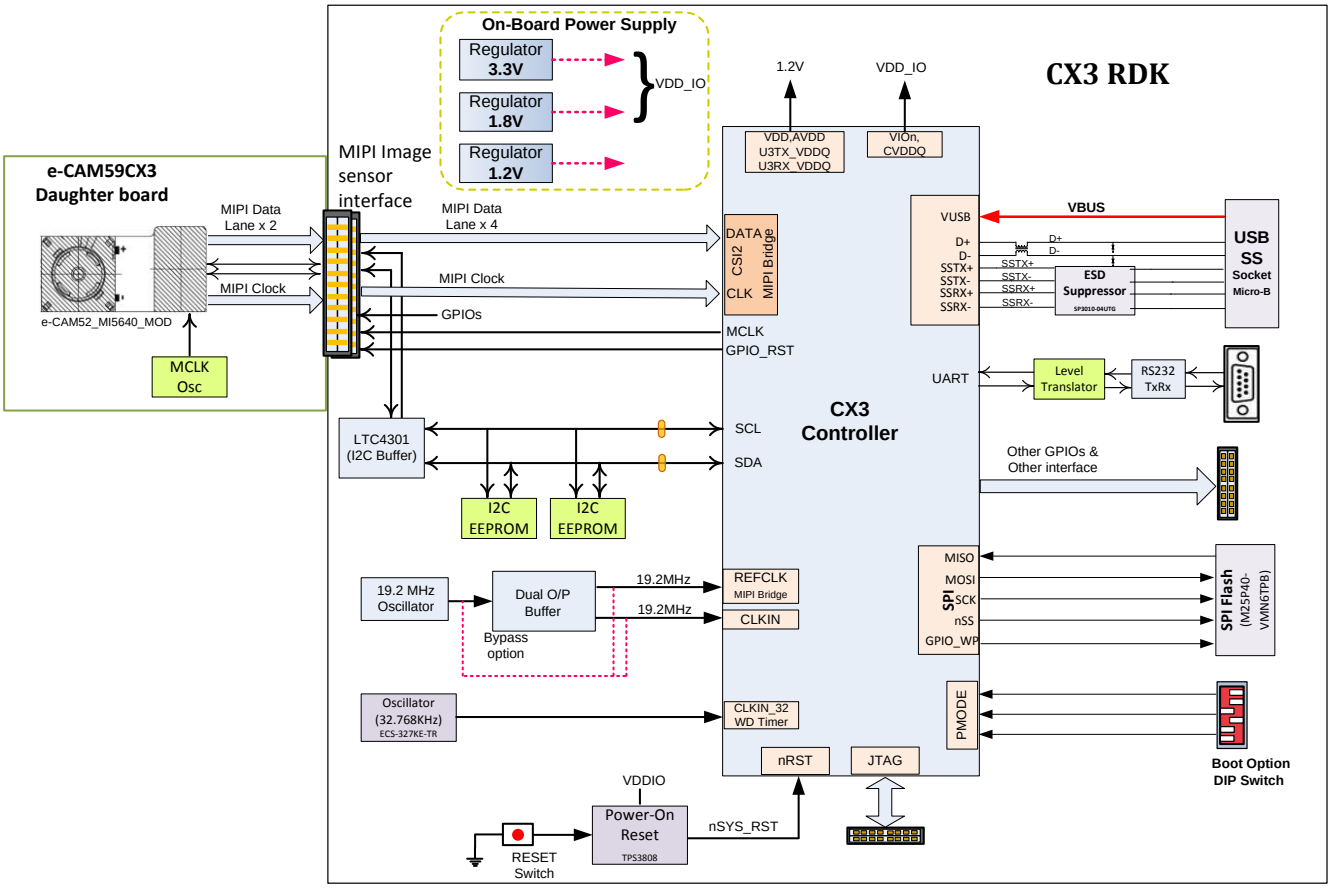


Figure 5.1:CX3RDK Functional Block Diagram

6. DENEBOLA CX3 RDK

6.1 BASE BOARD

TOP:

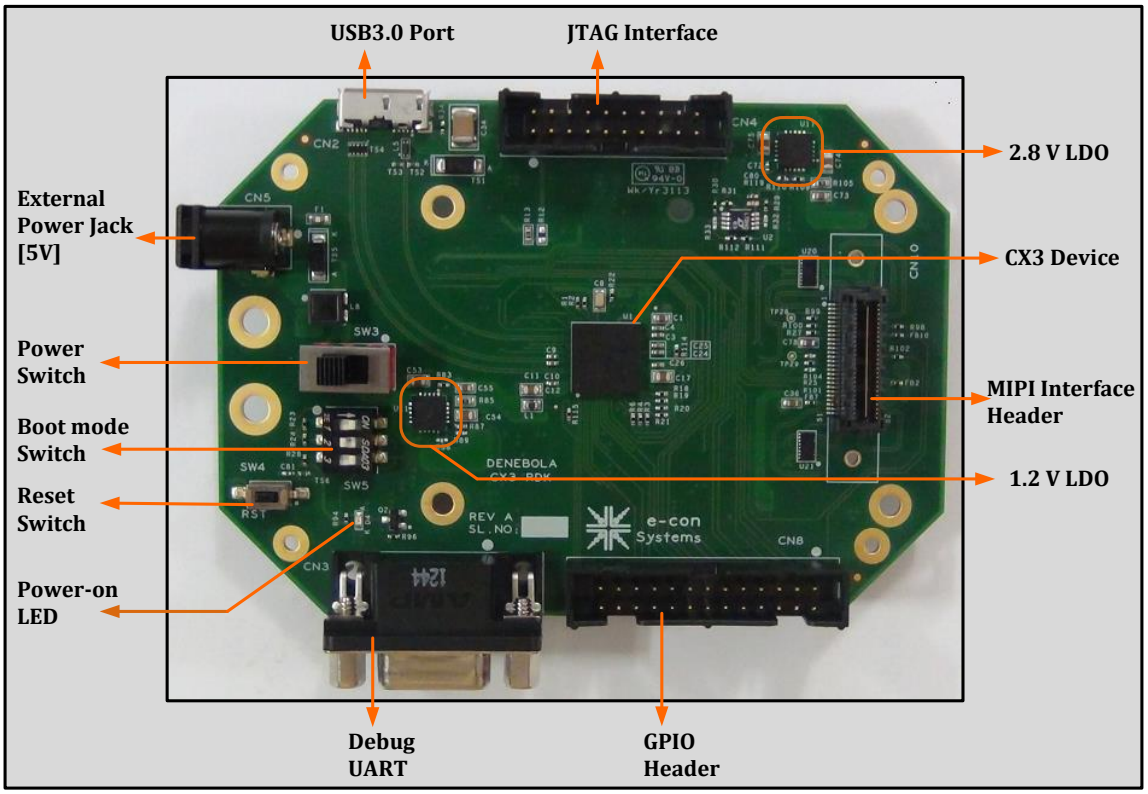


Figure 6.1:CX3 RDK Base Board-Top View

BOTTOM:

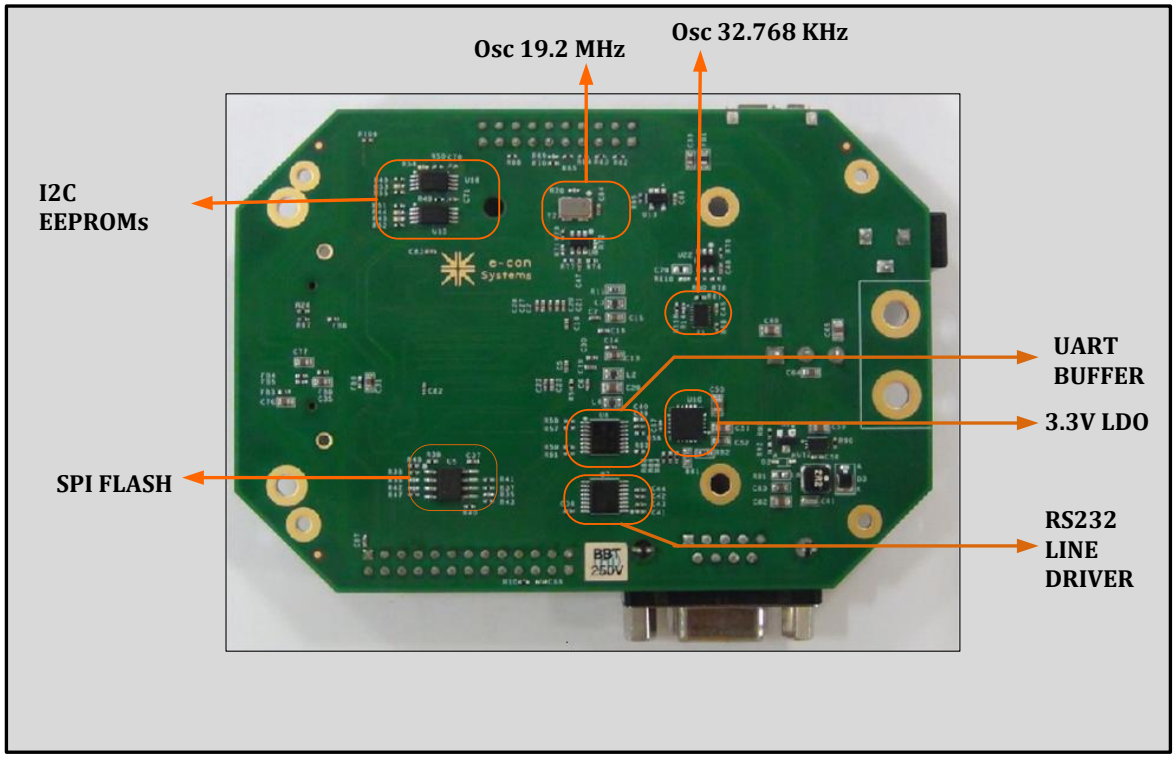


Figure 6.2:CX3 RDK Base Board- Bottom View

6.2 DENEBOLA CX3 RDK SETUP:

DENEBOLA kit consists of two boards to demonstrate the CX3- 5MP MIPI Camera .

- EZ-USB CX3 Reference Design Kit (CX3 RDK) Base Board
- OV5640 sensor daughter board : e-CAM59CX3

The CX3 RDK by default comes with OV5640 daughter board fixed on CX3 RDK base board. The CX3 RDK setup is shown in below Figure6.3.

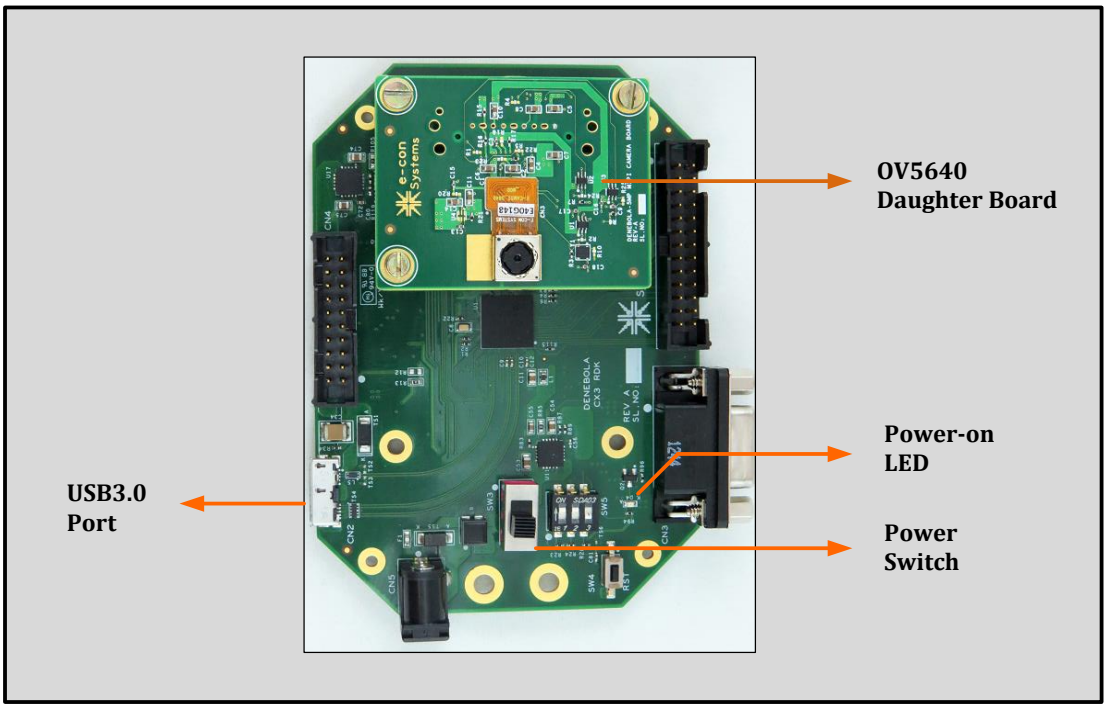


Figure 6.3:CX3 RDK Setup

The details about connecting the Image sensor daughter board with CX3 RDK base board is shown below.

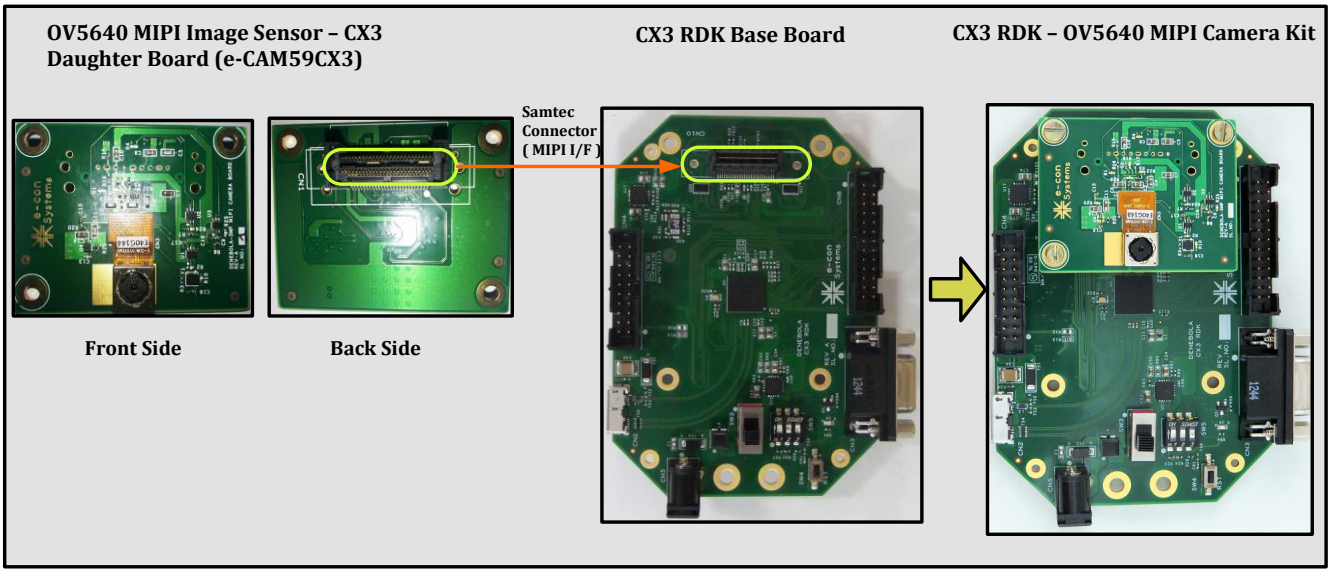


Figure 6.4:CX3 RDK Board Interface

7. ELECTRICAL SPECIFICATION

The CX3 RDK board can be powered in two ways:

- Self power: Use the external DC 5V, 1A power adapter (not supplied with the RDK).
- Bus power: The board can be powered using the USB 3.0 cable by connecting to USB Host.

The recommended DC operating supply voltage specification

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
VBUS / VCC_5V	USB 3.0 Cable Bus Power / External 5V power Adaptor	4.75	5	5.25	V

Table 7.1: Recommended Operating Voltage

8. BOARD SPECIFICATION

8.1 USB3.0 CONNECTOR (CN2)

A standard USB3.0 Micro B receptacle is used in CX3_RDK. The part number is Hirose's ZX360D-B-10P. The USB 3.0 pins (SS_TX_M, SS_TX_P, SS_RX_P, and SS_RX_M) and USB 2.0 pins (OTG_ID, D+, and D–) with power (VBUS and GND) are available on the CN2 USB3.0 receptacle. CX3 is capable of operating in Super-Speed, High-speed and Full speed protocols.

The USB3.0 and USB2.0 lines go through an ESD protection device for additional ESD protection. The CX3 RDK board can be bus-powered using VBUS pin on the connector.

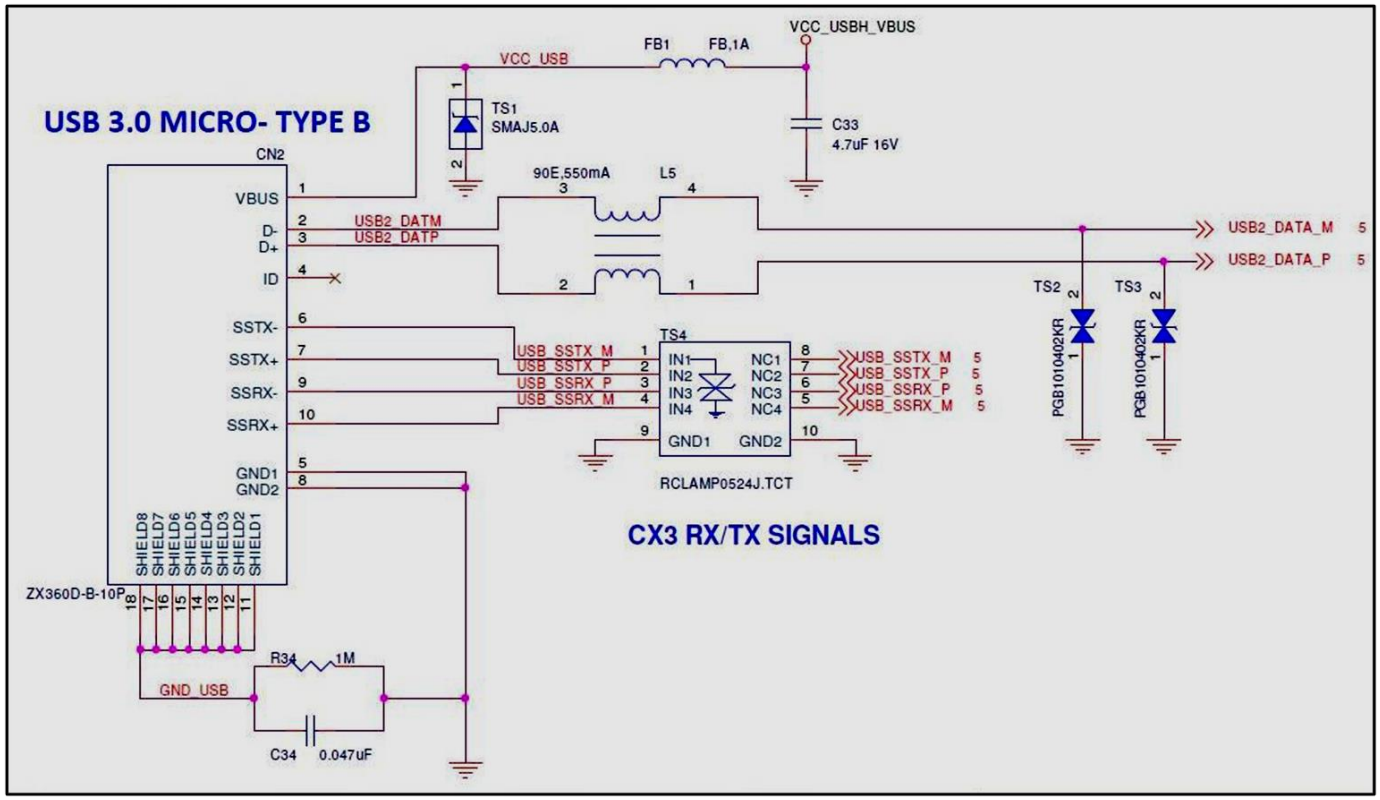
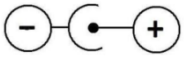


Figure 8.1: CX3 RDK USB3.0 Circuit

8.2 POWER JACK (CN5)

The CX3 RDK board can be powered in two ways:



- Self power: Use the external DC 5V, 1A power adapter (not supplied with the RDK).
- Bus power: The board can be powered using the USB 3.0 cable by connecting to PC Host

The Slide switch SW3 is provided for power selection from either of the above sources, as explained in the below table and figure.

SW3 POSITION	POWERED THROUGH
1	USB RECEPTACLE (CN2) – Bus Powered
2	5V DC JACK (CN5) – Self Powered

Table 8.1: SW3 Settings

The green LED, D4 glows when the board is powered–on.

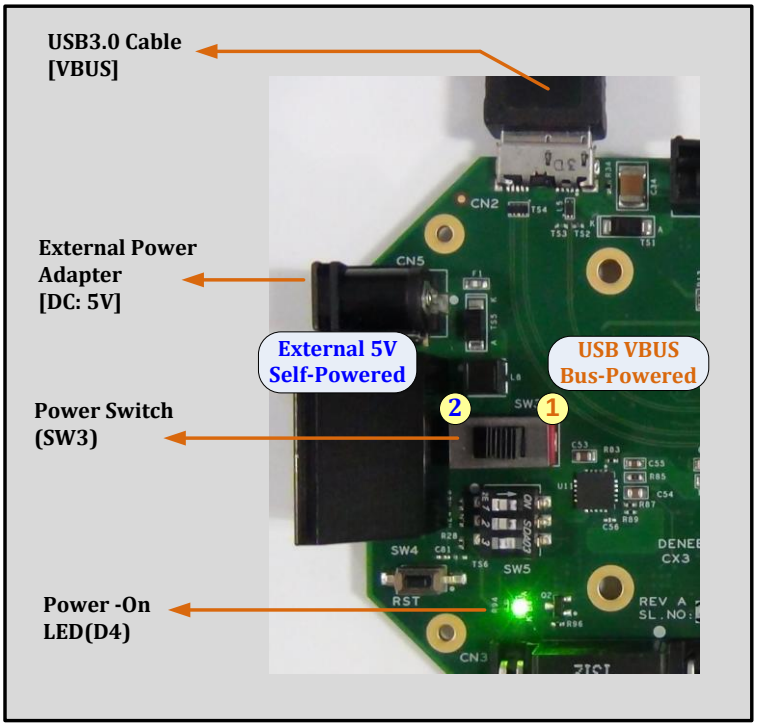


Figure 8.2: Power-On Switch Configuration

8.3 MIPI CSI-2 RX INTERFACE (CN10)

The 4-lane MIPI CSI-2 interface from CX3 is routed to Samtec High-speed interface connector (CN10). The OmniVision OV5640 sensor based daughter board designed to plug with this connector. The daughter board image data communication occurs through 2-lane MIPI CSI-2 interface.
This connector (CN10) interface is also compatible with Aptina DEMO3 Sensor Head Board interface.

The I2C lines, few GPIOs from CX3 and power supplies (1.8V, 2.8V and 3.3V) are also terminated in CN10 to support Image Sensor daughter board Interface.

The following figure shows the high-speed interface connector.

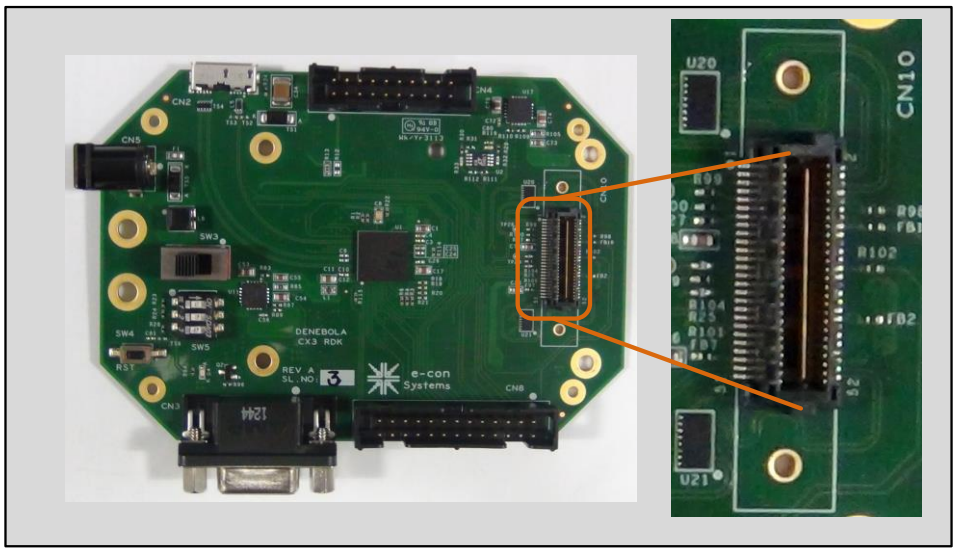


Figure 8.3:MIPI Interface Connector

The Pin-out of MIPI Interface Connector (CN10) provided below in Table 8.2.

CN10 PIN NO	SIGNAL NAME	DESCRIPTION		CN10 PIN NO	SIGNAL NAME	DESCRIPTION
1	MIPI_DAT1+	MIPI Data Lane 1 Differential Pair +		2	MIPI_DAT2+	MIPI Data Lane2 Differential Pair +
3	MIPI_DAT1-	MIPI Data Lane 1 Differential Pair -		4	MIPI_DAT2-	MIPI Data Lane2 Differential Pair -
5	CLK_OUT	Clock from camera head board		6	MIPI_DAT3+	MIPI Data Lane3 Differential Pair +
7	NC	-		8	MIPI_DAT3-	MIPI Data Lane3 Differential Pair -
9	**CX3_GPIO23****	General purpose IO '23' from CX3		10	GND	Ground
11	CX3_GPIO44	General purpose IO '44' from CX3		12	**CX3_GPIO18****	General purpose IO '18' from CX3
13	GND	Ground		14	**CX3_GPIO24****	General purpose IO '24' from CX3
15	VDDIO_OUT	IO voltage of head/Daughter board		16	NC	-
17	NC	-		18	NC	-
19	NC	-		20	NC	-
21	NC	-		22	NC	-
23	NC	-		24	NC	-
25	NC	-		26	MIPI_CAM_PWDN	CX3 GPIO from base board
27	NC	-		28	NC	-
29	NC	-		30	NC	-
31	MIPI_CAM_RST	Image sensor reset from CX3 MIPI bridge		32	NC	-

CN10 PIN NO	SIGNAL NAME	DESCRIPTION		CN10 PIN NO	SIGNAL NAME	DESCRIPTION
33	NC	-		34	NC	-
35	NC	-		36	NC	-
37	CAM_I2C_SDA	Serial Data line of I2C from Base board		38	VCC2P8	2.8 V from base board
39	VCC_SYS	5V from base board		40	NC	-
41	NC	-		42	VCC1P8	1.8 V from base board
43	CAM_I2C_SCL	Serial Clock line of I2C from Base board		44	CLKM_CX3	Bridge clock output to image sensor clock input
45	NC	-		46	VCC1P2	1.2 V from base board
47	VCC_VIO4	3.3 V from base board		48	VCC2P8	2.8 V from base board
49	MIPI_DAT0+	MIPI Data Lane 0 Differential Pair +		50	MIPI_CLK-	MIPI Clock lane Differential Pair -
51	MIPI_DAT0-	MIPI Data Lane 0 Differential Pair -		52	MIPI_CLK+	MIPI Clock lane Differential Pair +

Table 8.2:MIPI Connector Pin-out

**Highlighted GPIOs are shared in both MIPI (CN10) and GPIO Header (CN8)

8.4 GPIO EXPANSION HEADER (CN8)

The expansion header (CN8) hosts the GPIO lines apart from SPI, I2C signals and CX3 interrupt signal. The same SPI interface used for on-board Flash memory terminated here. The 0 ohms series resistor option is provided in schematics, in case to isolate these signals from on-board SPI Flash chip. By default CX3 RDK settings, all the below GPIOs are 3.3V IO logic.

The pin out of GPIO Expansion Header (CN8)is shown below.

CN8 PIN NO	SIGNAL NAME	DESCRIPTION		CN8 PIN NO	SIGNAL NAME	DESCRIPTION
1	VCC_SYS	DC 5V from RDK Base Board		2	CX3_GPIO17	General purpose IO from CX3
3	GND	Ground		4	**CX3_GPIO18****	General purpose IO from CX3
5	CX3_SPI_MISO	SPI's MISO input to CX3 from slave device		6	CX3_GPIO19	General purpose IO from CX3
7	CX3_SPI_SSN	SPI's SSN from CX3		8	CX3_GPIO20	General purpose IO from CX3
9	CX3_SPI_MOSI	SPI's MOSI output from CX3 as master		10	CX3_GPIO21	General purpose IO from CX3
11	CX3_SPI_SCK	SPI clock from CX3		12	CX3_GPIO22	General purpose IO from CX3
13	CX3_GPIO26	General purpose IO from CX3		14	**CX3_GPIO23****	General purpose IO from CX3

CN8 PIN NO	SIGNAL NAME	DESCRIPTION		CN8 PIN NO	SIGNAL NAME	DESCRIPTION
15	CX3_GPIO57	General purpose IO from CX3		16	**CX3_GPIO24****	General purpose IO from CX3
17	CX3_GPIO52	General purpose IO from CX3		18	CX3_GPIO25	General purpose IO from CX3
19	CX3_GPIO50	General purpose IO from CX3		20	nINT_CX3	Active low interrupt input to CX3
21	CX3_GPIO51	General purpose IO from CX3		22	VCCIO	Base Board IO voltage
23	CAM_CX3_I2C_SCL	I2C's Serial clock		24	CAM_CX3_I2C_SDA	I2C's Serial data
25	GND	Ground		26	GND	Ground

Table 8.3: Expansion Header Pin-out

**Highlighted GPIOs are shared in both MIPI (CN10) and GPIO Header (CN8).

8.5 RS232-DB9 CONNECTOR (CN3)

The 4-wire UART signals (TX, RX, RTS and CTS) from CX3, level translated to RS232 level are terminated in DB9 connector. This RS232 port can be used as debug port by connecting to PC.

8.6 JTAG HEADER (CN4)

CX3's JTAG interface provides a standard five-pin interface for connecting to a JTAG debugger. The JTAG circuit on RDK board provides an option to debug the firmware through the CPU core's on-chip debug circuitry. The CX3 RDK board provides a 20 pin connector (CN4) for JTAG debugger that encompasses the standard JTAG interface signals.
For details on how to perform JTAG configuration and debugging, refer Cypress FX3/CX3 programmers manual. The document can be downloaded from the SDK webpage. The following figure shows the circuit diagram of schematic connections.

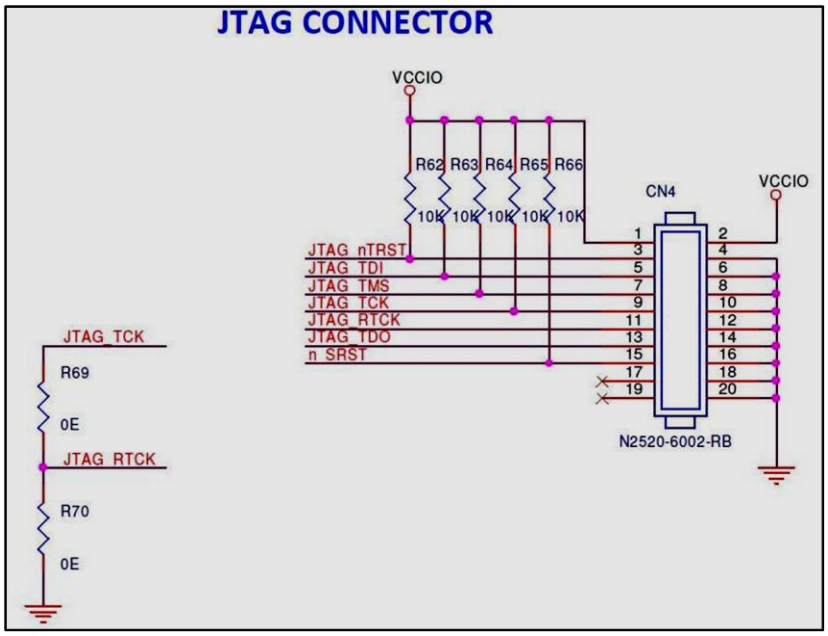


Figure 8.4: JTAG Connections Circuit Diagram

8.7 BOOT MODE SWITCH (SW5)

The EZ-USB CX3 RDK provides several booting options i.e the firmware to be loaded on CX3 can be selected from various available sources.
The boot option is determined by the PMODE[2:0] input pins. The PMODE[2:0] pins can be configured using combination of 3 positions SPST switch, SW5.

The RDK board is designed with combination of appropriate resistors and SPST Switch (SW5) for hassle-free boot mode settings as shown in the circuit diagram in Figure 8.5.

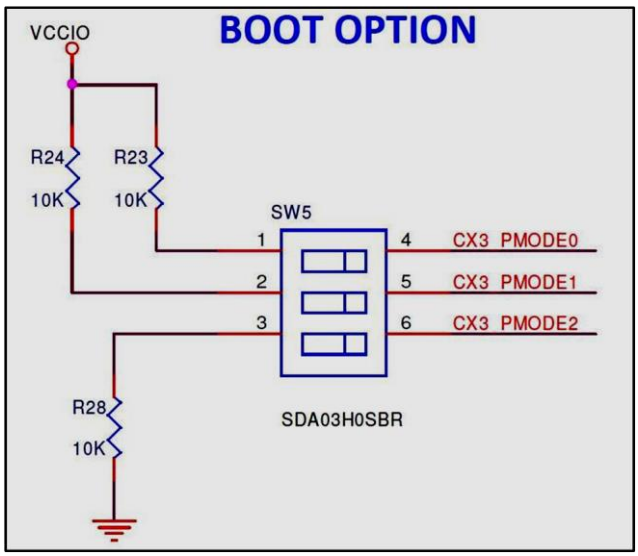


Figure 8.5:Boot Option Circuit diagram

Table-8.4 provides the list of boot interfaces supported on the CX3 device for corresponding PMODE[2:0] pins configuration.

PMODE2	PMODE1	PMODE0	BOOT MODE
Float	1	1	USB
Float	1	Float	I2C, with USB fallback
0	Float	1	SPI, with USB fallback

Table 8.4: Boot Mode Settings

The below Figure-8.6 shows the PMODE switch (SW5) of RDK board. Move SW5 to **'ON'** position for 0 and 1 PMODE configuration, and 'OFF' position for float configuration.

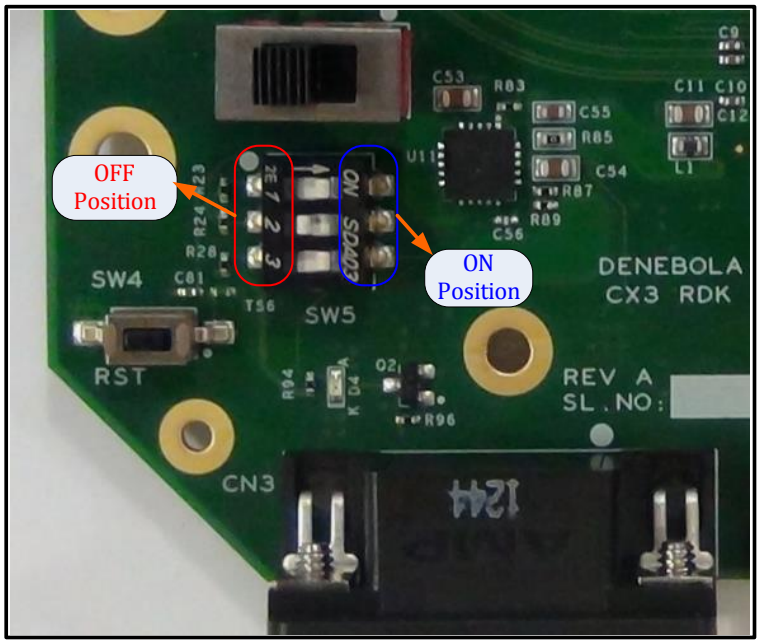


Figure 8.6:CX3 RDK's Boot mode Switch

8.7.1 USB BOOT:

In this mode, the firmware image is downloaded into CX3's RAM through the USB host. The CX3RDK board boots in USB mode if PMODE[2:0] pins are set as[Z11] .The board is by default set to PMODE[2:0]=[0Z1] (**SPI Boot**).

NOTE: Z indicates high impedance state (Float).

DOWNLOADINGFIRMWARE IMAGE TO CX3 RAM:

Follow the procedure outlined here to download the firmware image to CX3 RAM.

1. Enable USB boot, by setting the PMODE[2:0] pins to Z11as shown in the following table.

PMODE PINS	REQUIRED STATE	SW5 - SETTINGS
PMODE0	1	Set to SW5.4(ON position)
PMODE1	1	Set to SW5.5(ON position)
PMODE2	FLOAT	Set to SW5.3(OFF position)

Table 8.5: USB Boot Mode Settings

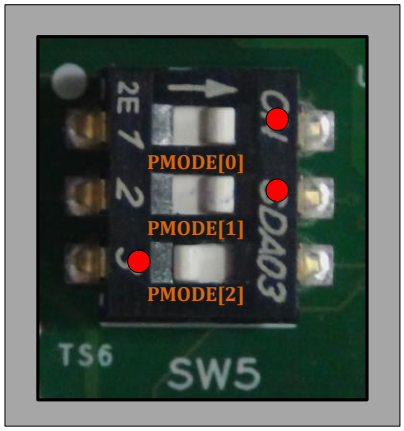


Figure 8.7:USB Boot Mode Settings

2. When connected to a USB host, the CX3 device enumerates in Cypress **USB Control Center**##as "Cypress USBBootloader".
3. In Control Center, select **Program →FX3→ RAM**.
4. Browse to the firmware image (.img) path to be programmed into the CX3 RAM. Double-click on the ".img " file.
5. A"**Programming Succeeded**" message is displayed on the bottom left pane of the Control Center and the CX3 device re-enumerates with the programmed firmware.

##-Refer Cypress Documentation for the information on **USB Control center** from cypress website.

8.7.2 I2C BOOT:

In this mode, the firmware image is downloaded into an external I2C EEPROM and on reset, the bootloader executes the firmware over I2C.The board boots from EEPROM if PMODE [2:0] are set as [Z1Z].

DOWNLOADING FIRMWARE IMAGE TO I2C EEPROM:

Follow the procedure outlined here to download the firmware image to I2C EEPROM:

1. Enable USB boot, by setting the PMODE[2:0] pins to Z11 as shown in Table-8.5.
2. Connect the RDK to a PC host using the USB 3.0 cable. The CX3 device enumerates in Control Center as "Cypress USB Bootloader".
3. Select the CX3 device and choose **Program →FX3 →I2C EEPROM**. CX3 device re-enumerates as **"Cypress USB BootProgrammer".**
4. Browse to the relevantfirmware binary to be loaded upon EEPROM, once the control center prompts for.
   NOTE: Before downloading, verify the firmware and EEPROM size and also ensure that the address signals of the EEPROM are configured correctly.
5. The bottom left corner of the window displays "Programming of I2C E2PROM Succeeded" once programming completed.

BOOTING FROM I2C EEPROM:

Change the PMODE[2:0] pins on the CX3_RDK board to Z1Z, to enable I2C boot, as in below table 8.6.This is realized by moving the appropriate buttons on SW5.Press RESET button SW4.The CX3_RDK board re-enumerates with the boot image in I2C EEPROM.

PMODE PINS	REQUIRED STATE	SW5- SETTINGS
PMODE0	FLOAT	Set to SW5.1 (OFF position)
PMODE1	1	Set to SW5.5 (ON position)
PMODE2	FLOAT	Set to SW5.3(OFF position)

Table 8.6: I2C Boot Mode Settings

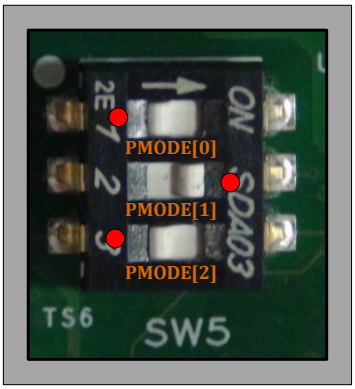


Figure 8.8:I2C Boot Mode Settings

I2C EEPROM CONFIGURATION:

The typical EEPROM consists of three address lines A2, A1 and A0. CX3 RDK can address eight address lines (000-111). If the firmware image size is less than the EEPROM size, then the corresponding address lines can be pulled low/high. If the firmware size exceeds the EEPROM size, multiple EEPROMs can be cascaded with sequential address lines assigned to them. The address selection can be done by mounting appropriate resistors on the address input pins.

CX3 RDK utilizes the ATMEL's, AT24CM01 EEPROM for storing the firmware image. Atmel EEPROMs use A2 and A1 for chip select and A0 is unused. Hence a maximum of four EEPROM devices can be interfaced for firmware storage. In this RDK, two EEPROMs, U15 and U16 are interfaced and its address lines fixed in schematics.

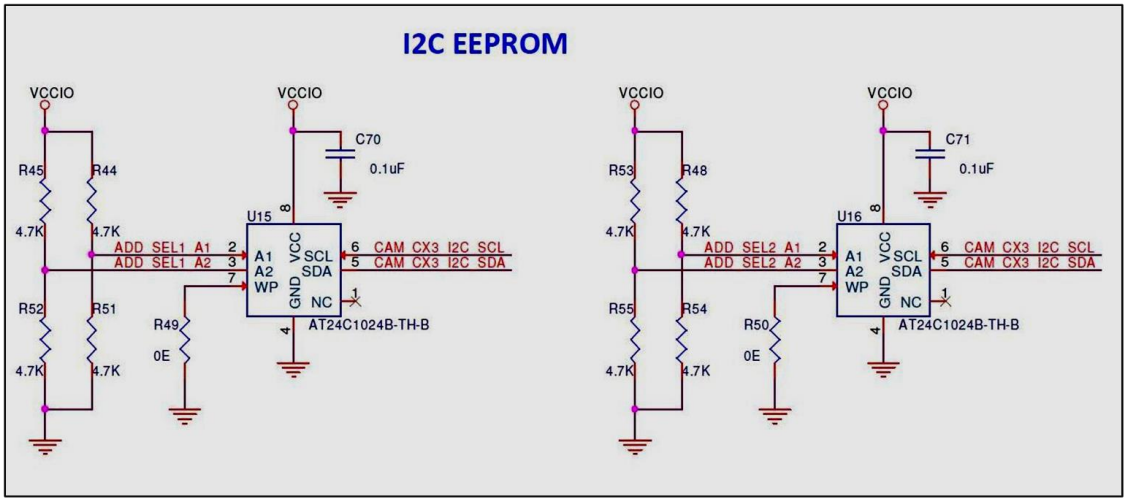


Figure 8.9: CX3 RDK I2C EEPROM Circuit

About AT24CM01:
AT24CM01 is an I2C compatible EEPROM. Its features include,

PROPERTY	VALUE
Memory	1Mbit (131,072X8)
Clock Frequency, SCL	1000 KHz (max)

Table 8.7: AT24CM01 specifications

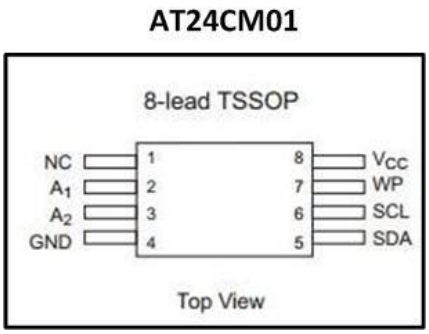


Figure 8.10:ATMEL's AT24C1024BPinout

The address range are indicated in the below Table-8.8.

DEVICE NO	ADDRESS RANGE	A2	A1	A0	SIZE
1	0x00000 – 0x1FFFF	0	0	NC	128 KB
2	0x20000 – 0x3FFFF	0	1	NC	128 KB

Table 8.8: EEPROM ADDRESS RANGE

NOTE: NC- No Connection

8.7.3 SPI BOOT:

CX3 boots from SPI Flash/EEPROM devices through a 4-wire SPI interface. CX3's firmware image is programmed into an external SPI Flash or SPI EEPROM. And on reset, CX3's bootloader executes the firmware over SPI. The SPI Flash/EEPROM devices from 1 Kbit to 32 Mbit in size are supported for boot.

In this mode, the firmware image is downloaded into an external SPI Flash and on reset, the bootloader downloads the firmware over SPI. The board boots from Flash if PMODE [2:0] are set as [0Z1].

DOWNLOADING FIRMWARE IMAGE TO SPI FLASH:

Follow the below steps to download the firmware into FLASH.

1. Enable **USB boot** by setting the PMODE[2:0] pins to Z11 as shown in Table-8.5.
2. Connect the RDK toa PC host using the USB 3.0 cable. The CX3device enumerates in Control Center as "Cypress USB Bootloader".
3. Select the CX3 device and choose **PROGRAM → FX3 → SPI FLASH** from Control center menu. The CX3_RDK board re-enumerates again as **"Cypress USB BootProgrammer**".
4. Browse to the relevant firmware binary (.img) and select the image, once the control center prompts for.

5. The application then starts downloading the firmware to the flash memory. The bottom left corner of the window displays "Programming of SPI FLASH Succeeded" once programming completed.

BOOTING FROM SPI FLASH:

After the firmware is programmed onto the SPI flash, change PMODE[2:0] pins to 0Z1.On the CX3_RDK board, this is done by configuring as shown in below table 8.9.

PMODE PINS	REQUIRED STATE	SW5- SETTINGS
PMODE0	1	SET TO SW5.4 (ON position)
PMODE1	FLOAT	SET TO SW5.2 (OFF position)
PMODE2	0	SET TO SW5.6 (ON position)

Table 8.9:SPI Boot Mode Settings

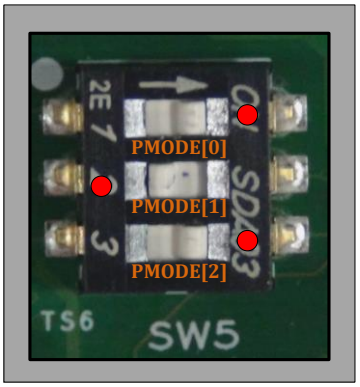


Figure 8.11:SPI Boot Mode Settings

ABOUT CX3_RDK'S SPI FLASH:

The on-board flash in CX3_RDK is Micron's M25P40-VMN6TPB.It has 4MB of flash memory and is SPI serial bus compatible. It has Write protect and hold pins that are hardware configurable. Options are fixed for these pins on CX3 RDK schematics.

8.8 CLOCK SCHEME OF CX3 RDK:

The EZUSB-CX3 controller requires two clocks for normal operation.

- 19.2MHZ clock for "Clock Input".
- 19.2 MHZ clock as reference clock.

Also a **32.768 KHz** clock is required for watchdog timer.The on-board 19.2MHz clock is provided as input for both clock input and reference. Table 8.10 provides the pin-out along with clock frequencies applied.

CX3 PIN NO	FUNCTION	FREQUENCY
D6	CLKIN_32	32.768 KHZ
F2	REFCLK	19.2 MHZ.
D7	CLKIN	19.2 MHZ.

Table 8.10: CLOCK SIGNALS

The following table lists the oscillator components on CX3_RDK.

CLOCK FREQUENCY	PART REFERENCE	MANUFACTURING PART NO
19.2 MHz	Y2	KC5032A19.2000CM0E00
32.768KHz	Y1	SG-3030LC 32.7680KB3: PURE SN

Table 8.11:CX3 RDK Clock

8.9 RESET SCHEME OF CX3 RDK:

Reset for EZUSB-CX3 controller

A supervisory IC from TI, TPS3808G01 (on board **U22**) is employed, that asserts an active low reset to CX3when either the SENSE or MR pins of the IC, falls below the threshold voltage. The on-board push button SW4 connected to MR (Manual Reset) pin of TPS3808.

External image sensor can be reset through XRST (PIN F4) of CX3 controller. The reset signal for image sensor is available on Pin 31 of MIPI Camera board connector (CN10).

9. MECHANICAL SPECIFICATION:

The mechanical dimensions of CX3 RDK is shown in below figure.
Note: All dimensions are in '**mm**'.

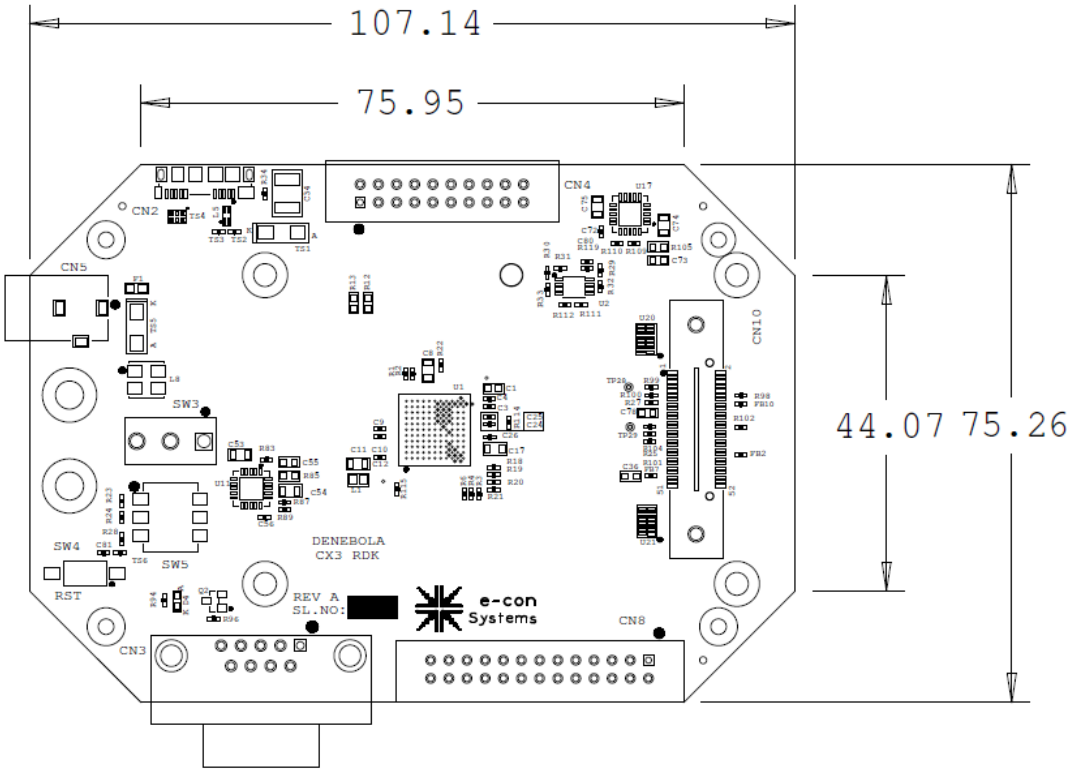


Figure 9.1: CX3 RDK Mechanical Dimension

10. ASSEMBLY DRAWING:

Following figures display, the top and bottom assembly drawings of CX3_RDK.

10.1 ASSEMBLY TOP:

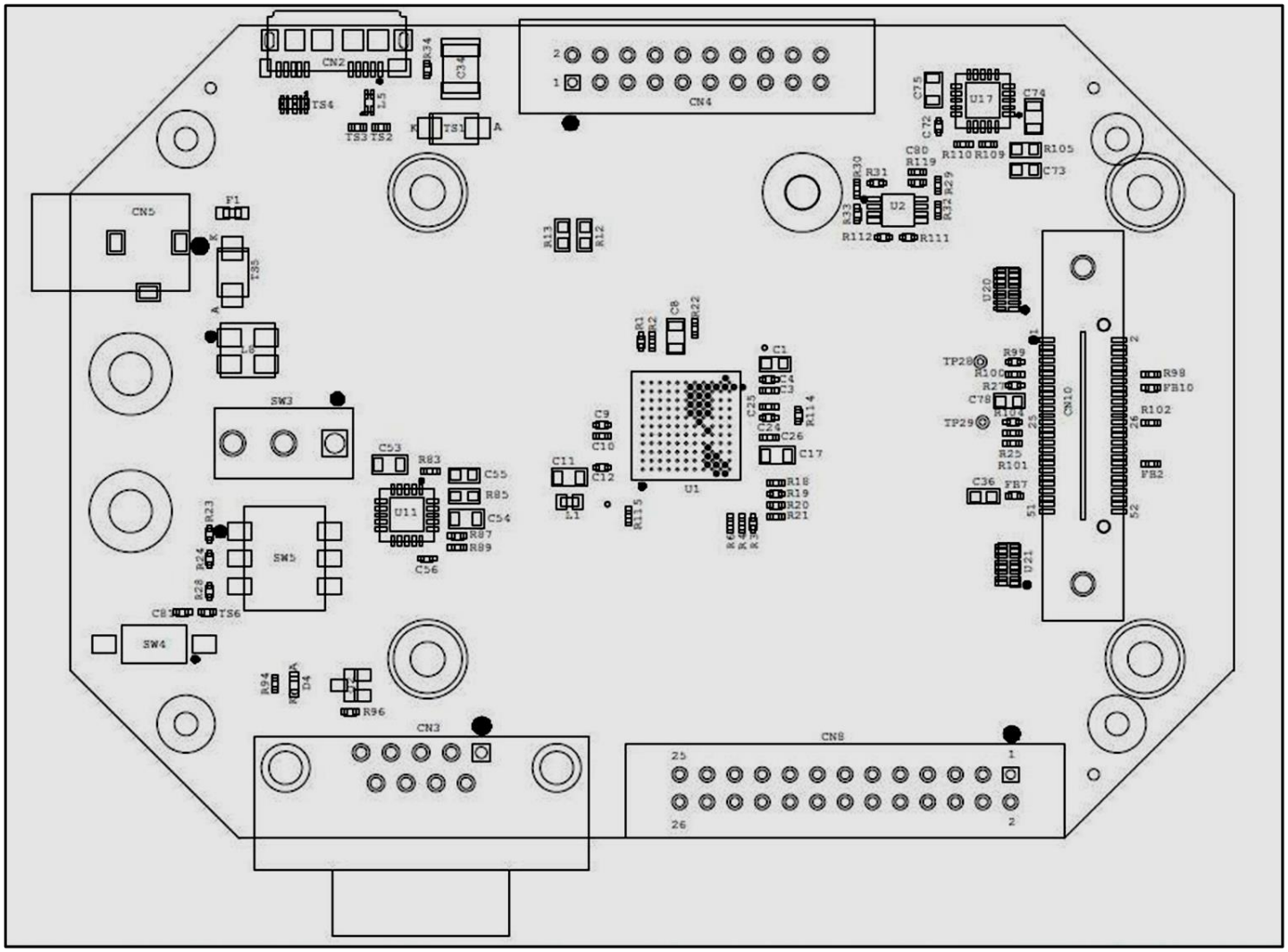


Figure 10.1: CX3 RDK- Assembly Top

10.2 ASSEMBLY BOTTOM:

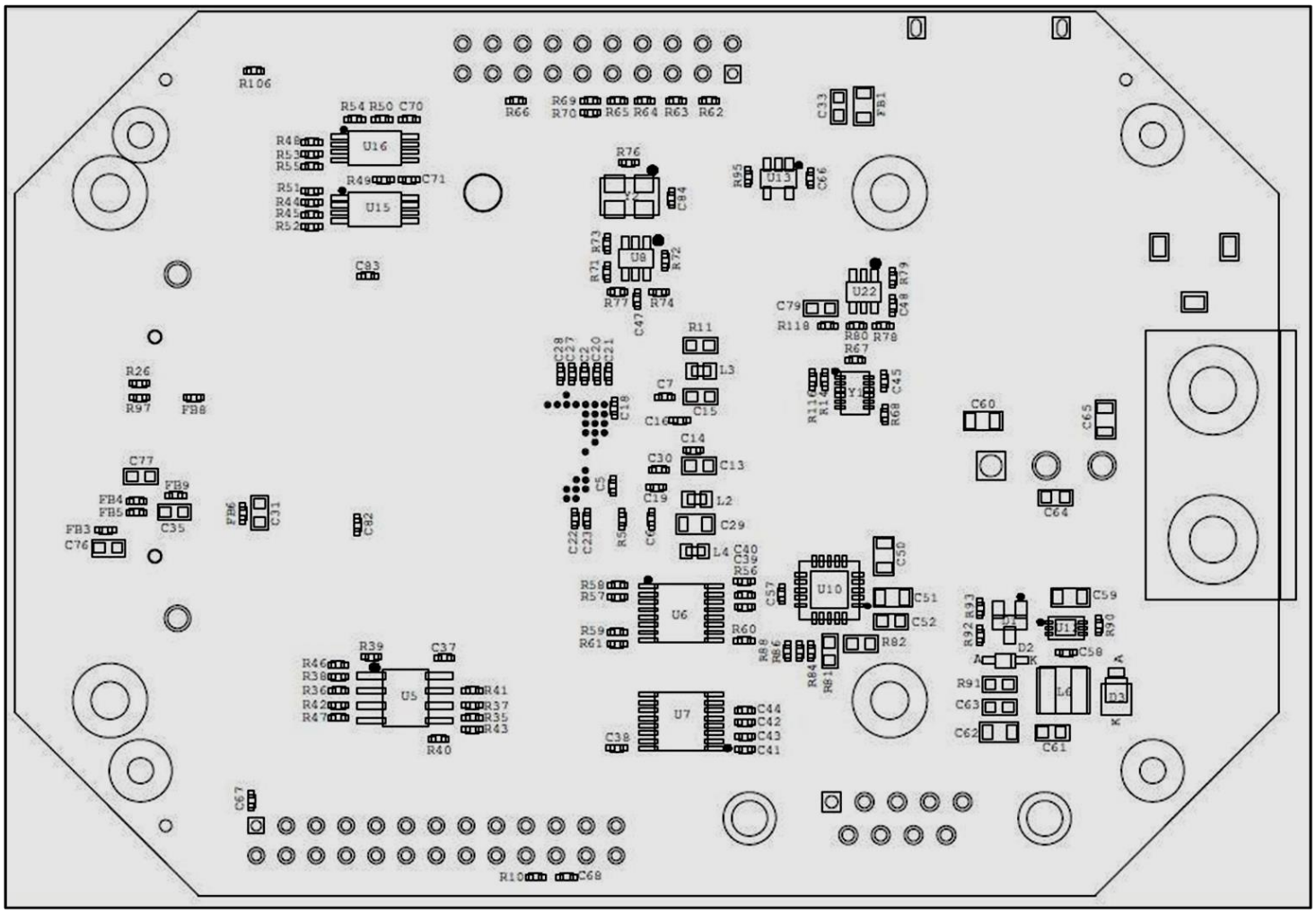


Figure 10.2: CX3 RDK- Assembly Bottom

10. LEARN MORE AT:

- Visit www.cypress.com/cx3 for additional learning resources in the form of data sheets, technical reference manual and application notes.
- Visit http://www.e-consystems.com/CX3-Reference-Design-Kit.asp for the latest information about this kit and its documentation