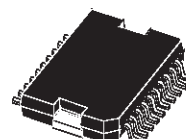


TWO-PHASE STEPPER MOTOR DRIVER

- 2 X 1.1A FULL BRIDGE OUTPUTS
- INTEGRATED CHOPPING CURRENT REGULATION
- MINIMIZED POWER DISSIPATION DURING FLYBACK
- OUTPUT STAGES WITH CONTROLLED OUTPUT VOLTAGE SLOPES TO REDUCE ELECTROMAGNETIC RADIATION
- SHORT-CIRCUIT PROTECTION OF ALL OUTPUTS
- ERROR-FLAG FOR OVERLOAD, OPEN LOAD AND OVERTEMPERATURE PREALARM
- DELAYED CHANNEL SWITCH-ON TO REDUCE PEAK CURRENTS
- MAX. OPERATING SUPPLY VOLTAGE 24V
- STANDBY CONSUMPTION TYPICALLY 40µA
- SERIAL INTERFACE (SPI)



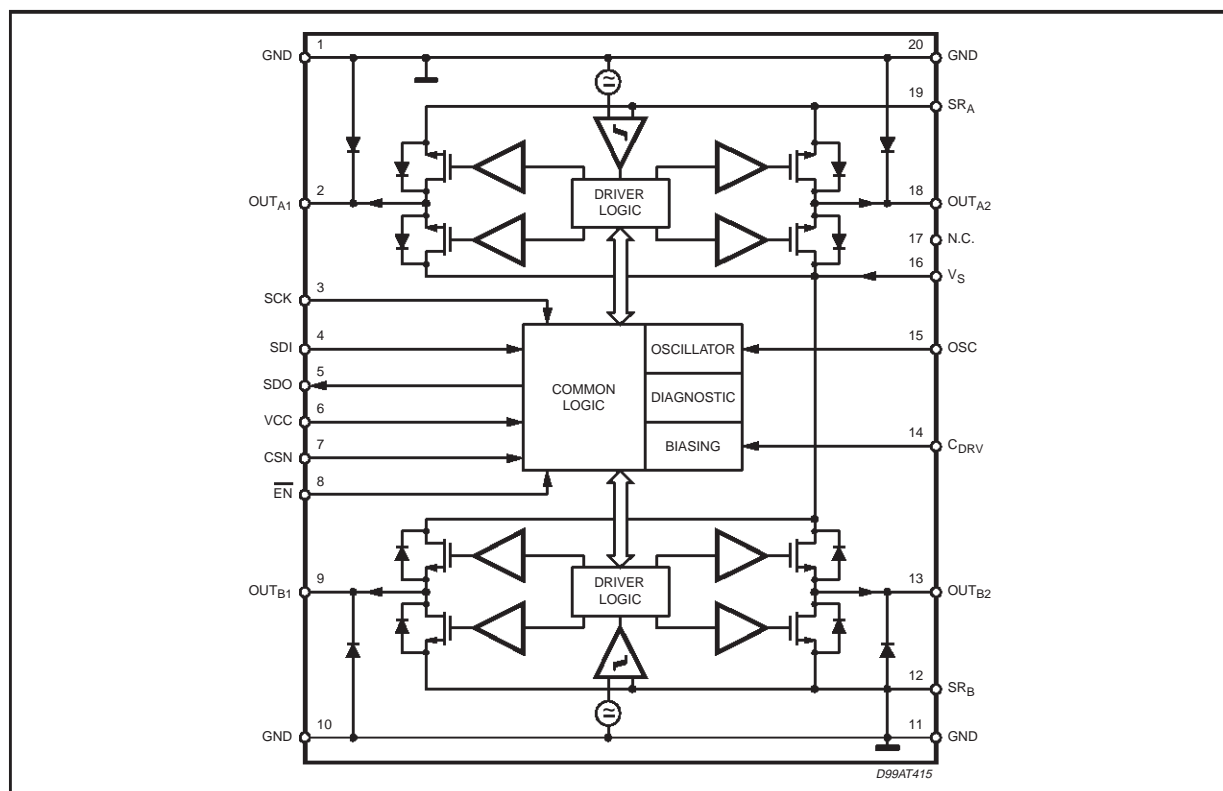
PowerSO20

ORDERING NUMBER: L9935

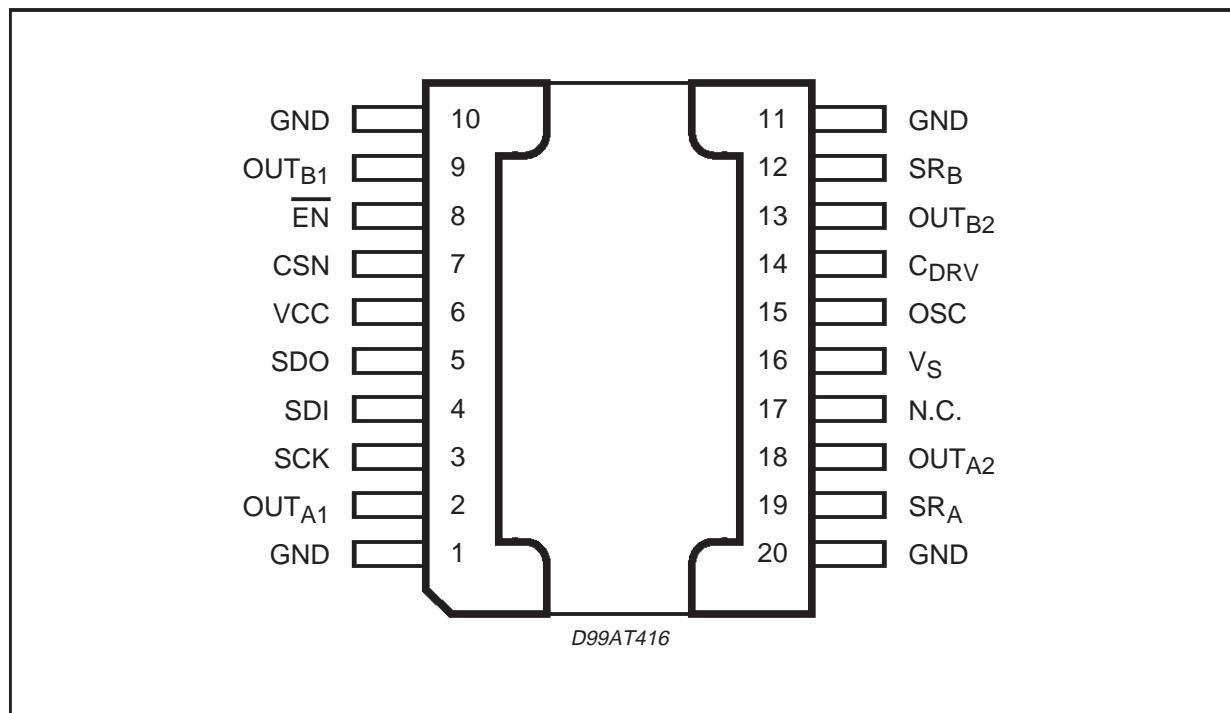
DESCRIPTION

The L9935 is a two-phase stepper motor driver circuit suited to drive bipolar stepper motors. The device can be controlled by a serial interface (SPI). All protections required to design a well protected system (short-circuit, overtemperature, cross conduction etc.) are integrated.

BLOCK DIAGRAM



PIN CONNECTION



PIN FUNCTIONS

Pin N°	Name	Description
1,10,11,20	GND	Ground. (All ground pins are internally connected to the frame of the device).
2	OUT _{A1}	Output 1 of full bridge 1
3	SCK	Clock for serial interface (SPI)
4	SDI	Serial data input
5	SDO	Serial data output
6	VCC	5V logic supply voltage
7	CSN	Chip select (Low active)
8	$\overline{\text{EN}}$	Enable (Low active)
9	OUT _{B1}	Output 1 of full bridge 2
12	SR _B	Current sense resistor of the chopper regulator for OUT _B
13	OUT _{B2}	Output 2 of full bridge 2
14	C _{DRV}	Charge pump buffer capacitor
15	OSC	Oscillator capacitor or external clock
16	V _S	Supply voltage
17	NC	Not connected
18	OUT _{A2}	Output of full bridge 1
19	SR _A	Current sense resistor of the chopper regulator for OUT _A

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	DC Supply Voltage	-0.3 to 35	V
$V_{SPulsed}$	Pulsed supply voltage $T < 400ms$	-0.3 to 40	V
$V_{OUT (Ai/Bi)}$	Output Voltages	internally clamped to V_S or GND depending on the current direction	
$I_{OUT (Ai/Bi)}$	DC Output Currents Peak Output Currents ($T/tp \geq 10$)	± 1.2 ± 2.5	A A
$V_{SRA/SRB}$	Sense Resistor Voltages	-0.3 to 6.2	V
V_{CC}	Logic Supply Voltages	-0.3 to 6.2	V
V_{CDRV}	Charge Pump Buffer Voltage versus V_S	-0.3 to 10	V
$V_{SCK}, V_{SDI}, V_{CSN}, V_{EN}$	Logic Input Voltages	-2 to 8	V
V_{OSC}, V_{SDO}	Oscillator Voltage Range, Logic Output	-0.3 to $V_{CC} + 0.3$	V

Note: ESD for all pins, except pins SDO, SRA and SRB, are according to MIL883C, tested at 2kV, corresponding to a maximum energy dissipation of 0.2mJ. SDO, SRA and SRB pins are tested with 800V.

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ j-case}$	Typical Thermal Resistance Junction to Case	5	°C/W
$R_{th\ j-amb}$	Typical Thermal Resistance Junction to Ambient (6cm ² Ground Plane 35µm Thickness)	35	°C/W
$R_{th\ j-amb, FR4}$	Typical Thermal Resistance Junction to Ambient (soldered on a FR 4 board with through holes for heat transfer and external heat sink applied)	8	°C/W
T_S	Storage Temperature	-40 to 150	°C
T_{SD}	Typical Thermal Shut-Down Temperature	180	°C

ELECTRICAL CHARACTERISTICS ($8V \leq V_S \leq 24V$; $-40^\circ C \leq T_j \leq 150^\circ C$; $4.5V \leq V_{CC} \leq 5.5V$, unless otherwise specified.)¹⁾

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SUPPLY						
I_{S85}	Total Supply Current $I_S + I_{VCC}$ (Both Bridges Off)	$V_S = 14V$ $\overline{EN} = HIGH$ $T_J \leq 85^\circ C$		40	100	µA
I_{SOP}	Operating Supply Current	$I_{OUT\ Ai/Bi} = 0$ $f_{OSC} = 30kHz$ $V_S = 14V$		4.5		mA
I_{CC}	5V Supply Current	$\overline{EN} = LOW$		1.4	10	mA
FULL BRIDGES						
$R_{OUT, Sink}$	$R_{DS(on)}$ of Sink Transistors	Current bit combinations LL, LH, $V_S \geq 12V$		0.4	0.7	Ω
$R_{OUT, Source}$	$R_{DS(on)}$ of Source Transistors			0.4	0.7	Ω
$R_{OUT8, Sink}$	$R_{DS(on)}$ of Sink Transistors + $R_{DS(on)}$ of Source Transistors	Current bit Combinations LL, LH, $V_S = 8V$		1.6	3	Ω
V_{FWD}	Forward Voltage of the DMOS Body Diodes	$\overline{EN} = HIGH$ $I_{FWD} = 1A$; $V_S \geq 12V$		1	1.4	V
V_{REV}	Reverse DMOS Voltage	$\overline{EN} = LOW$ $I_{REV} = 1A$		0.5	0.9	V
t_r, t_f	Rise and Fall Time of Outputs $OUT_{Ai/Bi}$	$0.1 \dots 0.9 V_{OUT}$ $V_S = 14V$ Chopping 550mA	0.3	0.6	1.5	µs

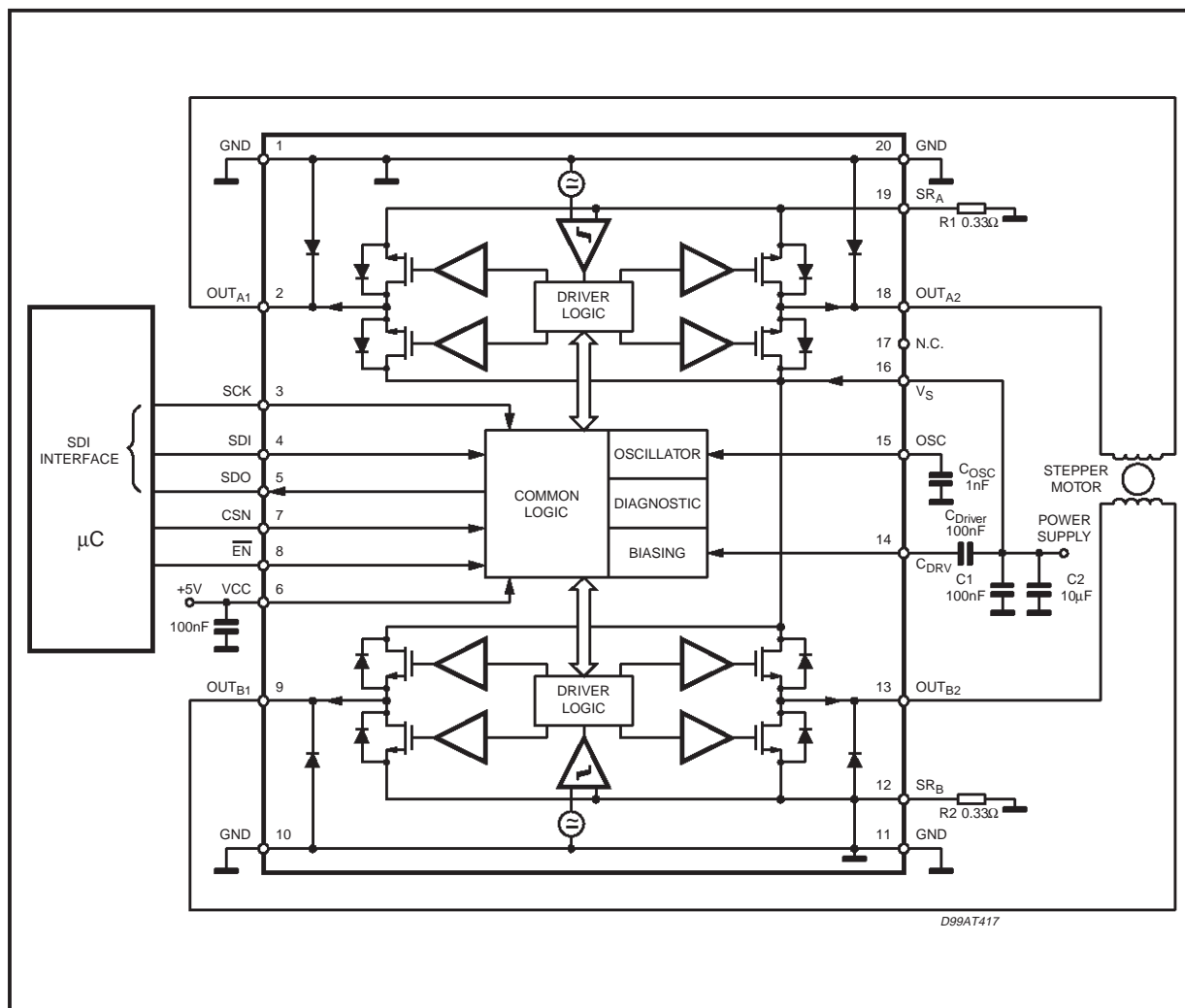
ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SWITCH OFF THRESHOLD OF THE CHOPPER (R ₁ · R ₂ = 0.33Ω)						
V _{SRHL}	Voltage Drops Across R ₁ · R ₂ ²⁾ (Voltage at Pin SR _A or SR _B vs. GND)	Bit 5, 2 = H Bit 4, 1 = L	12	20	35	mV
V _{SRLH}		Bit 5, 2 = L Bit 4, 1 = H	160	180	210	mV
V _{SRLL}		Bit 5, 4, 2, 1 = L	270	300	340	mV
ENABLE INPUT \overline{EN}						
V _{EN High}	High Input Voltage		V _{CC} -1.2V			V
V _{EN low}	Low Input Voltage				1.2	V
V _{EN Hyst}	Enable Hysteresis		0.1			V
I _{EN High}	High Input Current	V _{High} = V _{CC}	-10	0	10	μA
I _{EN Low}	Low Input Current	V _{LOW} = 0V	-3	-10	-30	μA
LOGIC INPUTS SDI, SCK, CSN						
V _{HIGH}	High Input Voltage	\overline{EN} = LOW	2.6		8	V
V _{LOW}	Low Input Voltage		-0.3		1	V
V _{Hyst}	Hysteresis		0.8	1.2	1.6	V
I _{HIGH}	High Input Current	V _{High} = V _{CC}	-10	0	10	μA
I _{Low}	Low Input Current	V _{Low} = 0V	-3	-10	-30	μA
LOGIC OUTPUTS (SDO)						
V _{SDO,High}	High Output Voltage	I _{SDO} = -1mA	V _{CC} -1	V _{CC} -0.17	V _{CC}	V
V _{SDO,Low}	Low Output Voltage	I _{SDO} = 1mA		0.17	1	V
OSCILLATOR						
V _{OSC, H}	High Peak Voltage	\overline{EN} = LOW	2.2	2.46	2.6	V
V _{OSC, L}	Low Peak Voltage	\overline{EN} = LOW	1	1.23	1.4	V
I _{OSC}	Charging/Discharging Current		45	62	80	μA
f _{OSC}	Oscillator Frequency	C _{OSC} = 1nF	20	25	31	kHz
t _{Start}	Oscillator Startup Time	EN = High → Low	2/f _{osc}	5/f _{osc}	8/f _{osc}	
THERMAL PROTECTION						
T _{J-OFF}	Thermal Shut-Down Temperature		160	180	200	°C
T _{J-ALM}	Thermal Prealarm		130	160		°C
ΔT _{MGN}	Margin Prealarm/Shut-Down		10	20	30	K

1) Parameters are tested at 125°C. Values at 140°C are guaranteed by design and correlation.

2) Currents of combinations LH and LL are sensed at the external resistors. The Current of bit combination HL is sensed internally and cannot be adjusted by changing the sense resistors.

Figure 1. General Application Circuit Proposal.

**Application hints:**

C1 and C2 should be placed as close to the device as possible. Low ESR of C2 is advantageous. Peak currents through C1 and C2 may reach 2A. Care should be taken that the resonance of C1, C2 together with supply wire inductances is not the chopping frequency or a multiple of it.

FUNCTIONAL DESCRIPTION**Basic structure**

The L9935 is a dual full bridge driver for inductive

Table 1.

bit5, bit2	bit4, bit1	I_{QX} (Typ.)	I_{RX}/max	Remark
H	H	0	0%	internally sensed
H	L	60mA		
L	H	550mA	61%	
L	L	900mA	100%	

loads with a chopper current regulation.

Outputs A1 and A2 belong to full bridge A

Outputs B1 and B2 belong to full bridge B

The polarity of the bridges can be controlled by bit0 and bit3 (for full bridge A, bit3, for full bridge B, bit0). Bit5, bit4 (for full bridge A) and bit2, bit1 (for full bridge B) control the currents. Bit3 high leads to output A1 high. Bit0 high leads to output B1 high.

Current setting Table 1 using a 0.33W sense resistor.



No current:

Bit 5, bit 4 (corresponding bit 2 and bit 1 for bridge B) both are HIGH, the current logic will inhibit all drivers D₁₁, D₁₂, D₂₁, D₂₂ turning off M₁₁, M₁₂, M₂₁, M₂₂ independently from the signal of the current sense comparator comp 1.

Turning on:

Changing bit 5 or bit 4 or both to LOW will turn on either M₁₁ and M₂₂ or M₂₁ and M₁₂ (depending on the phase signal bit 3). Current will start to flow through the load. The current will be sensed by the drop across R₁.

The threshold of the comparator comp 1 depends on the current settings of bit 5 and bit 4.

The current will rise until it exceeds the turn off threshold of comp 1.

Chopping:

Exceeding the threshold of comp 1 the drive logic will turn off the sink transistor (M₁₂ or M₂₂). The sink transistor periodically is turned on again by the oscillator. Immediately after turning on M₁₂ or M₂₂ the comparator comp 1 will be inhibited for a certain time to blank switch over spikes caused

by capacitive load components up to 5 nF.

Turning off for example M₁₂ will yield a flyback current through D₁₁. (So now the free wheeling current flows through M₂₁, the load and D₁₁). This leads to a slow current decay during flyback.

Maximum duty cycles of more than 85% (at f_{OSC} = 25kHz) are possible. In this case current flows of both bridges will overlap (not shown in Fig. 5).

Reversing phase:

Suppose the current flowed via M₂₁, the load and M₁₂ before reversing phase. Reversing phase M₂₁ and M₁₂ will be turned off. So now the current will flow through D₂₂, the load and D₁₁. This leads to a fast current decay.

Chopper control by oscillator

Both chopping circuits work with offset phase. One chopper will switch on the bridge at the maximum voltage of the oscillator while the other chopper will switch on the bridge at minimum voltage of the oscillator.

MS1 and MS2 blank switching spikes that could lead to errors of the current control circuit.

Figure 4. Principal chopper control circuit.

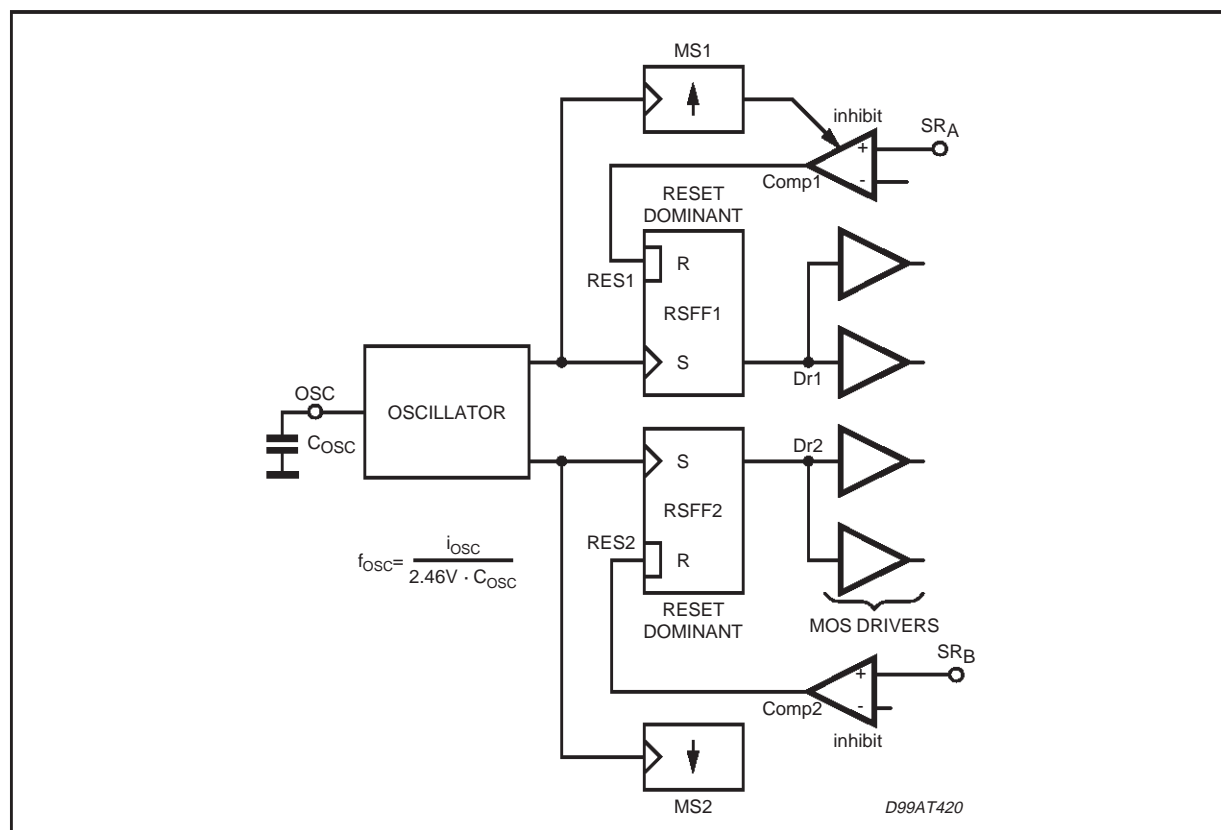
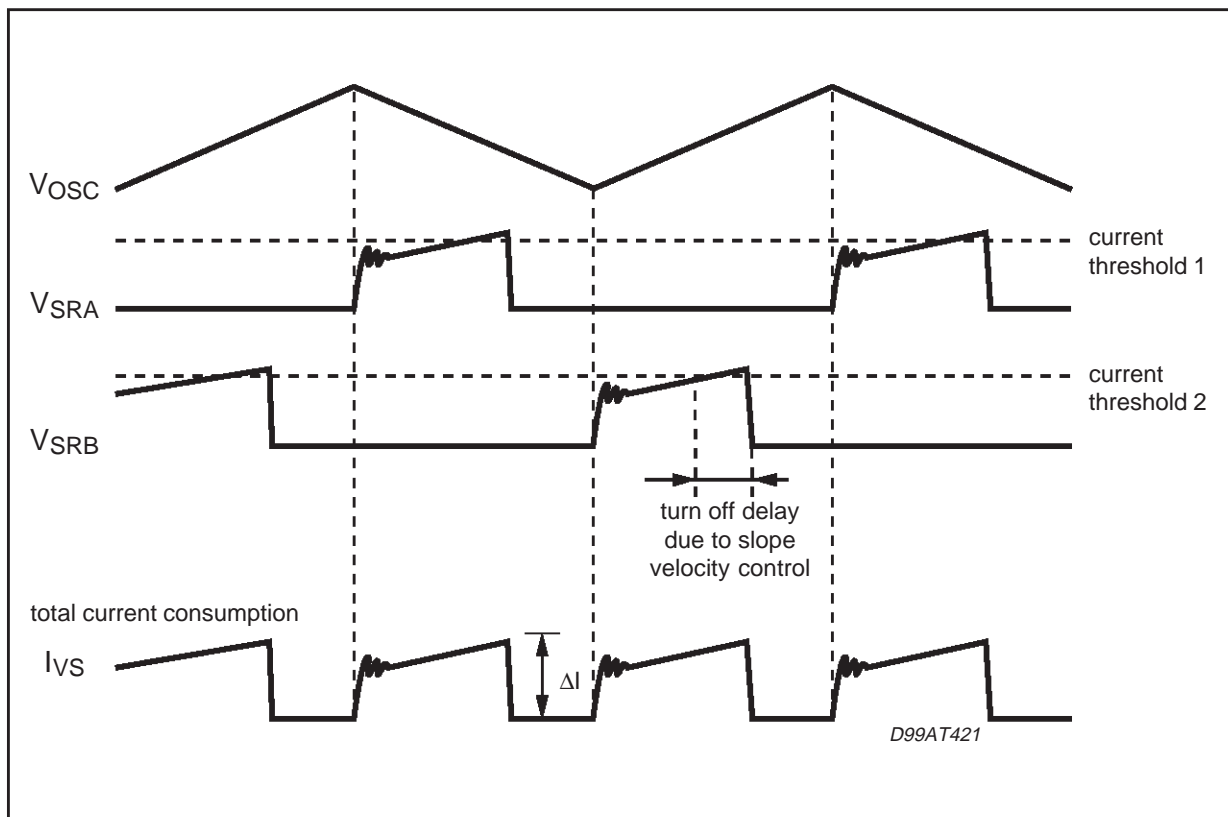


Figure 5. Pulse diagram to explain offset chopping.



Using offset chopping the changes of the supply current remain half as large as using non offset chopping.

Turning off the oscillator for example by shorting pin OSC to ground will hinder turning on of the bridges anymore after the comparators have generated a turn off signal.

External clocking is possible overdriving the charge and discharge currents of the oscillator for example with a push pull logic gate. So several devices can be synchronized.

Protection and Diagnosis Functions

The L9935 provides several protection functions and error detection functions. Current limitation usually is customer defined by the external current sense resistors. The current sensed there is used to regulate the current through the stepper motor windings by pulse width modulation. This PWM regulation protects the sink transistors. The source transistors are protected by an internal overcurrent shut down turning off the source transistors in case of overload.

Overload detection of the source transistor will turn off the bridge and set the corresponding error flag.

To turn on the bridge again a new byte must be written into the interface. (Rising slope of CSN resets the overload error flag).

Both bridges use the same flags. To locate which bridge is affected by an error the bridges can be tested individually (One bridge just is turned off to check for the error in the other bridge).

Short from an Output to the Supply Voltage VS

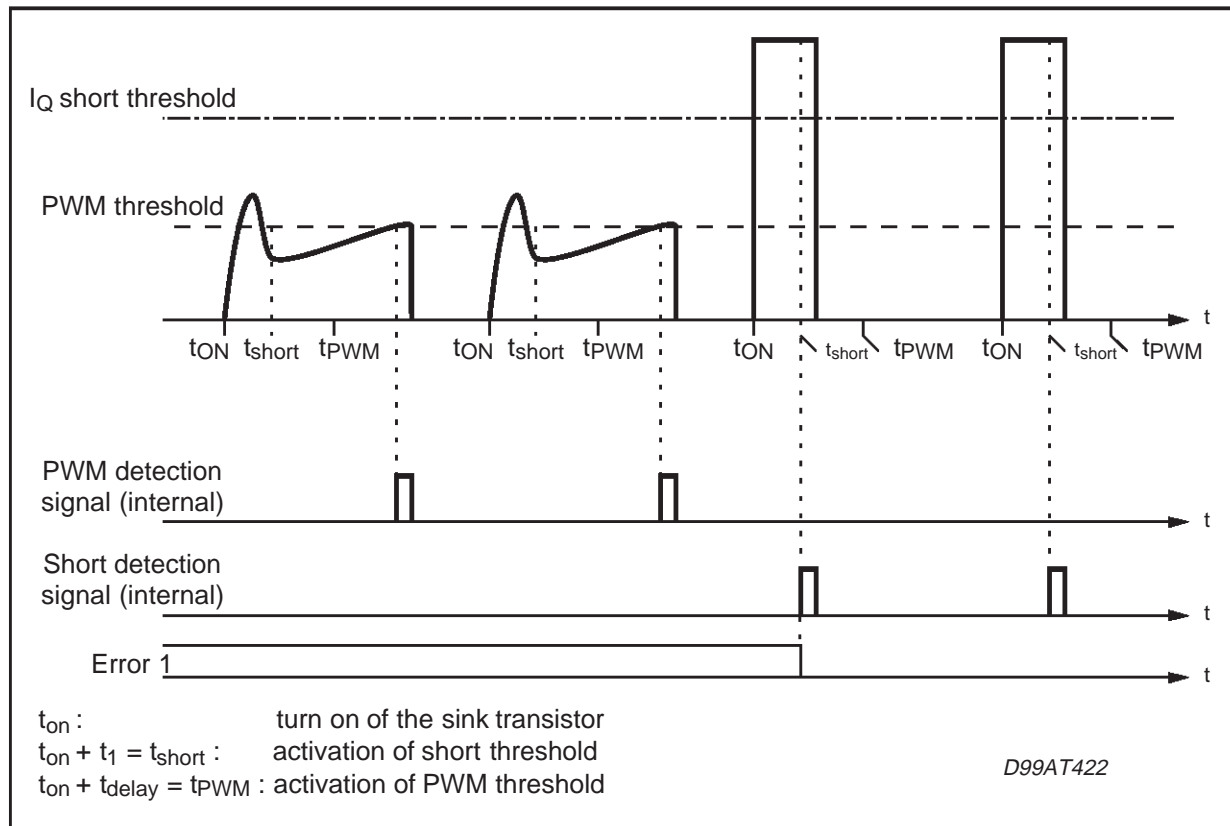
The current will be limited by the pulse width modulator. The sink transistor will turn off again after some microseconds. The transistor will periodically be turned on again by the oscillator 8 times. After having detected short 8 times the low side transistor will remain off until the next data transfer took place. After detection of a short to VS we suggest to turn off the corresponding bridge to reduce power dissipation for at least 1ms.

Diagnosis of a Short to VS

During the short current through the sink transistor will rise more rapidly than under normal load conditions. Reaching a peak current of 1.5 times the maximum PWM current between typically $2\mu\text{s}$ and $5\mu\text{s}$ after turn on will be detected as a short to VS.

Detecting a short the low side transistor will try to turn on again the next 7 trigger pulse of the oscillator. Simultaneously the error flag will updated on each pulse.

Figure 6. Normal PWM current versus short circuit current and detection of short to VS..



Between t_{ON} and t_{SHORT} the over current detection is totally blanked.

Between t_{SHORT} and t_{PWM} the current threshold is set to 1.5 times the maximum PWM current (1.5 times the current of current setting LL).

Overcurrent now will set the error flag.

After t_{PWM} the current threshold is the nominal PWM current set by the external resistor. Exceeding this current will just turn off the sink transistor. This is considered as normal operation. The error flag is detached from the comparator after t_{PWM} so no error flag is set during normal pulse width modulation.

Short from an Output to Ground

The current through the short will be detected by the protection of the source transistor. The source transistor will turn off exceeding a current of typically 1.8A. Minimum overload detection current is 1.2A. To obtain proper current regulation (by the sink transistors and not by source transistor shut down) the maximum current of the PWM regulator should be set to a maximum value of 1.1A.

Diagnosis of a Short to Ground

Detecting an overload will set an overcurrent error (Error2 = LOW) (bit6). To reset the error flag a new byte must be written into the interface. (Reset of the error flag takes place at the rising slope of CSN).

Shorted Load

With a shorted load both, the sink- and the source protection or the PWM alone will respond. In either case there will be no flyback pulse.

Diagnosis of a Shorted Load

Shorting the load two events may take place:

- overload (of the high side transistor) while low side transistor overcurrent is detected will set the following combinations:

bit6 = LOW

bit7 = HIGH

- overload is marginal. So the low side driver may turn off before overload is detected. This leads to the combination bit6 = HIGH and bit7 = LOW.

Open Load

An open load will not lead to any flyback pulses. Error detection will take advantage of the flyback pulse. Missing the flyback pulse after reversing the polarity of a motor winding bit7 will become LOW.

Open load will not be tested in the low current mode (current bits HL) to avoid the risk of instable diagnosis at low flyback currents. Open load immediately after reset or power down may on random be detected in the low current mode too. This diagnosis however will not persist longer than 8 changes of polarity. We strongly suggest to test open load at a high current mode (combination LH or LL).

Overtemperature Prealarm

Typically 20K before thermal shut down takes place an overtemperature prealarm (bit7 and bit6 low) takes place. Typically overtemperature prealarm temperature is between 150°C and 160°C.

Application hints using a high resistive stepper motor

The L9935 was originally targeted on stepper chopping stepper motor application with typical resistances of 8..12W. Using motors with higher resistance will work too but diagnosis behaviour will slightly change. This paragraph shows the details that should be taken in account using diagnosis for high resistive motors.

Startup behaviour:

The device has simple digital filter to avoid triggering diagnosis at a single event that could be random noise. This digital filter needs 4 chopping pulses to settle. Using a high resistive motor this chopping does not take place. Instead the digital filter samples each time a polarity change takes place. So the first three response telegrams after reset may show an 'open load' error.

Input data	High resistive motor (error bits)	Low resistive motor (error bits)
Standby		
1st telegram (550mA or 900mA)	HH	HH
Reverse phase (550mA or 900mA)	XH	HH
Reverse phase (550mA or 900mA)	XH	HH
Any data	XH	HH
Any data	HH	HH

H means check for HIGH at the error bits.

X means don't care because filter is not yet settled.

Using 75mA chopping immediately after stand by:

The high resistive motor can be forced to chopping operation in the low current range. This leads to the same behaviour as using a low resistive motor.

Short to V_S detection using high resistive motors:

The short to VS flag is overwritten each time the chopper comparator responds. Having detected a short this flag only can be reset by reaching chopping operation or resetting the circuit (ENN=1). For a high resistive motor this leads to the following consequence: Once a short to VS is detected the error flag will persist even if the short is removed again until either a reset (ENN=1) or chopping (for example in 75mA mode) has taken place. We suggest to return to operation once a short to VS was detected by using the low current mode to reset the flag.

Limitation of the Diagnosis

The diagnosis depends on either detecting an overcurrent of more than typically 1.8A through the source transistor or on not detecting a flyback pulse, or on detecting severe overcurrents of the sink transistor immediately after turn on.

- Small currents bypassing the load will not be detected.
- In the low current range (hold current) the flyback pulse (especially commutating against the supply voltage after changing phase) may (depending on the inductivity of the stepper motor windings) be too short to be detected correctly. For this reason diagnosis using the flyback pulse is blanked at phase reversal at hold current.
- In the low current range (hold current) the current capability of the bridge is reduced on purpose. Short to VS may not be detected. In stead the bridge may just chop like normal operation.
- Flyback pulse detection is not blanked during PWM regulation at hold current (here commutation voltage is less than 1V thus providing a longer pulse duration.) This however should be taken in account using stepper motors with low inductivity (less than 0.5mH). Using motors with such a low inductivity the flyback voltage in hold mode may decay too fast.
- Motors with extremely low ohmic resistance tend to pump up the current because current decay during flyback approaches zero while at bridge turn on the current will increase. This may lead to overcurrent detection. We suggest to use stepper motors with an ohmic resistance of approximately 3Ω or more.

Partial shorts of windings or shorts of stepper motors with coils in series may still yield a flyback pulses that are accepted by the diagnosis as a proper signal.

Table 2. Error table.

Error 1 bit7	Error 2 bit6	Description
H	H	Normal operation
L	H	Short to VS (sink overload immediately after turn on) shorted load (no flyback) open load (no flyback)
H	L	short to gnd (source overload, missing flyback is masked)
L	L	overtemperature prealarm

At stepping rates faster than 1ms/data transfer error flags indicating a short should be used to initiate a pause of at least 1ms to allow the power bridges to cool down again.

Serial Data Interface (SPI)

The serial data interface itself consists of the pins SCL (serial clock), SDI (serial data input) and SDO (serial data output).

To especially support bus controlled applications the additional signals $\overline{\text{EN}}$ (chip enable not) and CSN (chip select not) are available.

Startup of the Serial Data Interface

Falling slope of $\overline{\text{EN}}$ activates the device. After $t_{\text{en.sck}}$ the device is ready to work.

Falling slope of CSN indicates start of frame. Data transfer (reading SDI into the register) takes place at the rising slopes of SCK.

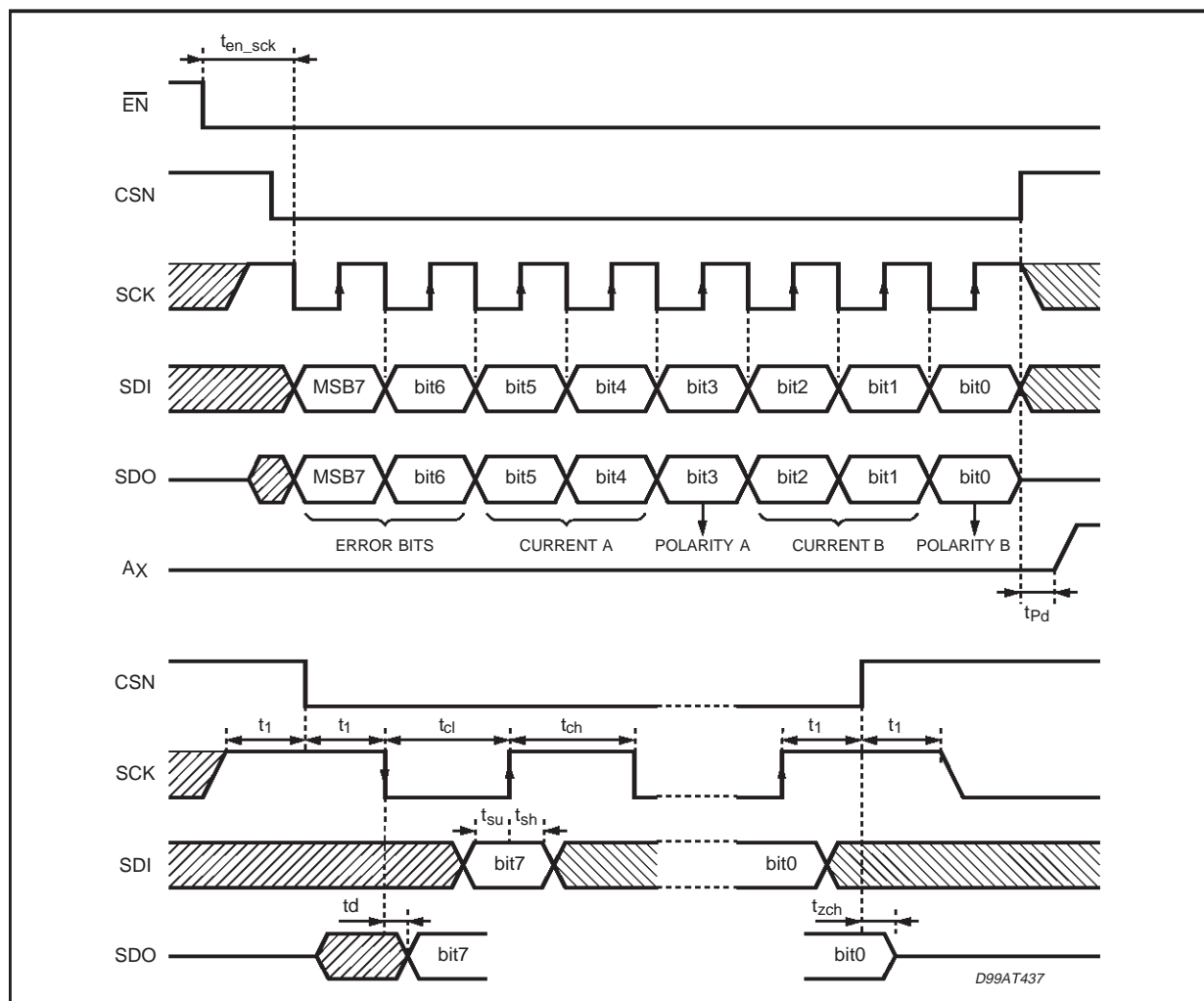
Data transfer of the register to SDO takes place at the falling slope of SCK.

Rising slope of CSN indicates end of frame. At the end of frame data will only be accepted if modulo 8 bit (modulo 8 falling slopes to SCK) have been transferred. If this is not the case the input will be ignored and the bridges will maintain the same status as before.

SDO is a tristate output.

SDO is active while CSN = LOW, while CSN = HIGH SDO is high resistive.

Figure 7. SPI Data/Clock Timing.



Test condition for all propagation times (unless otherwise specified)

HIGH $\geq 3V$; LOW $\leq 0.8V$; $t_r, t_f = 10ns$, Enable: ENN Low $< 0.8V$, ENN High $> V_{CC} - 0.8V$

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
f_{SCLK}	SCK-Frequency		DC		2MHz	
t_1	SCK stable before and after CSN = 0		100			ns
t_{ch}	Width of SCK high pulse		200			ns
t_{cl}	Width of SCK low pulse		200			ns
t_{su}	SDI setup time		80			ns
t_{sh}	SDI hold time		80			ns
t_d	SDO delay time (CL = 50pF)			100		ns
t_{zc}	SDO high Z CSN high			100		ns
t_{en_sck}	Setup time ENABLE to SCK	HIGH $> V_{CC} - 1.2V$	30			μs
t_{pd}	Propagation delay SPI to output Q_{XX}			2 (*)		μs

(*) Measured at a transition from High impedance (Bridge off) to bridge on. (Reversing polarity takes about 1 μs longer because the bridge first turns off before turning on in reverse direction).

Table of bits

bit5,bit4 : current range of bridge A (Outputs A1 and A2)

bit3 : polarity of bridge A

bit2,bit1 : current range of bridge B (Outputs B1 and B2)

bit0 : polarity of bridge B

bit7,bit6 : Error1 and Error 2

Cascading several Devices

Cascading several devices can be done using the SDO output to pass data to the next device. The whole frame now consists of n byte. n is the number of devices used.

Figure 8. Cascading Several Stepper motor drivers.

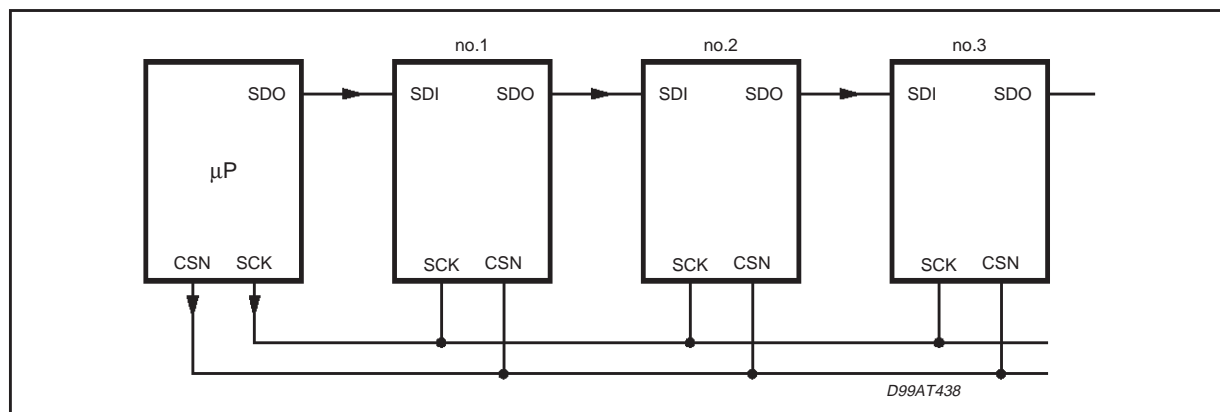


Figure 9. Control sequence for 3 Stepper motor drivers.

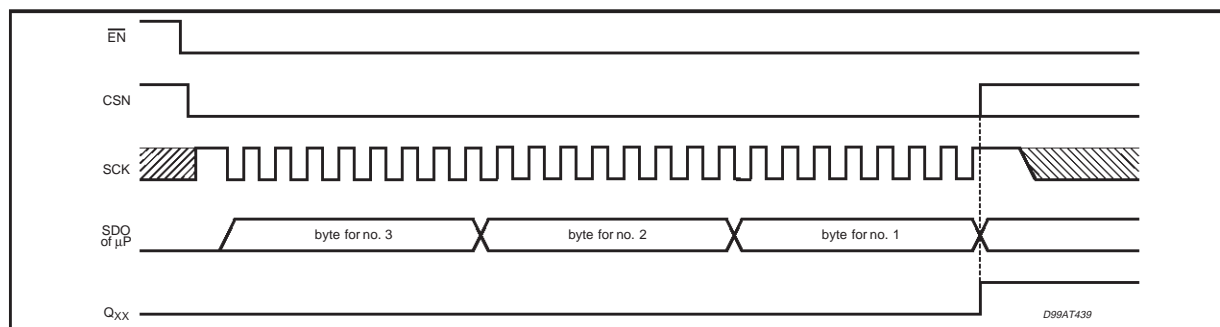
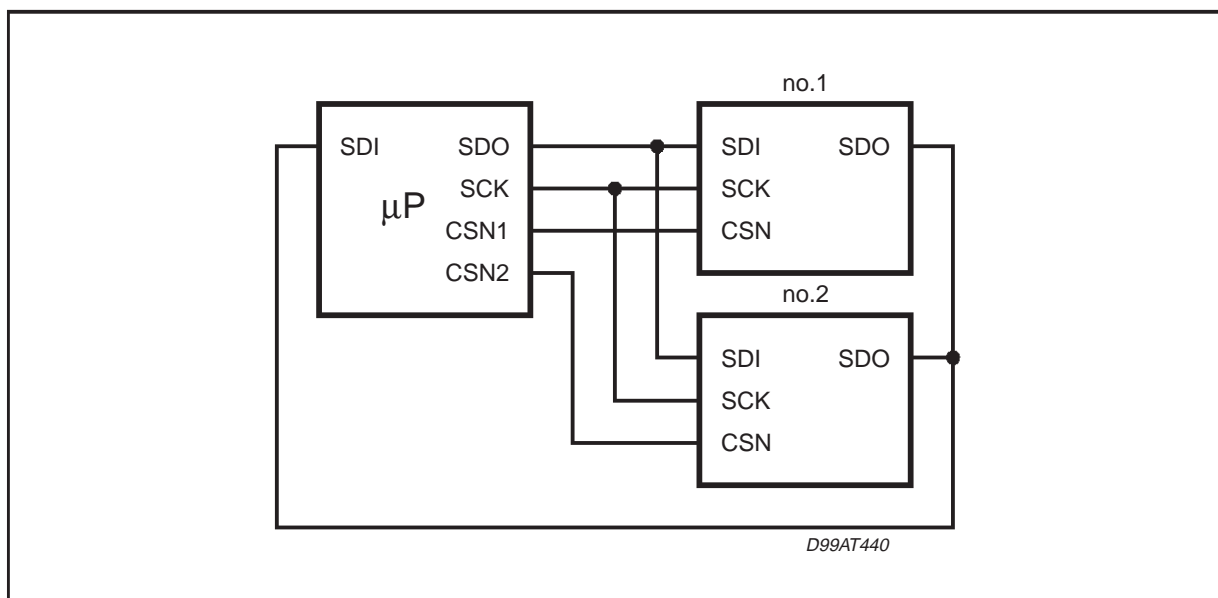


Figure 10. Paralleling several Devices.



here usually only one Stepper motor driver is selected at a time while all others are deselected.

Application Information

For driving a stepper motor we suggest to use the following codes. The columned 'SDO correct' shows the data returned at SDO in correct function. The columnes presented under 'Error cases' display the diagnosis bits if errors are detected.

Examples of control sequences

Full step mode control sequences and diagnosis response.

SDI	SDO correct	Error cases and SDObit7, bit6											
		A	B	A1	A2	B1	B2	A1)	A2)	B1)	B2)	therm. alarm	therm. shut down (reset operating codes)
		O P E N	O P E N	S H O R T	S H O R T	S H O R T	S H O R T	S H O R T	S H O R T	S H O R T	S H O R T		
				VS	VS	VS	VS	GND	GND	GND	GND		
bit	76543210	76543210	76	76	76	76	76	76	76	76	76	76	76543210
	XX111111	SDO PRESENT LAST DATA OR 11111111 IN CASE PREV. STATE WAS STAND BY											
	XX011011	11111111	11	11	11	11	11	11	11	11	11	00	00111111
	XX010011	11011011	11	11	11	01	11	01	10	11	10	11	00111111
	XX010010	11010011	01	11	01	01	11	01	01	10	10	11	00111111
	XX011010	11010010	11	01	01	11	01	01	11	10	01	10	00111111
	XX011011	11011010	01	11	01	01	01	11	10	01	11	10	00111111
	XX010011	11011011	11	01	11	01	01	01	10	11	10	01	00111111
	XX010010	11010011	01	11	01	01	11	01	01	10	10	11	00111111
	XX011010	11010010	11	01	01	11	01	01	11	10	01	10	00111111

*) Motor resistance approximately 10Ω and $V_s = 12V$. So a short to ground only is detected on one branche of the bridge. Lower resistivity of the motor may lead to detection of short to ground on both branches of the bridge leading to code 10 on all steps.

These sequences are intended to give the user a good starting point for his software development. Besides these two there are further possibilities how to implement control sequences for this device (other currents, quarters step etc.).

	SDI	SDO	A O P E N	B O P E N	A1 S H O R T VS	A2 S H O R T VS	B1 S H O R T VS	B2 S H O R T VS	A1 *) S H O R T GND	A2 *) S H O R T GND	B1 *) S H O R T GND	B2 *) S H O R T GND	therm. alarm	therm. shut down (reset operating codes)
bit	76543210	76543210	76	76	76	76	76	76	76	76	76	76	76	76543210
	XX111111	previous code	11	11	11	11	11	11	11	11	11	11	00	00111111
	XX011111	11111111	11	11	11	01	11	11	10	11	11	11	00	00111111
	XX011111	11011111	11	11	11	01	11	11	10	11	11	11	00	00111111
	XX011111	11011111	11	11	11	01	11	11	10	11	11	11	00	00111111
	XX011011	11011111	11	11	11	01	11	11	10	11	11	11	00	00111111
	XX111011	11011111	11	11	11	01	11	01	10	11	10	11	00	00111111
	XX010011	11011011	01	11	01	01	11	01	01	11	10	11	00	00111111
	XX010111	11111011	11	11	01	11	11	01	11	10	10	11	00	00111111
	XX010010	11010011	11	01	01	11	01	01	11	10	01	11	00	00111111
	XX110010	11010111	11	11	01	11	01	11	11	10	11	10	00	00111111
	XX011010	11110010	01	11	01	01	01	11	11	01	11	10	00	00111111
	XX011110	11011010	11	11	11	01	01	11	10	11	11	10	00	00111111
	XX011011	11011110	11	01	11	01	01	01	01	11	11	01	00	00111111
	XX111011	11011011	11	11	01	01	11	01	10	11	10	11	00	00111111
	XX010011	11111011	01	11	01	01	11	01	01	11	10	11	00	00111111
	XX010111	11010011	11	11	01	11	11	01	11	10	10	11	00	00111111
	XX010010	11010111	11	01	01	11	01	01	11	10	01	11	00	00111111
	XX110010	11010010	11	11	01	11	01	11	11	10	11	10	00	00111111

Double errors: Double errors will create composite codes by an AND operation between columns of the same dominance. Open and short to VS are the least dominant error codes. (first 6 error code columns). Short to ground is the second dominant error code. detection of short to gnd will overwrite error codes of the least dominant kind (open, short to VS). Temperature prealarm and thermal shut down are the most dominant error codes. Thermal prealarm returns error code 00 but the device still is working and returns the appropriate operation code (bits 0..5).

Thermal shut down returns error code 00 and turns off the device. The opcode returned corresponds the action eventually performed (bit 0..5 become 1).

For example open bridge A and simultaneously open bridge B will lead to error code 01 by performing an AND operation between the two corresponding columns.

*) Motor resistance approximately 10Ω and $V_S = 12V$. So a short to ground only is detected on one branche of the bridge. Lower resistivity of the motor may lead to detection of short to ground on both branches of the bridge leading to code 10 on all steps.

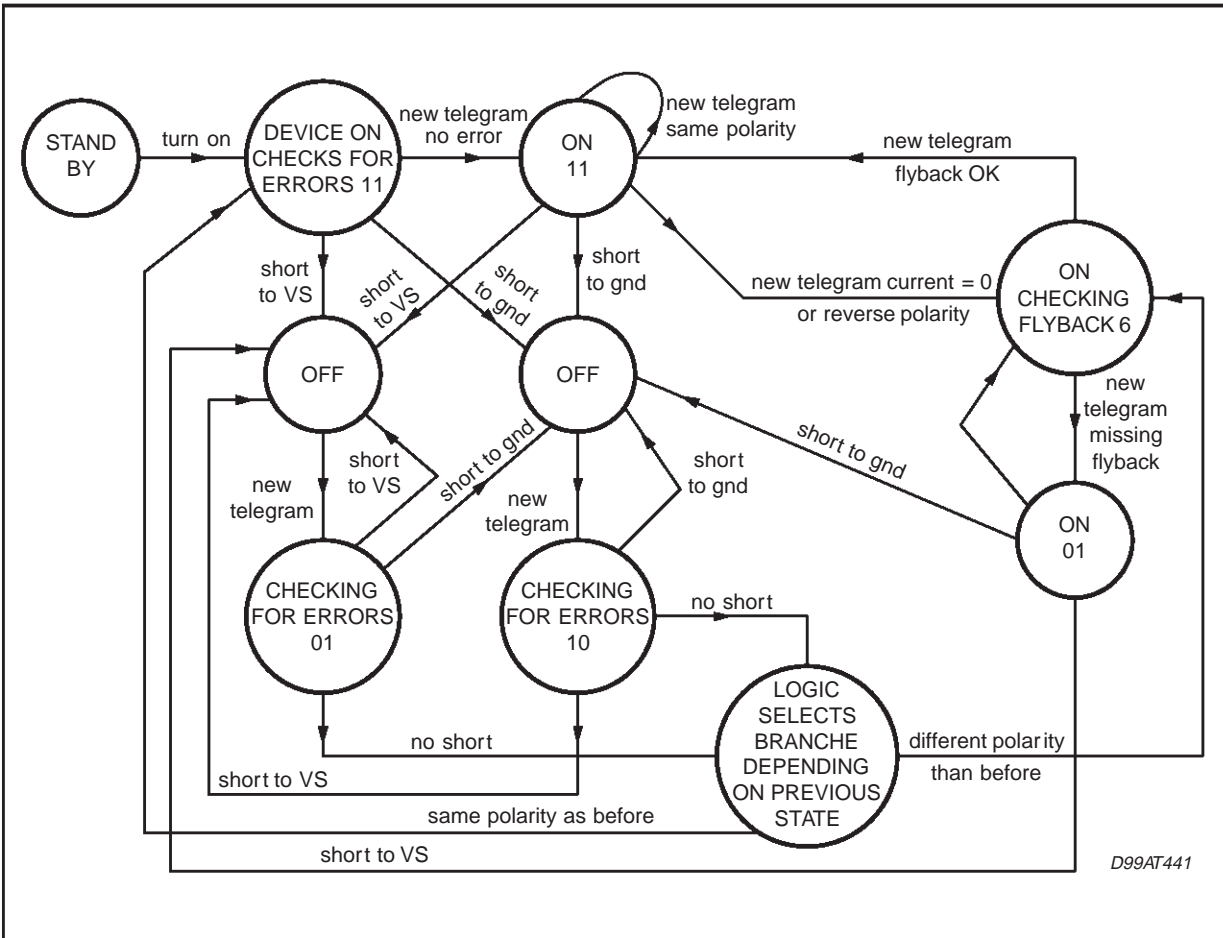
Electromagnetic Emission classification(EME)

Electromagnetic Emission classes presented below are typical data found on bench test. For detailed test description please refer to 'Electromagnetic Emission (EME) Measurement of Integrated Circuits, DC to 1GHz' of VDE/ZVEI work group 767.13 and VDE/ZVEI work group 767.14 or IEC project number 47A 1967Ed. This data is targeted to board designers to allow an estimation of emission filtering effort required in application.

Pin	EME class			Remark
GND	E	10	0	1Ω test
V_{CC}	E		e	Blocked with 100nF close to the device
EN, SDI, CSN, CSK, SDO in tristate	K		h	
SDO	G		f	SDO in low-Z state, no data transfer
Power output A ₁ , A ₂ , B ₁ , B ₂	E	5	f	Sourcing output
Power output A ₁ , A ₂ , B ₁ , B ₂		6	f	Sinking output in chopping mode $f_{osc} = 20kHz$

Electromagnetic Emission is not tested in production.

Figure 11. State diagram.



Remark: Return to stand by is possible from every state

Note: Reversing polarity in low current mode no flyback check will be performed.

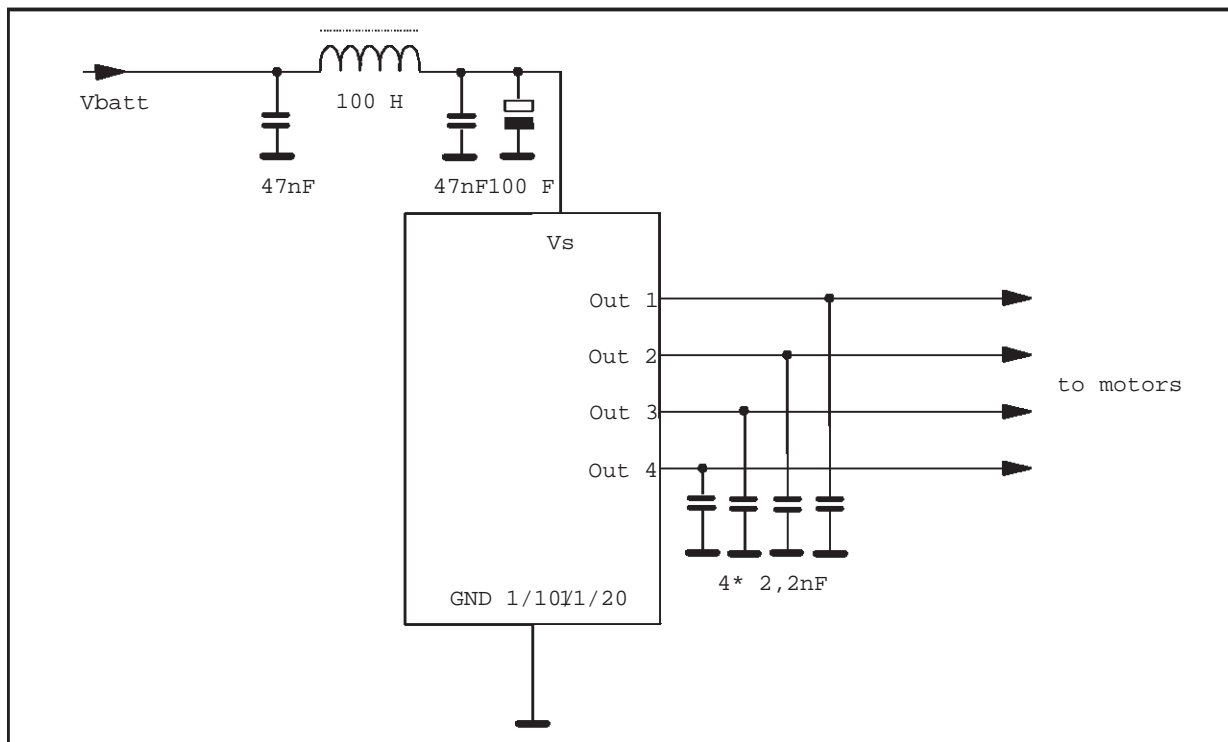
Electromagnetic Emission classification(EME)

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Pin	EME class			Remark
GND	E	10	o	1Ω test
Vcc	E		e	Blocked with 100nF close to the device
EN, SDI, CSN, SCK, SDO in tristate	K		h	
SDO	G		f	SDO in low-state, no data transfer
Power output A ₁ , A ₂ , B ₁ , B ₂	E	5	f	Sourcing output
Power output A ₁ , A ₂ , B ₁ , B ₂		6	f	Sinking output in chopping mode fOSC = 20kHz

Electromagnetic Emission is not tested in production.

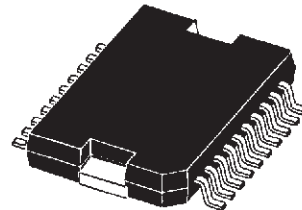
Figure 12. EMC Compatibility for L9935



DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.6			0.142
a1	0.1		0.3	0.004		0.012
a2			3.3			0.130
a3	0		0.1	0.000		0.004
b	0.4		0.53	0.016		0.021
c	0.23		0.32	0.009		0.013
D (1)	15.8		16	0.622		0.630
D1	9.4		9.8	0.370		0.386
E	13.9		14.5	0.547		0.570
e		1.27			0.050	
e3		11.43			0.450	
E1 (1)	10.9		11.1	0.429		0.437
E2			2.9			0.114
E3	5.8		6.2	0.228		0.244
G	0		0.1	0.000		0.004
H	15.5		15.9	0.610		0.626
h			1.1			0.043
L	0.8		1.1	0.031		0.043
N	10° (max.)					
S	8° (max.)					
T		10			0.394	

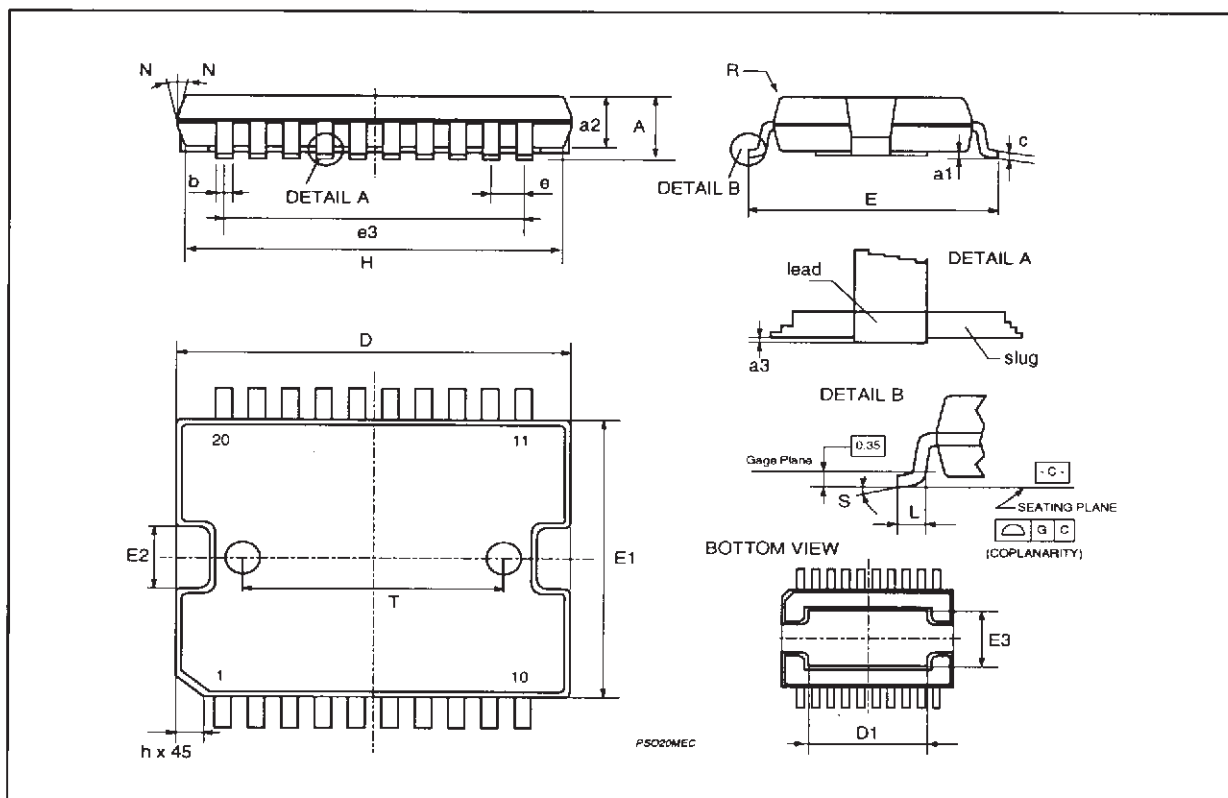
- (1) "D" and "F" do not include mold flash or protrusions.
 - Mold flash or protrusions shall not exceed 0.15 mm (0.006").
 - Critical dimensions: "E", "G" and "a3"

OUTLINE AND MECHANICAL DATA



JEDEC MO-166

PowerSO20



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