AR0330 Register Reference

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AR0330 Register Reference
Rev. C

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Registers

The AR0330 provides a 16-bit register address space accessed through a serial interface Each register location is 8 or 16 bits in size.

The address space is divided into the five major regions shown in Table 1. The remainder of this section describes these registers in detail.

Table 1: Address Space Regions

Address Range	Description
0x0000–0x0FFF	Reserved
0x1000–0x1FFF	Reserved
0x2000–0x2FFF	Reserved
0x3000–0x3FFF	Manufacturer-specific registers (read-only and read-write dynamic registers)
0x4000–0xFFFF	Reserved

Register Notation

The underlying mechanism for reading and writing registers provides byte write capability. However, it is convenient to consider some registers as multiple adjacent bytes. The AR0330 uses 8-bit, 16-bit, and 32-bit registers, all implemented as 1 or more bytes at naturally aligned, contiguous locations in the address space.

In this document, registers are described either by address or by name. When registers are described by address, the size of the registers is explicit. For example, R0x3024 is an 8-bit register at address 0x3024, and R0x3000–1 is a 16-bit register at address 0x3000–0x3001. When registers are described by name, the size of the register is implicit. It is necessary to refer to the register table to determine that model_id is a 16-bit register.

Bit Fields

Some registers provide control of several different pieces of related functionality, and this makes it necessary to refer to bit fields within registers. As an example of the notation used for this, the least significant 4 bits of the fine_gain register are referred to as fine_gain[3:0] or R0x3060–1[3:0].

Bit Field Aliases

In addition to the register aliases described above, some register fields are aliased in multiple places. For example, R0x301C (mode_select) has only one operational bit, R0x301C[0]. This bit is aliased to R0x301A–B[2]. The effect of reading or writing a bit field through any of its aliases is identical.

Byte Ordering

Registers that occupy more than one byte of address space are shown with the lowest address in the highest-order byte lane to match the byte-ordering on the bus. For example, the model_id register is R0x3000–1. In the register table the default value is shown as 0x2600. This means that a read from address R0x3000 would return 0x26, and a read from address 0x0001 would return 0x04. When reading this register as two 8-bit transfers on the serial interface, the 0x26 will appear on the serial interface first, followed by the 0x04.

Address Alignment

All register addresses are aligned naturally. Registers that occupy 2 bytes of address space are aligned to even 16-bit addresses, and registers that occupy 4 bytes of address space are aligned to 16-bit addresses that are an integer multiple of 4.

Bit Representation

For clarity, 32-bit hex numbers are shown with an underscore between the upper and lower 16 bits. For example: 0x3000_01AB.

Data Format

Most registers represent an unsigned binary value or set of bit fields. For all other register formats, the format is stated explicitly at the start of the register description. The notation for these formats is shown in Table 2.

Table 2: Data Formats

Name	Description
FIX16	Signed fixed-point, 16-bit number: two's complement number, 8 fractional bits. Examples: 0x0100 = 1.0, 0x8000 = –128, 0xFFFF = –0.0039065
UFIX16	Unsigned fixed-point, 16-bit number: 8.8 format. Examples: 0x0100 = 1.0, 0x280 = 2.5
FLP32	Signed floating-point, 32-bit number: IEEE 754 format. Example: 0x4280_0000 = 64.0

Register Behavior

Registers vary from "read-only," "read/write," and "read, write-1-to-clear."

Register Changes

All register writes are delayed by 1x frame. A register that is written to during the readout of frame n will not be updated to the new value until the readout of frame $(n + 2)$. This includes writes to the sensor gain and integration registers.

Changes to Integration Time

If the integration time is changed while FV is asserted for frame n, the first frame output using the new integration time is frame $(n + 2)$. The sequence is as follows:

1. During frame n, the new integration time is held in the pending register.
2. At the start of frame $(n + 1)$, the new integration time is transferred to the live register. Integration for each row of frame $(n + 1)$ has been completed using the old integration time.
3. The earliest time that a row can start integrating using the new integration time is immediately after that row has been read for frame $(n + 1)$. The actual time that rows start integrating using the new integration time is dependent upon the new value of the integration time.
4. When frame $(n + 2)$ is read out, it will have been integrated using the new integration time.

If the integration time is changed on successive frames, each value written will be applied for a single frame; the latency between writing a value and it affecting the frame readout remains at two frames.

Bad Frames

A bad frame is a frame where the rows are not integrated or read correctly by the sensor. By default, bad frames are not masked. If the “mask bad frame” option is enabled, both LV and FV are inhibited during the bad frames so that the bad frames are masked as vertical blanking.

In the register tables, the “Bad Frame” column shows where changing a register or register field will cause a bad frame. This notation is used:

N—No. Changing the register value will not produce a bad frame.
Y—Yes. Changing the register value might produce a bad frame.
YM—Yes; but the bad frame will be masked out when mask_corrupted_frames (R0x0105) is set to “1.”

Real-Time Context Switching

In the AR0330, the user may switch between two full register sets A and B by writing to a context switch change bit in R0x30B0[13]. When the context switch is configured to context A the sensor will reference the "Context A Registers". If the context switch is changed from A to B during the readout of frame n, the sensor will then reference the context B coarse_integration_time registers in frame (*n + 1*) and all other context B registers at the beginning of reading frame (*n + 2*). The sensor will show the same behavior when changing from context B to context A.

The context switching functions the same way when switching from B to A as it does from A to B.

Table 3: Registers for Context A and Context B

Context A		Context B	
Register Description	Address	Register Description	Address
Coarse_integration_time	0x3012	Coarse_integration_time_CB	0x3016
Fine_integration_time	0x3014	Fine_integration_time_CB	0x3018
Line_length_pck	0x300C	Line_length_pck_CB	0x303E
Frame_length_lines	0x300A	Frame_length_lines_CB	0x30AA
COL_SF_BIN_EN	0x3040[9]	COL_SF_BIN_EN_CB	0x3040[8]
ROW_BIN	0x3040[12]	ROW_BIN_CB	0x3040[10]
COL_BIN	0x3040[13]	COL_BIN_CB	0x3040[11]
FINE_GAIN	0x3060[3:0]	FINE_GAIN_CB	0x3060[11:8]
COARSE_GAIN	0x3060[5:4]	COARSE_GAIN_CB	0x3060[13:12]
x_addr_start	0x3004	x_addr_start_CB	0x308A
y_addr_start	0x3002	y_addr_start_CB	0x308C
x_addr_end	0x3008	x_addr_end_CB	0x308E
y_addr_end	0x3006	y_addr_end_CB	0x3090
Y_odd_inc	0x30A6	Y_odd_inc_CB	0x30A8
X_odd_inc	0x30A2	X_odd_inc_CB	0x30AE
ADC_HIGH_SPEED	0x30BA[6]	ADC_HIGH_SPEED_CB	0x30BA[7]
GREEN1_GAIN	0x3056	GREEN1_GAIN_CB	0x30BC
BLUE_GAIN	0x3058	BLUE_GAIN_CB	0x30BE
RED_GAIN	0x305A	RED_GAIN_CB	0x30C0
GREEN2_GAIN	0x305C	GREEN2_GAIN_CB	0x30C2
GLOBAL_GAIN	0x305E	GLOBAL_GAIN_CB	0x30C4

Register Map

Table 4 shows the locations used within the address space. Locations that are not shown in the table are reserved for future use; they return 0x00 on read, but should not be read from or written to maintain compatibility with future designs. Locations that are shown as “Reserved” should not be accessed. The default read values of these registers are subject to change.

Caution **The effect of writing to reserved registers is undefined and may include the possibility of causing permanent electrical damage to the sensor.**

Table 4 lists sensor registers and their default values. Table 5 on page 6 lists sensor registers and their descriptions.

Register List and Default Values

Manufacturer Specific Register List

Table 4: Manufacturer-Specific Register List
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12288 (R0x3000)	chip_version_reg	dddd dddd dddd dddd	9732 (0x2604)
R12290 (R0x3002)	y_addr_start	0000 0ddd dddd dddd	124 (0x007C)
R12292 (R0x3004)	x_addr_start	0000 dddd dddd dddd	6 (0x0006)
R12294 (R0x3006)	y_addr_end	0000 0ddd dddd dddd	1419 (0x058B)
R12296 (R0x3008)	x_addr_end	0000 dddd dddd dddd	2309 (0x0905)
R12298 (R0x300A)	frame_length_lines	dddd dddd dddd dddd	1308 (0x051C)
R12300 (R0x300C)	line_length_pck	dddd dddd dddd dddd	1248 (0x04E0)
R12302 (R0x300E)	revision_number	dddd dddd	0 (0x00)
R12304 (R0x3010)	lock_control	dddd dddd dddd dddd	48879 (0xBEEF)
R12306 (R0x3012)	coarse_integration_time	dddd dddd dddd dddd	16 (0x0010)
R12308 (R0x3014)	fine_integration_time	dddd dddd dddd dddd	0 (0x0000)
R12310 (R0x3016)	coarse_integration_time_cb	dddd dddd dddd dddd	16 (0x0010)
R12312 (R0x3018)	fine_integration_time_cb	dddd dddd dddd dddd	0 (0x0000)
R12314 (R0x301A)	reset_register	d00d dddd dddd dddd	88 (0x0058)

Table 4: Manufacturer-Specific Register List (continued)
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12316 (R0x301C)	mode_select	0000 000d	0 (0x00)
R12317 (R0x301D)	image_orientation	0000 00dd	0 (0x00)
R12318 (R0x301E)	data_pedestal	0000 dddd dddd dddd	168 (0x00A8)
R12321 (R0x3021)	software_reset	0000 000d	0 (0x00)
R12328 (R0x3028)	row_speed	0000 0000 0ddd 0000	16 (0x0010)
R12330 (R0x302A)	vt_pix_clk_div	0000 0000 000d dddd	6 (0x0006)
R12332 (R0x302C)	vt_sys_clk_div	0000 0000 000d dddd	1 (0x0001)
R12334 (R0x302E)	pre_pll_clk_div	0000 0000 00dd dddd	4 (0x0004)
R12336 (R0x3030)	pll_multiplier	0000 0000 dddd dddd	98 (0x0062)
R12342 (R0x3036)	op_pix_clk_div	0000 0000 000d dddd	12 (0x000C)
R12344 (R0x3038)	op_sys_clk_div	0000 0000 000d dddd	1 (0x0001)
R12346 (R0x303A)	frame_count	dddd dddd dddd dddd	65535 (0xFFFF)
R12348 (R0x303C)	frame_status	0000 0000 0000 00??	0 (0x0000)
R12350 (R0x303E)	line_length_pck_cb	dddd dddd dddd dddd	1248 (0x04E0)
R12352 (R0x3040)	read_mode	dddd dddd ddd0 0000	0 (0x0000)
R12354 (R0x3042)	extra_delay	dddd dddd dddd dddd	0 (0x0000)
R12358 (R0x3046)	flash	??d0 000d d0dd dddd	0 (0x0000)
R12360 (R0x3048)	flash2	dddd dddd dddd dddd	256 (0x0100)
R12374 (R0x3056)	green1_gain	0000 0ddd dddd dddd	128 (0x0080)
R12376 (R0x3058)	blue_gain	0000 0ddd dddd dddd	128 (0x0080)
R12378 (R0x305A)	red_gain	0000 0ddd dddd dddd	128 (0x0080)
R12380 (R0x305C)	green2_gain	0000 0ddd dddd dddd	128 (0x0080)
R12382 (R0x305E)	global_gain	0000 0ddd dddd dddd	128 (0x0080)
R12384 (R0x3060)	analog_gain	00dd dddd 00dd dddd	0 (0x0000)

Table 4: Manufacturer-Specific Register List (continued)
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12388 (R0x3064)	smia_test	000d dddd d0d0 dddd	6402 (0x1902)
R12394 (R0x306A)	datapath_status	0000 0000 00dd 0000	0 (0x0000)
R12398 (R0x306E)	datapath_select	dddd dddd 000d 00dd	36880 (0x9010)
R12400 (R0x3070)	test_pattern_mode	0000 000d 0000 0ddd	0 (0x0000)
R12402 (R0x3072)	test_data_red	0000 dddd dddd dddd	0 (0x0000)
R12404 (R0x3074)	test_data_greenr	0000 dddd dddd dddd	0 (0x0000)
R12406 (R0x3076)	test_data_blue	0000 dddd dddd dddd	0 (0x0000)
R12408 (R0x3078)	test_data_greenb	0000 dddd dddd dddd	0 (0x0000)
R12410 (R0x307A)	test_raw_mode	0000 0000 0000 00dd	0 (0x0000)
R12418 (R0x3082)	operation_mode_ctrl	0000 0000 0000 00??	1 (0x0001)
R12422 (R0x3086)	seq_data_port	dddd dddd dddd dddd	0 (0x0000)
R12424 (R0x3088)	seq_ctrl_port	?d00 00dd dddd dddd	49152 (0xC000)
R12426 (R0x308A)	x_addr_start_cb	0000 dddd dddd dddd	134 (0x0086)
R12428 (R0x308C)	y_addr_start_cb	0000 0ddd dddd dddd	4 (0x0004)
R12430 (R0x308E)	x_addr_end_cb	0000 dddd dddd dddd	2181 (0x0885)
R12432 (R0x3090)	y_addr_end_cb	0000 0ddd dddd dddd	1539 (0x0603)
R12448 (R0x30A0)	x_even_inc	0000 0000 0000 000?	1 (0x0001)
R12450 (R0x30A2)	x_odd_inc	0000 0000 0000 0ddd	1 (0x0001)
R12452 (R0x30A4)	y_even_inc	0000 0000 0000 000?	1 (0x0001)
R12454 (R0x30A6)	y_odd_inc	0000 0000 0000 0ddd	1 (0x0001)
R12456 (R0x30A8)	y_odd_inc_cb	0000 0000 0000 0ddd	1 (0x0001)
R12458 (R0x30AA)	frame_length_lines_cb	dddd dddd dddd dddd	1548 (0x060C)
R12462 (R0x30AE)	x_odd_inc_cb	0000 0000 0000 0ddd	5 (0x0005)
R12464 (R0x30B0)	digital_test	ddd0 0000 d000 0000	32768 (0x8000)

Table 4: Manufacturer-Specific Register List (continued)
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12474 (R0x30BA)	digital_ctrl	0000 0000 ddd0 dddd	44 (0x002C)
R12476 (R0x30BC)	green1_gain_cb	0000 0ddd dddd dddd	128 (0x0080)
R12478 (R0x30BE)	blue_gain_cb	0000 0ddd dddd dddd	128 (0x0080)
R12480 (R0x30C0)	red_gain_cb	0000 0ddd dddd dddd	128 (0x0080)
R12482 (R0x30C2)	green2_gain_cb	0000 0ddd dddd dddd	128 (0x0080)
R12484 (R0x30C4)	global_gain_cb	0000 0ddd dddd dddd	128 (0x0080)
R12494 (R0x30CE)	grr_control1	0000 0000 dddd 0d0d	0 (0x0000)
R12496 (R0x30D0)	grr_control2	0000 0000 dddd dddd	5 (0x0005)
R12498 (R0x30D2)	grr_control3	dddd dddd dddd dddd	4 (0x0004)
R12506 (R0x30DA)	grr_control4	dddd dddd dddd dddd	10 (0x000A)
R12716 (R0x31AC)	data_format_bits	dddd dddd dddd dddd	2570 (0x0A0A)
R12718 (R0x31AE)	serial_format	0000 00dd 0000 0ddd	772 (0x0304)
R12720 (R0x31B0)	frame_preamble	dddd dddd dddd dddd	36 (0x0024)
R12722 (R0x31B2)	line_preamble	dddd dddd dddd dddd	12 (0x000C)
R12724 (R0x31B4)	mipi_timing_0	dddd dddd dddd dddd	9795 (0x2643)
R12726 (R0x31B6)	mipi_timing_1	???? dddd dddd dddd	4430 (0x114E)
R12728 (R0x31B8)	mipi_timing_2	dddd dddd dddd dddd	8264 (0x2048)
R12730 (R0x31BA)	mipi_timing_3	???d dddd dddd dddd	390 (0x0186)
R12732 (R0x31BC)	mipi_timing_4	?d?? ???? ?ddd dddd	32773 (0x8005)
R12734 (R0x31BE)	mipi_config_status	???? ??d? ???? ??dd	8195 (0x2003)
R12736 (R0x31C0)	hispi_timing	dddd dddd dddd dddd	32768 (0x8000)
R12742 (R0x31C6)	hispi_control_status	??dd dddd dddd dddd	32768 (0x8000)
R12752 (R0x31D0)	compression	0000 0000 0000 00dd	0 (0x0000)
R12754 (R0x31D2)	stat_frame_id	dddd dddd dddd dddd	0 (0x0000)

Table 4: Manufacturer-Specific Register List (continued)
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12758 (R0x31D6)	i2c_wrt_checksum	dddd dddd dddd dddd	65535 (0xFFFF)
R12776 (R0x31E8)	horizontal_cursor_position	0000 0ddd dddd dddd	0 (0x0000)
R12778 (R0x31EA)	vertical_cursor_position	0000 dddd dddd dddd	0 (0x0000)
R12780 (R0x31EC)	horizontal_cursor_width	0000 0ddd dddd dddd	0 (0x0000)
R12782 (R0x31EE)	vertical_cursor_width	0000 dddd dddd dddd	0 (0x0000)
R12796 (R0x31FC)	i2c_ids	dddd dddd dddd dddd	12320 (0x3020)
R14208 (R0x3780)	poly_sc_enable	d000 0000 0000 0000	0 (0x0000)

Register Descriptions

Manufacturer Specific Register Descriptions

Table 5: Manufacturer-Specific Register Descriptions
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12288 R0x3000	15:0	0x2604	chip_version_reg (R/W)	N	N
	Model ID. Read-only. Can be made read/write by clearing R0x301A-B[3].				
12290 R0x3002	15:0	0x007C	y_addr_start (R/W)	Y	YM
	The first row of visible pixels to be read out (not counting any dark rows that may be read). To move the image window, set this register to the starting Y value.				
12292 R0x3004	15:0	0x0006	x_addr_start (R/W)	Y	N
	The first column of visible pixels to be read out (not counting any dark columns that may be read). To move the image window, set this register to the starting X value.				
12294 R0x3006	15:0	0x058B	y_addr_end (R/W)	Y	YM
	The last row of visible pixels to be read out.				
12296 R0x3008	15:0	0x0905	x_addr_end (R/W)	Y	N
	The last column of visible pixels to be read out.				
12298 R0x300A	15:0	0x051C	frame_length_lines (R/W)	Y	YM
	The number of complete lines (rows) in the frame timing. This includes visible lines and vertical blanking lines.				
12300 R0x300C	15:0	0x04E0	line_length_pck (R/W)	Y	YM
	The number of pixel clock periods in one line (row) time. This includes visible pixels and horizontal blanking time. Only even values are allowed.				
12302 R0x300E	7:0	0x00	revision_number (R/W)	N	N
12304 R0x3010	15:0	0xBEEF	lock_control (R/W)	N	N
	This register protects the mirror mode select (register read mode). When set to value 0xBEEF, the horizontal and vertical mirror modes can be changed; otherwise these values are locked.				
12306 R0x3012	15:0	0x0010	coarse_integration_time (R/W)	Y	N
	Integration time specified in multiples of line_length_pck_.				
12308 R0x3014	15:0	0x0000	fine_integration_time (R/W)	Y	N
	Fine integration is used to delay the shutter operation after the sample operation is finished. Thus, the integration time is decreased. The resolution is 1 pixel clock time. Note that for short line length (R0x300c, R0x303e) values, the available time for fine shutter is limited. If programmed for more than available time, the normal sensor operation will be disrupted.				
12310 R0x3016	15:0	0x0010	coarse_integration_time_cb (R/W)	N	N
	Coarse integration time in context B.				
12312 R0x3018	15:0	0x0000	fine_integration_time_cb (R/W)	N	N
	Fine integration time in context B.				
12314 R0x301A	15:0	0x0058	reset_register (R/W)	N	Y
	15	0x0000	Reserved		
	14:13	X	Reserved		
	12	0x0000	smia_serialiser_dis This bit disables the serial interfaces (MIPI and HiSPi)	N	N

Table 5: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
	11	0x0000	forced_pll_on When this bit is set, the PLL will be enabled even when the sensor is in "standby" (low power mode).	N	N
	10	0x0000	restart_bad 1: A restart is forced any time a bad frame is detected. This can shorten the delay when waiting for a good frame, since the delay for masking out a bad frame will be the integration time rather than the full-frame time.	N	N
	9	0x0000	mask_bad 0: The sensor will produce bad (corrupted) frames as a result of some register changes. 1: Bad (corrupted) frames are masked within the sensor by extending the vertical blanking time for the duration of the bad frame.	N	N
	8	0x0000	gpi_en 0: The primary input buffers associated with the OE_BAR, TRIGGER and STANDBY inputs are powered down and cannot be used. 1: The input buffers are enabled and can be read through R0x3026-7.	N	N
	7	0x0000	parallel_en 0: The parallel data interface (DOUT[11:0], LINE_VALID, FRAME_VALID, and PIXCLK) is disabled and the outputs are placed in a high-impedance state. 1: The parallel data interface is enabled. The output signals can be switched between a driven and a high-impedance state using output-enable control.	N	N
	6	0x0001	drive_pins 0: The parallel data interface (DOUT[11:0], LINE_VALID, FRAME_VALID, and PIXCLK) may enter a high-impedance state (depending upon the enabling and use of the pad OE_BAR) 1: The parallel data interface is driven. This bit is "do not care" unless bit[7]=1.	N	N
	5	0x0000	Reserved		
	4	0x0001	reset_register_unused	N	Y
	3	0x0001	lock_reg Many parameter limitation registers that are specified as read-only are actually implemented as read/write registers. Clearing this bit allows writing to such registers.	N	N
	2	0x0000	stream Setting this bit places the sensor in streaming mode. Clearing this bit places the sensor in a low power mode. The result of clearing this bit depends upon the operating mode of the sensor. Entry and exit from streaming mode can also be controlled from the signal interface.	Y	N
	1	0x0000	restart This bit always reads as 0. Setting this bit causes the sensor to truncate the current frame at the end of the current row and start resetting (integrating) the first row. The delay before the first valid frame is read out is equal to the integration time.	N	Y
	0	0x0000	reset This bit always reads as 0. Setting this bit initiates a reset sequence: the frame being generated will be truncated.	N	Y
	Controls the operation of the sensor. For details see the bit field descriptions.				

Table 5: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12316 R0x301C	7:0	0x00	mode_select (R/W)	Y	N
	This bit is an alias of R0x301A-B[2].				
12317 R0x301D	7:0	0x00	image_orientation (R/W)	Y	YM
	7:2	X	Reserved		
	1	0x00	vert_flip This bit is an alias of R0x3040[15].	Y	YM
	0	0x00	horiz_mirror This bit is an alias of R0x3040[14].	Y	YM
12318 R0x301E	15:0	0x00A8	data_pedestal (R/W)	N	Y
	Constant offset that is added to pixel values at the end of datapath (after all corrections).				
12321 R0x3021	7:0	0x00	software_reset (R/W)	N	Y
	This bit is an alias of R0x301A-B[0].				
12328 R0x3028	15:0	0x0010	row_speed (R/W)	N	N
	Bits [6:4] of this register define the phase of the output pixclk. Two sets of values are correct: a) 000, 010, 100, 110 => 0 delay (rising edge of pixclk coincides DOUT change). b) 001, 011, 101, 111 => 1/2 clk delay (falling edge of pixclk coincides DOUT change).				
12330 R0x302A	15:0	0x0006	vt_pix_clk_div (R/W)	N	N
	Input is the vt_sys_clk. The output is the vt_pix_clk . The vt_pix_clk is the CLK_PIX when the sensor is configured to use the serial MIPI or HiSPi transmitter. It is the CLK_OP when the sensor is configured to use the parallel interface.				
12332 R0x302C	15:0	0x0001	vt_sys_clk_div (R/W)	N	N
	Divides the input VCO clock and outputs the vt_sys_clk. Set this divider to "2" to enable 2-lane MIPI and "4" to enable 1-lane MIPI. Refer to the sensor datasheet for more details.				
12334 R0x302E	15:0	0x0004	pre_pll_clk_div (R/W)	N	N
	Divides the input clock before being multiplied by the VCO.				
12336 R0x3030	15:0	0x0062	pll_multiplier (R/W)	N	N
	PLL_MULTIPLIER				
12342 R0x3036	15:0	0x000C	op_pix_clk_div (R/W)	N	Y
	Clock divisor applied to the op_sys_clk to generate the output pixel clock. The divisor indicates the bit-depth of the output pixel word. (i.e. "12" 12-bit, "10" 10-bit, "8", 8-bit)				
12344 R0x3038	15:0	0x0001	op_sys_clk_div (R/W)	N	Y
	Clock divisor applied to PLL output clock to generate output system clock. Can only be programmed to "1" in the AR0330 sensor. Read-only.				
12346 R0x303A	15:0	0xFFFF	frame_count (R/W)	N	N
	Counts the number of output frames. At the startup is initialized to 0xffff.				

Table 5: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12348 R0x303C	15:0	0x0000	frame_status (RO)	N	N
	15:2	X	Reserved		
	1	RO	standby_status This bit indicates that the sensor is in standby state. It can be polled after standby is entered to see when the real low-power state is entered, which can happen at the end of row or frame depending on bit R0x301A[4].	N	N
	0	RO	framesync Set on register write and reset on frame synchronization. Acts as debug flag to verify that register writes completed before last frame synchronization.	N	N
12350 R0x303E	15:0	0x04E0	line_length_pck_cb (R/W)	Y	N
	Line length in context b. The number of pixel clock periods in one line (row) time. This includes visible pixels and horizontal blanking time. Only even values are allowed.				

Table 5: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12352 R0x3040	15:0	0x0000	read_mode (R/W)	Y	YM
	15	0x0000	vert_flip 0: Normal readout 1: Readout is flipped (mirrored) vertically so that the row specified by y_addr_end_ (+1) is read out of the sensor first. Changing this register can only be done when streaming is disabled	Y	YM
	14	0x0000	horiz_mirror 0: Normal readout 1: Readout is mirrored horizontally so that the column specified by x_addr_end_ (+1)is read out of the sensor first. Changing this register can only be done when streaming is disabled	Y	YM
	13	0x0000	read_mode_col_bin Column binning mode in context A. Pixel values are averaged in the digital domain. Use when skipping is enabled by setting x_odd_inc.	Y	N
	12	0x0000	read_mode_row_bin Analog row binning control in context A. Use when row-wise skipping is enabled by setting y_odd_inc. The y_addr_start must be an even number when using row binning.	Y	N
	11	0x0000	read_mode_col_bin_cb Column binning mode in context B. Pixel values are averaged in the digital domain. Use when skipping is enabled by setting x_odd_inc.	Y	N
	10	0x0000	read_mode_row_bin_cb Analog row binning control for context B. Use when row-wise skipping is enabled by setting y_odd_inc. The y_addr_start must be an even number when using row binning.	Y	N
	9	0x0000	read_mode_col_sf_bin_en Column analog binning control for context A. Use when skipping is enabled by setting x_odd_inc.	Y	N
	8	0x0000	read_mode_col_sf_bin_en_cb Column analog binning control for context B. Use when skipping is enabled by setting x_odd_inc.	Y	N
	7:6	X	Reserved		
	5	0x0000	read_mode_col_sum Column sum mode. Pixel values are summed in the digital domain. Use when skipping is enabled by setting x_odd_inc.	Y	N
	4:0	X	Reserved		
12354 R0x3042	15:0	0x0000	extra_delay (R/W)	Y	N
	The last row in the frame is extended by the number of the sensor core clock periods specified here. The extra_delay must be configured to an even value. This register can be used to fine-tune the sensor maximum frame-rate.				

Table 5: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12358 R0x3046	15:0	0x0000	flash (R/W)	Y	Y
	15	RO	strobe Reflects the current state of the FLASH output signal. Read-only.	N	N
	14	RO	triggered Indicates that the FLASH output signal was asserted for the current frame. Read-only.	N	N
	13:9	X	Reserved		
	8	0x0000	en_flash Enables the flash. The flash is asserted when an integration (either T1, T2 or T3 is ongoing).	Y	Y
	7	0x0000	invert_flash Invert flash output signal. When set, the FLASH output signal will be active low.	N	N
	6	X	Reserved		
	5:3	0x0000	xenon_frames_enable XENON_FRAMES_ENABLE[2:0] 0: Xenon flash disabled. 1-6: Number of frames with Xenon flash. 7 : Xenon flash enable for all frames.	N	N
	2:0	0x0000	xenon_frames_delay XENON_FRAMES_DELAY[2:0]: Number of the frames before the first time Xenon flash is actuated.	Y	N
	See bit fields for definition of flash and Xenon Flash control.				
12360 R0x3048	15:0	0x0100	flash2 (R/W)	N	N
	Xenon flash pulse width in clock periods.				
12374 R0x3056	15:0	0x0080	green1_gain (R/W)	Y	N
	Digital gain for green1 (Gr) pixels, in format of xxxx.yyyyyyy.				
12376 R0x3058	15:0	0x0080	blue_gain (R/W)	Y	N
	Digital gain for Blue pixels, in format of xxxx.yyyyyyy.				
12378 R0x305A	15:0	0x0080	red_gain (R/W)	Y	N
	Digital gain for Red pixels, in format of xxxx.yyyyyyy.				
12380 R0x305C	15:0	0x0080	green2_gain (R/W)	Y	N
	Digital gain for green2 (Gb) pixels in format of xxxx.yyyyyyy.				
12382 R0x305E	15:0	0x0080	global_gain (R/W)	Y	N
	Writing a gain to this register is equivalent to writing that code to each of the 4 color-specific gain registers. Reading from this register returns the value most recently written to the green1_gain register.				
12384 R0x3060	15:0	0x0000	analog_gain (R/W)	Y	N
	15:14	X	Reserved		
	13:12	0x0000	coarse_gain_cb Coarse analog gain in context B.	Y	N
	11:8	0x0000	fine_gain_cb Fine analog gain in context b	Y	N
	7:6	X	Reserved		
	5:4	0x0000	coarse_gain Coarse analog gain in context A.	Y	N

Table 5: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
	3:0	0x0000	fine_gain Fine analog gain in context A.	Y	N
	Defines analog gains for both contexts				
12388 R0x3064	15:0	0x1902	smia_test (R/W)	N	N
	15:13	X	Reserved		
	12	0x0001	Reserved		
	11:10	0x0002	Reserved		
	9	0x0000	Reserved		
	8	0x0001	embedded_data 1: Frames of data out of the sensor include 2 rows of embedded data. 0: Frames out of the sensor exclude the embedded data. This register field should only be change while the sensor is in software standby. Disabling the embedded data will not reduce the number of vertical blanking rows.	N	N
	7:4	X	Reserved		
	3:0	0x0002	Reserved		
12394 R0x306A	15:0	0x0000	datapath_status (RO)	Y	N
	15:6	X	Reserved		
	5	0x0000	mipi_preamble_error MIPI_PREAMBLE_ERROR	N	N
	4	0x0000	mipi_line_byte_error	N	N
	3:0	X	Reserved		

Table 5: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12398 R0x306E	15:0	0x9010	datapath_select (R/W)	N	N
	15:13	0x0004	slew_rate_ctrl_parallel Selects the slew (edge) rate for the DOUT[9:0], FRAME_VALID, LINE_VALID and FLASH outputs. Only affects the FLASH output when parallel data output is disabled. The value 7 results in the fastest edge rates on these signals. Slowing down the edge rate can reduce ringing and electro-magnetic emissions.	N	N
	12:10	0x0004	slew_rate_ctrl_pixclk Selects the slew (edge) rate for the PIXCLK output. Has no effect when parallel data output is disabled. The value 7 results in the fastest edge rates on this signal. Slowing down the edge rate can reduce ringing and electromagnetic emissions.	N	N
	9	0x0000	high_vcm Configures the sensor to use the normal or high VCM mode in the AR0330 sensor. 0: Low Vcm. VDD_HiSPI_TX = 0.4V - 0.8V 1: High Vcm. VDD_HISPI_TX = 1.7V - 1.9V This register must be changed when the sensor streaming is disabled. (R0x301A[2]=0)	N	N
	8	0x0000	datapath_select_bit8 Not used.	N	N
	7:5	X	Reserved		
	4	0x0001	Reserved		
	3:2	X	Reserved		
	1:0	0x0000	special_line_valid 00: Normal behavior of LINE_VALID 01: LINE_VALID is driven continuously (continue generating LINE_VALID during vertical blanking) 10: LINE_VALID is driven continuously as LINE_VALID XOR FRAME_VALID	N	N
12400 R0x3070	15:0	0x0000	test_pattern_mode (R/W)	N	Y
	0: Normal operation. Generate output data from pixel array 1: Solid color test pattern. 2: Full color bar test pattern 3: Fade-to-gray color bar test pattern 256: Walking 1s test pattern (12 bit) Other: Reserved.				
12402 R0x3072	15:0	0x0000	test_data_red (R/W)	N	Y
	The value for red pixels in the Bayer data used for the solid color test pattern and the test cursors.				
12404 R0x3074	15:0	0x0000	test_data_greenr (R/W)	N	Y
	The value for green pixels in red/green rows of the Bayer data used for the solid color test pattern and the test cursors.				
12406 R0x3076	15:0	0x0000	test_data_blue (R/W)	N	Y
	The value for blue pixels in the Bayer data used for the solid color test pattern and the test cursors.				

Table 5: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12408 R0x3078	15:0	0x0000	test_data_greenb (R/W)	N	Y
	The value for green pixels in blue/green rows of the Bayer data used for the solid color test pattern and the test cursors.				
12410 R0x307A	15:0	0x0000	test_raw_mode (R/W)	N	N
	15:2	X	Reserved		
	1	0x0000	Reserved		
	0	0x0000	Reserved		
12418 R0x3082	15:0	0x0001	operation_mode_ctrl (RO)	N	N
	15:2	X	Reserved		
	1:0	RO	Reserved		
12422 R0x3086	15:0	0x0000	seq_data_port (R/W)	N	N
	Register used to write to or read from the sequencer RAM.				
12424 R0x3088	15:0	0xC000	seq_ctrl_port (R/W)	N	N
	15	RO	sequencer_stopped Showing that sequencer is stopped (STANDBY mode) and the RAM is available for read or write.	N	N
	14	0x0001	auto_inc_on_read If 1 => The access_address is incremented (by 1) after each read operation from seq_data_port (which returns only1 byte)	N	N
	13:9	X	Reserved		
	8:0	0x0000	access_address When in STANDBY (not streaming) mode: address pointer to the sequencer RAM.	N	N
	Register controlling the read and write to sequencer RAM.				
12426 R0x308A	15:0	0x0086	x_addr_start_cb (R/W)	N	N
	x_address_start context B				
12428 R0x308C	15:0	0x0004	y_addr_start_cb (R/W)	N	N
	Y_ADDR_START for context B				
12430 R0x308E	15:0	0x0885	x_addr_end_cb (R/W)	N	N
	X_ADDR_END for context B				
12432 R0x3090	15:0	0x0603	y_addr_end_cb (R/W)	N	N
	Y_ADDR_END for context B				
12448 R0x30A0	15:0	0x0001	x_even_inc (RO)	N	N
	Read-only.				
12450 R0x30A2	15:0	0x0001	x_odd_inc (R/W)	Y	YM
	1 : No skip. 3: Skip 2. 5: Skip 3. Other values are not supported.				
12452 R0x30A4	15:0	0x0001	y_even_inc (RO)	N	N
	Read-only.				
12454 R0x30A6	15:0	0x0001	y_odd_inc (R/W)	Y	YM
	1 : No skip. 3: Skip 2. 5: Skip 3. Other values are not supported.				

Table 5: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12456 R0x30A8	15:0	0x0001	y_odd_inc_cb (R/W)	N	N
	Y_ODD_INC context B				
12458 R0x30AA	15:0	0x060C	frame_length_lines_cb (R/W)	N	N
	FRAME_LENGTH_LINES context B. See description for R0x300a				
12462 R0x30AE	15:0	0x0005	x_odd_inc_cb (R/W)	N	N
	X_ODD_INC context B				
12464 R0x30B0	15:0	0x8000	digital_test (R/W)	N	Y
	15	0x0001	Reserved		
	14	0x0000	Reserved		
	13	0x0000	context_b 0: Use context A 1: Use Context B	N	N
	12:0	X	Reserved		
12474 R0x30BA	15:0	0x002C	digital_ctrl (R/W)	Y	N
	15:8	X	Reserved		
	7	0x0000	Reserved		
	6	0x0000	Reserved		
	5	0x0001	dither_enable Enables dithering after digital gain.	N	N
	4	X	Reserved		
	3:2	0x0003	Reserved		
	1:0	0x0000	Reserved		
12476 R0x30BC	15:0	0x0080	green1_gain_cb (R/W)	N	N
	Digital gain green1 context B				
12478 R0x30BE	15:0	0x0080	blue_gain_cb (R/W)		
	digital gain blue context B				
12480 R0x30C0	15:0	0x0080	red_gain_cb (R/W)	N	N
	digital gain red context B				
12482 R0x30C2	15:0	0x0080	green2_gain_cb (R/W)		
	digital gain green 2 context B				
12484 R0x30C4	15:0	0x0080	global_gain_cb (R/W)	N	N
	global digital gain context B				

Table 5: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12494 R0x30CE	15:0	0x0000	grr_control1 (R/W)	N	N
	15:8	X	Reserved		
	7	0x0000	shutter_always_open 1: 1The shutter pin will always be asserted (OPEN) in GRR mode.	N	N
	6	0x0000	shutter_disable 1: The shutter pin will be disabled (CLOSED) in GRR mode.	N	N
	5	0x0000	frame_start_mode 1: The sensor will match the frame time to the frame length lines and line_length_pck. It will not increase the frame time even if the integration time specified by coarse integration time is longer than the minimum frame-time.	N	N
	4	0x0000	slave_mode 1: The sensor readout start will be synchronized with the rising edge of the input trigger signal. (applied to pad TRIGGER).	N	N
	3	X	Reserved		
	2	0x0000	Reserved		
	1	X	Reserved		
	0	0x0000	grr_mode 0: Normal ERS mode. 1: Global reset release mode.	N	N
12496 R0x30D0	15:0	0x0005	grr_control2 (R/W)		
	15:8	X	Reserved		
	7:0	0x0005	gr_delay Delay between external trigger and global reset in number of rows.	N	N
12498 R0x30D2	15:0	0x0004	grr_control3 (R/W)	N	N
	15:0	0x0004	ext_shut_pulse_width Width of the external shutter pulse in clock cycles. 0: The shutter pulse will be controlled by GRR_CONTROL4.	N	N
12506 R0x30DA	15:0	0x000A	grr_control4 (R/W)	N	N
	15:0	0x000A	ext_shut_delay	N	N
	Delay between external trigger and close of external shutter in number of rows.				
12716 R0x31AC	15:0	0x0A0A	data_format_bits (R/W)	Y	N
	[7:0] = The bit-width of the compressed pixel data [15:8] = The bit-width of the uncompressed pixel data				
12718 R0x31AE	15:0	0x0304	serial_format (R/W)	N	N
	When the serial interface is enabled (reset_register[12]=0), this register controls which serial interface is in use. Any non-zero serial_format_descriptor value is a legal value for this register. The upper byte of this register (interface type) is read-only. The lower byte is read/write.				
12720 R0x31B0	15:0	0x0024	frame_preamble (R/W)	N	N
	MIPI timing configuration: Number of clock cycles for frame short packet and transition from LP to HS.				
12722 R0x31B2	15:0	0x000C	line_preamble (R/W)	N	N
	MIPI timing: Number of clock cycles for line transition from LP to HS.				

Table 5: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12724 R0x31B4	15:0	0x2643	mipi_timing_0 (R/W)	N	N
	15:12	0x0002	mipi_timing_0_t_hs_prepare Time (in clk cycles) to drive LP-00 prior to entering HS data transmission mode	N	N
	11:8	0x0006	t_hs_zero Time, in op_pix_clk periods, to drive HS-0 before the sync sequence	N	N
	7:4	0x0004	t_hs_trail Time, in op_pix_clk periods, to drive flipped differential state after last payload data bit of an HS transmission burst	N	N
	3:0	0x0003	t_clk_trail Time, in op_pix_clk periods, to drive HS differentialstate after last payload clock bit of an HS transmission burst	N	N
12726 R0x31B6	15:0	0x114E	mipi_timing_1 (R/W)	N	N
	15:12	RO	reserved Reserved. Read as 0	N	N
	11:6	0x0005	t_hs_exit Time, in op_pix_clk periods, to drive LP-11 after HS burst	N	N
	5:0	0x000E	t_clk_zero Minimum time, in op_pix_clk periods, to drive HS-0 on clock lane prior to starting clock	N	N
12728 R0x31B8	15:0	0x2048	mipi_timing_2 (R/W)		
	15:12	0x0002	t_bgap bandgap settling time. This is the top 4 bits of a 5 bit register. The lsb is tied to 1. Time to enable the bandgap before driving the LP drivers in 512 clk cycles	N	N
	11:6	0x0001	t_clk_pre Time, in op_pix_clk periods, to drive the HS clock before any data lane might start up	N	N
	5:0	0x0008	t_clk_post Time, in op_pix_clk periods, to drive the HS clock after the data lane has gone into low-power mode	N	N
12730 R0x31BA	15:0	0x0186	mipi_timing_3 (R/W)	N	N
	15:13	RO	reserved Reserved. Read as 0	N	N
	12:7	0x0003	t_lpx Time, in op_pix_clk periods, of any low-power state period	N	N
	6:0	0x0006	t_wake_up Time to recover from ultra low-power mode (ULPM). ULPM is exited by applying a mark state for (8192) * T_WAKE_UP * op_pix_clk	N	N

Table 5: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12732 R0x31BC	15:0	0x8005	mipi_timing_4 (R/W)		
	15	RO	cont_tx_clk Reserved. Read as 0	N	N
	14	0x0000	mipi_heavy_lp_load contol of phy heavy_lp_load pin	N	N
	13:7	RO	reserved_0 Reserved. Read as 0	N	N
	6:0	0x0005	t_init Initialization time when first entering stop state (LP-11) after powerup or reset. LP-11 is transmitted for a minimum of (1024) * T_INIT * op_pix_clk.	N	N
12734 R0x31BE	15:0	0x2003	mipi_config_status (R/W)	N	N
	15:10	RO	reserved_1 Reserved. Read as 0	N	N
	9	0x0000	start_checksum start checksum 1: 16-bit checksum will be calculated over the next complete frame	N	N
	8:2	RO	reserved_0 Reserved. Read as 0	N	N
	1:0	0x0003	frame_cnt_mode MIPI frame start and frame end short packets contain a 16-bit frame number field. The behaviour of the frame number field is controlled as follows: 0: The frame number is always set to 0. 1: The frame number is reset during sensor reset. The frame number for the first frame generated in streaming mode after reset is 1, and the frame number increments for subsequent frames. The frame number wraps from 0xFF to 0x01. 2: The frame number is reset when the sensor is in the software standby system state. The frame number for the first frame generated in streaming mode is 1, and the frame number increments for subsequent frames. The frame number wraps from 0xFF to 0x01. 3: Reserved.	N	N

Table 5: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12736 R0x31C0	15:0	0x8000	hispi_timing (R/W)		
	15	0x0001	Reserved		
	14:12	0x0000	clock_del Delay applied to the clock lane in 1/8 unit interval (UI) steps.	N	N
	11:9	0x0000	data3_del Delay applied to Data Lane 3 in 1/8 unit interval (UI) steps.	N	N
	8:6	0x0000	data2_del Delay applied to Data Lane 2 in 1/8 unit interval (UI) steps.	N	N
	5:3	0x0000	data1_del Delay applied to Data Lane 1 in 1/8 unit interval (UI) steps.	N	N
	2:0	0x0000	data0_del Delay applied to Data Lane 0 in 1/8 unit interval (UI) steps.	N	N
	Within the HiSPi PHY there is a DLL connected to the clock lane and each data lane, which acts as a control master for the output delay buffers. This additional delay allows the user to increase the setup or hold time at the receiver circuits and can be used to compensate for skew introduced in PCB design. If the DLL timing adjustment is not required, the data and clock lane delay settings should be set to a default code of 0x000 to reduce jitter, skew, and power dissipation.				

Table 5: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
12742 R0x31C6	15:0	0x8000	hispi_control_status (R/W)		
	15:14	X	Reserved		
	13	0x0000	Reserved		
	12	X	Reserved		
	11:10	0x0000	hispi_mode_sel Select the HiSPi output protocol: b00: Streaming S b01: Streaming SP or Packetized SP note: Use the streaming_mode parameter to configure between Streaming SP and Packetized SP.	N	N
	9	0x0000	Reserved		
	8	0x0000	Reserved		
	7	0x0000	test_enable When asserted, the test pattern is output through the HiSPi PHY interface.	N	N
	6:4	0x0000	test_mode For the MIPI interface: 0: Transmit LP-00 on all enabled data and clock lanes 1: Transmit LP-11 on all enabled data and clock lanes 2: Transmit HS-0 on all enabled data and clock lanes 3: Transmit HS-1 on all enabled data and clock lanes 4: Transmit a square wave at half the potential serial data rate on all enabled data and clock lanes 5: Transmit a square wave at the pixel data rate on all enabled data and clock lanes 6: Transmit a LP square wave at half the pixel data rate on all enabled data and clock lanes 7: Tansmit a continuous, repeated, sequence of pseudo random data (non-packetized), copied on all enabled data lanes For the HiSPi interface: 0: Reserved 1: Reserved 2: Transmit differential 0 on all enabled data lanes 3: Transmit differential 1 on all enabled data lanes 4: Transmit a square wave at half the potential serial data rate on all enabled data lanes 5: Transmit a square wave at the pixel data rate on all enabled data lanes 6 : Reserved 7: Transmit a continuous, repeated, sequence of pseudo random data, with no SAV code, copied on all enabled data lanes	N	N
	3	0x0000	blanking_data_enable This parameter allows the user to define the idle (IDL) data output during horizontal and vertical blanking periods. This parameter will affect the HiSPi transmitter when it is configured to Streaming SP. O: The default pattern (constant 1) is output during horizontal and vertical blanking periods !: The pattern defined by the blanking_data input is output during horizontal and vertical blanking periods	N	N

Table 5: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
	2	0x0000	streaming_mode This register bit can be used to configure the HiSPi output between the Streaming SP and Packetized SP protocol. This register bit is only effective when hispi_mode_sel is configured to "1". 0: Data will be transmitted in 'packetized' format when hispiSP protocol is selected 1: Data will be transmitted in 'streaming' format when hispiSP protocol is selected	N	N
	1	0x0000	output_msb_first Configures the active data transmitted by the HiSPi interface to MSB or LSB. 0: Active data will be in LSB 1: Active data will be in MSB Note: The SYNC code and idle (IDL) data are not affected by the output_msb_first bit.	N	N
	0	0x0000	vert_left_bar_en Inserts the optional filler (FLR) data described in the HiSPi protocol specification. When the filler codes are enabled, the receiver must window the received image to eliminate first 4 data words (columns per PHYs).	N	N
	HiSPi Control status for the output PHY.				
12752 R0x31D0	15:0	0x0000	compression (R/W)	N	N
	15:1	X	Reserved		
	0	0x0000	compression_enable Enables A-LAW compression. Inputs 12-bit RAW pixel data. Outputs 10-bit compressed data using A-LAW compression.	N	N
12754 R0x31D2	15:0	0x0000	stat_frame_id (R/W)		
12758 R0x31D6	15:0	0xFFFF	i2c_wrt_checksum (R/W)		
	Checksum of I2C write operations.				
12776 R0x31E8	15:0	0x0000	horizontal_cursor_position (R/W)		
	Specify the start row for the test cursor.				
12778 R0x31EA	15:0	0x0000	vertical_cursor_position (R/W)		
	Specify the start column for the test cursor.				
12780 R0x31EC	15:0	0x0000	horizontal_cursor_width (R/W)		
	Specify the width, in rows, of the horizontal test cursor. A width of 0 disables the cursor.				
12782 R0x31EE	15:0	0x0000	vertical_cursor_width (R/W)		
	Specify the width, in columns, of the vertical test cursor. A width of 0 disables the cursor.				
12796 R0x31FC	15:0	0x3020	i2c_ids (R/W)	N	N
	I2C addresses.				

Table 5: Manufacturer-Specific Register Descriptions (continued)
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
14208 R0x3780	15:0	0x0000	poly_sc_enable (R/W)	N	N
	15	0x0000	enable Turn on shading correction.	N	N
	14:0	X	Reserved		
	When POLY_SC_ENABLE bit is set poly_sc will generate polynomial function and correct stream of pixels. When not set poly_sc will bypass data.				

Revision History

Rev. C 11/10/14

- Updated to Production
- Applied ON Semiconductor template

Rev. B 5/23/11

- Updated to Preliminary
- Updated to Rev 2 database
- Updated document number in footer to reflect change in file location

Rev. A 1/18/11

- Initial release