INDIAN INSTITUTE OF TECHNOLOGY GUWAHATI

EE 311: VLSI LAB

July-Nov 2016

Assignment 4

6th September 2016

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NOTE: IF PICTURE ARE UNCLEAR, SCREENSHOTS ARE THERE IN FOLDER.

Objective:

To design an AND Gate using NAND Gate and NOT Gate with following specification:

1. Input Frequency, f = 400 MHz
2. Load Capacitance, C_L = 300 fF
3. Worst case risetime, falltime = 5 % of input time period

Calculations:

Given input frequencies = 400 MHz. Therefore time period of input T = 2.5ns.

Rise Time, t_r = Fall Time, t_f = 5 % of T

=> $t_r = t_f = 0.05 * 2.5$ ns = 0.125ns

This is the worst case scenario. We have to keep the risetime and falltime less than this.

We can find charging and discharging of capacitor between 10% to 90% using following equation:

$$t = 2.2 * R_{eq} * C_L$$

Since,

$$t <= t_r$$

$$\Rightarrow \quad 2.2 * R_{eq} * C_L <= 0.125\text{ns}$$

$$\Rightarrow \quad R_{eq} <= 189.4\ \Omega \qquad \text{----------(i)}$$

For NMOS,

R_{NORM} = 3660 Ω, and since $R_{eq} = R_{NORM} / m_n$ where m_n is the multiplicity of NMOS,

$$\Rightarrow \quad m_n >= 19.32$$

For PMOS,

R_{NORM} = 10980 Ω, and since $R_{eq} = R_{NORM} / m_p$ where m_p is the multiplicity of PMOS,

=> $m_p >= 58$

So for this assigment, I have chosen $m_n = 24$ and $m_p = 60$.

Therefore expected value of risetime:

$$t = 2.2 * R_{eq} * C_L$$

=> $t_r = 120.78$ ps

Therefore expected value of falltime:

$$t = 2.2 * R_{eq} * C_L$$

=> $t_r = 100.65$ ps

Hence width chosen was for PMOS, with finger = 2:

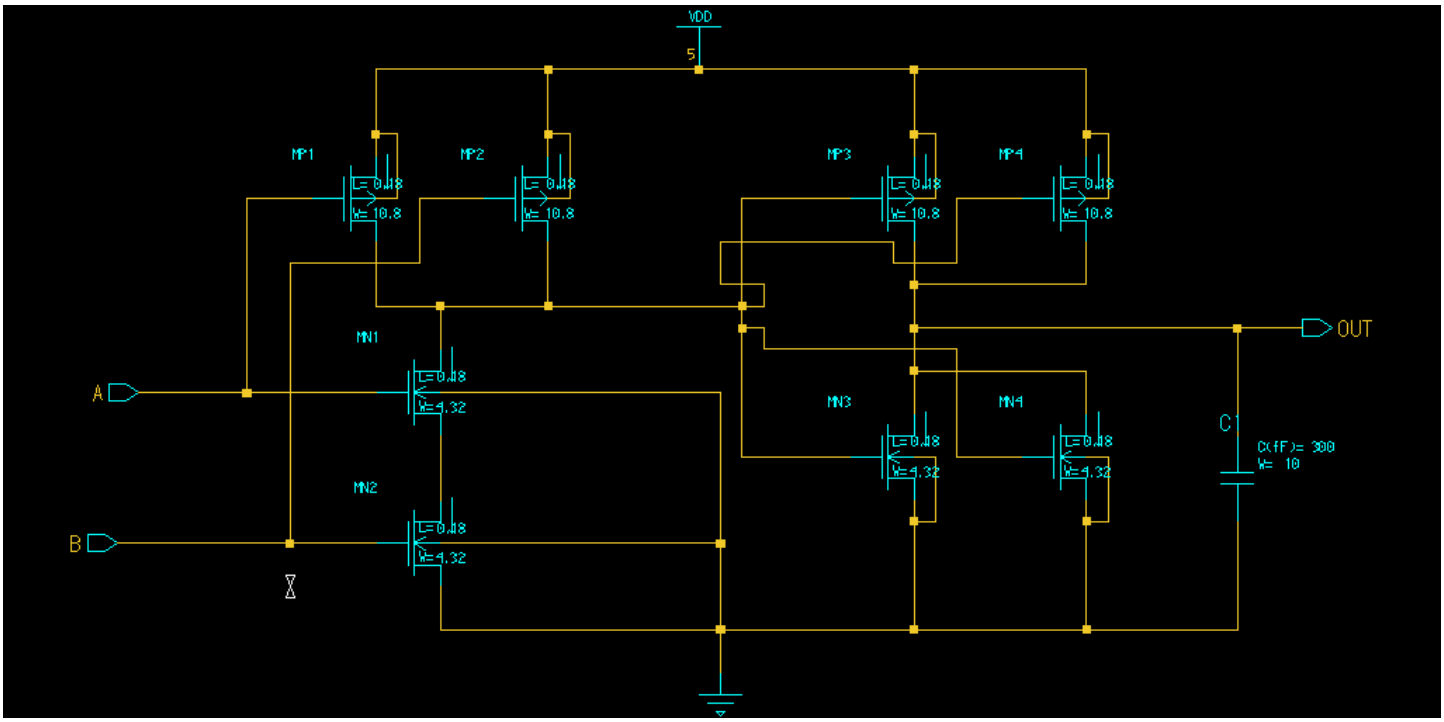
$w = (m_p / 2) * 0.36 = 10.8u$

Hence width chosen was for NMOS, with finger = 2:

$w = (m_n / 2) * 0.36 = 4.32u$

Schematic:

1. Screenshot:

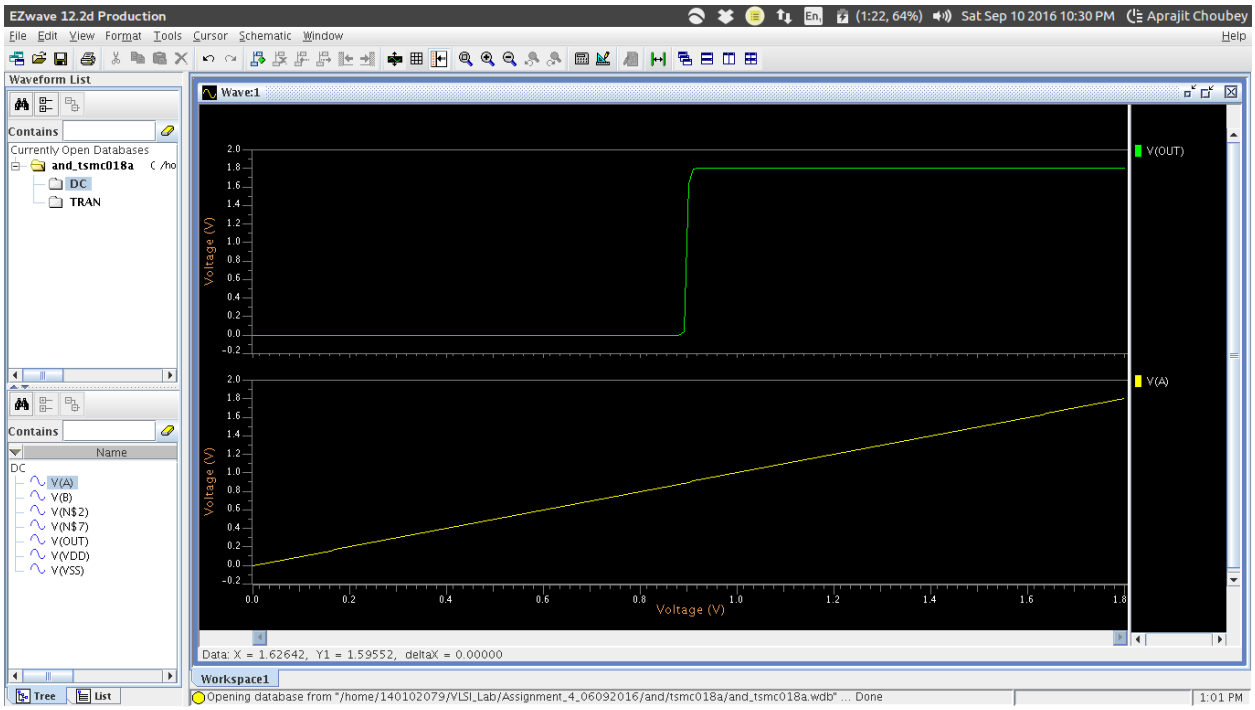


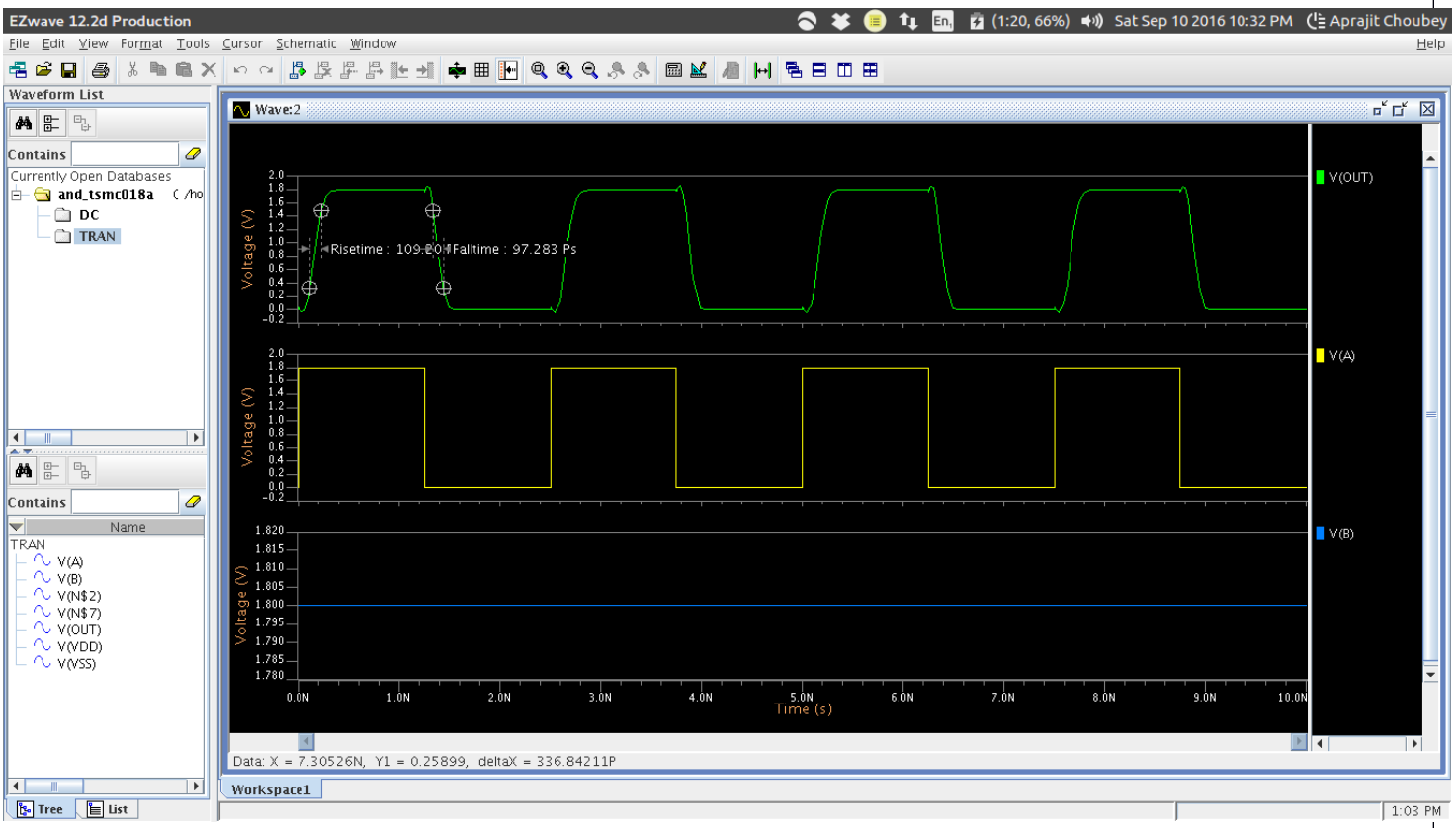
Observed:

1. Case I: Rise Time = 109.204ps Fall Time = 97.283ps
2. Case II: Rise Time = 114.09ps Fall Time = 101.59ps

2. Simulation:

I) A – Pulse, B – High





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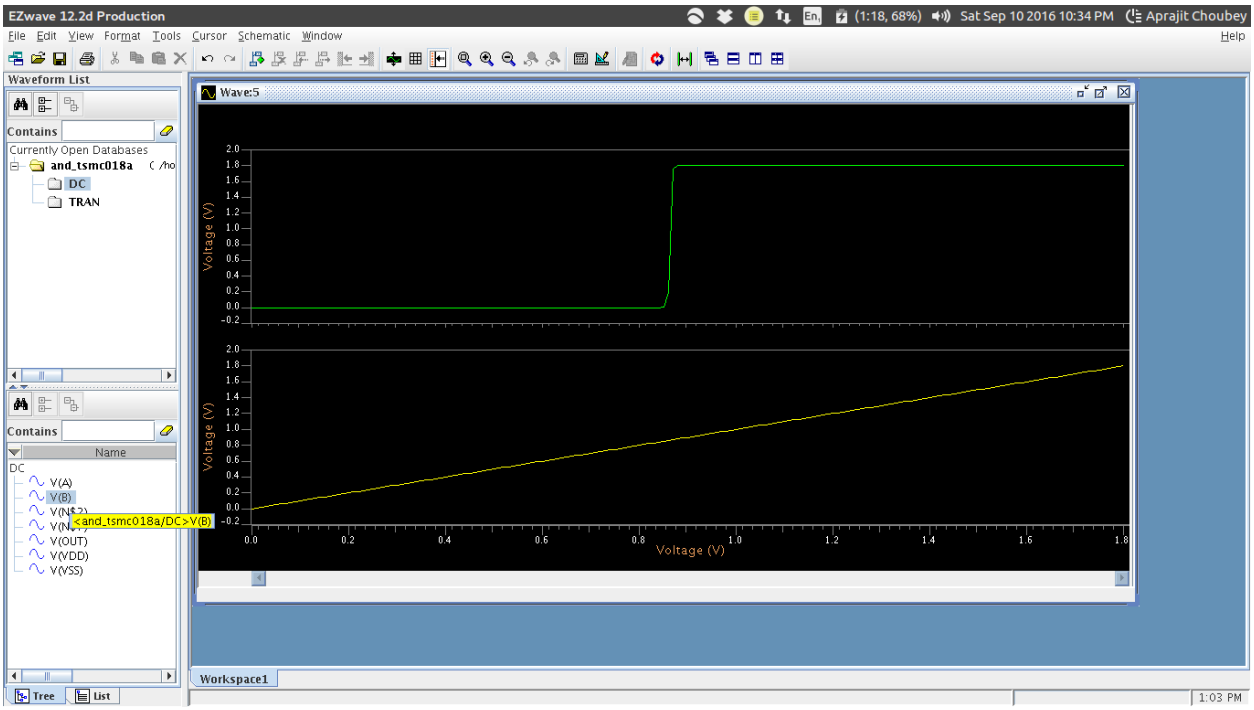
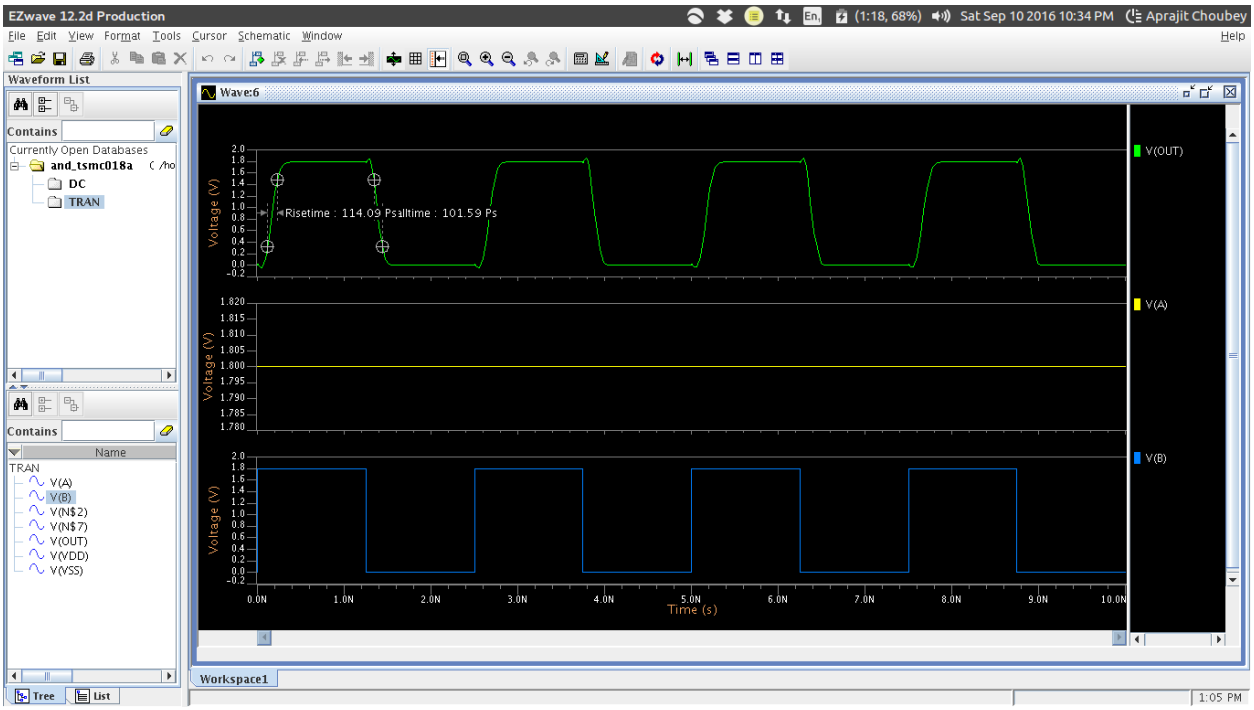
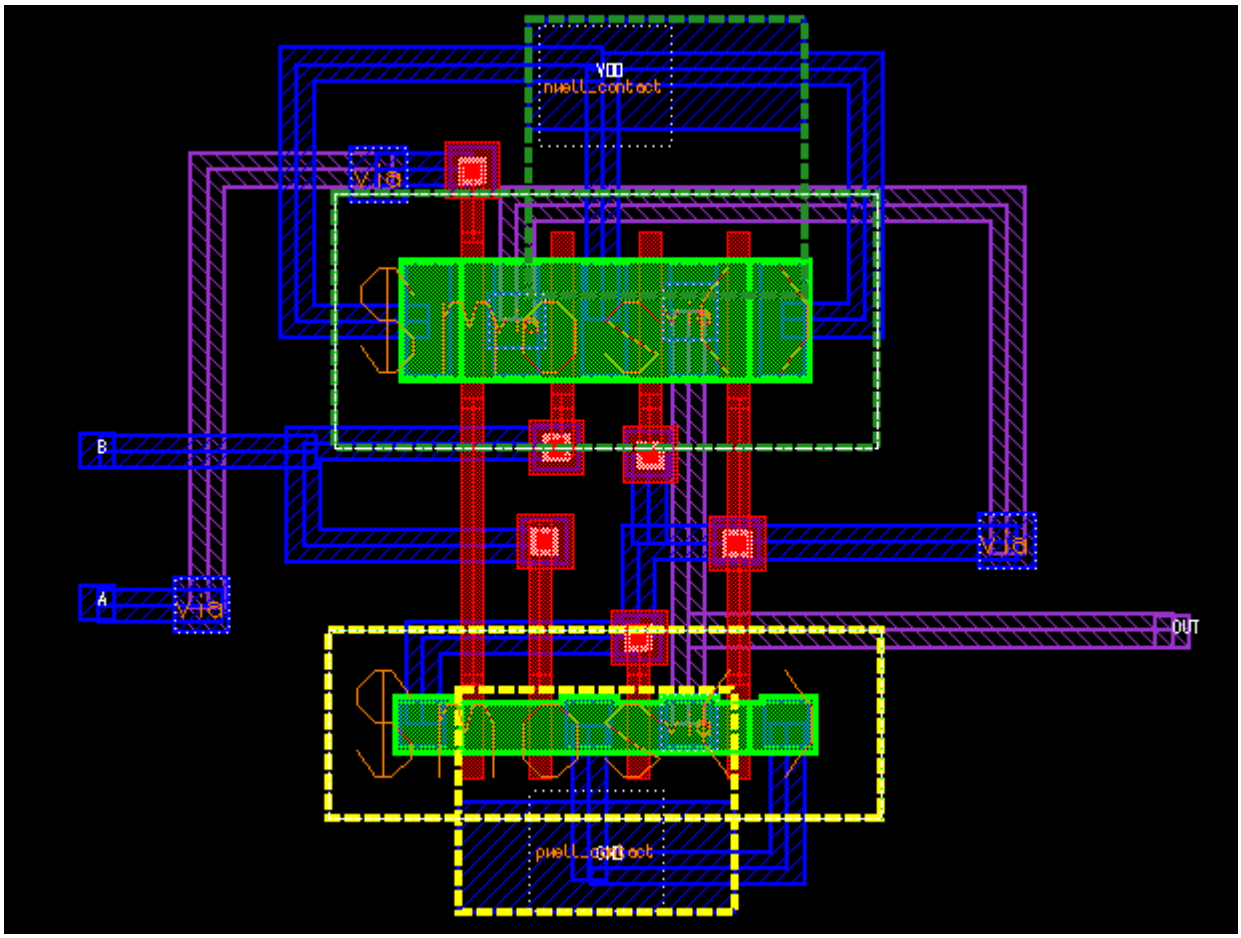
I) A – Pulse, B – High





Layout:

1. Screenshot:



Observed:

1. Rise Time = 118.85ps Fall Time = 113.33ps

2. Post Layout Simulation: