

# Zain Siddavatam

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## Education

### Veermata Jijabai Technological Institute

December 2021 – Present

*B.Tech Student in Electrical Engineering*

*Mumbai*

- Relevant coursework: Analog and Digital Circuits 9/10, Electronic Devices and Circuits 10/10, Control Systems 9/10, Microprocessors and Microcontrollers 10/10.

## Experiences

### Embedded Software Engineer Intern at Beagleboard.org

*Verilog HDL, TCL, Polarfire SoCs, ARM AMBA, C/C++*

*June 2024 - September 2024*

- Created CI workflow for generating custom Debian GNU/Linux images for the **BeagleY-AI** single-board computer.
- Contributed to the documentation and on-boarding examples for **BeagleV-Fire** single-board computer.
- Added support for industrial communication addon board for the BeagleV-Fire thus allowing **CAN**, **RS485**, and **4-20 mA current loop** peripherals.
- Created examples demonstrating the usage of **AXI4** and **APB3 peripherals** on the BeagleV-Fire's **PolarFire MPFS025T SoC**. These examples enable users to control peripherals from Linux using C/C++.

### Hardware Acceleration Intern at Acceleration Robotics

*C++/C, Vitis HLS, Vivado, KV260, Kria Robotics Stack*

*January 2024 - June 2024*

- Accelerated **ROS2** workloads by optimizing **Adaptive Monte-Carlo Localization (AMCL)**.
- Designed and deployed a ROS2 node with a kernel for an accelerated particle filter algorithm on the **KV260** platform.
- Developed a custom KV260 platform in Vivado for HLS kernel deployment, achieving a **1.95x speedup** over the onboard SoC's CPU.

### Research Intern at CASL, University of Maryland

*C++/C, Vitis HLS, Vivado*

*February 2023 - October 2023*

- Researched Domain-Specific Architectures, focusing on dataflows for Sparse Matrix General Matrix Multiplication (SpGEMM).
- Conducted a comprehensive survey of prevalent techniques used in SpGEMM.
- Implemented two sparse matrix multiplication algorithms using **Vitis High-Level Synthesis (HLS)**: an **Outer Product dataflow** and a **Row Product dataflow**.

## Projects

### Hackathon: RISC-V Softmax Microcode (RISC-V Intl. x Andes)

*RISC-V Spike, C, Inline Assembly, Performance Optimization*

*April 2025*

- Implemented a custom **softmax instruction** for RISC-V CPUs, using **inline assembly** and **C** for microcode generation.
- Increased signal-to-noise ratio and improved execution speed by **50%** using a custom **exp function** via **Estrin's scheme**.
- Awarded the **Favourite Implementation Prize** for performance improvements and approach.

### 32-bit RISC-V CPU Design & Verification

*Verilog HDL, Cyclone II, Quartus Prime*

*August 2022, May 2025*

- Implemented a **5-stage RV32I-compliant** CPU core in Verilog and deployed it on a Cyclone II FPGA with seven-segment display output.
- Built a custom assembler for RV32I instructions and ran example programs like Fibonacci sequence.
- Verified the CPU using Cocotb with Python-based testbenches and instruction tests from the official RISC-V ISA test suite.
- Developed monitors, scoreboards, and self-checking test cases to catch bugs in ALU ops, branching, etc.

### WiFi Controlled Bot

*C/C++, ESP-IDF framework*

*April 2022 - May 2022*

- Developed a **remote controlled bot** using ESP-32.
- Used the **WiFi** onboard the ESP32 for relaying data from the car.
- **FreeRTOS** is used to facilitate the task of moving as well as relaying data.
- Implemented a web page for remote control, which can accept touch as well as keyboard inputs.

## Habitica Sync [↗](#)

*Typescript, React, NodeJS*

2021

- Developed a widget for the Obsidian note taking app, for allowing users to access their tasks and rewards from the widely used Habitica Todo-list application.
- Designed a UI using react and material-ui, and integrated habitica's features using their API.
- The widget received 1000+ downloads from Obsidian's plugin store.

## Google Code-in [↗](#)

*Java, CSS, HTML, Javascript*

2017, 2018

- Mentee in Google Code-In contest, mentored by open source companies. [↗](#)
- Developed a **terrain generator**, to generate different kinds of blocks at different rarities and vary terrain features at different heights. [↗](#).
- Composed **two web pages** for BRL-CAD, an about page and an onepager website. [↗](#) [↗](#).

## Competitions

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### Competition: FPGA-based Maze Solving Robot [↗](#)

*Verilog, Quartus, SPI/UART*

Sept 2022 – Jan 2023

- Created a **maze-solving robot** on **Cyclone IV FPGA** using Verilog, implementing PID control and Dijkstra's algorithm for pathfinding.
- Integrated sensor data via **onboard ADCs, SPI, and UART** for communicating with the host via ZigBee.
- Advanced to Stage 2 in the E-Yantra national-level robotics challenge.

## Technical Skills, Language Skills

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**Programming Languages:** Verilog HDL, TL-Verilog, C/C++, Python, Java, JavaScript, TypeScript

**Hardware Frameworks:** Quartus Prime, Vivado, Vitis HLS, ESP-IDF Toolchain

**Software Frameworks:** Linux, OpenCV, Numpy, ReactJS, NodeJS, Git, CocoTB, UVM (familiar)

**Hardware Platforms:** Arty A7, Cyclone, iCE40, Zynq SoCs, Kria KV260

**Languages:** English (Fluent)

## Extracurricular

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### Joint General Secretary - Society of Robotics and Automation, VJTI

*Student-run robotics and automation club [↗](#)*

May 2023 – May 2024

- Oversee the day-to-day management of the club, including strategic planning, event coordination, and team leadership for a 40-member strong team.
- Successfully organized and conducted workshops for 200+ first-year students on cutting-edge topics, such as ESP-32 based Line following robots, Image Processing, and ROS based 3-DOF manipulators. These workshops provided hands-on experience and introduced newcomers to advanced robotics concepts.
- Pioneered the Eklavya Mentorship Program, a two-month initiative, guiding three teams second-year students through FPGA-based projects.