SERDES RTL DESIGN

6 MONTH INTERNSHIP AT SYNOPSYS,HYDERABAD

DONE BY

VASEEKARAN E R

108121131

ECE A

GUIDE:DR MURALI KRISHNA

GUIDE SIGNATURE

Ramakrishna.U

MANAGER SIGNATURE

WORK DONE

•Currently in the training phase for the RTL design of 32Gbps serdes.The Learnings as of now includes:

•Understanding Different fundamental blocks of Serdes and Verilog implementations.Accustomed to linux commands and to work on directories in Perforce(version control system)

•Understanding protocols for high speed data transfer like PCIe(Peripheral Component Interface express) based on PAM-4 architecture