Saish Patil

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Internship Experience

Synopsys Inc. Hyderabad, India

ASIC Digital Design Intern 01/2025 - Present

- Contributing to the Design team for SerDes PHY, focusing on PCS RAW of PHY.
- Responsible for Firmware Debugging and Compilations, ensuring reliable integration and functionality.

Semi Conductor Laboratory Mohali, India

Project Trainee 05/2024 - 06/2024

- Worked with VLSI Testing and Applications Division. Studied the Serdes system and LVDS channels. Conducted testing and verification of 21-bit Serdes using CPLD and FPGA.
- Successfully tested operation of 21-bit Serdes for variable frequencies using Pseudo Random Number Generator. Pseudo Random Number Generator was implemented using LFSR Technique.
- Simulated and implemented Encoder and Decoder Modules using Serdes and CPLD and verified the operation.

Project Experience

8-bit Processor Design NIT Trichy

Personal Project 12/2024

- Designed and implemented a basic 8-bit processor using Verilog HDL. Integrated core components including an Arithmetic Logic Unit (ALU), a FIFO-based register file, and control logic.
- Developed a custom instruction set architecture supporting operations such as ADD, SUB, MUL, LOAD, COPY, NAND, NOR, and XOR.
- Enabled instruction loading through pseudo code, with built-in decoding and execution mechanisms to generate the desired output.

Radiation Hardened Non-Volatile SRAM IIT BHU

Guide - Dr. SHivam Verma, Department of Electronics Engineering, IIT BHU 05/2023 - 07/2023

- Underwent a Summer Project program at IIT BHU under Dr. Shivam Verma. The research involved circuit simulations of Non-Volatile SRAM using MTJ on HSpice Software.
- Successfully carried out circuit simulations of PCSA (Read and Write), Singe and Double Column MRAM, Verification of Radiation Hardening of Non-Volatile Magnetic Latch and Non-Volatile SRAM using MTJ(Magnetic Tunnel Junction) using HSpice Software.

Education

National Institute of Technology Trichy CGPA - 8.40/10.0

B.Tech, Electrical and Electronics Engineering 06/2021 - 05/2025

Indore Public School Grade - 91.8/100.0

Class XII, CBSE 06/2019 - 05/2021

R.C. Patel English Medium Secondary School Grade - 93.4/100.0

Class X, Maharashtra State Board 06/2019 - 05/2021

Technical Skills

Verilog HDL, VHDL
C
Perl
Xylinx Vivado
HSpice