

1	2	3	4	5	6
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# PLEIADES MOTHERBOARD

PLEIADES

P15

Revision 1.00

Date: 2024-01-30

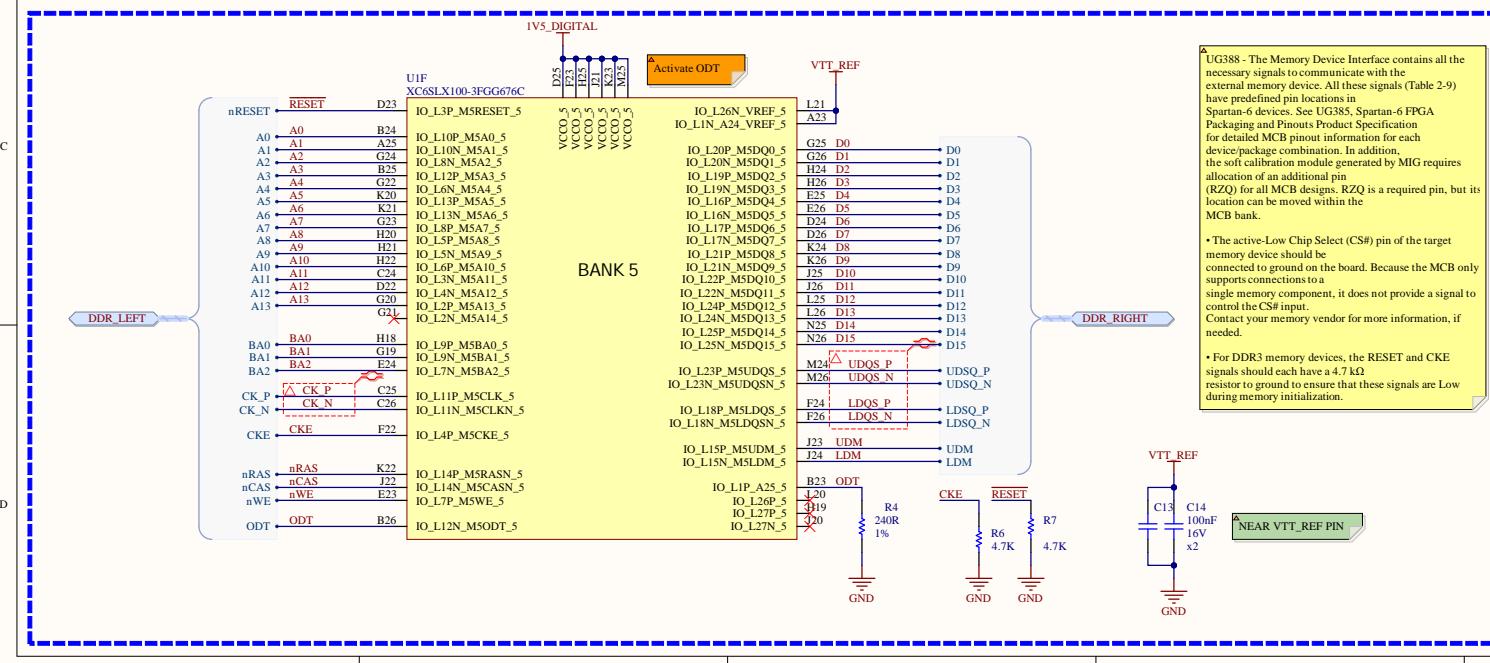
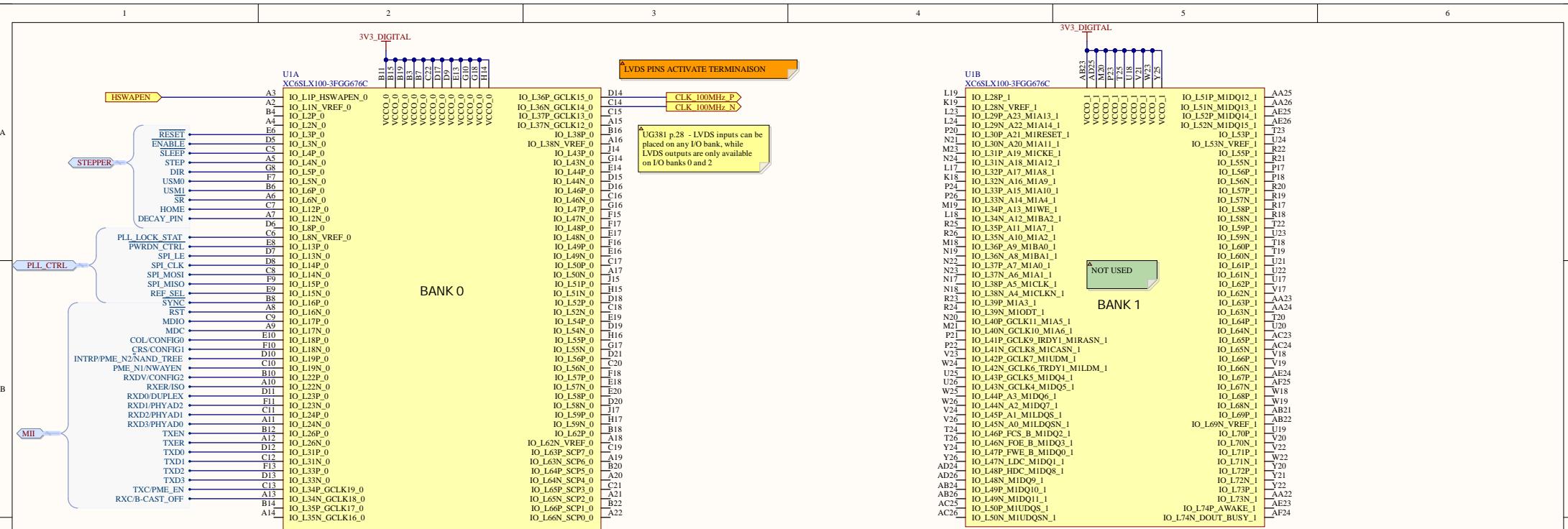
Revision history	

Package size conversion	
Metric	Imperial
1005	0402
1608	0603
2012	0805
3216	1206
3225	1210
6432	2512

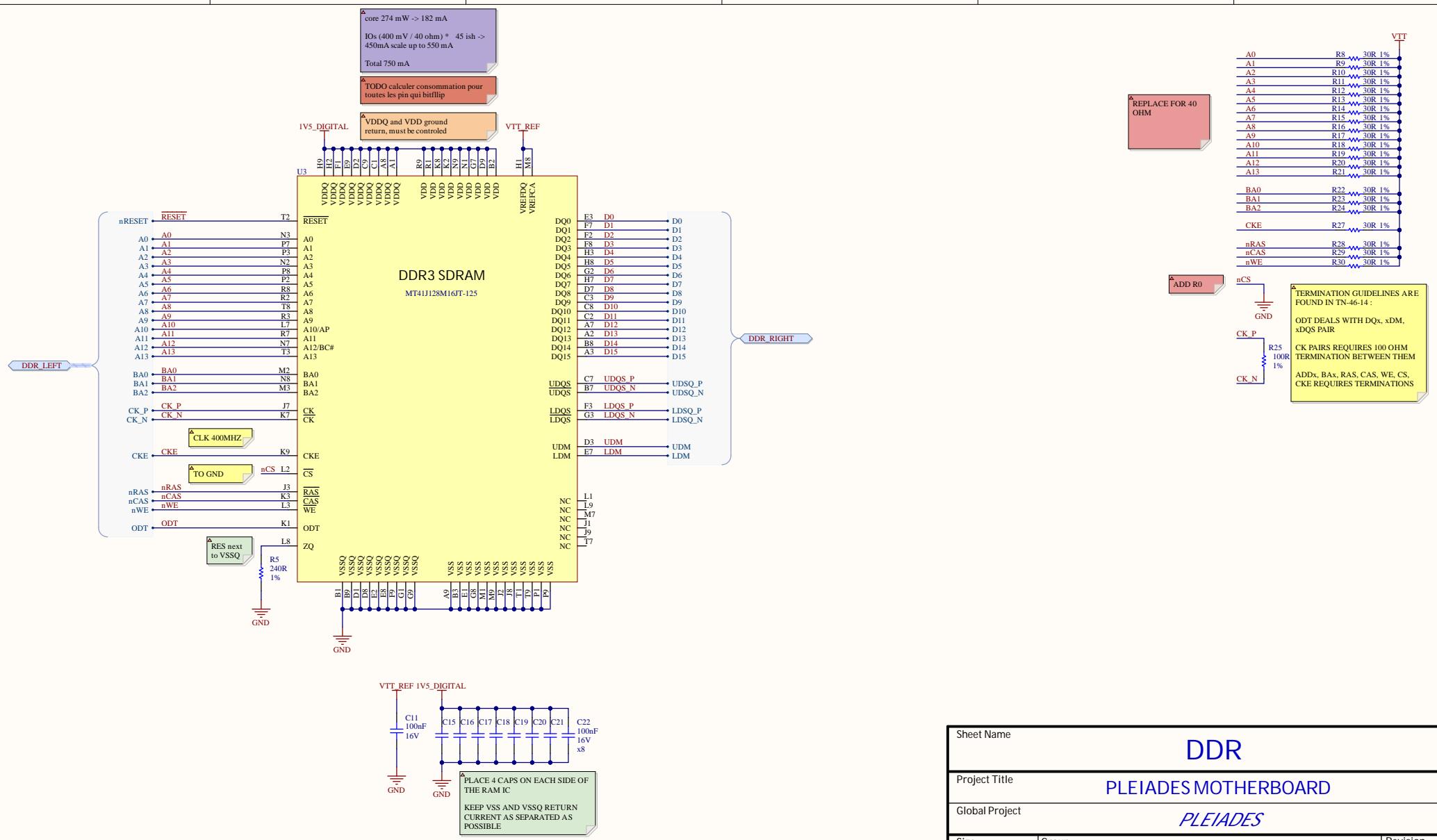
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Global Project	PLEIADES		
Size	11x17	Group	P15
Revision			1.00
Date	2024-01-30	Sheet	1 of 18
Filename	S7CAS-PLEIADES-CARTE-MERE_Pxx_TITLE.SchDoc		
Designers	Julien Guay Brahim Khalil Tekil		

1	2	3	4	5	6
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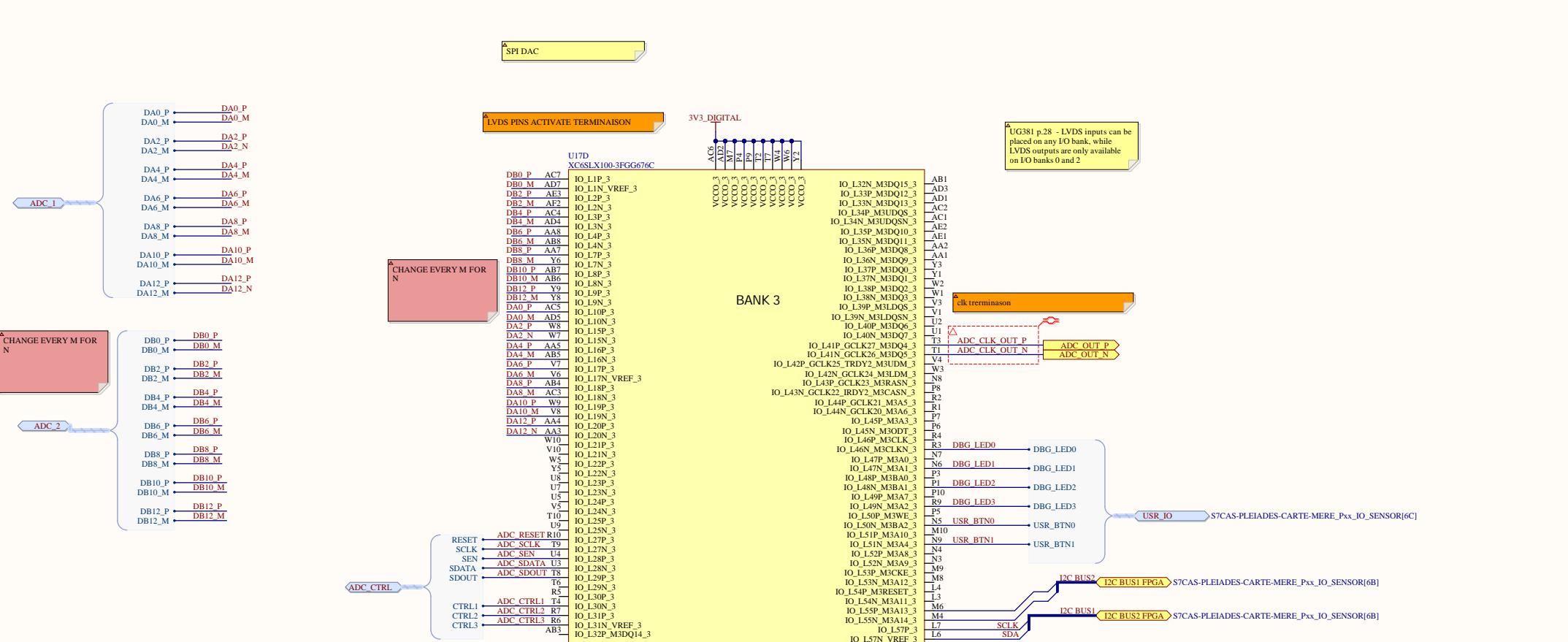
1	2	3	4	5	6
A				<p>PROGRAMMER'S NOTES</p> <p>SCHEMATIC DECISION NOTES</p> <p>TO DO NOTES</p> <p>POWER DRAW NOTES</p> <p>ROUTING NOTES</p>	A
B					B
C					C
D				<p>Sheet Name</p> <h2>OVERVIEW</h2> <p>Project Title</p> <p>PLEIADES MOTHERBOARD</p> <p>Global Project</p> <p>PLEIADES</p> <p>Size</p> <p>11x17</p> <p>Group</p> <p>P15</p> <p>Revision</p> <p>1.00</p> <p>Date</p> <p>2024-01-30</p> <p>Sheet</p> <p>2</p> <p>of</p> <p>18</p> <p>Filename</p> <p>S7CAS-PLEIADES-CARTE-MERE_Pxx OVERVIEW.SchDoc</p> <p>Designers</p> <p>Julien Guay Brahim Khalil Tekil</p>	D
1	2	3	4	5	6

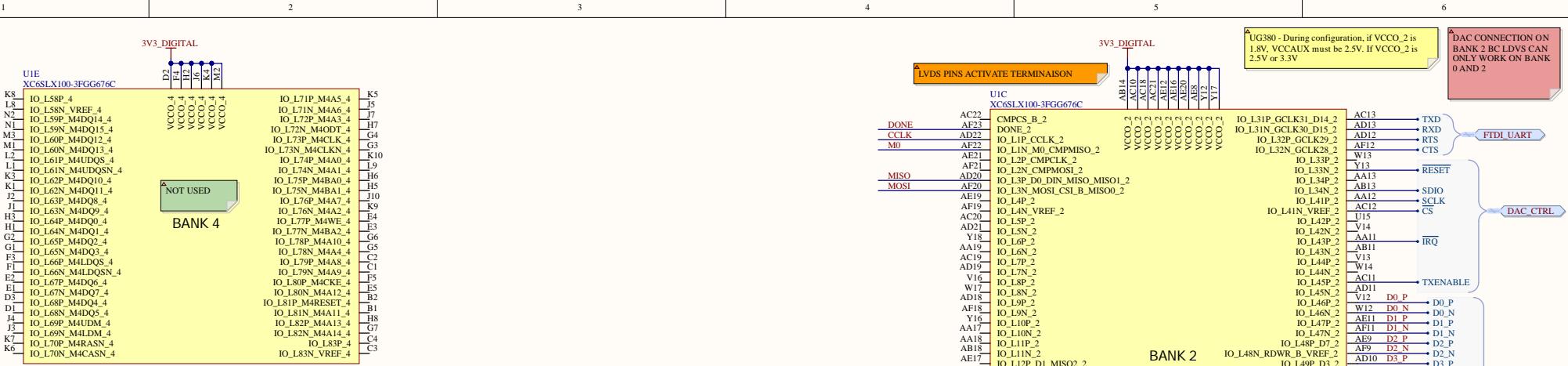


Sheet Name	BANK 0, 1 & 5		
Project Title	PLEIADES MOTHERBOARD		
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	Designers Julien Guay Brahim Khalil Tekil		



Sheet Name	DDR		
Project Title	PLEIADES MOTHERBOARD		
Global Project	PLEIADES		
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Filename S7CAS-PLEIADES-CARTE-MERE_Pxx_DDR.SchDoc	Designers Julien Guay Brahim Khalil Tekil		





Power-On Rese

Spartan-6 FPGAs have a built-in power-on reset (POR) circuit that monitors the three power rails required to successfully configure the FPGA (see Figure 4-1). At power-up, the POR circuit holds the FPGA in a reset state until the  $V_{CCINT}$ ,  $V_{CCALD}$ , and  $V_{CCIO3}$  supplies reach their respective input threshold levels. A time  $t_{Q3}$  after all three supplies reach the respective thresholds, the POR reset is released and the FPGA begins its configuration process.

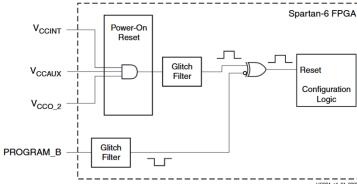
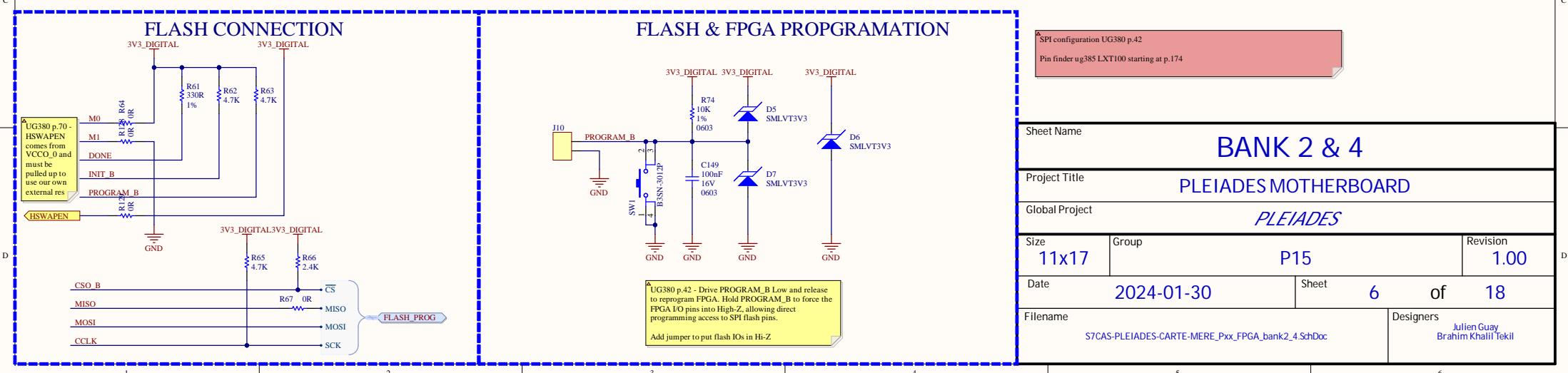


Figure 4-1: Simplified POB Circuit Diagram



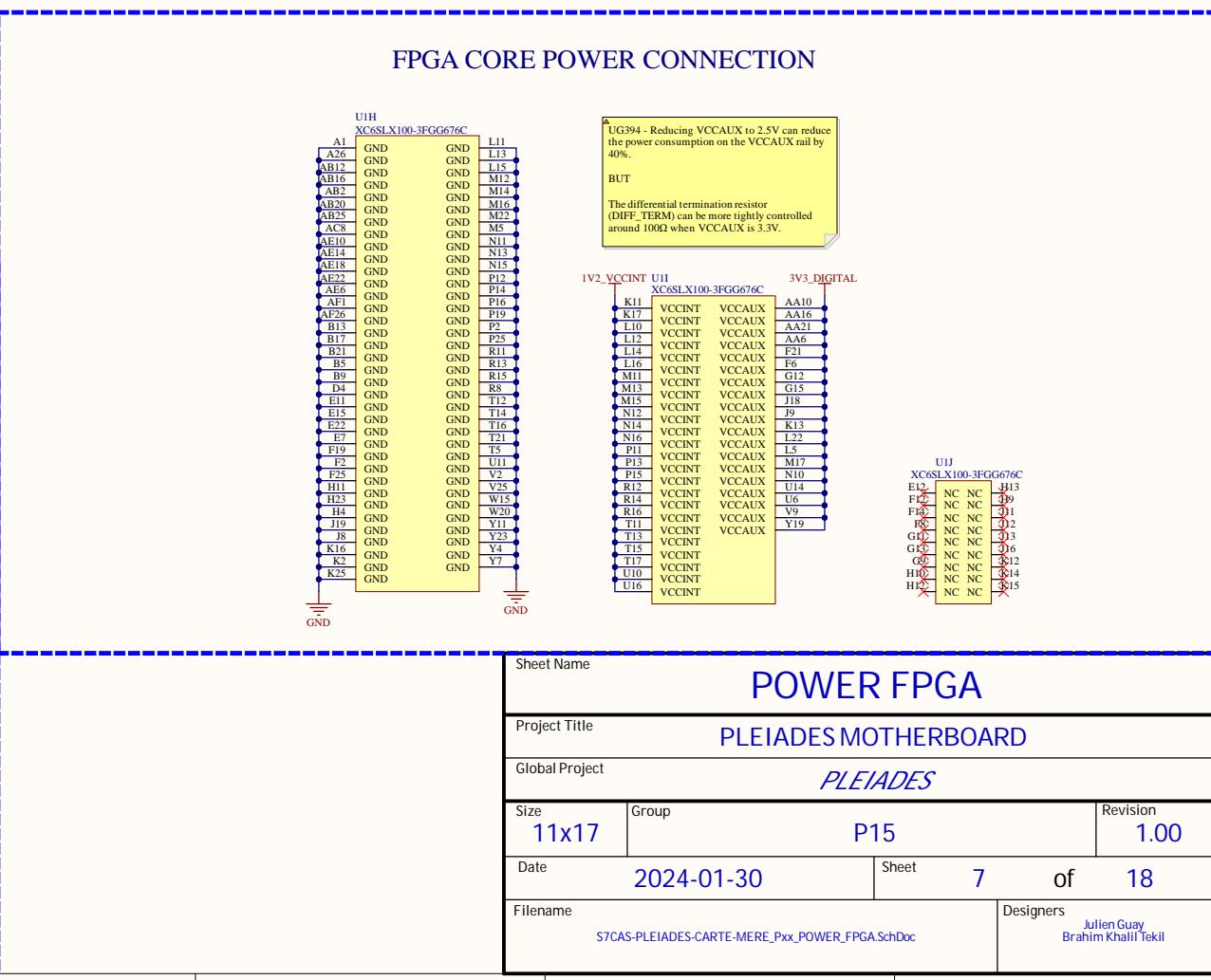
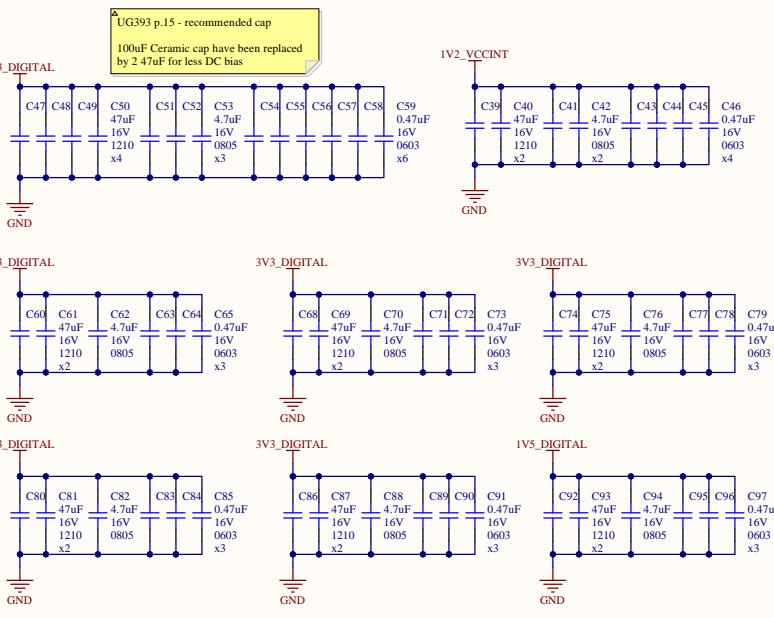
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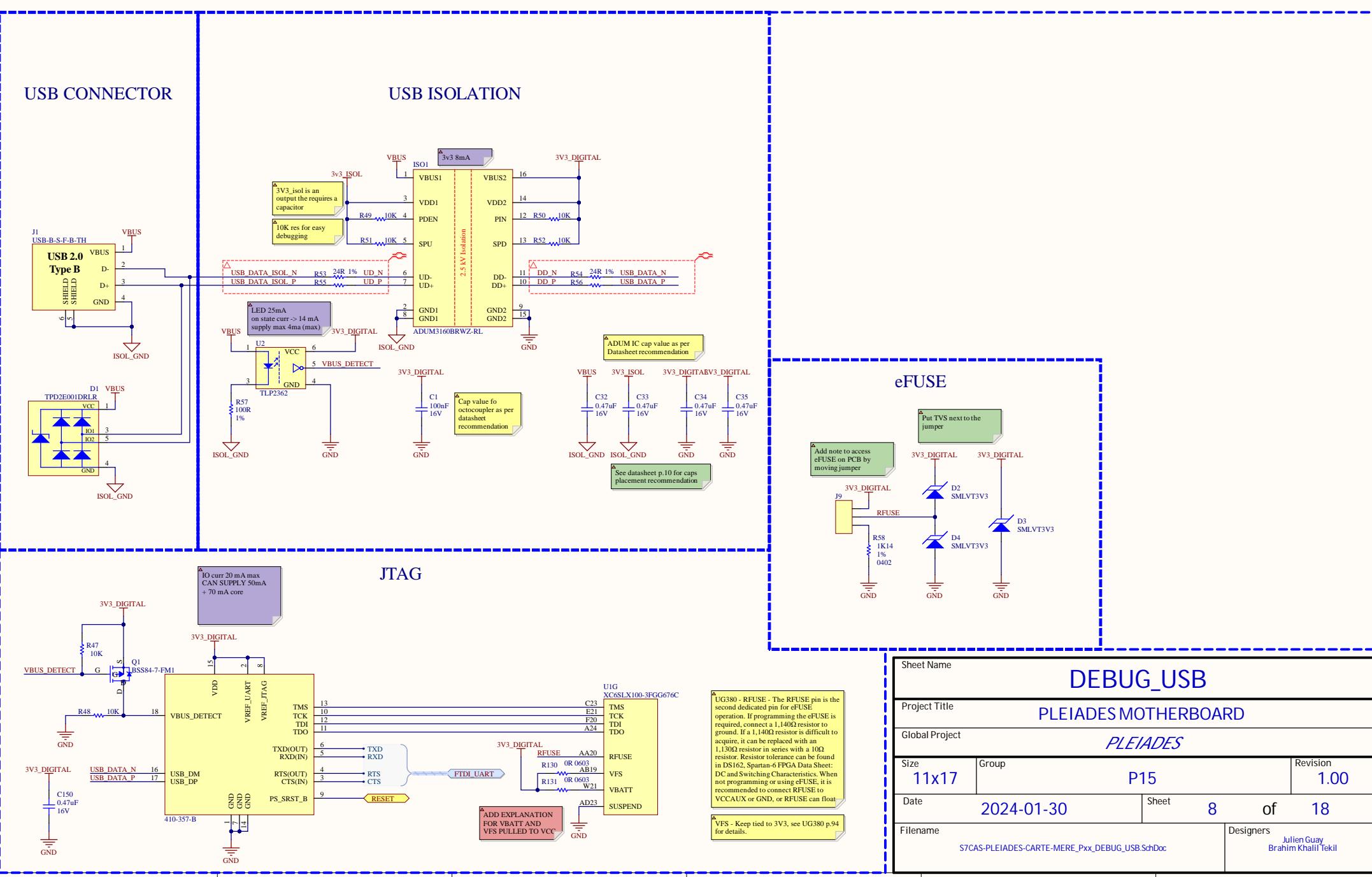
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B

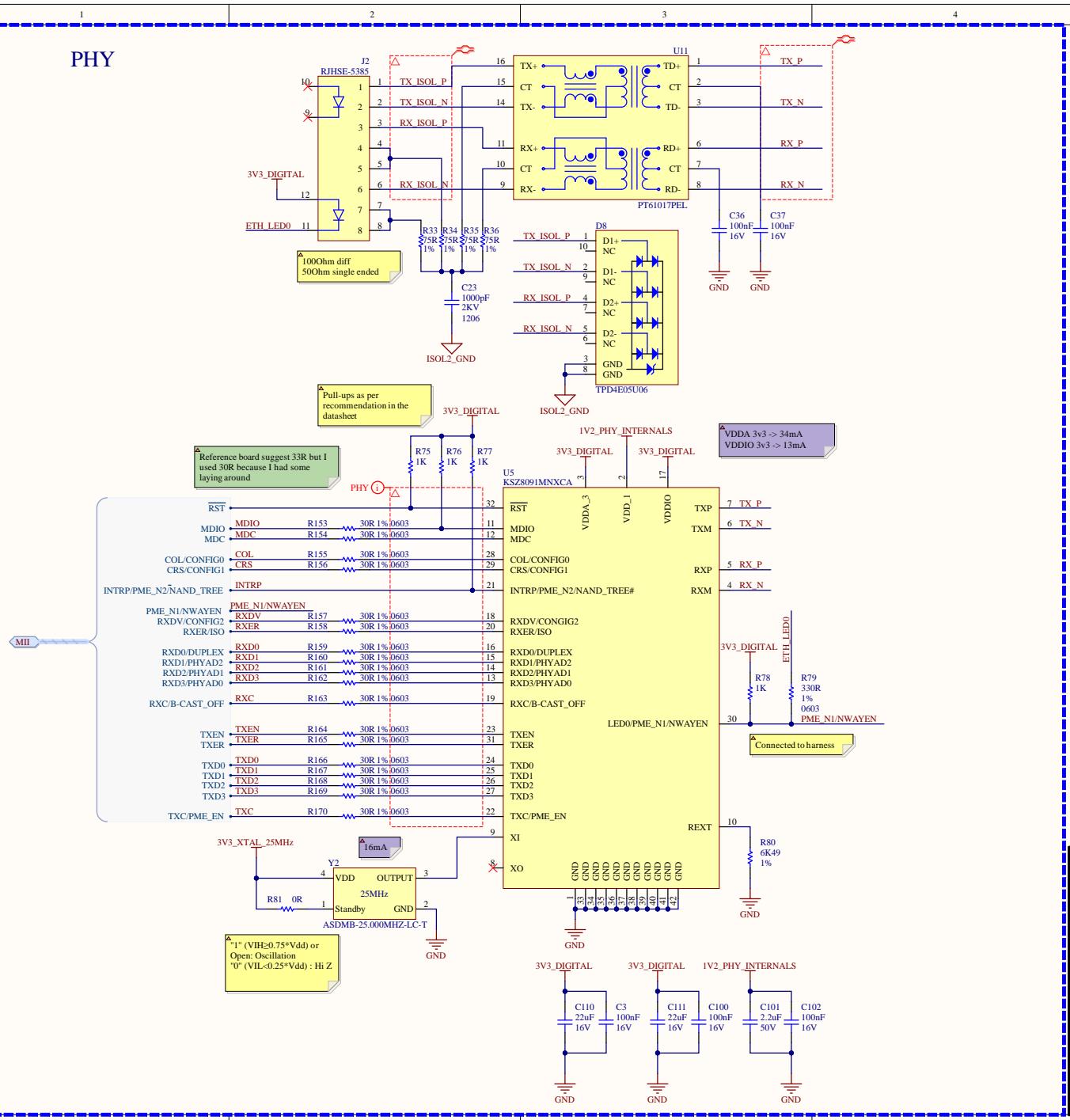
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## FPGA DECOUPLING CAPS





# PHY



Sheet Name

PHY

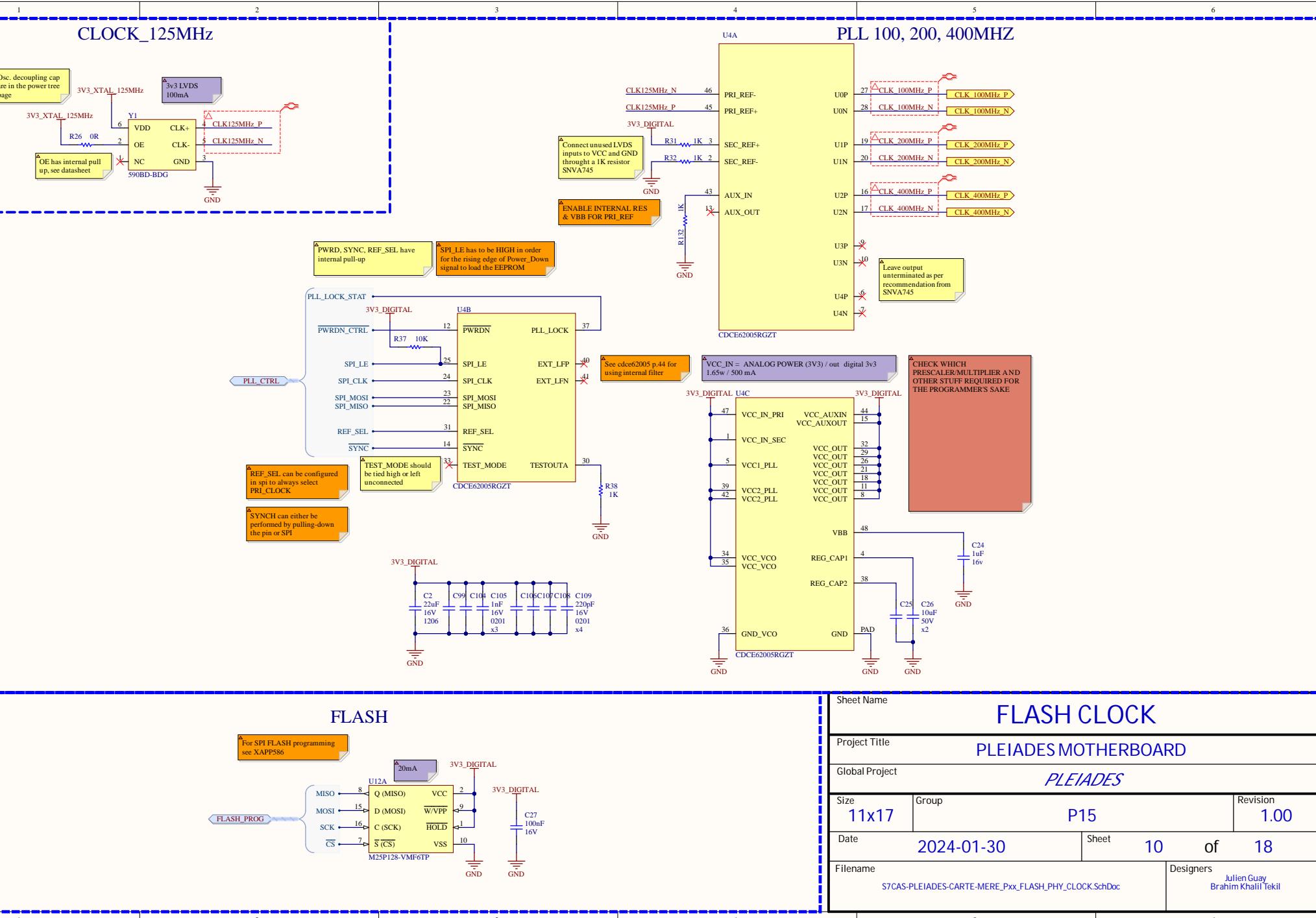
PLEIADES MOTHERBOARD

PLEIADES

Size	11x17	Group	P15	Revision	1.00
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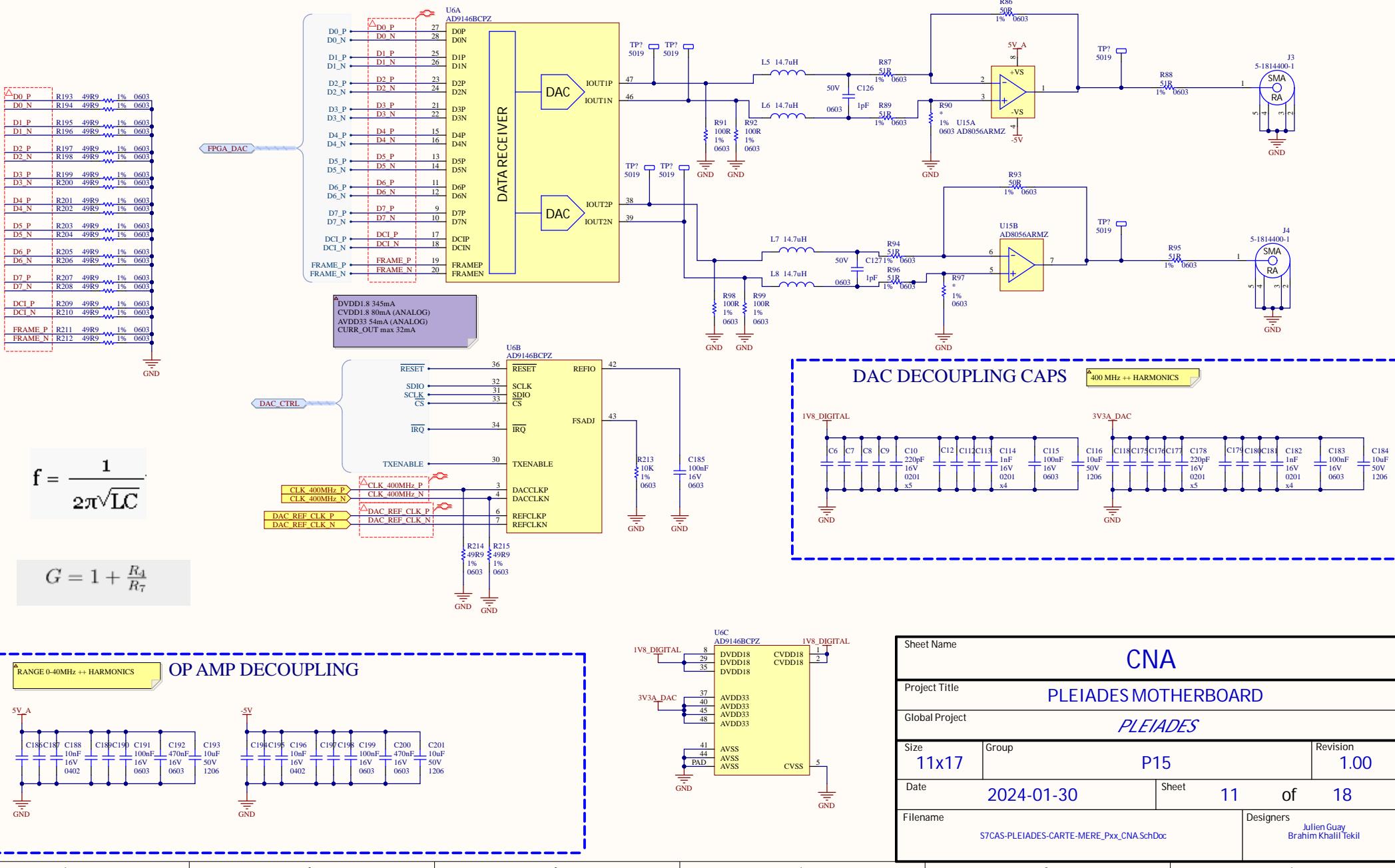
Date	2024-01-30	Sheet	9	of	18
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Filename	S7CAS-PLEIADES-CARTE-MERE_Pxx.PHY.SchDoc	Designers	Julien Guay Brahim Khalil Tekil
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1 2 3 4 5 6

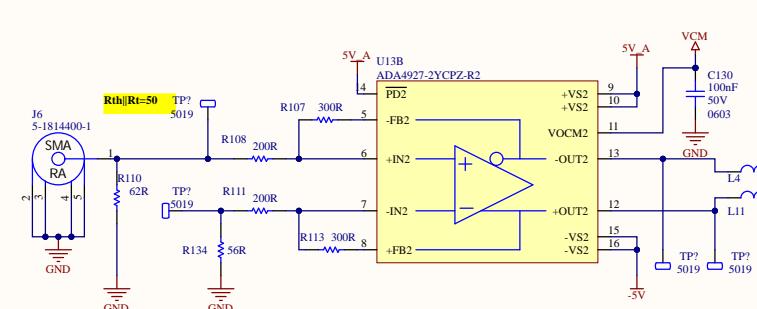
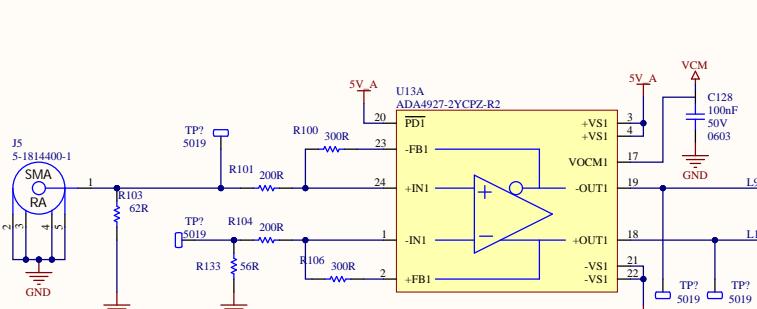
# DAC



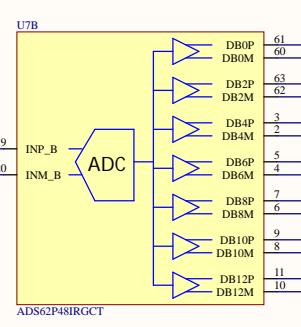
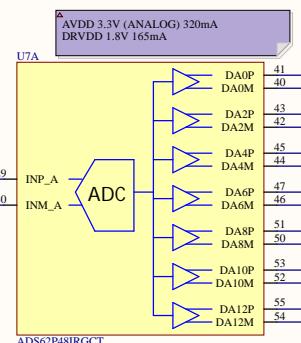
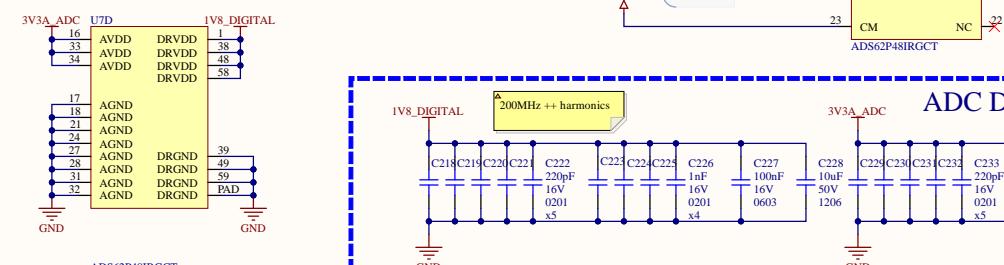
1 2 3 4 5 6

## TODO FILTRE

PROBABLY between -5V to 5V



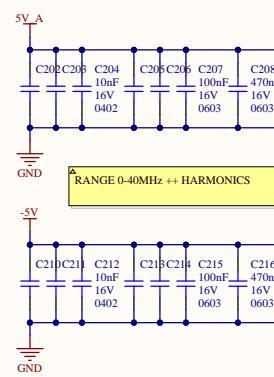
Parallel configuration => RESET High  
CLK 200MHz P CLK 200MHz N  
CLK 200MHz N  
The ADC has a set of internal registers, which can be accessed by the serial interface formed by pins SEN (Serial Interface Enable), SCLK (Serial Interface Clock) and SDATA (Serial Interface Data).



## ADC

CHANGE EVERY M FOR N

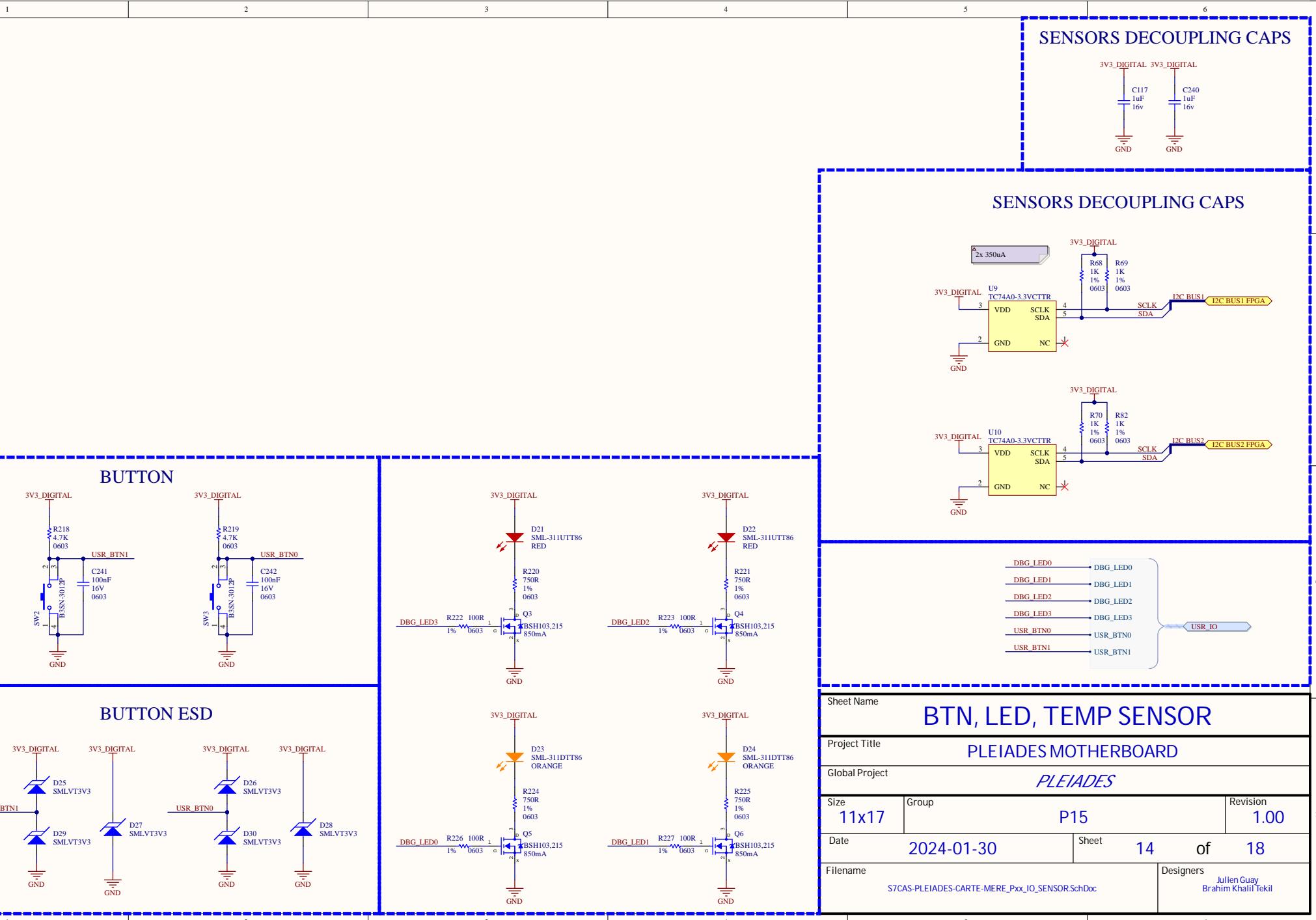
## OP AMP DECOUPLING

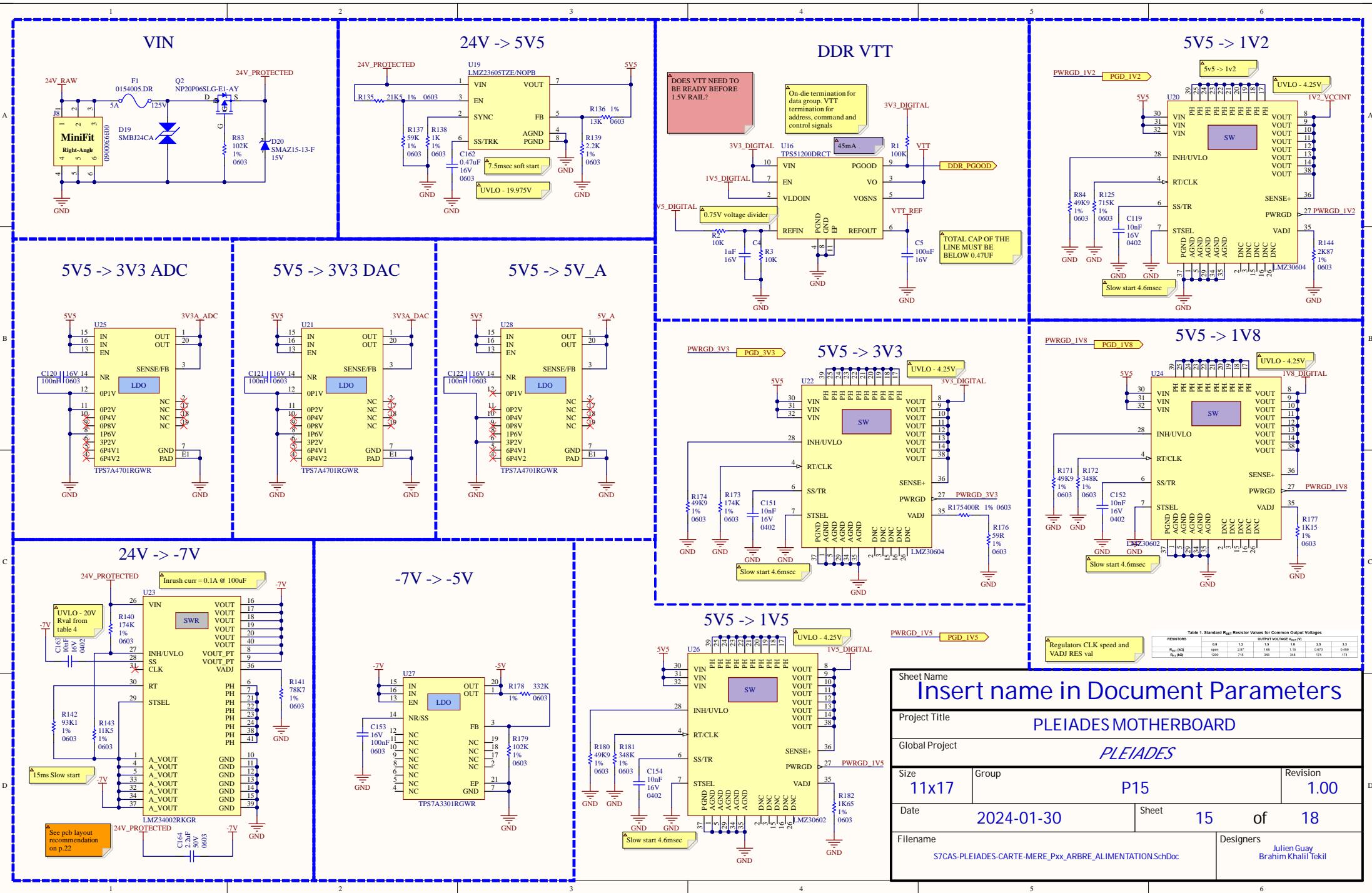


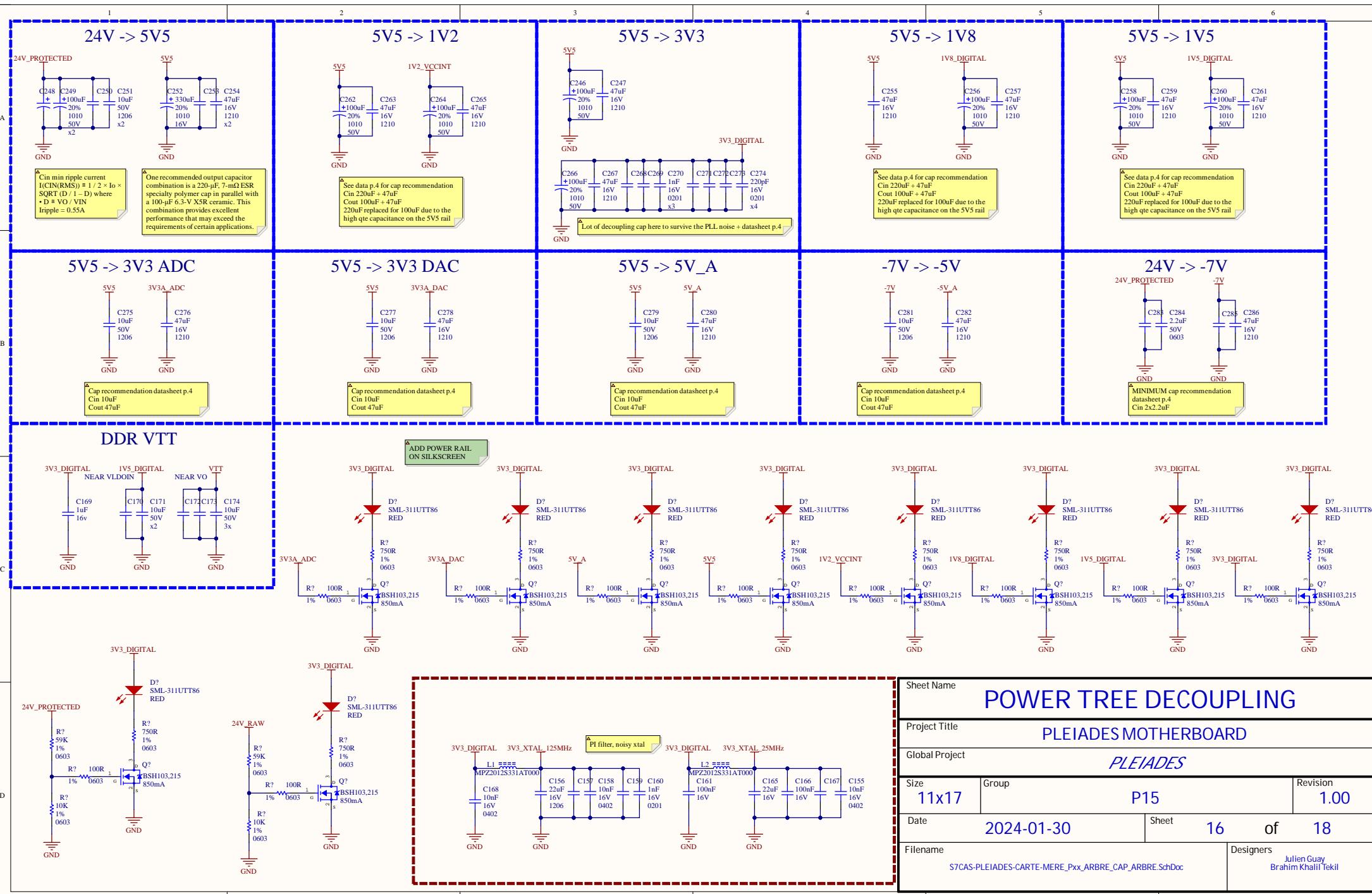
## ADC DECOUPLING CAPS

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CAN	
PLEIADES MOTHERBOARD	
PLEIADES	
Size	Group
11x17	P15
Date	Revision
2024-01-30	1.00
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Filename	
S7CAS-PLEIADES-CARTE-MERE_Pxx_CAN.SchDoc	Designers
Julien Guay Brahim Khalil Tekil	

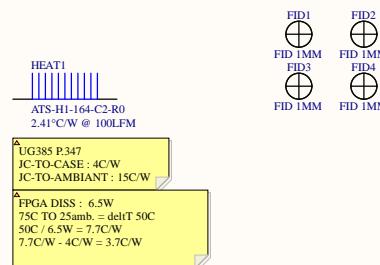




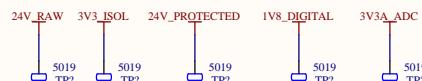




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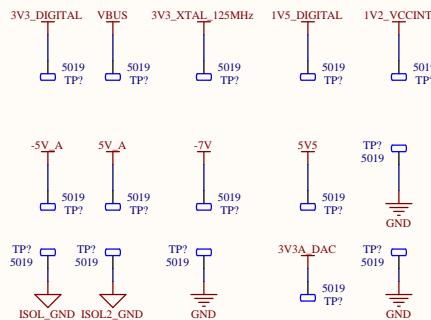


B



A

C



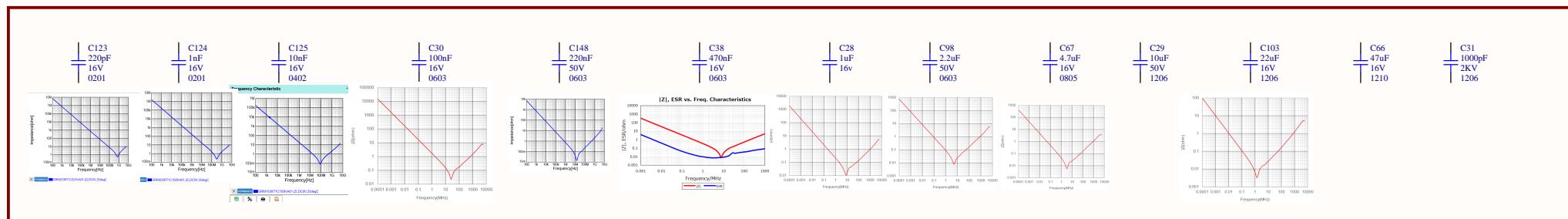
B

D

Sheet Name			
MECANICAL			
Project Title			
Size	Group	P15	Revision
11x17	2024-01-30		1.00
Date	Sheet 17 of 18		
Filename		Designers	
S7CAS-PLEIADES-CARTE-MERE_Pxx_MECHANICAL.SchDoc		Julien Guay Brahim Khalil Tekil	

1 2 3 4 5 6

## DNF CAPS VAL



## DNF RES VAL

B

R71 0R 1/2W 0805	R126 0R22 1% 1206	R46 30R 1% 0603	R183 59R 1% 0603	R40 240R 1% 0603	R184 400R 1% 0603	R60 1K14 1% 0402	R149 2.2K 1% 0603	R185 2K87 1% 0603	R85 6K49 1% 0603	R150 13 1% 0603	R146 78K 1% 0603	R147 93K1 1% 0603	R186 348K 1% 0603
R44 0R 1% 0603	R59 24R 1% 0402	R43 30R 1% 0603	R39 100R 1% 0603	R72 1K 1% 0603	R42 2.4K 1% 0603	R73 1K5 1% 0603	R187 1K5 1% 0603	R145 11K5 1% 0603	R151 21K5 1% 0603	R152 39K 1% 0603	R148 71K 1% 0603	R148 102K 1% 0603	R188 102K 1% 0603
R229 49R9 1% 0603	R228 750R 1K65 1% 0603	R189 1K65 1% 0603	R41 10K 1% 0603	R190 49K9 1% 0603	R127 1K 1% 0603	R191 47K 1% 0603	R192 715K 1% 0603	R192 332K 1% 0603					

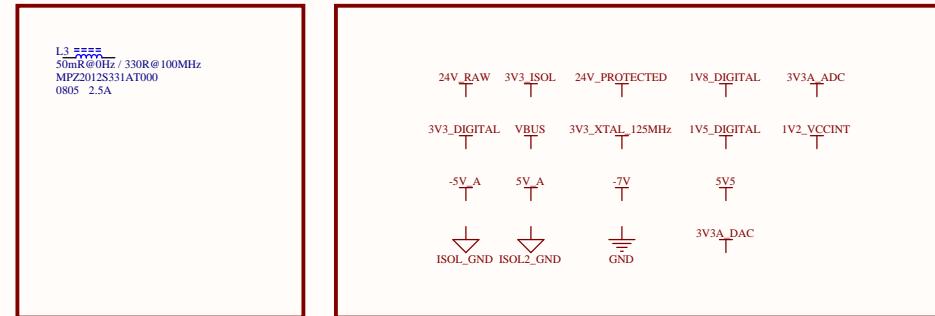
## CAP POL

B

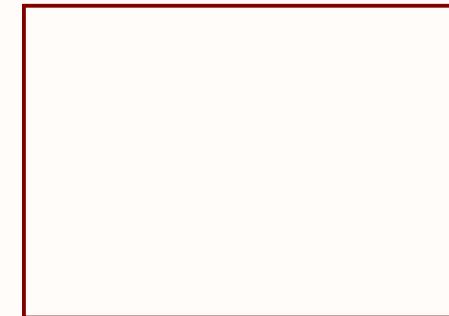
C243 +100uF 20% 1010 50V	C244 +330uF 20% 1010 16V	C245 +470uF 20% 1616 50V
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Iripple 490mA @ 100KHz Iripple 670mA @ 100KHz Iripple 235mA @ 100KHz

## DNF FERR VAL



## INDUCTOR



D

Sheet Description		
Project Title PLEIADES MOTHERBOARD		
Global Project PLEIADES		
Size 11x17	Group P15	Revision 1.00
Date 2024-01-30	Sheet 18 of 18	
Filename S7CAS-PLEIADES-CARTE-MERE_TO_BE_DELETED.SchDoc	Designers Julien Guy Brâhim Khalil Tekil	

1 2 3 4 5 6



## PLEIADES MOTHERBOARD

PLEIADES

Revision 1.00  
.Project\_DateCode

Designed by:  
Julien Guay  
Brahim Khalil Tekil

.Project\_Designer4

Serial #

