MLX75027 VGA Time-of-Flight Sensor

DATASHEET v002

Features & Benefits

- 1/2" optical Time-of-Flight image sensor
- VGA (640 x 480) pixel resolution
- ISO 26262 support (ASIL-B, version -RTI)
- AEC-Q100 qualified (grade 2)
- 10 x 10 µm DepthSense® pixels
- Integrated MLA (micro lens array)
- Backside illumination (BSI technology)
- External quantum efficiency 51% (850nm)
- External quantum efficiency 28% (940nm)
- High distance accuracy due to programmable modulating frequencies up to 100 MHz
- AC Demodulation contrast 85 % (40 MHz)
- AC Demodulation contrast 78 % (100 MHz)
- Differential light source control with phase delay feedback loop
- Full resolution distance frame rate of max. 120 FPS (/w 4 raw phases, Tint 300µs, 4 data lanes @960Mbps)
- Up to 8 raw phases (or quads) per frame
- Per-phase statistics & diagnostics
- Continuous or triggered operation mode(s)
- Configurable over I^2C (up to 400kHz)
- CSI-2 serial data output, MIPI D-PHY, 1 clock lane, 2 or 4 data lanes (< 960 Mbps/lane)
- Build-in temperature sensor
- Region of interest (ROI) selection
- Integrated support for binning
- Operating temperature range of -40 to 105°C
- 14x14mm (-RTC) or 11x9.5mm (-RTI) package
- Number of pins = 141 (-RTC) or 143 (-RTI)

Description

MLX75027 is a fully integrated optical Time-of-Flight image sensor. It's perfectly suited for automotive applications, including, but not limited to, gesture recognition, driver monitoring, skeleton tracking, people or obstacle detection and traffic monitoring. MLX75027RTI is ASIL-B capable making it a great option for applications requiring functional safety. The sensor features a VGA (640x480) pixel array based on the DepthSense® pixel technology. Combined with a modulated light source this sensor is capable of measuring object distance and reflectivity under extreme background light conditions (up to 120klux when used together with an optical band pass filter). This distance information can be used to calculate a complete 3D point cloud representation of a scene. Full resolution image acquisition up to 120 distance frames per second while supplied to a microcontroller via a standardized MIPI CSI-2 serial camera interface. The device is available in a CBGA and IBGA package and offers a variety of integration possibilities.

CBGA (left), IBGA (right)

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Document Revision History

Version	Date	Changes
002	24/06/2024	Removal of LEDFB references
		Rephrasing of PRETIME timing
		Updated Melexis logo
		Section Ordering Information: Added mixed pixel variants
		Section 2: Updated image
		Section 8.1: Removal of Data Rate Configuration Settings 2 table requirement
		Section 9: Added information to META_LENGTH description
		Section 11.4: Added Register Configuration Table

Table 1: Changelog

Ordering Information

Product	Temperature Rating	Package Identifier	Option Code	Packing Style	Comment
MLX75027	R	TC	ABA-210	TR	Not recommended for new designs & projects
MLX75027	R	TC	ABA-200	TR	
MLX75027	R	TC	ABA-210	SP	
MLX75027	R	TC	ABM-210	TR	
MLX75027	R	TC	ABM-200	TR	
MLX75027	R	TI	ABA-210	TR	
MLX75027	R	TI	ABA-200	TR	
MLX75027	R	TI	ABA-210	SP	
MLX75027	S	TI	ABA-210	TR[1]	
MLX75027	S	TI	ABA-200	TR[1]	
MLX75027	R	TI	ABM-210	TR	
MLX75027	R	TI	ABM-200	TR	
MLX75027	S	TI	ABM-210	TR[1]	
MLX75027	S	TI	ABM-200	TR[1]	

Table 2: Device ordering information

Temperature Rating	R : -40°C to 105°C – automotive variant S : -20°C to 85°C – industrial variant
Package Identifier	TC : Ceramic ball grid array (MSL1) - Not recommended for new designs & projects TI : Interstitial ball grid array (MSL3)
Option Code	ABA-200 : incl. double sided ARC coating, no optical filter, without cover tape ABA-210 : incl. double sided ARC coating, no optical filter, with cover tape[2] ABM-200 : incl. double sided ARC coating, no optical filter, without cover tape, with mixed pixel technology ABM-210 : incl. double sided ARC coating, no optical filter, with cover tape[2], with mixed pixel technology
Packing Style	TR : Tray (MLX75027RTC: 119pcs or MLX75027RTI/STI: 168pcs) SP : Sample Pack (10pcs)
Ordering Example	MLX75027RTI-ABA-210-TR

Table 3: Ordering options

Note[1] : Sample pack for MLX75027STI is unavailable, it is recommended to order MLX75027RTI sample pack when ordering sample quantities.

Note[2] : The properties of the cover tape are guaranteed for one year after shipping date if the devices are stored in appropriate conditions according the device MSL rating.

1. System Architecture

A complete TOF system or camera module includes at least these components:

- MLX75027 VGA (640x480 pixels) TOF pixel array
- A synchronized high bandwidth near infrared (NIR) active illumination source
- Beam shaping optics for the light distribution
- A receiving sensor lens (optimized for maximum NIR wavelength transmittance)
- A microprocessor, DSP, FPGA or SOC (system on chip) to calculate and process the data, compatible with MIPI camera serial interface CSI-2

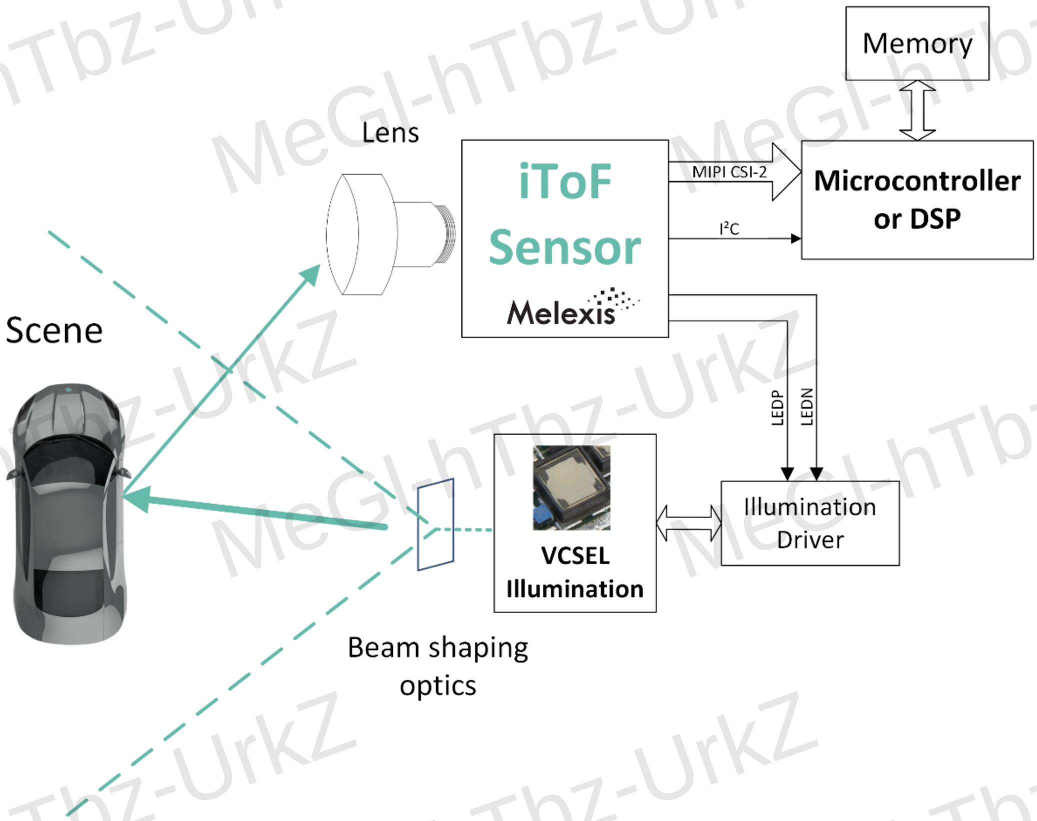


Figure 1: System block diagram

2. Sensor Block Diagram

MLX75027 is a Time-of-Flight (TOF) camera sensor with two tap Current Assisted Photo Demodulator (CAPD) pixels offering high responsivity. These backside illuminated pixels are connected to low noise analog amplifiers and converted by column ADCs which enable high speed & accurate image acquisition. Furthermore, it consists of a PLL timing generator, a high speed CSI2 serial interface, controllable registers via I²C and a digital control unit in charge of the different internal blocks.

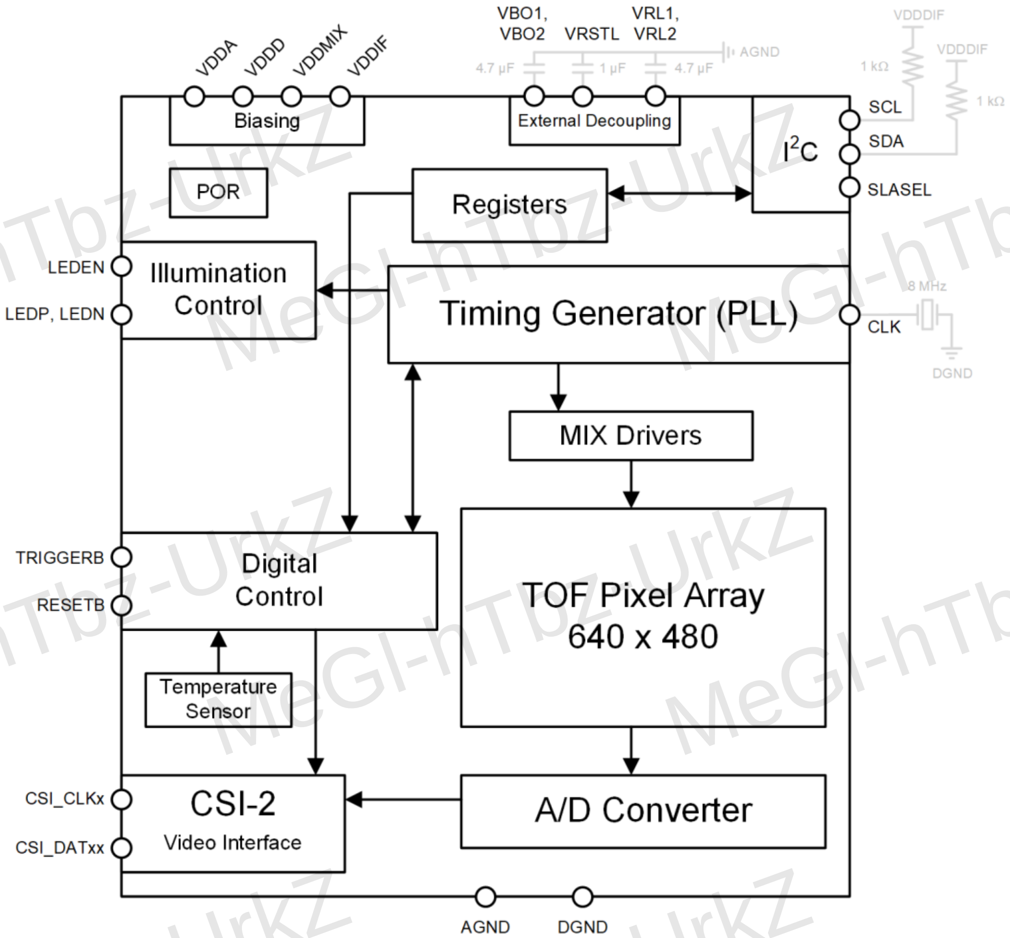


Figure 2: Sensor block diagram

3. Electrical Specifications

3.1. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Supply voltage (analog)	VDDA	-0.3	3.3	V
Supply voltage (MIX drivers)	VDDMIX	-0.3	1.8	V
Supply voltage (digital)	VDDD	-0.3	1.8	V
Supply voltage (interfaces)	VDDIF	-0.3	3.3	V
Input voltage (digital IOs)	VI	-0.3	3.3	V
Output voltage (digital IOs)	VO	-0.3	3.3	V
Storage temperature		-40	125	°C

Table 4: Absolute Maximum Ratings

Note : Absolute maximum ratings should not be exceeded at any time to avoid permanent hardware damage.

3.2. Typical Operating Conditions

Parameter		Min.	Typ.	Max.	Unit
VDDA Supply Voltage[1]		2.6	2.7	2.8	V
VDDMIX Supply Voltage[1]		1.1	1.2	1.3	V
VDDD Supply Voltage [1]		1.1	1.2	1.3	V
VDDIF Supply Voltage [1]		1.7	1.8	1.9	V
LEDP, LEDN single ended high level[2] LEDEN[2]		VDDIF - 0.2			V
LEDP, LEDN single ended low level[3] LEDEN[3]				0.2	V
LEDP/LEDN differential common mode (LVDS_EN = 1)		VDDIF / 2 - 0.1	VDDIF / 2	VDDIF / 2 + 0.1	mV
LEDP/LEDN differential swing[4] (with R = 100Ω, LVDS_EN = 1)		100	150	220	mV
LEDP, LEDN termination resistor			100		Ohm
Minimum TRIGGERB pulse length			1		µs
Minimum RESETB pulse length			1		µs
TRIGGERB RESETB SLASEL	Maximum input low			0.2* VDDIF	V
TRIGGERB RESETB SLASEL	Minimum input high	0.8* VDDIF			V

Table 5: Typical operating conditions 1

Note[1] : It is recommended to use the typical supply voltages
Note[2] : current of -2mA, LVDS_EN = 0, typical load 15pF
Note[3] : current of 2mA, LVDS_EN = 0, typical load 15pF
Note[4] : The differential swing during hardware preparation and software standby is 0mV

Parameter	Min.	Typ.	Max.	Unit
Junction to Ambient Thermal Resistance		12		K/W
Operating ambient temperature	-40		105	°C
Temperature sensor accuracy @ -40°C Tj			±7	°C
Temperature sensor accuracy @ 60°C Tj			±5	°C
Temperature sensor accuracy @ 125°C Tj			±6	°C

Table 6: Typical operating conditions 2

3.3. Video Interface

MLX75027 is fully compliant with the hardware description as described in the MIPI Alliance Specification for D-PHY version 1.20.00, released in September 2014. For design guidelines or a more detailed description about the parameters please consult the D-PHY MIPI documentation.

3.3.1. MIPI DC specification

	Parameter	Min.	Typ.	Max.	Unit
HSDC	VOHHS			360	mV
	VOD	140		270	mV
	dVOD			14	mV
	VCMTX	150		250	mV
	dVCMTX			5	mV
	ZOS	40		62.5	Ω
LPDC	VOH	1.1		1.3	V
	VOL	-50		50	mV
	ZOLP	110			Ω

Table 7: MIPI DC specification

Note: For a detailed explanation of the different parameters, please consult the MIPI D-PHY specifications v1.20.00.

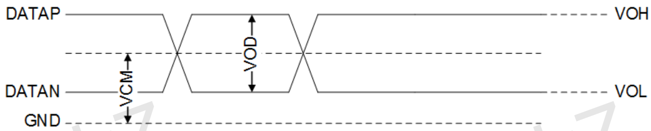


Figure 3: MIPI DC layout

3.3.2. MIPI AC specification

	Parameter	Min.	Typ.	Max.	Unit
HSAC	Trise, Tfall	50		312.5	psec
	dVCMTX(>400MHz)			15	mVrms
	dVCMTX(50-400MHz)			25	mVpeak
LPAC	Trise, Tfall			25	ns
	Slew rate with Cload=0pF			500	mV/nsec
	Slew rate with Cload=5pF			300	mV/nsec
	Slew rate with Cload=20pF			250	mV/nsec
	Slew rate with Cload=70pF			150	mV/nsec

Table 8: MIPI AC specification

Note: For a detailed explanation of the different parameters, please consult the MIPI D-PHY specifications v1.20.00.

3.4. Power Consumption

3.4.1. Standby Power Consumption

Standby power consumption depends on the standby mode. Table 9 lists both hardware and software standby typical power consumption for each voltage domain. Hardware standby is at the end of hardware preparation with stable supply levels. For more information please consult Figure 23 section 7 Start-up Sequence.

Parameter	Symbol	Hardware Standby[1]	Software Standby[1]	Unit
Analog Supply Current	PDDA	1.87	5.25	mW
MIX Drivers Supply Current	PDDMIX	5.44	5.44	mW
Digital Supply Current	PDDD	9.84	11.83	mW
I/O Supply Current	PDDIF	0.03	0.05	mW
Total		17.18	22.57	mW

Table 9: Standby power consumption

Note[1] : Typical power consumption at worst case temperature with VDDA = 2.8V, VDDMIX=1.3V, VDDD=1.3V,VDDDIF=1.9V.

3.4.2. Video Streaming Power Consumption

The total power consumption is divided over four domains, neither of the four domains are consuming at the same time. VDDMIX and VDDIF are dominantly active during the integration time, VDDD and VDDA during the readout time and a small amount of VDDD is active constantly. As shown below in Figure 4.

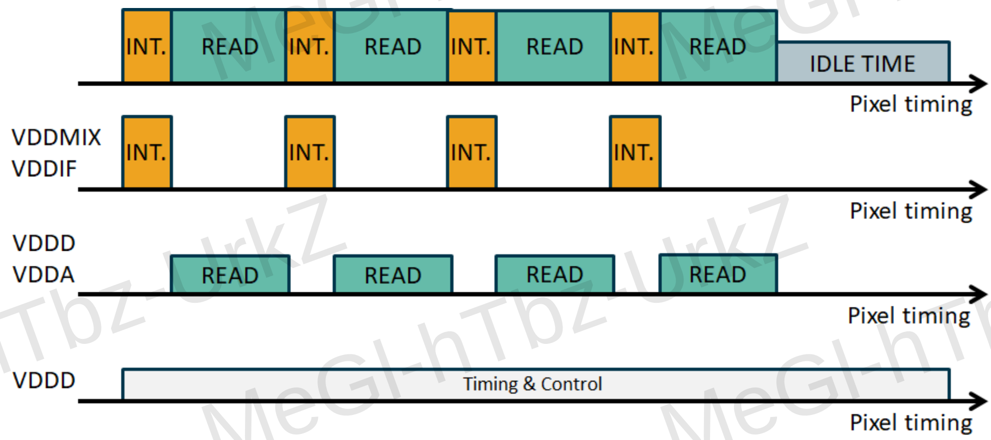


Figure 4: Power domains

Table 10 lists the absolute pulse current per domain,
however the typical duty cycle of each active period is only around 10%.

Parameter	Symbol	Typ.	Max. [1]	Unit
Analog Supply Current	IDDA	39.8	52.0	mA
MIX Drivers Supply Current	IDDMIX	1455.1	3000[2]	mA
Digital Supply Current	IDDD	98.2	130.8	mA
I/O Supply Current	IDDIF	2.1	2.6	mA

Table 10: Pulse current

Note[1] : The max value is the worst case pulse current over the complete ambient operating temperature range including part to part variation measured under dark conditions.
Note[2] : Due to the pulse current behaviour of IDDMIX it is not required to dimension the PSU according to max. value.

In Table 11 you can find a representative device power consumption for two different application conditions.

		Application A		Application B		
Parameter	Symbol	Typ.[1]	Max.[2]	Typ.[1]	Max.[2]	Unit
Analog Supply	PDDA	28.1	35.3	42.7	54.6	mW
MIX Drivers Supply	PDDMIX	65.2	127.4	296.5	535.5	mW
Digital Supply	PDDD	65.4	88.7	82.4	108.3	mW
I/O Supply	PDDIF	1.7	2.0	2.4	2.9	mW
Total Supply	P	160.3	253.5	423.8	701.5	mW

Table 11: Power consumption

Note[1] : Typical values are the average power consumption with nominal voltage levels (at room temperature) for two defined application conditions:

Application A : Typical
- Full resolution (640x480 pixels)
- 4 raw phases per distance frame
- 30 distance frames per second
- 250 µs integration time
- 60 MHz modulation frequency
- 800 mbps (4 lane MIPI data rate)

Application B : Performance
- Full resolution (640x480 pixels)
- 4 raw phases per distance frame
- 60 distance frames per second
- 600 µs integration time
- 100 MHz modulation frequency
- 960 mbps (4 lane MIPI data rate)

Note[2] : Max. is the worst case power consumption over the full ambient operating temperature range and over the full process variation.

See Figure 5 for typical power consumption at 40MHz modulation frequency in function of integration time for [MIPI speed, FPS]:

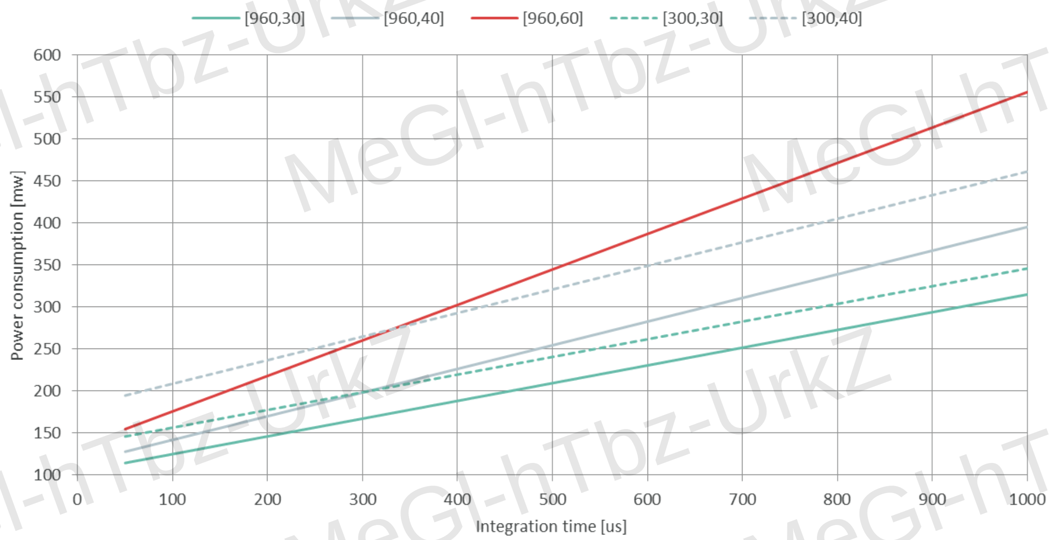


Figure 5: Power consumption in function of integration time

Note that there is only a minor effect on power consumption at different MIPI speeds.

The previous plot does not take into account temperature variation. Over the full temperature range VDDMIX has the largest variation in power dissipation. Figure 6 indicates how MIX pulse current changes over the full automotive -40°C to 105˚C temperature range.

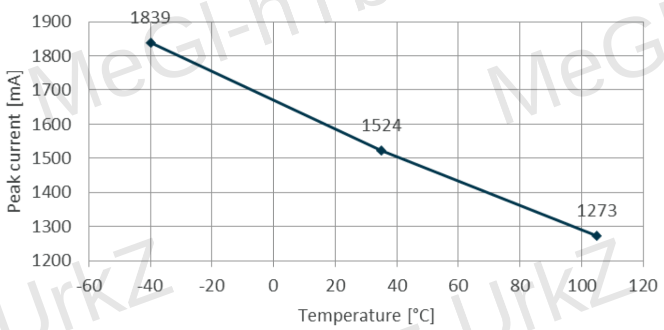


Figure 6: MIX current over temperature

Note that due to device self-heating in reality the device will always operate at a higher than ambient temperature resulting in a reduced overall power consumption.

3.5. Maximum Distance Frame Rate

The maximum distance frame rate that can be achieved depends on the integration time, the minimum readout time per phase and the total amount of raw phases for each distance frame. Please consult the following section for more information how each parameter influences frame time: 8.8
The phase readout time is determined by the MIPI configuration settings as explained in section 8.4. In Figure 7: Theoretical Maximum Distance Frame Rate in function of Integration Time (per phase) is the Max. frame rate plotted for five typical MIPI settings.

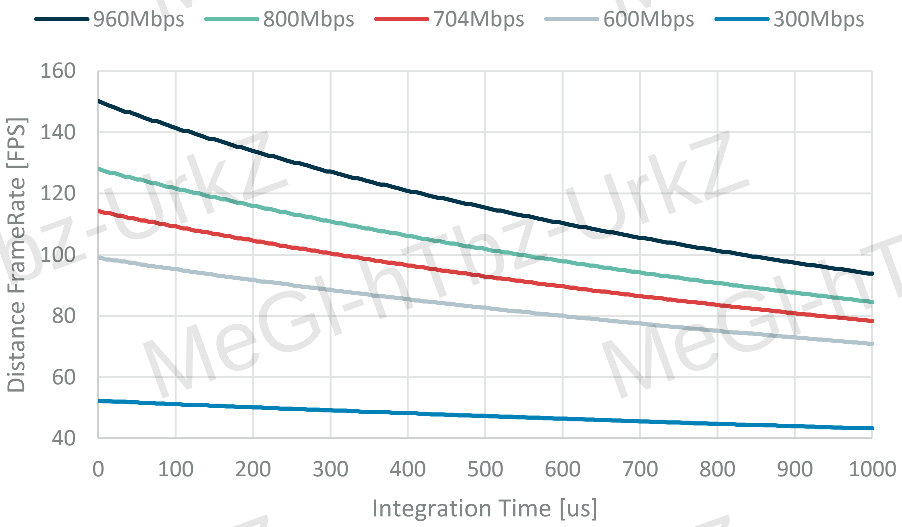


Figure 7: Theoretical Maximum Distance Frame Rate in function of Integration Time (per phase)

Using higher integration time will increase the power consumption and self-heating. For safe operation within the automotive ambient temperature range of -40 to 105 °C this self-heating must be limited to 20 °C. A typical thermal resistance of 12K/W will result in max. allowed power of 1666mW which will not be reached by the device. However, a poor PCB design will result in worse thermal resistance and thus the framerate will not be readout but thermal / power limited, please make sure sufficient ground planes / heat dissipation is available.

3.6. Decoupling Recommendations

It is generally known that sensor performance can degrade with noisy input supplies. Specifications in this datasheet are only valid when stable voltage levels are available. Common decouple techniques use a two-step architecture consisting of a small capacitor (~10-100nF) as close as possible to the supply pin, combined with a bigger capacitor further away from the device, both connected to a low impedance ground plane to minimize inductance. Additionally, a small series ferrite bead can be used to keep high frequency noise outside of the IC, but also to keep internally generated noise from propagating to the rest of the system.

External Voltage Supplies
- VDDA : min. 1x 4.7µF
- VDDMIX : min. 1x 100nF & 4.7µF
- VDDD : min. 1x 100nF & 4.7µF
- VDDIF : min. 1x 100nF & 1µF

Internal Generated Voltage Supplies
- VBO1, VBO2 combined: min. 1x 4.7µF
- VRSTL : min. 1x 1µF
- VRL1, VRL2 combined: min. 1x 4.7µF

These recommendations are based on analysis of different available hardware platforms.
Each new hardware design requires an individual analysis to find & optimize the correct decoupling strategy.

3.7. Power-up Sequence

VDDD and VDDMIX both use a 1V2 supply and it is possible to combine them on a single regulator source. However, VDDMIX exhibits high peak currents during the integration time that could compromise the stability of VDDD. It is recommended to separate both domains by ferrite bead and adequate filtering.
When using two regulators it is mandatory that VDDD is enabled simultaneously or not later than VDDMIX, and that VDDMIX is disabled before VDDD on power-down. More detailed power-up timings can be found in chapter 7. A slew rate of maximum 25 mV/µs has been specified for each power supply to avoid oscillations during power-up.

3.8. Input Clock Requirements

MLX75027 requires a fixed clock input signal of 8 MHz generated by an external crystal oscillator.

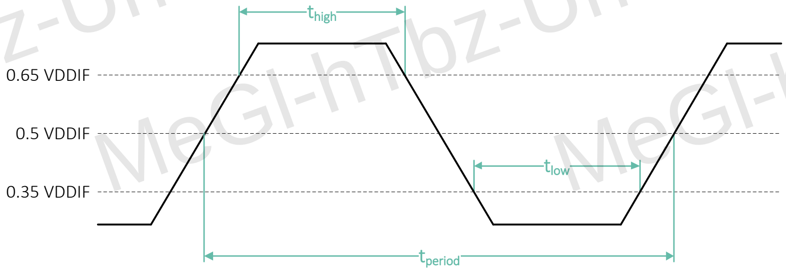


Figure 8: CLK square waveform input diagram

Parameter	Symbol	Min.	Typ.	Max.	Unit
CLK high level	CLK_{HIGH}	1.2			V
CLK low level	CLK_{LOW}			0.6	V
CLK frequency			8		MHz
CLK low level width	t_{low}	50	62.5	75	ns
CLK high level width	t_{high}	50	62.5	75	ns
CLK jitter				600	ps

Table 12: CLK input characteristics

3.9. I²C Specifications

MLX75027 features a standard (up to 400 kHz) inter-integrated circuit communication interface, known as I²C. The sensor operates as I²C slave with default slave address of 0x57. This address can be changed via the external PIN SLASEL (more information can be found in section 6.1.6). The master I²C device is responsible to initiate all communication, it is in control of the clock line (SCL) & sends data via the SDA line. Each I²C slave on the bus monitors this communication and will respond to the master when requested.

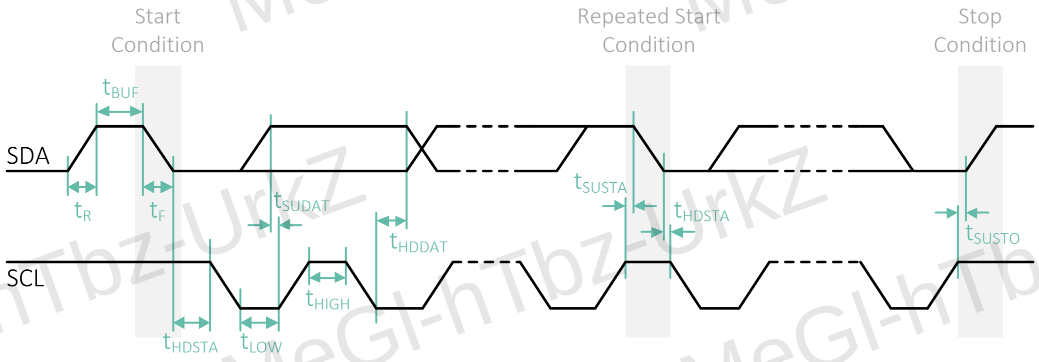


Figure 9: I²C serial communication diagram

Parameter	Symbol	Condition	Min.	Max.	Unit
Low level input voltage	V_{IL}		-0.3	0.3*VDDIF	V
High level input voltage	V_{IH}		0.7*VDDIF	1.9	V
Low level output voltage	V_{OL}	VDDIF < 2V, sink 3mA	0	0.2*VDDIF	V
Output fall time	t_{of}	Load 10pF - 400 pF 0.7*VDDIF - 0.3*VDDIF		250	ns
Input current	I_i	0.1*VDDIF - 0.9*VDDIF	-10	10	µA
SDA I/O capacitance	$C_{I/O}$			10	pF
SCL input capacitance	C_I			10	pF

Table 13: I²C Electrical Specifications

Parameter	Symbol	Min.	Max.	Unit
SCL clock frequency	f_{SCL}	0	400	kHz
Rise time (SCD & SCL)	t_R		300	ns
Fall time (SDA & SCL)	t_F		300	ns
Hold time (start condition)	t_{HDSTA}	0.6		ns
Setup time (rep.-start condition)	t_{SUSTA}	0.6		µs
Setup time (stop condition)	t_{SUSTO}	0.6		µs
Data setup time	t_{SUDAT}	100		µs
Data hold time	t_{HDDAT}	0	0.9	µs
Bus free time between stop and start condition	t_{BUF}	1.3		µs
Low period of the SCL clock	t_{LOW}	1.3		µs
High period of the SCL clock	t_{HIGH}	0.6		µs

Table 14: I²C Fast Mode Specifications

4. Optical Characteristics

4.1. VGA Pixel Array Configuration

The pixel array has a total of 640 x 480 DepthSense® pixels. Each pixel consists of 2 individual taps called tap A and tap B. Information from both taps is needed for a reliable distance calculation. The data format (or output modes) available via the MIPI CSI2 video interface can be selected by the user and are described in more detail in section 8.3. The pixels are read out from bottom left, to top right, first horizontally, afterwards vertically, like indicated in this figure. This picture represents the physical pixel orientation, please note that output will have pixel 1 on top left to compensate for the lens by default as explained in section 8.21.

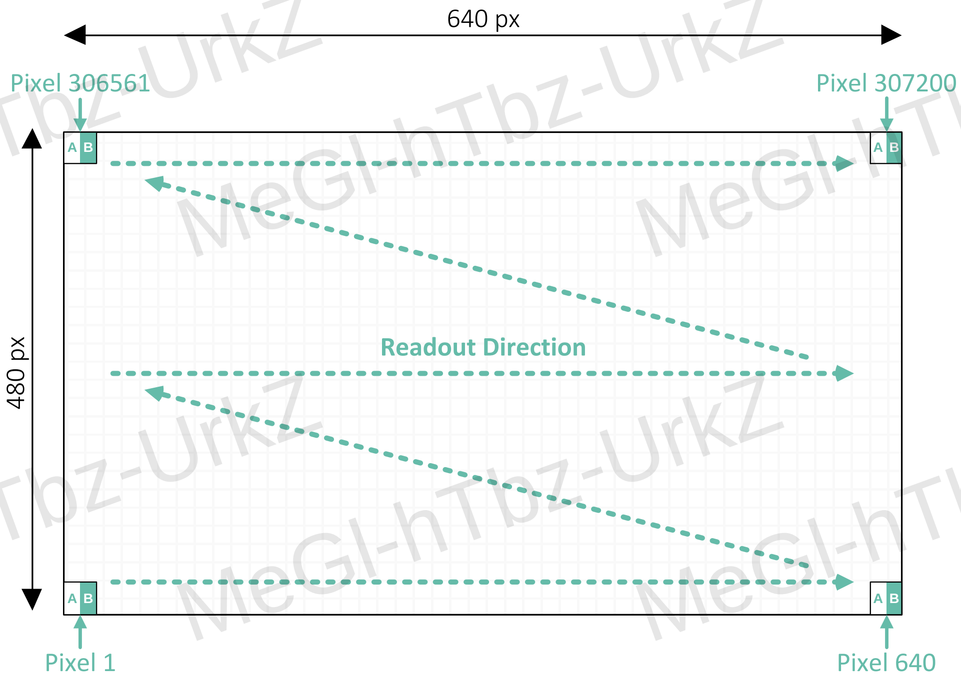


Figure 10: VGA readout

4.2. Pixel & Image Array Characteristics

Parameter		Min.	Typ.	Max.	Unit
Pixel pitch			10		µm
Pixel architecture		Dual Tap Current Assisted Photonic Demodulator			
External Quantum Efficiency[1] @ 850nm			51.0		%
External Quantum Efficiency[1] @ 940nm			28.0		%
Pixel dark noise			83		e-
AC demodulation contrast[2] @ 40MHz			85		%
AC demodulation contrast[2] @ 100MHz			78		%
Single tap dark current		20	51	508	ke-/s
Single tap full well capacity		106	160		ke-
Single tap conversion gain			0.0106		DN/e-
Phase drift over temperature[3]			0.046		deg/°C
Local PDNU (before calibration)[4 7]	-40ºC 35ºC 105ºC		1.8 2.2 2.7	6 6 6	mm
Global PDNU (before calibration)[5 7]	-40ºC 35ºC 105ºC		15 19 27	50 50 60	mm
Microlense(s)[6]		yes			
Maximum CRA (chief ray angle)	-RTC -RTI -STI			30 15 15	°

Table 15: Pixel & Image Array Characteristics

Note[1] : External quantum efficiency (EQE) can be calculated as $\mathrm{EQE}_\lambda = \frac{\mathrm{RE}_\lambda}{\lambda} \cdot \frac{\mathrm{h} \cdot \mathrm{c}}{\mathrm{e}} \cdot \mathrm{FF} = \frac{\mathrm{RE}_\lambda}{\lambda} \cdot 1240 \cdot \mathrm{FF}$

RE_λ = responsivity at wavelength (in A/W)
λ = the wavelength (in nm)
h = Planck's constant
c = speed of light in vacuum
e = elemental charge
FF = fill factor (in %)

Note[2] : Detailed AC demodulation contrast data can be found in Figure 11.
Note[3] : Stability of the calculated phase (= distance) over temperature
Note[4] : Local PDNU (phase depth non uniformity) is a metric for the phase offset between 3x3 pixel blocks for a homogeneous flat field measurement
Note[5] : Global PDNU is similar to local PDNU but data is based on 10x10 pixel blocks
Note[6] : The microlens array material is sensitive to excessive UV radiation. In product qualification it has been exposed with a constant UV equivalent of 10 years of sunlight without discernible degradation of the structure integrity. It is our recommendation to limit direct UV radiation during camera assembly/glue processes as much as possible
Note[7] : Operating conditions: 100MHz, 940nm

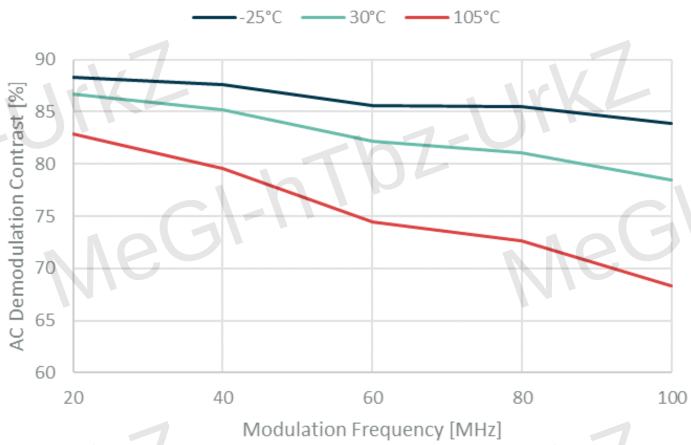


Figure 11: AC Demodulation Contrast in function of Modulation Frequency

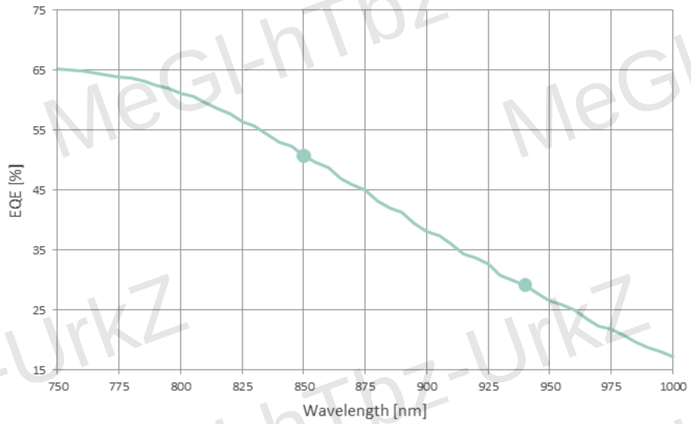


Figure 12: External Quantum Efficiency in function of Wavelength

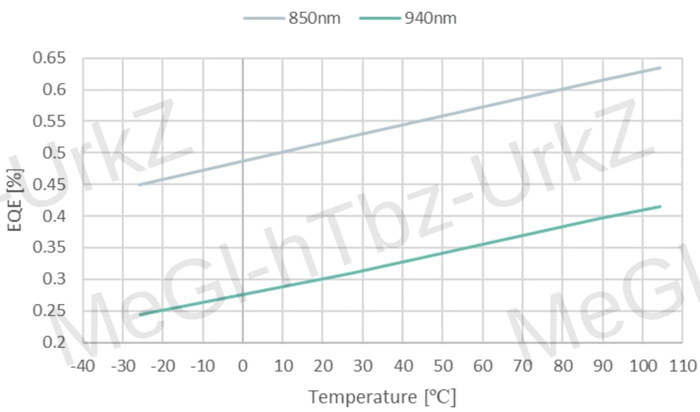


Figure 13: External Quantum Efficiency in function of Temperature

4.3. CRA (Chief Ray Angle)

		CRA (°)	
Image Height[1] (%)	Image Height[1] (mm)	MLX75027RTC	MLX75027RTI MLX75027STI
0	0.0	0	0
10	0.4	3.3	1.7
20	0.8	6.6	3.3
30	1.2	9.8	4.9
40	1.6	13	6.5
50	2.0	16.1	8.0
60	2.4	19.1	9.6
70	2.8	22.0	11.0
80	3.2	24.8	12.4
90	3.6	27.5	13.7
100	4.0	30	15

Table 16: Image Height vs CRA

Note[1] : Image height is defined along the diagonal axis of the image array as shown in Figure 14: Image Height Definition.

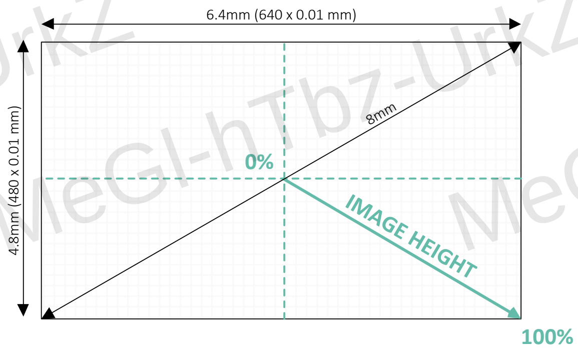


Figure 14: Image Height Definition

4.4. MTF (Modulation Transfer Function)

The modulation transfer function is an indication on the system response to different spatial frequencies.
It tends to decrease with an increase in spatial frequency. A typical example is an out of focus lens, which has a low modulation factor for higher frequencies, resulting in an overall blur of the edges in the image.

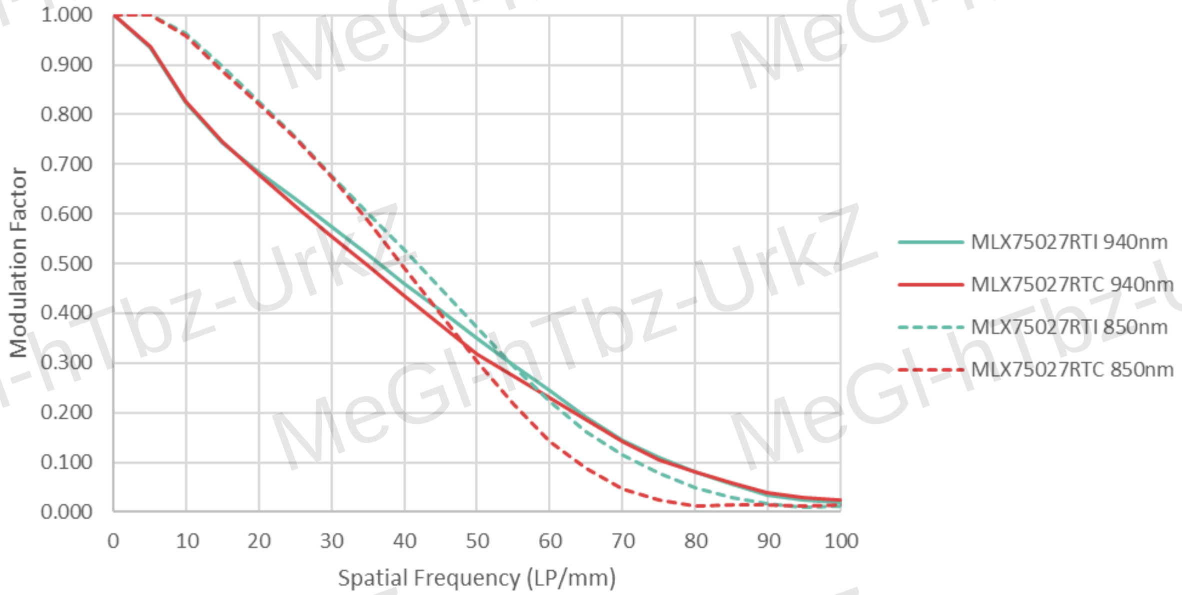


Figure 15: Modulation Transfer Function

The system MTF is the combination of the image sensor and the selected optics.
The shown data is considered the sensor only MTF, as it has been compensated for lens influences.

4.5. Application Lens Design Recommendations

When designing or selecting external optics to focus the light on the optical sensitive pixel area there are a few recommendations to take into account:

- To avoid pixel saturation under strong sunlight an optical band pass filter is highly recommended. The spectral width of this filter depends on the type of illumination, LED or VCSEL, and should be as small as possible, taken into account the spectral drift over temperature.
- To reduce the illumination radiant intensity and to maximize the system efficiency the lens aperture should be as high as possible (= low F-number)

4.6. Defective Pixels and Clusters

Parameter		Typ.	Max.
Defective White Pixel	35ºC 105ºC	2 7	10 150
Defective Dark Pixel	35ºC 105ºC	0 0	16 16
Defective Norm Pixel	35ºC 105ºC	0 0	10 100
Defective Phase pixel	35ºC 105ºC	0 0	18 110
Clusters "Type 1"	35ºC 105ºC	0 0	3 5
Clusters "Type 2"		0	0
Clusters "Type 3"		0	0

Table 17: Defective pixels and clusters

The definition of the defective pixel types and clusters can found in section 4.6.1 and 4.6.2.

4.6.1. Defective Pixels

Defective pixels are pixels that are not performing as expected.
There are two main categories (each with two subcategories)

- Pixels that fail to sense light levels correctly
- Pixels that behave differently compared to its neighbours

4.6.1.1. Definition of Defective Pixel Based On Light Response

Based on light response the following definitions are applicable:

- White Pixel: Pixel that exceeds a threshold value on either tap under dark conditions
- Dark Pixel: Pixel that fails to exceed a threshold on either tap under AC light conditions

Each threshold is based on the statistical mean value and standard deviation of all pixels including a margin.

4.6.1.2. Definition of Defective Pixel Based on Non-Uniformity

The phase and amplitude for each pixel is calculated and compared with the local PDNU (Pixel Depth Non Uniformity) and local PNNU (Pixel Norm Non Uniformity) value, to avoid local outliers

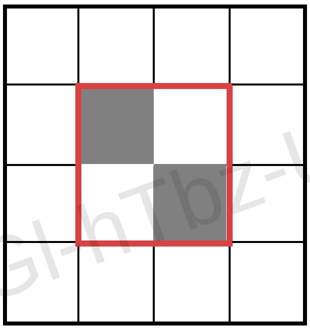
If the pixel value substantially deviates from the median value for each 10*10 ROI including a margin, it's flagged as a defective pixel, both for depth and norm.

4.6.2. Defective Clusters

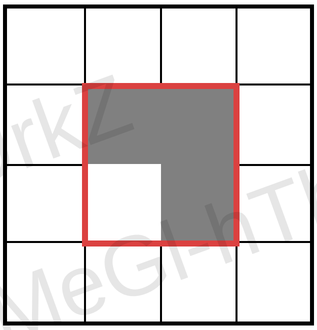
4.6.2.1. Definition

A cluster is defined as a ROI of 2x2 or 3x3 pixels that includes more than one defective pixel.
There are three types of clusters:

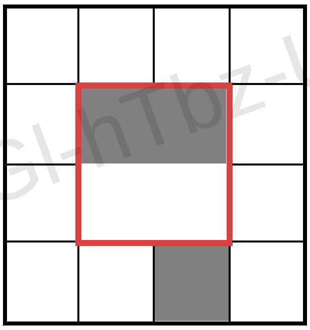
- Type 1 – clusters with 2 defective pixels in any 2x2 ROI. (This also includes type 2 and 3)
- Type 2 – clusters with >2 defective pixels in any 2x2 ROI.
- Type 3 – clusters with >3 defective pixels in any 3x3 ROI



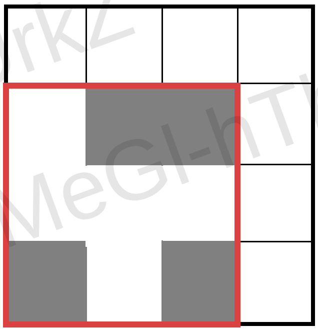
Type 1 – 2 defective pixels in 2x2 ROI



Type 2 – >2 defective pixels in 2x2 ROI



Type 1 – 2 defective pixels in 2x2 ROI



Type 3 – >3 defective pixels in 3x3 ROI

5. ISO 26262 - Functional Safety

ISO 26262 acts as a guidance to provide the appropriate standardized requirements and processes to determine integrity levels, also known as **Automotive Safety Integrity Levels or ASILs.**
The purpose is to reduce the risks caused by systematic and random failures for critical applications.

At Melexis we embrace a culture of safety with demonstrated competencies and products.
Detailed information can be found inside our Melexis "ASIL ready" program :
https://www.melexis.com/en/tech-talks/melexis-functional-safety

MLX75027RTI is ASIL capable and ready for integration in safety applications as described in the Safety Integration Guidelines (available on request).

- Compliance with ISO26262-8:2018 chapter 13
- FMEDA exceeds hardware metrics required for ASIL-B in line with relevant Technical Safety Requirements as listed in the Safety Integration Guidelines

For specific functional safety support we invite you to contact us on tof3d@melexis.com.

6. Communication Interface(s)

MLX75027 uses one low speed bidirectional I2C interface for register control and one unidirectional high speed MIPI CSI2 serial video output interface.

6.1. I²C (Inter-Integrated Circuit)

This 2-wire serial communication protocol supports 16-bit register addresses and 8-bit data messages.

6.1.1. I²C Timing Sequence

S	Slave Address [7:1]	R/W	A	Register Address [15:8]	A	Register Address [7:0]	A	Data [7:0]	A/Ā	P

From master to slave
From slave to master
Direction depends on operation

S = Start condition
Sr = Repeated start condition
P = Stop condition

A = Acknowledge
Ā = Negative acknowledge

R/W = read/write command
0 : Write (master > slave)
1 : Read (slave > master)

The data is transferred serially, MSB first in 8-bit units. After each data byte is transferred, A (Acknowledge) / Ā (Negative acknowledge) is transferred. Data (SDA) is transferred at the clock (SDL) cycle. SDA can change only while SCL is low, so the SDA value must be held while SCL is high. The Start condition is defined by SDA changing from high to low while SCL is high. When the Stop condition is not generated in the previous communication phase and Start condition for the next communication is generated, that Start condition is recognized as a Repeated Start condition.

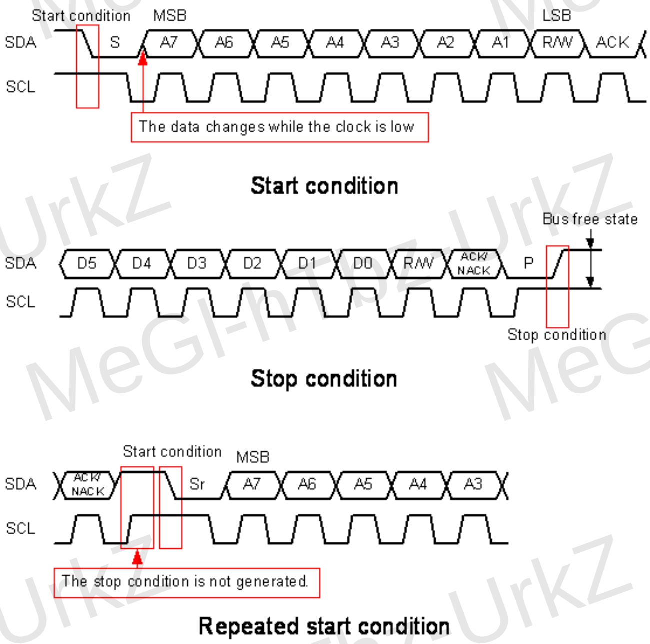
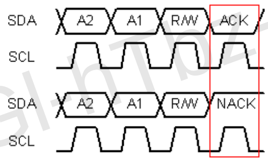


Figure 16: I2C conditions

After transfer of each data byte, the Master or the sensor transmits an Acknowledge / Negative acknowledge and releases (does not drive) SDA. When a Negative acknowledge is generated, the Master must immediately generate the Stop Condition and end the communication.

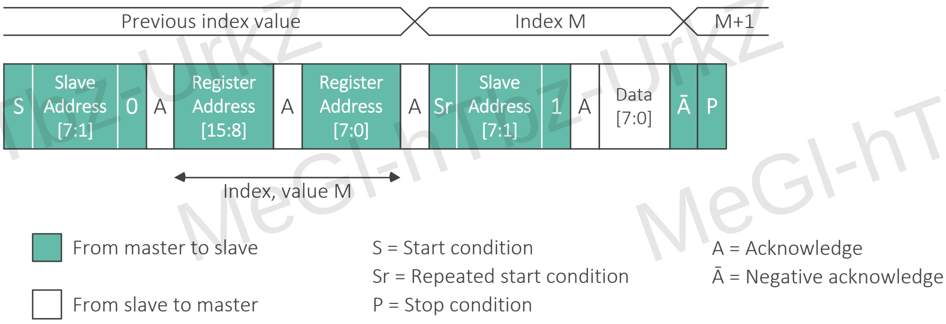


Acknowledge, Negative Acknowledge

Figure 17: I2C negative acknowledge

6.1.2. Single I²C Read

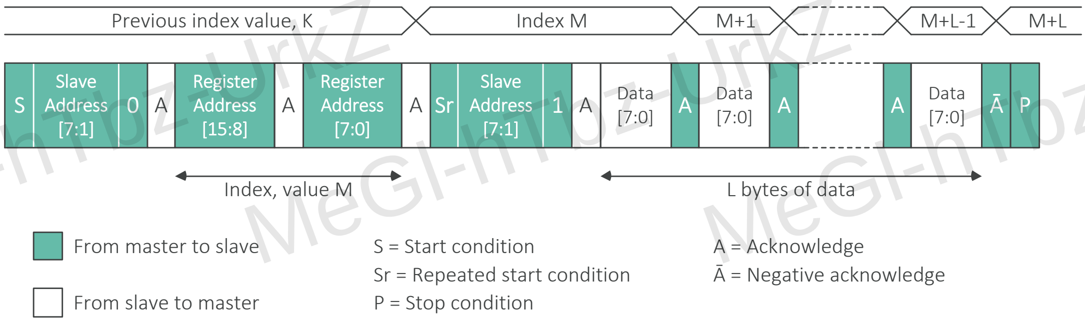
The sensor has an index function that indicates which address it is focusing on. When reading data, the Master must set the index value to the address to be read. For this purpose, it performs a dummy write operation up to the register address. The upper level of the figure shows the sensor internal index value, and the lower level of the figure shows the SDA I/O data flow. The Master sets the sensor index value to M by designating the sensor slave address with a write request, then designating the address (M). Then, the Master generates the start condition. The Start Condition is generated without generating the Stop Condition, so it becomes the Repeated Start Condition. Next, when the Master sends the slave address with a read request, the sensor outputs an Acknowledge immediately followed by the address data from index M on SDA. After the Master receives the data, it generates a Negative Acknowledge and the Stop Condition to end the communication



Note: It is possible to omit the Register Address [15:0] from the communication, in that case the sensor will simply read the value of register previously set to index M.

6.1.3. Sequential I²C Read

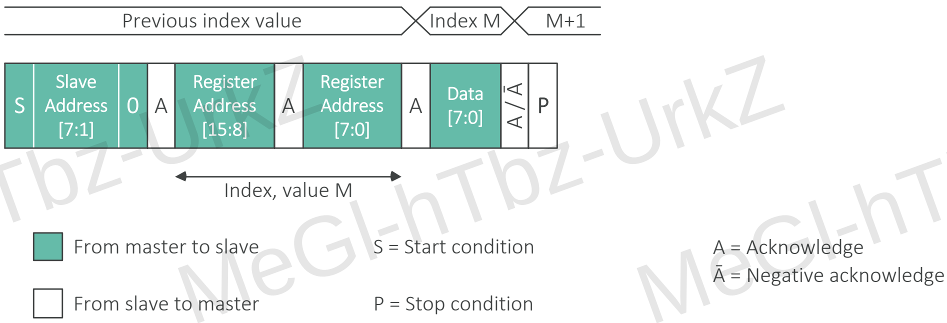
A sequential read of the data reads multiple registers sequentially without setting the register addresses individually. The Master must set the index value to the start of the addresses to be read. For this purpose, a dummy write operation includes the register address setting. The Master sets the sensor index value to M by designating the sensor slave address with a read request, then designating the address (M). Then, the Master generates the Repeated Start Condition. Next, when the Master sends the slave address with a read request, the sensor outputs an Acknowledge followed immediately by the data from index M on SDA. When the Master outputs an Acknowledge (instead of Negative acknowledge for a single I²C read) after it receives the data, the index value inside the sensor is incremented and the data at the next address is output on SDA. This allows the Master to read data sequentially. After reading the necessary data, the Master generates a Negative Acknowledge and the Stop Condition to end the communication.



Note: It is possible to omit the Register Address [15:0] from the communication, in that case the sensor will simply read the values of the registers starting at the previously set index M.

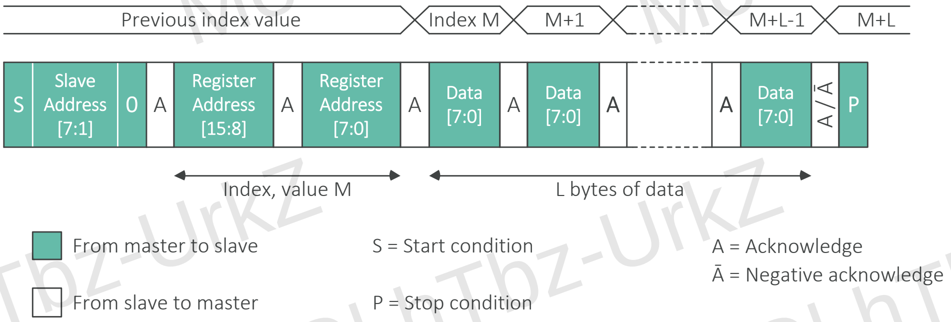
6.1.4. Single I²C Write

The Master sets the sensor index value to M by designating the sensor slave address with a write request, and designating the register address (M). After that the Master can write the value in the designated register by transmitting the data to be written. After writing the necessary data, the Master generates the Stop Condition to end the communication.



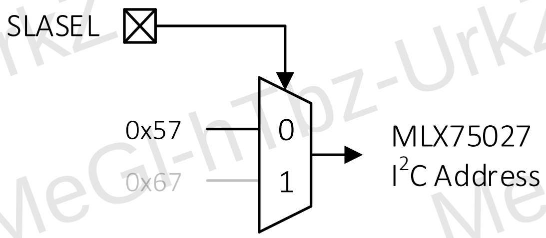
6.1.5. Sequential I²C Write

The Master can write a value to register address M by designating the sensor slave address with a write request, designating the address (M), and then transmitting the data to be written. After the sensor receives the write data, it outputs an Acknowledge and at the same time increments the register address, so the Master can write to the next address simply by continuing to transmit data. After the Master writes the necessary number of bytes, it generates the Stop Condition to end the communication.



6.1.6. I²C Slave Address

For communication with MLX75027 via I²C the user has to choose between two different 7bit slave addresses. Selection can be done by the external SLASEL pin, by connecting it either to VDDIF (high) or DGND (low).



Note : I2C slave address 0x67 might not be programmed on engineering samples.
To avoid bring-up issues, please connect SLASEL to GND.

6.2. MIPI Alliance CSI-2 Description

This section describes a limited set of CSI-2 functionality needed to understand operation of MLX75027. For a full interface description, please refer to MIPI Alliance CSI-2 Specification version 1.20.

6.2.1. Packet Structure

CSI-2 uses a byte oriented, packet based protocol that supports the transport of arbitrary data using *Short Package* (SP) and *Long Package* (LP) formats. A 32bit *Short Packet* does not have any data or a *Package Footer* (PF). Only FS (*Frame Start*) or FE (*Frame End*) indicators use *Short Packets*.

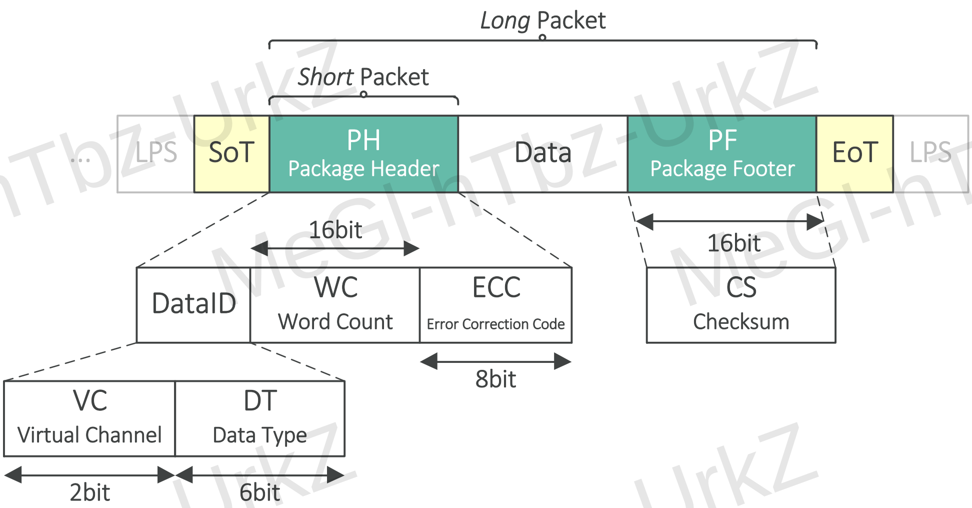


Figure 18: Package structure

Every packet starts with a SoT (start of transmission) sequence preceded by a LPS (low power state). An EoT (end of transmission) sequence followed by the low power state indicates the end of a packet.

Each byte is transmitted with the least significant bit first, in case of multi-byte data (such as WC or CS) the least significant byte will be transmitted first, unless otherwise specified by the data format.

VC: The virtual channel identifier provides separate channels for different data flows that are interleaved in the data stream (lane indicator). The default value is 0.

DT: The data type value specifies the format and content of the data payload.
0x00 = FS (Frame Start) 0x12 = Embedded data (or MetaData)
0x01 = FE (Frame End) 0x2C = RAW12 pixel data

WC: For *short* packets the word count field is considered a 16bit data field, representing the Frame Count [7:0]. After each FS (Frame Start) transmission, the Frame Count will be increased by 1. For *long* packets word count specifies the total amount of bytes between the end of PH and start of PF.

ECC: The error correction code used is a 7+1bits Hamming-modified code. This code allows single-bit errors to be corrected and 2-bit errors to be detected in the DataID and WC fields but is not capable of doing both simultaneously.

CS: To detect possible errors in the data transmission, a checksum is calculated over each data packet. The checksum is a 16bit CRC generated by this polynomial:

$$CRC = x^{16} + x^{12} + x^5 + x^0$$

When WC is zero, CS will be 0xFFFF

6.2.2. Data Format RAW12

Each DepthSense® pixel is represented by 12bit data packed like 8bit data.

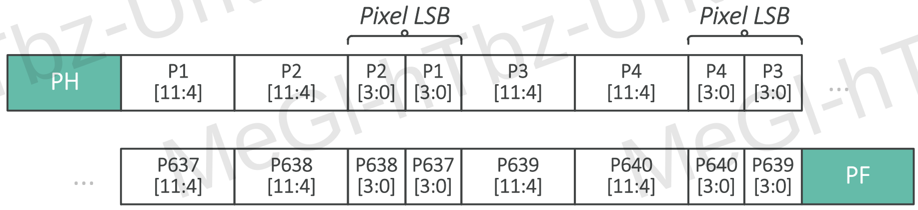


Figure 19: Example of pixel ordering for one full line transmission

Figure 20: Example of pixel ordering for one full frame transmission

Table 18 specifies the minimum packet data size constraints.
The total length of each packet must be a multiple of the values in this table.

# Pixels	# Bytes	# Bits
2	3	24

Table 18: RAW12 Packet size constraints

6.2.2.1. Data Format in 4 Lane MIPI Configuration

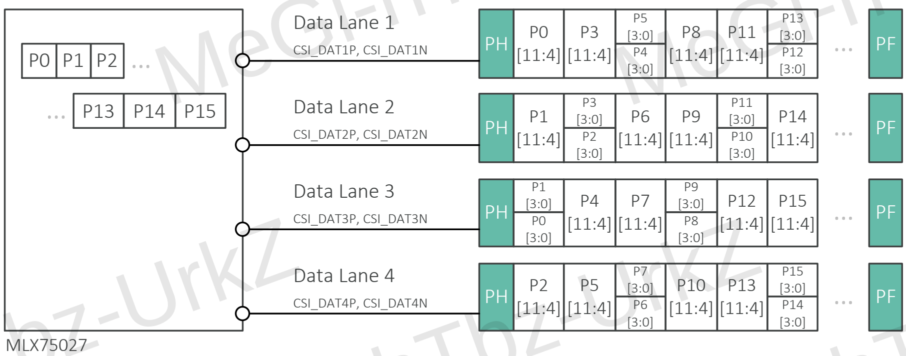


Figure 21: Pixel Data Format in 4 Lane Data Configuration

6.2.2.2. Data Format in 2 Lane MIPI Configuration

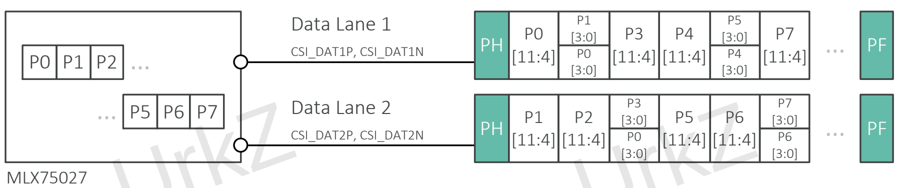


Figure 22: Pixel Data Format in 2 Lane Data Configuration

7. Start-up Sequence

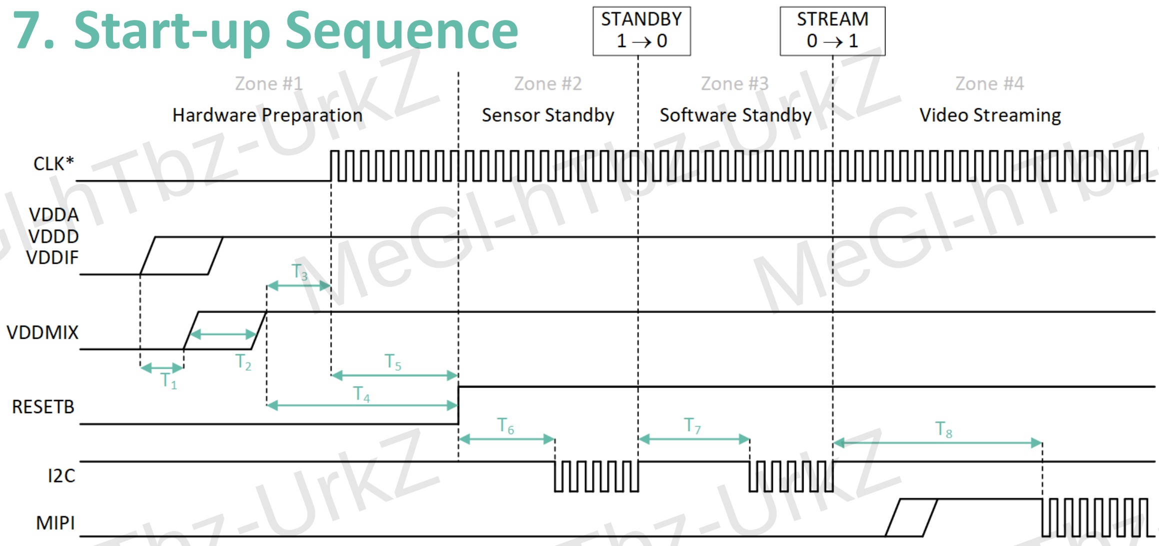


Figure 23: Sensor start-up sequence

* Availability of CLK signal before voltage domain bring up is also accepted

0x1000	7	6	5	4	3	2	1	0
R/W	-	-	-	-	-	-	-	**STANDBY**

Default Value 0x01

0x1001	7	6	5	4	3	2	1	0
R/W	-	-	-	-	-	-	-	**STREAM**

Default Value 0x00

Zone #1 : **Hardware Preparation :** Time to supply the clock, the required voltage domains and initialize the RESETB level. RESETB is a digital control signal, the µC keeps it low until all requirements of zone 2 have been fulfilled.

Zone #2 : **Sensor Standby :** Time to define input clock settings, as shown in section 7

Zone #3 : **Software Standby :** In this period it's advised to write all frame acquisition parameters (like integration time, modulation frequency & others) before video streaming.

Zone #4 : **Video Streaming :** Frame capture is active and MIPI output data is available. Register changes during active frame acquisition will be applied on the next frame.

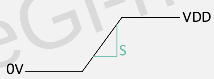
Description		Symbol	Min.	Max.	Unit
Slew rate for VDDA, VDDD, VDDIF, VDDMIX		S		25	mV/µs
Time between VDDA, VDDD, VDDIF ON and VDDMIX ON		T_1	0		µs
Time between VDDMIX OFF and VDDMIX ON		T_2	48		µs
Time between VDDDMIX ON and CLK ON		T_3	0		µs
Time between VDDA, VDDD, VDDIF, VDDMIX, CLK ON and RESETB OFF		T_4	100		µs
Time between CLK ON and RESETB OFF		T_5	0		µs
Time between RESETB and first I²C command		T_6	100		µs
Time between STANDBY OFF and STREAM ON		T_7	12		ms
Time between STREAM ON and first video data		T_8		$2.8 + T_{int}$	ms

Table 19: Startup timing

7.1. Initialization Process

MLX75027 requires a SW initialization on each start-up/reset and/or power cycle.

Operating Mode	Register Address	Register Value	Comment
Hardware Preparation			End *Hardware Preparation* by pulling RESETB high
Sensor Standby	0x1006	0x08	Fixed Input Clock Settings
	0x1007	0x00	
	0x1040	0x00	
	0x1041	0x96	
	0x1042	0x01	
	0x1043	0x00	
	0x1044	0x00	
	0x1046	0x01	
	0x104A	0x01	
	0x1000	0x00	Change from *Sensor Standby* to *Software Standby* by changing register 0x1000 (default value 0x01) to value 0x00
Software Standby	263 initialization registers		Program the FULL initialization map from section 7.2
	Add here relevant application registers that require an update of their reset value (examples listed below)		
	0x100C ... 0x1071	custom	Configure video output interface (see section 8.1)
	0x2020	custom	Configure TRIGGER or CONTINUOUS mode (see section 8.2)
	0x2100	custom	
	0x2F05	custom	
	0x2F06	custom	
	0x2F07	custom	
	0x3071	custom	
	0x0828	custom	Configure Data Output Mode (see section 8.3)
	0x0800	custom	Configure HMAX related settings (see section 8.4)
	0x5267	custom	
	0x21BE ... 0x104B	custom	Configure Modulation Frequency (see section 8.7)
	0x21E8	custom	Configure number of phases (see section 8.11)
	0x2120 ... 0x213F	custom	Configure Integration Time per phase (see section 8.13)
	0x21B4 ... 0x21B7	custom	Configure PHASE_SHIFT per phase (see section 8.14)
	End of relevant application registers		
	0x1001	0x01	Enter *Video Streaming* by changing register 0x1001 (value 0x00) to value 0x01
Video Streaming			Application is now running

Table 20: Initialisation process

A complete application register map can be requested from Melexis by contacting tof3d@melexis.com

7.2. Initialization Register Map

This set of initialization registers are listed in order or priority (top > bottom, left > right, next page) :

Register Address	Register Value	Register Address	Register Value	Register Address	Register Value	Register Address	Register Value
0x10D3	0x10	0x414A	0x01	0x479B	0x00	0x4955	0xA0
0x1448	0x06	0x414B	0x01	0x479C	0x1F	0x4957	0xA1
0x1449	0x40	0x414C	0x01	0x479D	0xFF	0x4984	0x00
0x144A	0x06	0x414D	0x01	0x479E	0x00	0x4985	0xA0
0x144B	0x40	0x4158	0x01	0x479F	0x00	0x4987	0xA1
0x144C	0x06	0x4159	0x01	0x47A2	0x00	0x49B9	0x78
0x144D	0x40	0x415A	0x01	0x47A3	0x00	0x49C3	0x3C
0x144E	0x06	0x415B	0x01	0x47A6	0x00	0x49C9	0x76
0x144F	0x40	0x415C	0x01	0x47A7	0x00	0x49D3	0x3F
0x1450	0x06	0x415D	0x01	0x47AA	0x00	0x49DC	0x00
0x1451	0x40	0x415E	0x01	0x47AB	0x00	0x49DD	0xA0
0x1452	0x06	0x415F	0x01	0x47AC	0x1F	0x49DF	0xA1
0x1453	0x40	0x4590	0x00	0x47AD	0xFF	0x49EF	0x78
0x1454	0x06	0x4591	0x2E	0x47AE	0x00	0x49F9	0x3C
0x1455	0x40	0x4684	0x00	0x47AF	0x00	0x49FF	0x78
0x1456	0x06	0x4685	0xA0	0x47B2	0x00	0x4A05	0x3C
0x1457	0x40	0x4687	0xA1	0x47B3	0x00	0x4A0B	0x76
0x2203	0x1E	0x471E	0x07	0x47B6	0x00	0x4A11	0x3F
0x2C08	0x01	0x471F	0xC9	0x47B7	0x00	0x4A1A	0x00
0x3C2B	0x1B	0x473A	0x07	0x47BA	0x00	0x4A1B	0xA0
0x400E	0x01	0x473B	0xC9	0x47BB	0x00	0x4A1D	0xA1
0x400F	0x81	0x4770	0x00	0x47BC	0x1F	0x4A1F	0x78
0x40D1	0x00	0x4771	0x00	0x47BD	0xFF	0x4A29	0x3C
0x40D2	0x00	0x4772	0x1F	0x47BE	0x00	0x4A4A	0x00
0x40D3	0x00	0x4773	0xFF	0x47BF	0x00	0x4A4B	0xA0
0x40DB	0x3F	0x4778	0x06	0x47C2	0x00	0x4A4D	0xA1
0x40DE	0x40	0x4779	0xA4	0x47C3	0x00	0x4A7A	0x00
0x40DF	0x01	0x477A	0x07	0x47C6	0x00	0x4A7B	0xA0
0x4134	0x04	0x477B	0xAE	0x47C7	0x00	0x4A7D	0xA1
0x4135	0x04	0x477D	0xD6	0x47CA	0x00	0x4AEE	0x00
0x4136	0x04	0x4788	0x06	0x47CB	0x00	0x4AEF	0xA0
0x4137	0x04	0x4789	0xA4	0x4834	0x00	0x4AF1	0xA1
0x4138	0x04	0x478C	0x1F	0x4835	0xA0	0x4B2E	0x00
0x4139	0x04	0x478D	0xFF	0x4837	0xA1	0x4B2F	0xA0
0x413A	0x04	0x478E	0x00	0x4878	0x00	0x4B31	0xA1
0x413B	0x04	0x478F	0x00	0x4879	0xA0	0x4B5A	0x00
0x413C	0x04	0x4792	0x00	0x487B	0xA1	0x4B5B	0xA0
0x4146	0x01	0x4793	0x00	0x48BC	0x00	0x4B5D	0xA1
0x4147	0x01	0x4796	0x00	0x48BD	0xA0	0x4B86	0x00
0x4148	0x01	0x4797	0x00	0x48BF	0xA1	0x4B87	0xA0
0x4149	0x01	0x479A	0x00	0x4954	0x00	0x4B89	0xA1

Table 21: Initialization Map Part I

Register Address	Register Value	Register Address	Register Value	Register Address	Register Value	Register Address	Register Value
0x4B9F	0x1A	0x4CFF	0xC9	0x4D70	0x06	0x4EA1	0x03
0x4BAF	0x1A	0x4D04	0x06	0x4D71	0xA4	0x4EA5	0x00
0x4BB7	0x1A	0x4D05	0x98	0x4D72	0x07	0x4EA7	0x00
0x4BC7	0x1A	0x4D06	0x07	0x4D73	0x49	0x4F05	0x04
0x4BCF	0x1A	0x4D07	0xB1	0x4D78	0x06	0x4F0D	0x04
0x4BEE	0x00	0x4D18	0x06	0x4D79	0xA4	0x4F15	0x04
0x4BEF	0xA0	0x4D19	0xA4	0x4D7A	0x07	0x4F19	0x01
0x4BF1	0xA1	0x4D1A	0x07	0x4D7B	0xAE	0x4F20	0x01
0x4BF7	0x1A	0x4D1B	0x49	0x4D7C	0x1F	0x4F66	0x0F
0x4C01	0x1A	0x4D1E	0x07	0x4D7D	0xFF	0x500F	0x01
0x4C58	0x00	0x4D1F	0xC9	0x4D7E	0x1F	0x5225	0x2F
0x4C59	0xA0	0x4D2A	0x07	0x4D7F	0xFF	0x5227	0x1E
0x4C5B	0xA1	0x4D2B	0xC9	0x4D80	0x06	0x5231	0x19
0x4C6E	0x00	0x4D4A	0x07	0x4D81	0xA4	0x5245	0x07
0x4C6F	0xA0	0x4D4B	0xC9	0x4D82	0x07	0x5252	0x07
0x4C71	0xA1	0x4D50	0x06	0x4D83	0xAE	0x5253	0x08
0x4C7A	0x01	0x4D51	0x9B	0x4D84	0x1F	0x5254	0x07
0x4C7B	0x35	0x4D52	0x07	0x4D85	0xFF	0x5255	0xB4
0x4CF2	0x07	0x4D53	0xAE	0x4D86	0x1F	0x5272	0x04
0x4CF3	0xC9	0x4D56	0x07	0x4D87	0xFF	0x5273	0x2E
0x4CF8	0x06	0x4D57	0xC9	0x4E39	0x07	0x5282	0x04
0x4CF9	0x9B	0x4D5C	0x06	0x4E7B	0x64	0x5283	0x2E
0x4CFA	0x07	0x4D5D	0x98	0x4E8E	0x0E	0x5286	0x00
0x4CFB	0xAE	0x4D5E	0x07	0x4E9C	0x01	0x5287	0x5D
0x4CFE	0x07	0x4D5F	0xB1	0x4EA0	0x01		

Table 22: Initialization Map Part II

8. Register Settings

8.1. Video Output Configuration

Correct data communication settings have to be programmed in *Software Standby* mode. This is part of the initialization map as described in section 7.

0x1010	7	6	5	4	3	2	1	0
R/W	-	-	-	-	-	-	**DATA_LANE_CONFIG**	**1**

Reset Value 0x03

- 1b0: 2 data lane configuration
- 1b1: 4 data lane configuration (= default)

Registers listed in Table 23 need to be updated to support the individual lanes data transmission speeds of 300, 600, 704, 800, 904 & 960 Mbps.

# Data Lanes	Comm. Speed	0x100C	0x100D	0x100E	0x100F	0x1016	0x1017	0x1045	0x1047	0x1060	0x1071
2	300 Mbps	0x02	0x58	0x00	0x00	0x09	0x99	0x4B	0x02	0x01	0x0C
	600 Mbps	0x04	0xB0	0x00	0x00	0x04	0xCC	0x4B	0x02	0x00	0x06
	704 Mbps	0x05	0x80	0x00	0x00	0x04	0x17	0x58	0x02	0x00	0x06
	800 Mbps	0x06	0x40	0x00	0x00	0x03	0x99	0x64	0x02	0x00	0x06
	904 Mbps	0x07	0x10	0x00	0x00	0x03	0x2F	0x71	0x00	0x00	0x06
	960 Mbps	0x07	0x80	0x00	0x00	0x03	0x00	0x78	0x02	0x00	0x06
4	300 Mbps	0x04	0xB0	0x00	0x00	0x09	0x99	0x4B	0x02	0x01	0x0C
	600 Mbps	0x09	0x60	0x00	0x00	0x04	0xCC	0x4B	0x02	0x00	0x06
	704 Mbps	0x0B	0x00	0x00	0x00	0x04	0x17	0x58	0x02	0x00	0x06
	800 Mbps	0x0C	0x80	0x00	0x00	0x03	0x99	0x64	0x02	0x00	0x06
	904Mbps	0x0E	0x20	0x00	0x00	0x03	0x2F	0x71	0x00	0x00	0x06
	960 Mbps	0x0F	0x00	0x00	0x00	0x03	0x00	0x78	0x00	0x00	0x06

Table 23: Data Rate Configuration Settings 1

0x1C40	7	6	5	4	3	2	1	0
R/W	-	-	-	-	-	-	-	**CLK_OFF**

Reset Value 0x01

The clock enters a low power state (LPS) between the different data frames (CLK_OFF=1) by default. It is possible to enable to clock continuously (stay in HS mode during frame blanking) via parameter CLK_OFF=0 for compatibility with some microcontrollers.

0x0810	7	6	5	4	3	2	1	0
R/W	-	-	-	-	-	-	**VC**	

Reset Value 0x00

It is possible to modify the MIPI virtual channel (VC) identifier, supported values are 0, 1, 2 and 3.

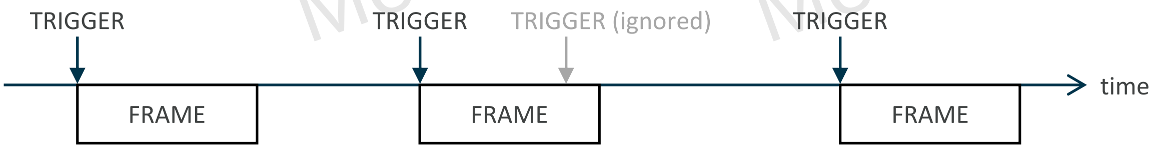
8.2. Modes of Operation

MLX75027 features three modes of operation: hardware triggered, software triggered or continuous mode. It's mandatory to change the operating mode during *Software Standby* as described in section 7.

Register Address	Register Value		
	HARDWARE TRIGGERED MODE (by external pin K11)	SOFTWARE TRIGGERED MODE	CONTINUOUS MODE (trigger will occur internally at each FRAME_TIME interval, see section 8.10)
0x2020	0x00	0x01	0x01
0x2100	0x00	0x01 (bit[0] is a self-clearing bit that acts as trigger when set to 0x1 via I2C)	0x08
0x2F05	0x07	0x01	0x01
0x2F06	0x00	0x09	0x09
0x2F07	0x00	0x7A	0x7A
0x3071	0x03	0x00	0x00

Table 24: Modes of operation

In hardware triggered mode the TRIGGERB pin accepts active low pulses to start a new frame. In software triggered mode the trigger is set by writing a 0x01 to the 0x2100 register. Both in software triggered and continuous mode TRIGGERB will act as output and will generate a 66.6ns active low signal at the start of each frame.
When using Software Triggered Mode the first frame will be automatically triggered when entering streaming mode (0x1001=0x01).
Triggers send during an active frame acquisition will be ignored as indicated here:



8.3. Data Output Modes

One Depthsense® pixel has two outputs, known as tap A and tap B, each in counterphase (180° shifted) of one another. To reduce the calculation time from raw data to distance information MLX75027 supports output modes that already combine the information from both taps, either as sum or as difference.
For Time-of-Flight experts the raw information of both taps is also available either in Raw A, Raw B or Raw A & B output modes. Regular users should use the default output mode A-B since this directly reduces the required processing power to calculate the distance map on the microcontroller. More information on the distance calculation is available section 10.
The data output mode cannot change during *video streaming*, it is mandatory to change the data output mode during *Software Standby* as described in section 7.

0x0828	7	6	5	4	3	2	1	0
R/W	-	-	-	-	-	OUTPUT_MODE		

Reset Value 0x00

- 3b000: Mode A-B (=12bit signed data)
- 3b001: Mode A+B (=12bit unsigned data)
- 3b010: Mode Raw A
- 3b011: Mode Raw B
- 3b100: Mode Raw A & B

(other values are prohibited)

A full VGA frame in Mode A-B looks like Figure 24. The default horizontal resolution is 640 pixels, except in Mode Raw A & B where two values per pixel (=1280) will be read out.

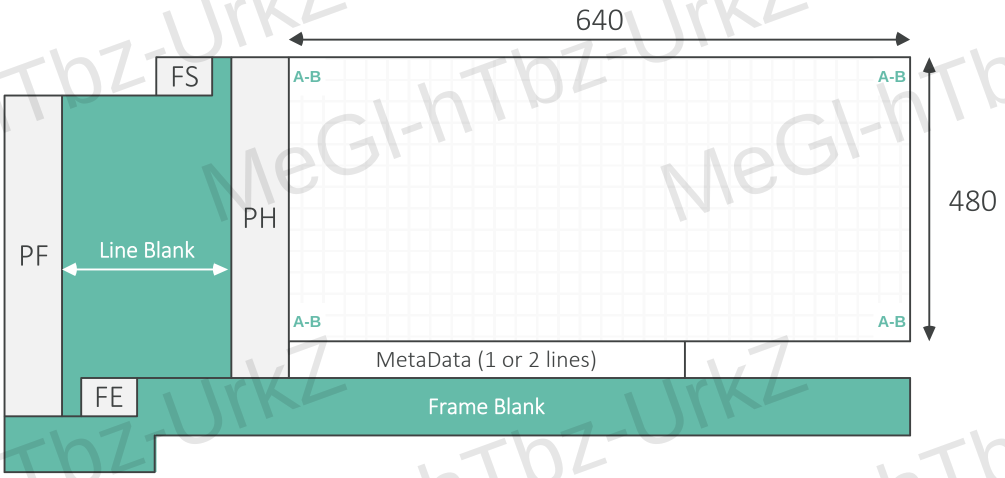


Figure 24: A single MIPI Frame

8.4. HMAX & Frame Read-Out Time

The HMAX parameter represents a number of internal clock pulses needed for one data row transmission. This time includes the communication protocol overhead (like data headers and power stage transitions), but also the actual data payload. It is a fixed value dependent on the data output configuration (section 8.1) and the output mode (section 8.3), it cannot be modified during *video streaming*. Other configuration parameters, expressed in function of HMAX, need to be modified accordingly. (see section 8.4.1, 8.4.2 and 0)

0x0800	7	6	5	4	3	2	1	0
R/W	-	-	**HMAX [13:8]**					

Reset Value 0x02

0x0801	7	6	5	4	3	2	1	0
R/W	**HMAX [7:0]**							

Reset Value 0xB6

The time needed to read out a single phase is highly linked with the HMAX parameter, the corresponding read out time can be found in Table 25: HMAX.

Operation Mode	DATA_LANE_CONFIG	Communication Speed (Mbps)	HMAX	Single Phase Readout Time[1] (ms)
Mode A-B Mode A+B Mode Raw A Mode Raw B	2	300	0x0E78	7.87
		600	0x0750	3.98
		704	0x0640	3.40
		800	0x0584	3.00
		904	0x04E8	2.70
		960	0x049E	2.51
	4	300	0x0860	4.56
		600	0x0444	2.32
		704	0x03A8	1.99
		800	0x033A	1.76
		904	0x02E2	1.57
		960	0x02B6	1.47
Mode Raw A&B	2	300	0x1A80	14.42
		600	0x0D54	7.25
		704	0x0B60	6.19
		800	0x0A06	5.45
		904	0x08E6	4.84
		960	0x0860	4.56
	4	300	0x0E60	7.82
		600	0x0744	3.95
		704	0x0636	3.38
		800	0x057A	2.98
		904	0x0514	2.76
		960	0x0514	2.76

Table 25: HMAX

Note[1] : Continuous wave time of flight typically uses 4 phases/quads to calculate a single distance image. These four snapshots are taken sequentially in time, which leads to the fact that any time delay between these images can contribute to motion blur, depending on the speed of the detected object. The time between the images is dominated by the sensor read out time. In order to minimize motion artefacts, the read out time should be chosen as short as possible. The timing listed in this table are maximum values (in millisecond) for a single phase at full resolution (640x480 pixels). Reducing the image size (with ROI or binning) has a direct and positive impact on the read out time.

Important : Different timing related registers are closely linked to the HMAX parameter.
It's the user responsibility to update PLLSETUP, PRETIME & RANDNM0 each time HMAX value is adjusted.

8.4.1. PLLSETUP

0x4010	7	6	5	4	3	2	1	0
R/W	**PLLSETUP**							

Reset Value 0x5F

PLLSETUP is the time required for the *Timing Generator* block (see section 2) to settle before each frame and it can be calculated as $\mathrm{ROUNDUP}\left(\frac{503 \cdot 120}{\mathrm{HMAX}} + 8\right)$

8.4.2. PRETIME

0x4015	7	6	5	4	3	2	1	0
R/W	-	-	-	**PRETIME [12:8]**				

Reset Value 0x00

0x4016	7	6	5	4	3	2	1	0
R/W	**PRETIME [7:0]**							

Reset Value 0x0A

The PRETIME registers both incorporate the pixel reset timing before each integration time and the Px_PREHEAT / Px_PREMIX functionality. In case no Px_PREHEAT / Px_PREMIX is enabled the register value can be calculated as $\mathrm{ROUNDUP}\left(\frac{Total\ pretime\ (us) \cdot 120}{\mathrm{HMAX}}\right)$, the total pretime must be at least 50us to accommodate for pixel reset timing but can be set longer. In this case the timing register is only used for pixel reset timing. If Px_PREHEAT or Px_PREMIX is desired the register value should be calculated as described in section 8.12.

8.4.3. RANDNM0

0x5265	7	6	5	4	3	2	1	0
R/W	-	-	**RANDNM0 [21:16]**					

Reset Value 0x00

0x5266	7	6	5	4	3	2	1	0
R/W	**RANDNM0 [15:8]**							

Reset Value 0x1F

0x5267	7	6	5	4	3	2	1	0
R/W	**RANDNM0 [7:0]**							

Reset Value 0x2C

RANDNM0 can be calculated as $\mathrm{HMAX} \cdot \mathrm{PRETIME}\ - \mathrm{RANDNM7}\ - 2098$
(RANDNM7 = 1070 with premix disabled, more information can be found in section 8.12)

8.5. PARAM_HOLD

Each frame consists of multiple configuration parameters, controlled via a *slow* I^2C interface. To avoid frame to frame data corruption when changing more than one parameter (like to modulation frequency or integration time) the user can enable *shadow* registers that temporarily store the updated values and apply all changes at once when the PARAM_HOLD bit is released.

0x0102	7	6	5	4	3	2	1	0
R/W	-	-	-	-	-	-	-	**PARAM_HOLD**

Reset Value 0x00

- 1b0: disable the shadow registers and update all registers at next TRIGGER pulse
- 1b1: enable the shadow registers

It is strongly recommended to use PARAM_HOLD for any register changes during video streaming.

8.6. USER_ID Register

A user programmable register, address 0x0824, will be read out in the first metadata line.
This register, for example, can be used as an identifier for customer defined register maps.
It is the user responsibility to program the USER_ID register, together with other register changes, during a single PARAM_HOLD period and after each phase it can be traced back which settings were used.

0x0824	7	6	5	4	3	2	1	0
R/W	**USER_ID**							

Reset Value 0x00

8.7. Modulation Frequency

The modulation frequency can be set for each frame between 4 and 100 MHz in steps of 1 MHz. Changing this frequency is possible during data streaming by changing the registers listed below. When updating the modulation frequency it's advised to use PARAM_HOLD like explained in section 8.5.

Changing the modulation frequency requires a set of five register values to be updated consecutively.

Register Address			Modulation Frequency [100-75] MHz [50-38] MHz [20-19] MHz	Modulation Frequency [74-51] MHz [37-21] MHz [18-10] MHz	Modulation Frequency [9-5] MHz	Modulation Frequency 4 MHz
0x21BE	R/W	DIVSELPRE	0x00	0x01	0x02	0x03

Register Address			Modulation Frequency [100-51] MHz	Modulation Frequency [50-21] MHz	Modulation Frequency [20-4] MHz
0x21BF	R/W	DIVSEL	0x00	0x01	0x02

0x1048	7	6	5	4	3	2	1	0
R/W	-	-	-	-	-	**FMOD [10:8]**		

Reset Value 0x00

0x1049	7	6	5	4	3	2	1	0
R/W	**FMOD [7:0]**							

Reset Value 0x50

FMOD[10:0] value is calculated as $2^{\mathrm{DIVSELPRE+DIVSEL}} \cdot \mathrm{Modulation\ Frequency}$

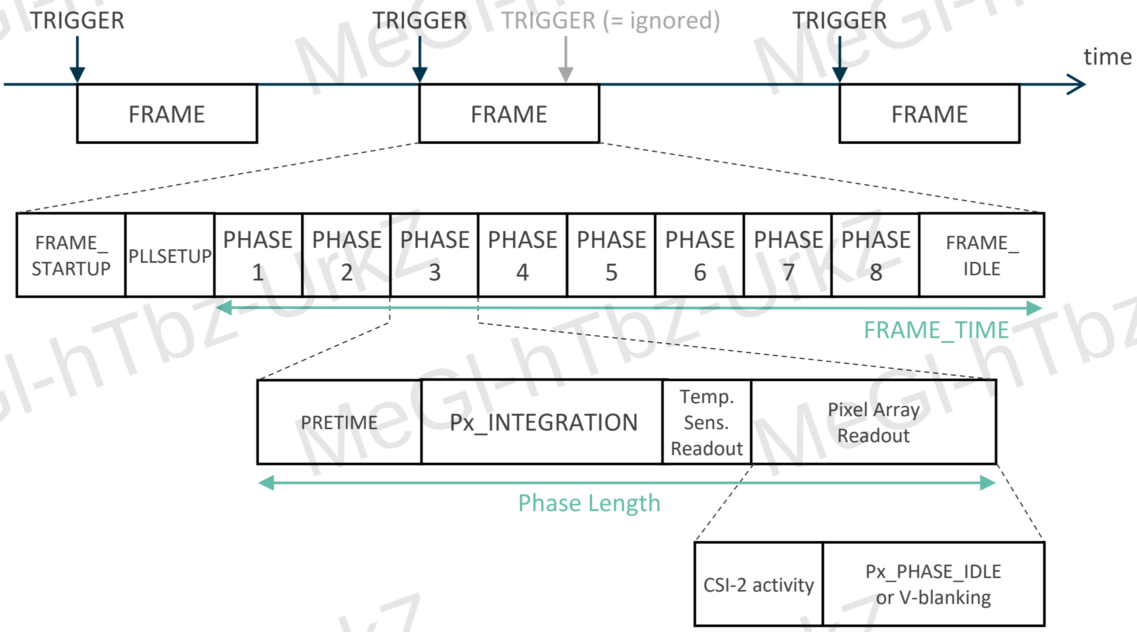
Example FMOD values:

- Modulation Frequency 100 MHz ➢ FMOD = 100 = 0x64
- Modulation Frequency 80 MHz ➢ FMOD = 80 = 0x50
- Modulation Frequency 40 MHz ➢ FMOD = 80 = 0x50
- Modulation Frequency 20 MHz ➢ FMOD = 80 = 0x50

Register Address		$500 \leq \mathrm{FMOD} \cdot 8 < 900$	$900 \leq \mathrm{FMOD} \cdot 8 \leq 1200$
0x104B	R/W	0x02	0x00

8.8. Frame Structure & Frame Rate

To reconstruct a 3D point cloud or a distance image based on indirect Time of Flight technology the sensor usually captures the phase interval for at least four sequential measurements, each called a phase. Each frame (or distance frame) can have up to eight individual phases configured (see section 8.11).



In continuous operating mode the system frame rate can be calculated as $\frac{1\,000\,000}{\text{Frame length (in µs)}}$

- Frame length (in µs) = $\frac{\text{FRAME\_STARTUP} * \text{HMAX}}{120} + \frac{\text{PLLSETUP} * \text{HMAX}}{120} + \text{FRAME\_TIME (in µs)}$ (eq.1)
- FRAME_TIME (in µs) = $\text{PHASE\_COUNT} * \text{Phase length (in µs)}$ (eq.2a)

  or

  FRAME_TIME (in µs) = $\frac{\text{FRAME\_TIME} \cdot \text{HMAX}}{120}$ (only if an optional wait time is defined) (eq.2b)
- Phase length (in µs) =

$$\left(\text{PRETIME} + \frac{\text{Px\_INTEGRATION}}{\text{HMAX}} + 7 + (\text{ROI\_ROW\_END} - \text{ROI\_ROW\_START} + 1) + 1 + 5 + \text{Px\_PHASE\_IDLE}\right) * \frac{\text{HMAX}}{120}$$

(eq.3)

In software or hardware triggered mode the frame rate is controlled by the microcontroller.
Note that in continuous mode the FRAME_TIME register must be set according to section 8.10, either by selecting a timing according to eq. 2a or eq. 2b.

8.9. FRAME_STARTUP

The frame start-up time is the time between a TRIGGER pulse and the start of the first phase acquisition. It can be used to synchronize multiple TOF systems and avoid optical interference.

0x21D4	7	6	5	4	3	2	1	0
R/W	**FRAME_STARTUP [15:8]**							

Reset Value 0x00

0x21D5	7	6	5	4	3	2	1	0
R/W	**FRAME_STARTUP [7:0]**							

Reset Value 0x00

The register value can be calculated as $\frac{\text{start up time (in µs)} \cdot 120}{\text{HMAX}}$

8.10. FRAME_TIME

The minimum length of a frame is dominated by the individual phase configurations. The length of a frame can be increased by programming a FRAME_TIME longer than the minimum time needed to capture all phases. The additional delay will be added after the final phase acquisition.
FRAME_TIME allows fixed distance frame rate operation in continuous operating mode.

Register Address		Register Name	Default Value
0x2108	R/W	FRAME_TIME [31:24]	0x00
0x2109	R/W	FRAME_TIME [23:16]	0x00
0x210A	R/W	FRAME_TIME [15:8]	0x00
0x210B	R/W	FRAME_TIME [7:0]	0x00

Table 26: Frame time

The register value can be calculated as $\frac{\text{Frame Time (in µs)} \cdot 120}{\text{HMAX}}$

8.11. PHASE_COUNT

It is possible to define up to eight raw phases in a single frame for more complex acquisition schemes. The amount of phases inside a frame has to be programmed into PHASE_COUNT.

0x21E8	7	6	5	4	3	2	1	0
R/W	-	-	-	-	**PHASE_COUNT**			

Reset Value 0x04

- 4b0001: Phase 1 enabled
- 4b0010: Phase 1 - 2 enabled
- 4b0011: Phase 1 - 3 enabled
- 4b0100: Phase 1 - 4 enabled
- 4b0101: Phase 1 - 5 enabled
- 4b0110: Phase 1 - 6 enabled
- 4b0111: Phase 1 - 7 enabled
- 4b1000: Phase 1 - 8 enabled

(other values are prohibited)

8.12. Px_PREHEAT, Px_PREMIX

It is important that the illumination signal per phase is constant because any inconsistency across the different raw phases will lead to a distance measurement error. Spikes, visible in the optical illumination signal, due to temperature effects in the first microseconds of an integration period can cause such non constant behaviour. This can be avoided by preheating the illumination signal per phase, known as Px_PREHEAT and it can be enabled or disabled for each of the phases individually.

0x21C0	7	6	5	4	3	2	1	0
R/W	**P7_ PREHEAT**	**P6_ PREHEAT**	**P5_ PREHEAT**	**P4_ PREHEAT**	**P3_ PREHEAT**	**P2_ PREHEAT**	**P1_ PREHEAT**	**P0_ PREHEAT**

Reset Value 0x00

- 1b0: preheat off
- 1b1: preheat on

Although the measurement error is small on application level, similar effects can arise from the pixel/sensor side, for that reason it is also possible to enable a Px_PREMIX time. This is the time the sensor will start integrating before the illumination control signal is enabled. Please note that during this time light will already be accumulated which can lead to faster pixel saturation during integration time. It is advised to keep Px_PREMIX disabled.

0x21C2	7	6	5	4	3	2	1	0
R/W	**P7_ PREMIX**	**P6_ PREMIX**	**P5_ PREMIX**	**P4_ PREMIX**	**P3_ PREMIX**	**P2_ PREMIX**	**P1_ PREMIX**	**P0_ PREMIX**

Reset Value 0x00

- 1b0: premixing off
- 1b1: premixing on

Both PREHEAT and PREMIX use the same internal timing. The register linked incorporates also pixel reset time, thus if no PREHEAT / PREMIX is used the register amounts to the value of the calculations as described in section 8.4.2. To calculate the register value:

- PRETIME = $ROUNDUP(\frac{\text{(PREHEAT or PREMIX(in µs)*120)}}{\text{HMAX}}) + 5$ *(in A&B mode)*
- PRETIME = $ROUNDUP(\frac{\text{(PREHEAT or PREMIX(in µs)*120)}}{\text{HMAX}}) + 9$ *(in any other mode)*

Note : In case Px_PREHEAT is used ($ROUNDUP\,\frac{\text{(PRETIME(in µs)*120)}}{\text{HMAX}}$) + Px_INTEGRATION should not exceed 1ms.
Note: PRETIME should always be larger than 30us, smaller than 1ms.

0x4015	7	6	5	4	3	2	1	0
R/W	-	-	-	**PRETIME[12:8]**				

Reset Value 0x00

0x4016	7	6	5	4	3	2	1	0
R/W	**PRETIME[7:0]**							

Reset Value 0x0A

Note : Both PREHEAT and PREMIX will increase the system power consumption.

When enabling premixing these other register values have to be updated. Important to know is that the following registers cannot be updated during video streaming.

0x5281	7	6	5	4	3	2	1	0
R/W	-	-	RANDNM7 [21:16]					

Reset Value 0x00

0x5282	7	6	5	4	3	2	1	0
R/W	RANDNM7 [15:8]							

Reset Value 0x05

0x5283	7	6	5	4	3	2	1	0
R/W	RANDNM7 [7:0]							

Reset Value 0x55

RANDNM7 can be calculated as: $1070 + \mathrm{HMAX} \cdot \mathrm{ROUNDUP}\left(\frac{\mathrm{PRETIME(in\ \mu s)}-11{,}13}{\mathrm{HMAX}} \cdot 120\right)$

0x5265	7	6	5	4	3	2	1	0
R/W	-	-	RANDNM0 [21:16]					

Reset Value 0x00

0x5266	7	6	5	4	3	2	1	0
R/W	RANDNM0 [15:8]							

Reset Value 0x1F

0x5267	7	6	5	4	3	2	1	0
R/W	RANDNM0 [7:0]							

Reset Value 0x2C

RANDNM0 can be calculated as $\mathrm{HMAX} \cdot \mathrm{PRETIME} - \mathrm{RANDNM7} - 2098$

8.13. Px_INTEGRATION

The integration time is configurable for each phase individually and set by units of HMAX.
When updating the registers it's advised to use PARAM_HOLD like explained in section 8.5.

The next boundary conditions have to be taken into account:

- $\frac{\text{HMAX}}{120}$ µs < integration time < 1ms
- Integration time in steps of $\frac{\text{HMAX}}{120}$ µs
- $\frac{\text{Total IntegrationTime}}{\text{Total Frame Time}} = \frac{\sum_{x=0}^{7} \text{Px\_INTEGRATION} + \text{PRETIME}}{\text{Total FRAME\_TIME}} < 0.4$

The value of registers Px_INTEGRATION can be calculated as $\text{ROUNDUP}\left(\frac{\text{Integration Time (in µs)} \cdot 120}{\text{HMAX}}\right) \cdot \text{HMAX}$

Register Address		Register Name	Default Value
0x2120	R/W	P0_INTEGRATION [31:24]	0x00
0x2121	R/W	P0_INTEGRATION [23:16]	0x01
0x2122	R/W	P0_INTEGRATION [15:8]	0xD4
0x2123	R/W	P0_INTEGRATION [7:0]	0xC0
0x2124	R/W	P1_INTEGRATION [31:24]	0x00
0x2125	R/W	P1_INTEGRATION [23:16]	0x01
0x2126	R/W	P1_INTEGRATION [15:8]	0xD4
0x2127	R/W	P1_INTEGRATION [7:0]	0xC0
0x2128	R/W	P2_INTEGRATION [31:24]	0x00
0x2129	R/W	P2_INTEGRATION [23:16]	0x01
0x212A	R/W	P2_INTEGRATION [15:8]	0xD4
0x212B	R/W	P2_INTEGRATION [7:0]	0xC0
0x212C	R/W	P3_INTEGRATION [31:24]	0x00
0x212D	R/W	P3_INTEGRATION [23:16]	0x01
0x212E	R/W	P3_INTEGRATION [15:8]	0xD4
0x212F	R/W	P3_INTEGRATION [7:0]	0xC0
0x2130	R/W	P4_INTEGRATION [31:24]	0x00
0x2131	R/W	P4_INTEGRATION [23:16]	0x01
0x2132	R/W	P4_INTEGRATION [15:8]	0xD4
0x2133	R/W	P4_INTEGRATION [7:0]	0xC0
0x2134	R/W	P5_INTEGRATION [31:24]	0x00
0x2135	R/W	P5_INTEGRATION [23:16]	0x01
0x2136	R/W	P5_INTEGRATION [15:8]	0xD4
0x2137	R/W	P5_INTEGRATION [7:0]	0xC0
0x2138	R/W	P6_INTEGRATION [31:24]	0x00
0x2139	R/W	P6_INTEGRATION [23:16]	0x01
0x213A	R/W	P6_INTEGRATION [15:8]	0xD4
0x213B	R/W	P6_INTEGRATION [7:0]	0xC0
0x213C	R/W	P7_INTEGRATION [31:24]	0x00
0x213D	R/W	P7_INTEGRATION [23:16]	0x01
0x213E	R/W	P7_INTEGRATION [15:8]	0xD4
0x213F	R/W	P7_INTEGRATION [7:0]	0xC0

Table 27: Integration registers

8.14. Px_PHASE_SHIFT

The phase shift difference between the internal modulation signal (towards the pixels) and the external illumination control signal can be set for each phase independently in steps of 45deg.
This phase shift can be calculated as 360 * Px_PHASE_SHIFT / 8.

0x21B4	7	6	5	4	3	2	1	0
R/W	-	**P1_PHASE_SHIFT**			-	**P0_PHASE_SHIFT**		

Reset Value 0x40

0x21B5	7	6	5	4	3	2	1	0
R/W	-	**P3_PHASE_SHIFT**			-	**P2_PHASE_SHIFT**		

Reset Value 0x62

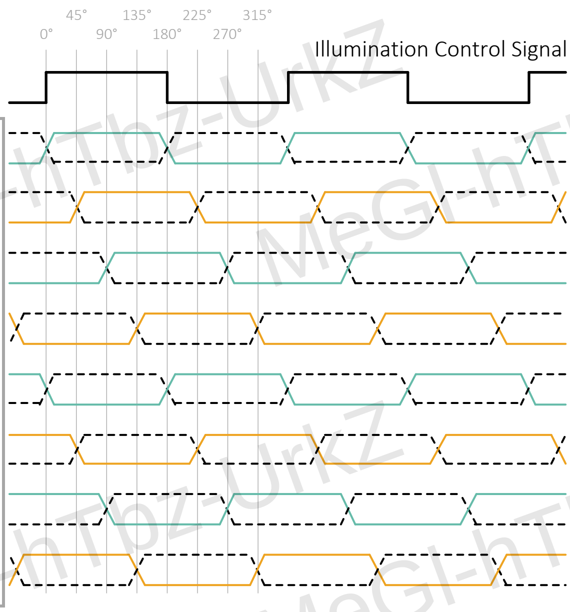
0x21B6	7	6	5	4	3	2	1	0
R/W	-	**P5_PHASE_SHIFT**			-	**P4_PHASE_SHIFT**		

Reset Value 0x00

0x21B7	7	6	5	4	3	2	1	0
R/W	-	**P7_PHASE_SHIFT**			-	**P6_PHASE_SHIFT**		

Reset Value 0x00

Px_PHASE_SHIFT	
3b000	0°
3b001	45°
3b010	90°
3b011	135°
3b100	180°
3b101	225°
3b110	270°
3b111	315°



The internal modulation signal (towards the pixels) is used as reference by default and the illumination signal (LEDP/LEDN) is shifted in phase. This reference signal can be selected.

0x4EA0	7	6	5	4	3	2	1	0
R/W	-	-	-	-	-	-	-	**MODREF**

Reset Value 0x00

- 1b0: illumination signal is used as reference, internal modulation signal is shifted in phase
- 1b1: internal modulation signal is used as reference, illumination signal is shifted in phase

8.15. Px_PHASE_IDLE (or V-blanking)

An artificial idle time (wait time or V-blanking) between 2 subsequent phases can be configured.
This function negatively impacts the system motion robustness (= the ability to measure fast moving objects), but it can be used for compatibility with certain microcontrollers.

Phase idle time (in ms) can be calculated as $\frac{\mathrm{Px\_PHASE\_IDLE} \cdot \mathrm{HMAX}}{120 \cdot 10^3}$

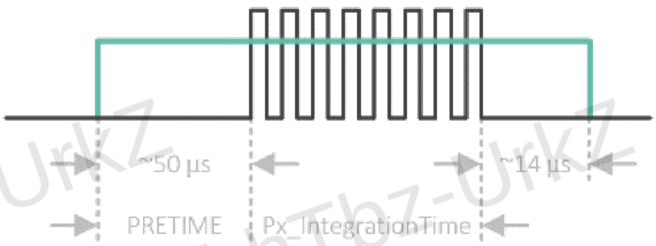
Register Address		Register Name	Default Value
0x21C8	R/W	P0_PHASE_IDLE*	0x05
0x21C9	R/W	P1_PHASE_IDLE*	0x05
0x21CA	R/W	P2_PHASE_IDLE*	0x05
0x21CB	R/W	P3_PHASE_IDLE*	0x05
0x21CC	R/W	P4_PHASE_IDLE*	0x05
0x21CD	R/W	P5_PHASE_IDLE*	0x05
0x21CE	R/W	P6_PHASE_IDLE*	0x05
0x21CF	R/W	P7_PHASE_IDLE*	0x05

Table 28: Phase idle registers

* Values outside [0x05 - 0xFF] are prohibited

8.16. Px_LEDEN

Enable or disable the LEDEN pulse(s). The pulse starts at the beginning of PRETIME and ends ~14µs after the integration time. It can be used as an extra control signal for the illumination (for example enable/disable the PSU) or to disable any significant external noise influencers during the integration time & pixel readout time. It can be enabled or disabled for each of the phases individually. LEDEN length can be extended by increasing the PRETIME setting. The electrical pulse toggles between GND and VDDIF.



0x21C4	7	6	5	4	3	2	1	0
R/W	P7_LEDEN	P6_LEDEN	P5_LEDEN	P4_LEDEN	P3_LEDEN	P2_LEDEN	P1_LEDEN	P0_LEDEN

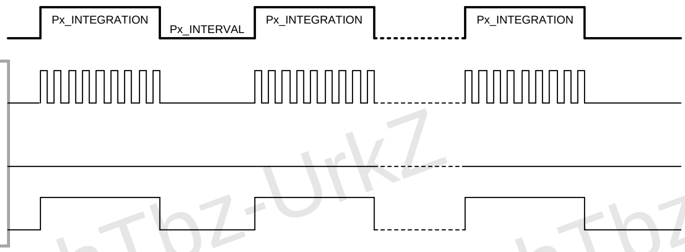
Reset Value 0x00

- 1b0: LEDEN pulse disabled
- 1b1: LEDEN pulse enabled

8.17. Px_DMIX0, Px_DMIX1 & Px_STATIC_LED

The patented Depthsense® pixel design includes 2 internal digital control signals, DMIX0 & DMIX1, that actively forces a guiding field inside the pixel and thus drives, by light photons generated, electrons either to pixel tap A or pixel tap B. In normal operating conditions these signals are modulating during Px_INTEGRATION, but for prototype purposes (or system debugging) it is possible to define their internal behaviour.

Px_DMIXx Px_STATIC_LED	
2b00	modulating
2b10	static low
2b11	static high



0x21A8	7	6	5	4	3	2	1	0
R/W	**P3_DMIX0**		**P2_DMIX0**		**P1_DMIX0**		**P0_DMIX0**	

Reset Value 0x00

0x21A9	7	6	5	4	3	2	1	0
R/W	**P7_DMIX0**		**P6_DMIX0**		**P5_DMIX0**		**P4_DMIX0**	

Reset Value 0x00

0x21AC	7	6	5	4	3	2	1	0
R/W	**P3_DMIX1**		**P2_DMIX1**		**P1_DMIX1**		**P0_DMIX1**	

Reset Value 0x00

0x21AD	7	6	5	4	3	2	1	0
R/W	**P7_DMIX1**		**P6_DMIX1**		**P5_DMIX1**		**P4_DMIX1**	

Reset Value 0x00

The same feature is possible for the illumination control signals LEDP & LEDN.

0x21B0	7	6	5	4	3	2	1	0
R/W	**P3_STATIC_LED**		**P2_STATIC_LED**		**P1_STATIC_LED**		**P0_STATIC_LED**	

Reset Value 0x00

0x21B1	7	6	5	4	3	2	1	0
R/W	**P7_STATIC_LED**		**P6_STATIC_LED**		**P5_STATIC_LED**		**P4_STATIC_LED**	

Reset Value 0x00

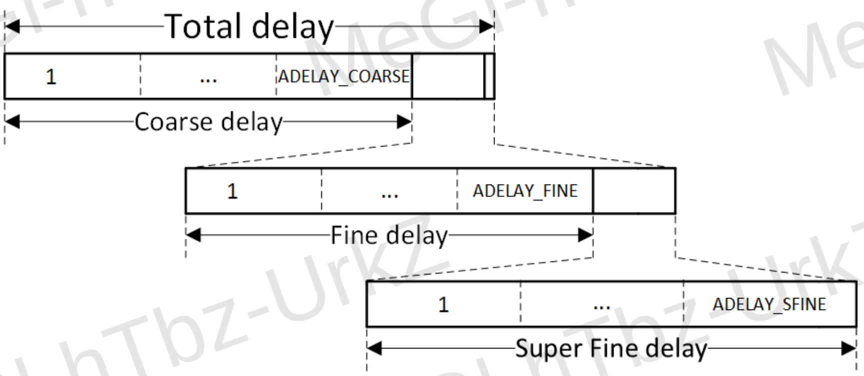
8.18. Analog Delay Setting

MLX75027 features the possibility to adjust the timing between the illumination and internal mixing signals.
This delay is analogue and thus subject to process and temperature variation.

It can be modified according to three different accuracies.

- Coarse delay : modulation frequency dependent
  (f.e. 1.56ns/step @ 40MHz, 1.25ns/step @ 100MHz)
- Fine delay : ~75ps/step
- Super fine delay : ~-20ps/step

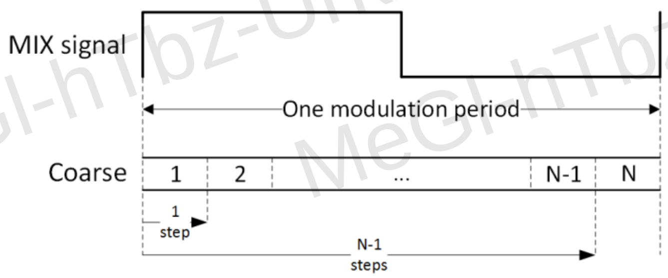
The total delay is the sum of delay generated by each individual setting.
The fine delay cannot exceed the delay of a single coarse step.
The super fine delay cannot exceed a fine delay step (75ps).



To set the registers accordingly determine the total required delay and start by setting the coarse delay register followed by the fine and super fine register.

8.18.1. Coarse Delay

Coarse delay covers up to one modulation period and has the lowest accuracy.



The amount of available steps in one period depends on the modulation frequency:

Modulation Frequency	N
4 to 20 MHz	32
21 to 50 MHz	16
51 to 100 MHz	8

The highest possible amount of delay steps per modulation frequency is N-1.

To calculate the coarse delay register setting:

$$\mathrm{ADELAY\_COARSE} = \mathrm{FLOOR}\left(\frac{TOTAL\ DELAY\ (s)}{\left(\frac{1}{\mathrm{FMOD} * \mathrm{N}}\right)}\right)\ with\ \mathrm{ADELAY\_COARSE}\ \leq \mathrm{N} - 1$$

The coarse setting can be set using the following 8-bit register:

0x201C	7	6	5	4	3	2	1	0
R/W	**ADELAY_COARSE**[1]							

Note [1] : The maximum register value cannot exceed N-1.

The delay generated by the coarse setting is the following:

$$COARSE\ DELAY\ (s) = \frac{\mathrm{ADELAY\_COARSE}}{\mathrm{FMOD} * \mathrm{N}}$$

This will be lower than the total required delay, the remaining delay to add by the fine or super fine setting is:

$$FINE\ DELAY\ TO\ ADD\ (s) = TOTAL\ DELAY\ (s) - COARSE\ DELAY\ (s)$$

8.18.2. Fine Delay

The fine delay step size is around 75ps and should max. cover up to one step of coarse delay. (only possible for modulation frequencies above 5 MHz).

To calculate the fine setting:

$$\mathrm{ADELAY\_FINE} = \mathrm{ROUNDUP}\left(\frac{FINE\ DELAY\ TO\ ADD\ (s)}{75 * 10^{-12}}\right), \qquad \text{with \#ADELAY\_FINE} < 69$$

The fine setting can be set using the following 8-bit register:

0x201D	7	6	5	4	3	2	1	0
R/W	**ADELAY_FINE**[1]							

Note [1]: The maximum register value cannot exceed 68 and the total fine delay cannot be longer than the coarse delay.

The delay generated by the fine setting is the following:

$$FINE\ DELAY\ (s) = \mathrm{ADELAY\_FINE} * 75 * 10^{-12}$$

Fine delay will add a delay that will be higher than needed, the remaining delay to subtract by super fine is:

$$SFINE\ DELAY\ TO\ SUBTRACT\ (s) = FINE\ DELAY\ TO\ ADD(s) - FINE\ DELAY(s)$$

8.18.3. Super Fine

The super fine delay step size is -20ps and can cover up to one step of fine delay.

To calculate the super fine register setting:

$$\text{ADELAY\_SFINE} = \text{FLOOR}\left(\frac{\mathit{SFINE\ DELAY\ TO\ SUBTRACT}\ (s)}{20 * 10^{-12}}\right), \quad \text{with \#ADELAY\_SFINE} < 4$$

The super fine setting can be set using the following 8-bit register:

0x201E	7	6	5	4	3	2	1	0
R/W	**ADELAY_SFINE[1]**							

Note [1]: The maximum register value cannot exceed 3.

The delay generated by the fine setting is the following:

$$\mathit{SFINE\ DELAY}\ (s) = -\text{ADELAY\_SFINE} * 20 * 10^{-12}$$

As with coarse and super fine the delay added by the super fine setting can be lower than required. In some cases, setting a delay higher than required can result in a closer match.
Please keep in mind the super fine delay is a negative delay (reduction).

8.19. Pixel Binning

Pixel binning is a technique to combine individual pixels together to create a set of *superpixels*. In binning mode, each pixel is read-out separately but is recombined digitally with its neighbouring pixels inside the sensor to increase the SNR (signal-to-noise ratio) and to decrease the data processing & bandwidth towards the microcontroller. There's no beneficial effect on the total read-out time (= no impact on motion robustness) as each pixel still has to be read out individually. The noise from the pixels is dominated by the photon shot noise according to a Poisson distribution, with a SNR in binning mode proven to increase with: $\sqrt{< \text{number of binned pixels} >}$.

0x14A5	7	6	5	4	3	2	1	0
R/W	-	-	-	-	-	-	**BINNING_MODE**	

Reset Value 0x00

- 2b00: no binning (= VGA resolution, 640x480 pixels)
- 2b01: 2x2 binning (= QVGA resolution, 320x240 pixels)
- 2b10: 4x4 binning (= QQVGA resolution, 160x120 pixels)
- 2b11: 8x8 binning (= QQQVGA resolution, 80x60 pixels)

When binning is enabled HMAX and HMAX related parameters (PLLSETUP, PRETIME, RANDNM0, PX_INTEGRATION, ...) can be fine-tuned. In case optimised readout is required for high framerate operation please contact tof3d@melexis.com.

8.20. Region of Interest (ROI)

Not all applications require the full VGA (640x480) pixel information. To reduce the total frame readout time, the data processing (or bandwidth) and power consumption it is possible to select only a subset of pixels eligible for readout, also known as a region of interest (ROI). Rows have to be read-out in multiples of 2.

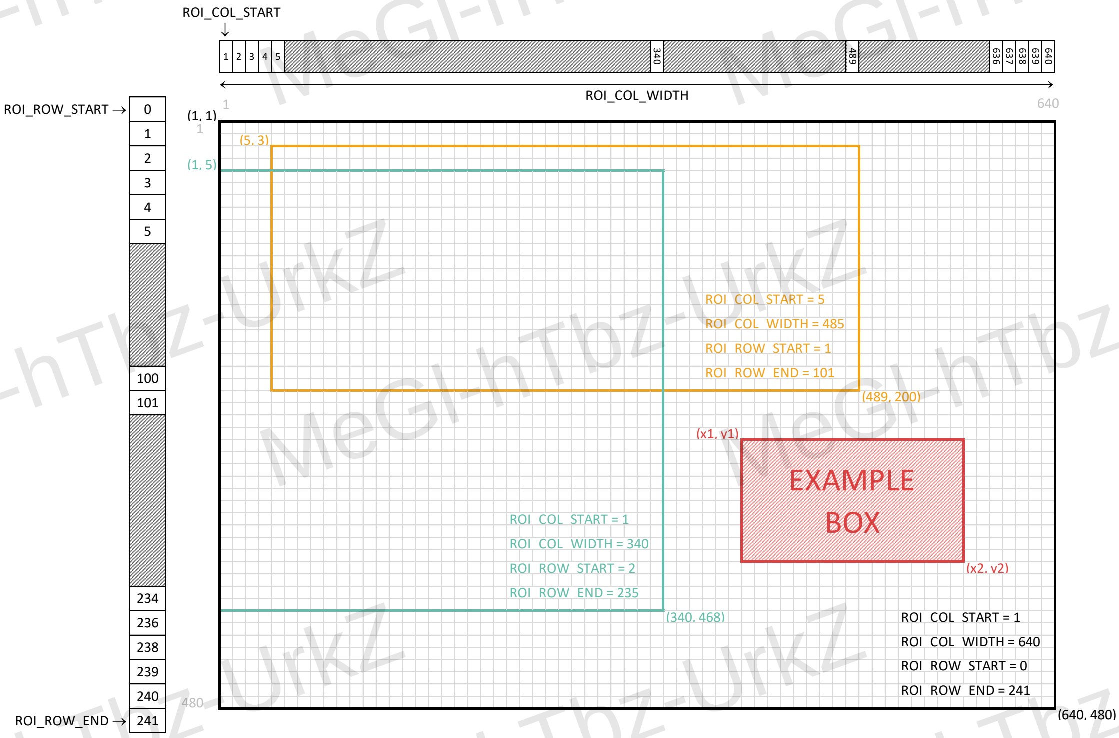


Figure 25: Region of Interest Settings

Note : Changing registers IMG_ORIENTATION_H or IMG_ORIENTATION_V (from section 8.21) also requires the user to reverse the applicable ROI registers for the same region to be readout.

Register Address[1]	Register Name	Calculated Register Value
0x0804 [5:0] 0x0805	ROI_COL_START [13:8] ROI_COL_START [7:0]	x1
0x0806 [1:0] 0x0807	ROI_COL_WIDTH [9:8] ROI_COL_WIDTH [7:0]	x2 - x1 + 1
0x0808 [0] 0x0809	ROI_ROW_START [8] ROI_ROW_START [7:0]	(y1 – 1) / 2
0x080A [0] 0x080B	ROI_ROW_END [8] ROI_ROW_END [7:0]	y2 / 2 + 1

Table 29: Binning registers

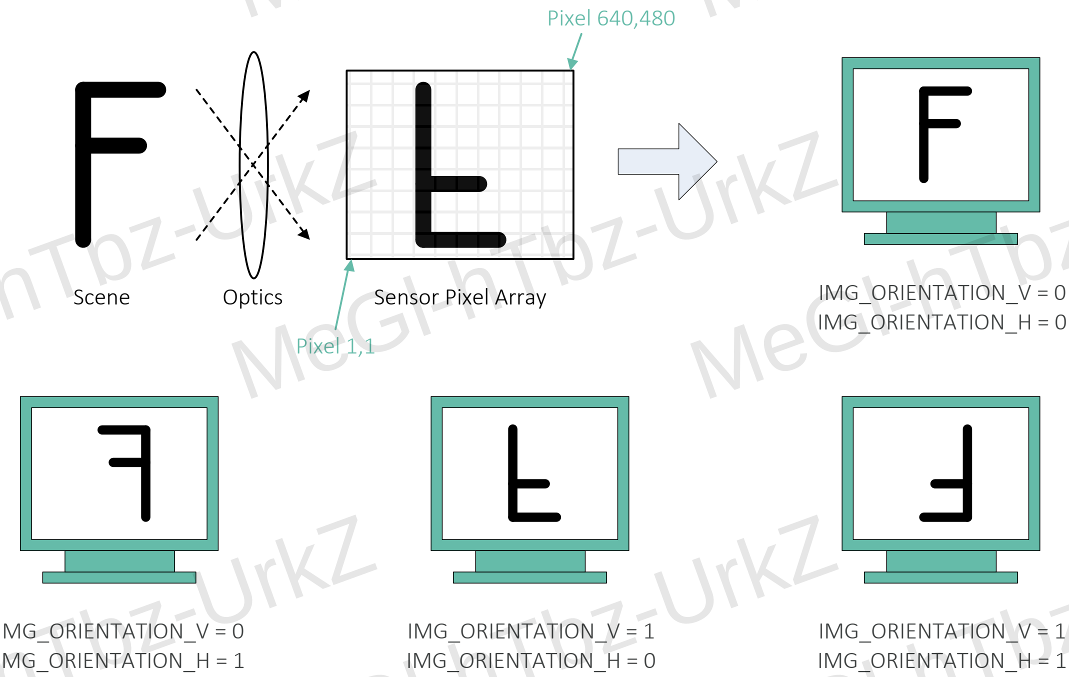
When defining the ROI region there is a list of minimum requirements that have to be taken into account: Y1 should be uneven while Y2 is even. The ROI also depends on the binning used.

Binning	Minimum ROI	Min. Column Increment x1,x2	Min. Row Increment y1,y2
x1	8 x 2	multiple of 4	multiple of 2
x2	16 x 2	multiple of 8	multiple of 2
x4	32 x 4	multiple of 16	multiple of 4
x8	64 x 8	multiple of 32	multiple of 8

8.21. Flip & Mirror

The physical sensor orientation on a PCB does not always match with application requirements or with a visually attractive picture for the user. For that reason, the images can be vertically flipped and/or horizontally mirrored before they are outputted via the video output interface.

The default read out position starting at pixel 1, like visualized in section 4.1, already inverts the image both vertically & horizontally to compensate for the sensor optics/lens behaviour.



0x080C	7	6	5	4	3	2	1	0
R/W	-	-	-	-	-	-	-	**IMG_ORIENTATION_V**

Reset Value 0x00

0x080D	7	6	5	4	3	2	1	0
R/W	-	-	-	-	-	-	-	**IMG_ORIENTATION_H**

Reset Value 0x00

8.22. Temperature Sensor

The internal junction temperature sensor information is available as a register value (or can be found inside the MetaData). The temperature is read right after the integration time and just before the frame readout period like shown in 8.8. It is only valid after a first phase acquisition with an absolute accuracy of ±7 °C @ -40°C, ±5 °C @ 60°C, ±6°C @ 125°C. The temperature sensor's information can be used for system temperature calibration due to its high linearity.

0x1403	7	6	5	4	3	2	1	0
R/W	**TEMP_VALUE**							

Reset Value 0x00

Temperature [in °C] = TEMP_VALUE - 40

8.23. Pixel & Phase Statistics

MLX75027 monitors each raw tap A and tap B value separately. Statistics are gathered when either of the two taps exceeds their minimum or maximum threshold. Feedback is provided as a single bit error flag or generic pixel error code via the metadata (or via I^2C). This data can be used as indicator to warn for pixel saturation or extreme low light conditions. The total amount of erroneous taps violating their thresholds can be found in Px_ERRCOUNTLOW or Px_ERRCOUNTHIGH registers for each phase.

0x1433[1]	7	6	5	4	3	2	1	0
R/W	-	-	-	-	-	-	-	STATS_EN

Reset Value 0x01

- 1b0: statistics disabled
- 1b1: statistics enabled

Note[1] : 0x1433 is set to zero in the 7.2 Initialisation Register Map

0x14BB	7	6	5	4	3	2	1	0
R/W	-	-	-	-	-	-	-	STATS_MODE

Reset Value 0x00

- 1b0: pixel error flag enabled

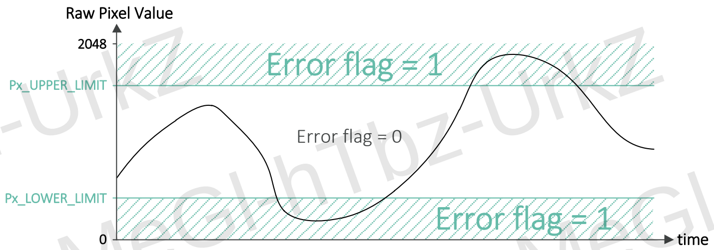


Figure 26: Pixel error flag

- 1b1: pixel error code enabled

The pixel error code is only available for output mode A-B and A+B as shown in Table 30.
Please note the pixel error flag replaces the pixel MSB.

Data Output Mode	STATS_EN = 0	STATS_EN = 1	
		STATS_MODE = 0 (Error flag enabled)	STATS_MODE = 1 (Error code enabled)
A-B	[11:0] = pixel data (signed)	[11] = error flag [10:0] = pixel data (signed)	[11:0] = pixel data (signed) or 0x800 (= error code)
A+B	[11:0] = pixel data (unsigned)	[11] = error flag [10:0] = pixel data	[11:0] = pixel data (unsigned) or 0xFFF (= error code)
A B A&B	[11] = 0 [10:0] = pixel data	[11] = error flag [10:0] = pixel data	[11] = 0 [10:0] = pixel data

Table 30: Register Table for Error Info

The minimum threshold for each tap is defined in Px_LOWER_LIMIT.

Register Address		Register Name	Default Value
0x1434	R/W	P0_LOWER_LIMIT [10:8]	0x00
0x1435	R/W	P0_LOWER_LIMIT [7:0]	0x00
0x1436	R/W	P1_LOWER_LIMIT [10:8]	0x00
0x1437	R/W	P1_LOWER_LIMIT [7:0]	0x00
0x1438	R/W	P2_LOWER_LIMIT [10:8]	0x00
0x1439	R/W	P2_LOWER_LIMIT [7:0]	0x00
0x143A	R/W	P3_LOWER_LIMIT [10:8]	0x00
0x143B	R/W	P3_LOWER_LIMIT [7:0]	0x00
0x143C	R/W	P4_LOWER_LIMIT [10:8]	0x00
0x143D	R/W	P4_LOWER_LIMIT [7:0]	0x00
0x143E	R/W	P5_LOWER_LIMIT [10:8]	0x00
0x143F	R/W	P5_LOWER_LIMIT [7:0]	0x00
0x1440	R/W	P6_LOWER_LIMIT [10:8]	0x00
0x1441	R/W	P6_LOWER_LIMIT [7:0]	0x00
0x1442	R/W	P7_LOWER_LIMIT [10:8]	0x00
0x1443	R/W	P7_LOWER_LIMIT [7:0]	0x00

Table 31: Px_LOWER_LIMIT

The maximum threshold for each tap is defined in Px_UPPER_LIMIT.

Register Address		Register Name	Default Value
0x1448	R/W	P0_UPPER_LIMIT [10:8]	0x00
0x1449	R/W	P0_UPPER_LIMIT [7:0]	0x00
0x144A	R/W	P1_UPPER_LIMIT [10:8]	0x00
0x144B	R/W	P1_UPPER_LIMIT [7:0]	0x00
0x144C	R/W	P2_UPPER_LIMIT [10:8]	0x00
0x144D	R/W	P2_UPPER_LIMIT [7:0]	0x00
0x144E	R/W	P3_UPPER_LIMIT [10:8]	0x00
0x144F	R/W	P3_UPPER_LIMIT [7:0]	0x00
0x1450	R/W	P4_UPPER_LIMIT [10:8]	0x00
0x1451	R/W	P4_UPPER_LIMIT [7:0]	0x00
0x1452	R/W	P5_UPPER_LIMIT [10:8]	0x00
0x1453	R/W	P5_UPPER_LIMIT [7:0]	0x00
0x1454	R/W	P6_UPPER_LIMIT [10:8]	0x00
0x1455	R/W	P6_UPPER_LIMIT [7:0]	0x00
0x1456	R/W	P7_UPPER_LIMIT [10:8]	0x00
0x1457	R/W	P7_UPPER_LIMIT [7:0]	0x00

Table 32: Px_UPPER_LIMIT

The total amount of pixels that violate their limit can be read in separate registers:

Register Address		Register Name	Default Value
0x145D [3:0]	R/W	P0_ERRCOUNTLOW [19:16]	0x00
0x145E	R/W	P0_ERRCOUNTLOW [15:8]	0x00
0x145F	R/W	P0_ERRCOUNTLOW [7:0]	0x00
0x1461 [3:0]	R/W	P1_ERRCOUNTLOW [19:16]	0x00
0x1462	R/W	P1_ERRCOUNTLOW [15:8]	0x00
0x1463	R/W	P1_ERRCOUNTLOW [7:0]	0x00
0x1465 [3:0]	R/W	P2_ERRCOUNTLOW [19:16]	0x00
0x1466	R/W	P2_ERRCOUNTLOW [15:8]	0x00
0x1467	R/W	P2_ERRCOUNTLOW [7:0]	0x00
0x1469 [3:0]	R/W	P3_ERRCOUNTLOW [19:16]	0x00
0x146A	R/W	P3_ERRCOUNTLOW [15:8]	0x00
0x146B	R/W	P3_ERRCOUNTLOW [7:0]	0x00
0x146D [3:0]	R/W	P4_ERRCOUNTLOW [19:16]	0x00
0x146E	R/W	P4_ERRCOUNTLOW [15:8]	0x00
0x146F	R/W	P4_ERRCOUNTLOW [7:0]	0x00
0x1471 [3:0]	R/W	P5_ERRCOUNTLOW [19:16]	0x00
0x1472	R/W	P5_ERRCOUNTLOW [15:8]	0x00
0x1473	R/W	P5_ERRCOUNTLOW [7:0]	0x00
0x1475 [3:0]	R/W	P6_ERRCOUNTLOW [19:16]	0x00
0x1476	R/W	P6_ERRCOUNTLOW [15:8]	0x00
0x1477	R/W	P6_ERRCOUNTLOW [7:0]	0x00
0x1479 [3:0]	R/W	P7_ERRCOUNTLOW [19:16]	0x00
0x147A	R/W	P7_ERRCOUNTLOW [15:8]	0x00
0x147B	R/W	P7_ERRCOUNTLOW [7:0]	0x00

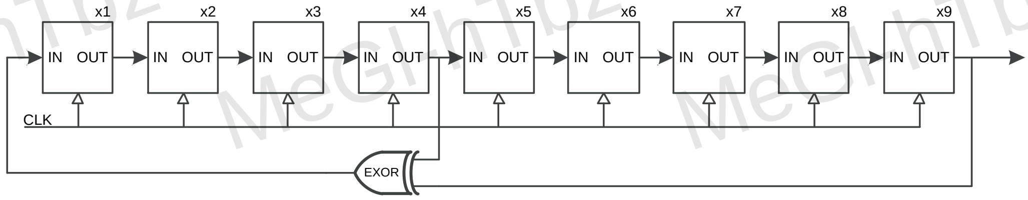
Table 33: Total Pixel count Px_LOWER_LIMIT

Register Address		Register Name	Default Value
0x1481 [3:0]	R/W	P0_ERRCOUNTHIGH [19:16]	0x00
0x1482	R/W	P0_ERRCOUNTHIGH [15:8]	0x00
0x1483	R/W	P0_ERRCOUNTHIGH [7:0]	0x00
0x1485 [3:0]	R/W	P1_ERRCOUNTHIGH [19:16]	0x00
0x1486	R/W	P1_ERRCOUNTHIGH [15:8]	0x00
0x1487	R/W	P1_ERRCOUNTHIGH [7:0]	0x00
0x1489 [3:0]	R/W	P2_ERRCOUNTHIGH [19:16]	0x00
0x148A	R/W	P2_ERRCOUNTHIGH [15:8]	0x00
0x148B	R/W	P2_ERRCOUNTHIGH [7:0]	0x00
0x148D [3:0]	R/W	P3_ERRCOUNTHIGH [19:16]	0x00
0x148E	R/W	P3_ERRCOUNTHIGH [15:8]	0x00
0x148F	R/W	P3_ERRCOUNTHIGH [7:0]	0x00
0x1491 [3:0]	R/W	P4_ERRCOUNTHIGH [19:16]	0x00
0x1492	R/W	P4_ERRCOUNTHIGH [15:8]	0x00
0x1493	R/W	P4_ERRCOUNTHIGH [7:0]	0x00
0x1495 [3:0]	R/W	P5_ERRCOUNTHIGH [19:16]	0x00
0x1496	R/W	P5_ERRCOUNTHIGH [15:8]	0x00
0x1497	R/W	P5_ERRCOUNTHIGH [7:0]	0x00
0x1499 [3:0]	R/W	P6_ERRCOUNTHIGH [19:16]	0x00
0x149A	R/W	P6_ERRCOUNTHIGH [15:8]	0x00
0x149B	R/W	P6_ERRCOUNTHIGH [7:0]	0x00
0x149D [3:0]	R/W	P7_ERRCOUNTHIGH [19:16]	0x00
0x149E	R/W	P7_ERRCOUNTHIGH [15:8]	0x00
0x149F	R/W	P7_ERRCOUNTHIGH [7:0]	0x00

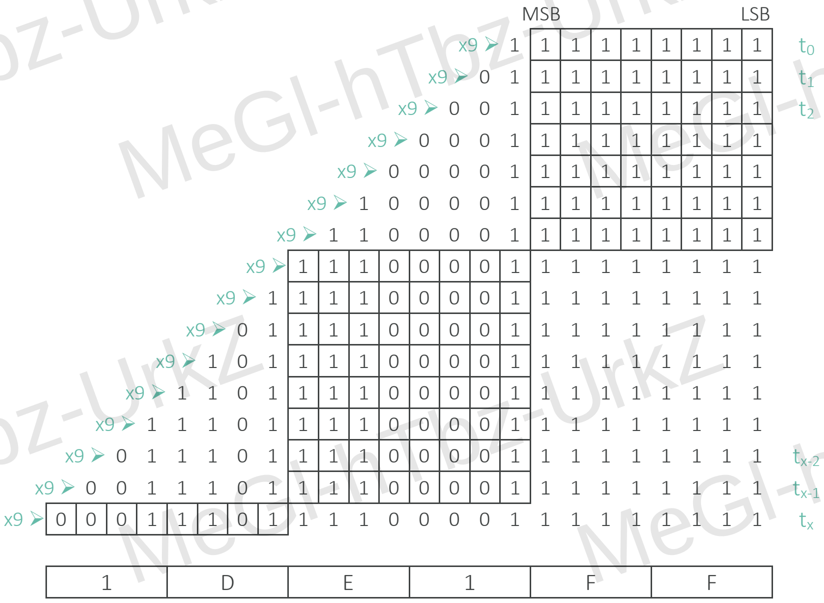
Table 34: Total Pixel count Px_UPPER_LIMIT

8.24. PN9 Test Pattern

MLX75027 has a built-in test pattern to verify the MIPI connectivity. This can be used for debugging purposes, but also as live diagnostic. The pattern is a pseudorandom code generated using a nine stage shift register.



At t_0 each shift register is pre-loaded with one. At every clock pulse the register shifts and the first stage input is replaced with the exclusive disjunction (EXOR operation) from bit 4 and 9. The output stream of register no.9 is recombined into an 8bit word. This sequence generates 512 unique values and will repeat itself.



Recombining this example bitstream into a single MIPI package, like explained in section 6.2.2, becomes 0xFFE11D, which translates into the first two pixels values 0xFFD (4093) and 0xE11 (3601). The bitstream of the next 2 pixels gives 0x85ED9A, which corresponds to a MIPI package of 0x9AED85, representing two pixel values 0x9A5 (2469) and 0xED8 (3800), ….

The test pattern is independent of the pixel values and output mode but is visually different for mode A&B.

To enable the test pattern, please follow this register sequence:

- Register 0x1405 > value 0x00
- Register 0x1406 > value 0x04
- Register 0x1407 > value 0x01

To disable the test pattern:

- Register 0x1407 > value 0x00

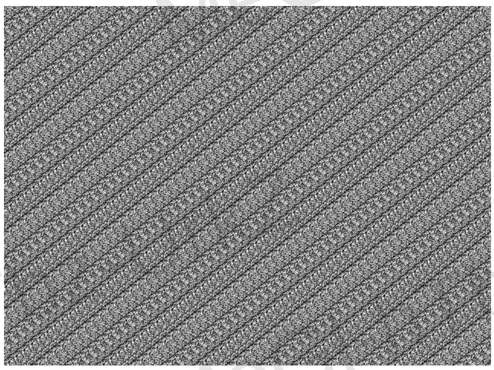


Figure 27: Visual representation of PN9 Test Pattern

8.25. Duty Cycle Adjustment

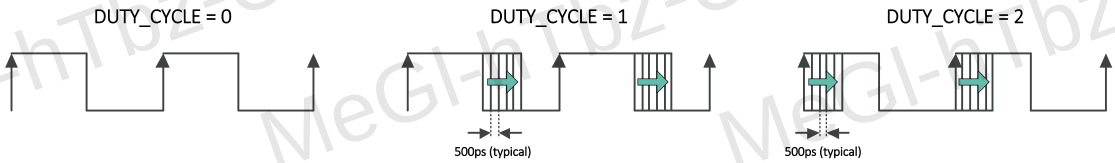
It is possible to adjust the duty cycle of the illumination signals (LEDP, LEDN). The default duty cycle is 50%, but it can be optimized to compensate certain driver effects. The adjustment is controlled by analogue circuitry in 16 delay steps (on the rising or falling edge of the light pulses). Each step is typically 500ps, but the absolute delay time is affected by process & temperature variation.

0x4E9E	7	6	5	4	3	2	1	0
R/W	-	-	-	-	-	DUTY_CYCLE		

Reset Value 0x00

- 2b00: no duty cycle correction (= disabled)
- 2b01: time delay on the falling edge (= increased duty cycle)
- 2b10: time delay on the rising edge (= decreased duty cycle)

(other values are prohibited)



0x21B9	7	6	5	4	3	2	1	0
R/W	-	-	-	-	DUTY_CYCLE_VALUE			

Reset Value 0x00

The total delay (of the rising and falling edge) = DUTY_CYCLE_VALUE · 500 ps (typical value)

Since the step size has an absolute value the duty cycle limits are affected by the modulation frequency. It's the user responsibility to stay within min. & max. limits to avoid illumination hardware failure.

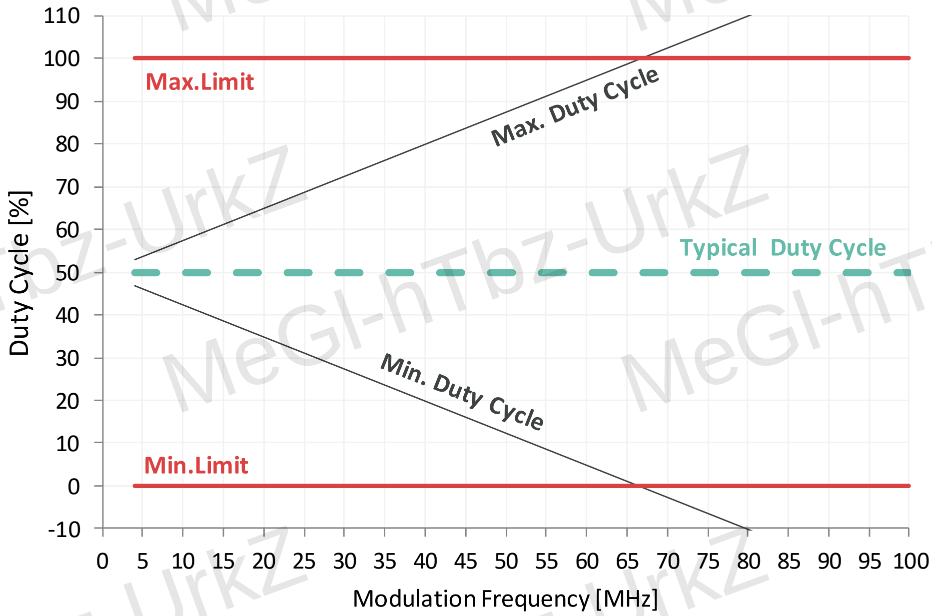


Figure 28: Modulation frequency versus allowed duty cycle

This graph for example shows that the duty cycle at 40 MHz can be changed between 20 & 80 %.

8.26. Illumination Signal (subLVDS or CMOS)

The illumination signal is available as differential signal (subLVDS) or as single ended pulses (CMOS). It is suggested to apply changes to this hardware configuration during the *Software Standby* mode.

0x10E2	7	6	5	4	3	2	1	0
R/W	-	-	-	-	-	-	-	LVDS_EN

Reset Value 0x01

- 1b0: CMOS mode (LEDP = LEDN)
- 1b1: subLVDS mode (LEDP positive, LEDN negative)

Important Note : We recommend to use subLVDS mode for an improved sunlight performance. For more detailed information, please contact us directly.

8.27. Device Identifiers

8.27.1. DeviceType

The sensor has a dedicated register indicating this sensor type. This register can be used to identify the connected device.

0x0308	7	6	5	4	3	2	1	0
R/W	DeviceType					-	-	-

DeviceType[7:3]:

- 27: MLX75027
- 26: MLX75026

Note : DeviceType is only programmed on samples produced as of June 2020 onwards.

8.27.2. SensorID

Each sensor has a unique identifier, SensorID.
SensorID[55:0] is composed based on the register set found in Table 35.

Register Address		Register Name
0x0000	R	SensorID[55:48]
0x0001	R	SensorID[47:40]
0x0002	R	SensorID[39:32]
0x0003	R	SensorID[31:24]
0x0016	R	SensorID[23:16]
0x0017	R	SensorID[15:8]
0x0018	R	SensorID[7:0]

Table 35: SensorID

9. MetaData Description

MetaData or embedded data (MIPI data type 0x12, EBD8) is available on two lines after the normal pixel data. These lines can be enabled via EN_META in register 0x3C18. Each line features 132 unique values.

0x3C18 R/W	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	EN_META	

Reset Value 0x02

- 2b00: no metadata lines enabled
- 2b01: first metadata line (line #1) enabled
- 2b10: first & second metadata lines (line #1 and line #2) enabled

(other values are prohibited)

The length of the MetaData lines can be controlled via META_LENGTH in register 0x2C0C and 0x2C0D. Increasing the length beyond 132 will pad the data with dummy pixels.

0x2C0C R/W	7	6	5	4	3	2	1	0
	META_LENGTH[10:3]							

0x2C0D R/W	7	6	5	4	3	2	1	0
	META_LENGTH[2:0]			-	-	-	-	-

The value of META_LENGTH represents the numbers of pixels output over MIPI (represented as 12-bit pixels).

Using for example 320 pixels MetaData:

- 0x2C0C : 0x28
- 0x2C0D : 0x00

Would equal to 320x12bit = 3840bit = 480 byte.

Line	Pixel	Description
#1	E000	0x0A (= fixed value)
#1	E042	IMG_ORIENTATION_V
#1	E044	IMG_ORIENTATION_H
#1	E058	USER_ID
#1	E062	OUTPUT_MODE
#1	E068	DATA_LANE_CONFIG
#1	E078	[11:4] TEMP_VALUE [3] 1b0 (= fixed value) [2] 1b1 (= fixed value) [1] 1b0 (= fixed value) [0] 1b1 (= fixed value)
#1	E082	BINNING_MODE
#1	E096	DIVSEL
#1	E098	DIVSELPRE
#1	E127	End of Data 0x07
#1	E128	End of Data 0x07
#1	E129	End of Data 0x07
#1	E130	End of Data 0x07
#1	E131	End of Data 0x07

Line	Pixel	Description
#2	E050	ERRCOUNTLOW [19:16]
#2	E052	ERRCOUNTLOW [15:8]
#2	E054	ERRCOUNTLOW [7:0]
#2	E058	ERRCOUNTHIGH [19:16]
#2	E060	ERRCOUNTHIGH [15:8]
#2	E062	ERRCOUNTHIGH [7:0]
#2	E090	FRAME_COUNT (= frame counter)
#2	E096	PHASE_COUNT (= number of phase inside a frame)
#2	E127	End of Data 0x07
#2	E128	End of Data 0x07
#2	E129	End of Data 0x07
#2	E130	End of Data 0x07
#2	E131	End of Data 0x07

Embedded data output example (assuming single data lane configuration):

PH	E000	E001	0x55	E002	E003	0x55	E004	E005	0x55	E006	…	E125	0x55	E126	E127	0x55	E128	E129	0x55	E130	E131	0x55	PF

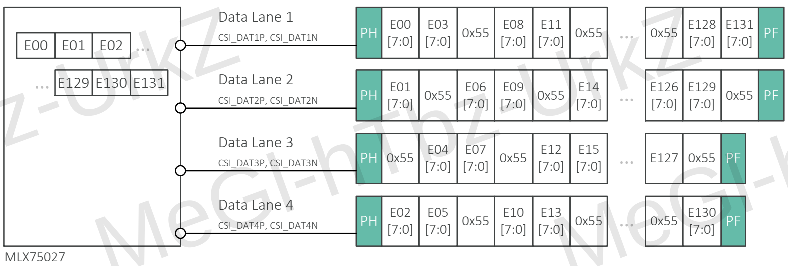
The data in each line is composed of a tag, data & dummy byte.
Each uneven pixel (E001, E003, E005, …) is an embedded data line *tag*.

PH	0x0A	*Tag*	0x55	Data	*Tag*	0x55	Data	*Tag*	0x55	Data	…	*Tag*	0x55	Data	*Tag*	0x55	Data	*Tag*	0x55	Data	*Tag*	0x55	PF

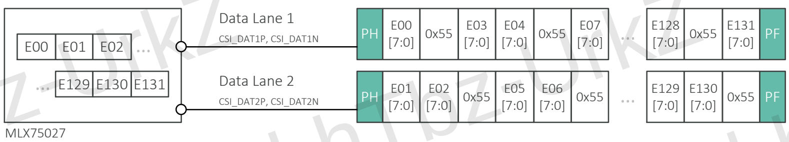
Tag values are listed below:

Tag	Data Byte Description
0x00	Illegal tag, if found treat as End of Data
0x07	End of Data
0xAA	CCI register Index MSB [15:8]
0xA5	CCI register Index LSB [7:0]
0x5A	Auto increment the CCI index after the data byte – valid data (Data byte contains valid CC register data)
0x55	Auto increment the CCI index after the data byte – null data. (A CCI register does NOT exist for the current CCI index, the data byte value is 0x07)
0xFF	Illegal tag, if found treat as End of Data

9.1. Embedded Data Format in 4 Lane MIPI Configuration



9.2. Embedded Data Format in 2 Lane MIPI Configuration



10. Distance & Amplitude Calculation

The distance data per pixel [in mm] can be calculated with the following formulas:

```
p0 = TwoComp_MKO(phase0);
p180 = TwoComp_MKO(phase180);
p90 = TwoComp_MKO(phase90);
p270 = TwoComp_MKO(phase270);

I = p0 - p180;
Q = p270 - p90; %When 0x4EA0 = 0x01

ampData = sqrt(I.^2 + Q.^2);
Phase = atan2(Q, I);

unAmbiguousRange = 0.5*299792458/(ModF*1000);
coef_rad = unAmbiguousRange / (2*pi);
distData = (Phase+pi) * coef_rad;
```

Figure 29: Example Matlab code of the raw to distance data calculation

- *phase0, phase180, phase90, phase270* are the raw A-B frames from the sensor at each phase interval
- *TwoComp_MKO* is a local function that converts the unsigned data from Mode A-B for each of the raw phases into signed values
- Calculation of Q depends on the setting of register 0x4EA0 from section 8.14
- *ModF* is the modulation frequency in MHz.
- *unAmbiguousRange* is the maximum range in mm determined by the system modulation frequency (at modulation frequency of 20MHz this would be ~7.49m, at 100MHz it will be ~1.49m)
- *coef_rad* is a conversion coefficient from radians to degree

11. Diagnostics

This section provides instructions on how to use the BIST features of the sensor. BIST, build in self test, can be used to verify correct internal operation of the sensor. There are two ways to access BIST information: using I2C registers or directly at runtime from MetaData. Melexis recommends using MetaData as it allows real-time access of the data without I2C overhead and is always synchronised to the relevant phase data.

Diagnostics are divided into three categories based on timing:

- At sensor standby
- Once after enabling video streaming
- Executed during video streaming
    - End of each phase
    - During streaming

Table 36 lists all available BISTs from the device.

Timing	BIST	Description
Sensor standby	Logic SRAM	Digital Built-in self-test. Compares an code from a scan-chain with the expected value.
After enabling streaming	Column logic	Used to test the readout logic of the ADC.
End of each phase	Column analog	Checks the correct counting and range of the column ADCs.
During streaming[1]	PLL MIX FMOD SRAM ECC	Checks the frequency generated by PLLs. Validates the selected FMOD frequency. Indicates an error was detected and corrected in the SRAM.

Table 36: BIST

Note [1]: All streaming BISTS require hardware triggered mode

11.1. Logic & SRAM BIST

Only runs at start-up.
Digital Built-in self-test. Compares an output code from a scan-chain with the expected value.

Register	Pixel	Name	Description
0x3062[3:0]		DV_CLKDIVSEL_CORE	Bits[3:0]: Set to 5 before enabling LBIST_EN
0x1090[0]		LBIST_EN	Bit[0]: Set to 1 to start LOGIC + SRAM BIST
0x1091[1:0]	E006	LBIST_RESULT	bit[0]: SRAM BIST Result: 0 OK, 1 NG bit[1]: LOGIC BIST Result: 0 OK, 1 NG
0x1083[0]		RAMERR_CLR	Bit[0]: Set to 1 to clear BIST flag

Table 37: Logic & SRAM BIST

In order to use Logic and SRAM BIST please follow the procedure below:

- Make sure the sensor is in sensor standby
- Set RAMERR_CLR to 1
- Set DV_CLKDIVSEL_CORE to 5
- Set LBIST_EN to 1 to start LOGIC and SRAM BIST
- Wait a minimum of 30ms
- Read out LBIST_RESULT using I2C or MetaData

During execution of the Logic & SRAM BIST the digital of the sensor will be in test mode preventing I2C communication. It is advised to hold the application program a minimum of 30ms before starting I2C communication like reading the BIST status. Please keep in mind that the logic BIST calls an auto-reset of the sensor after completion. In case you have any settings programmed register content will be lost and re-initialization will be needed.

11.2. Column Logic BIST

Executed once after enabling streaming.
Column Logic BIST is used to test the readout logic of the ADC.

Register	Pixel	Name	Description
0x14AD[0]	E024	READBIST_FAIL	bit[0]: Result: 0 OK, 1 NG

Table 38: Column Logic BIST

In order to use Column Logic BIST please follow the procedure below:

- Enable streaming
- Generate a hardware trigger (TRIGGERB)
- Wait at least 10ms
- Readout READBIST_FAIL once using I2C or MetaData

Column logic can only be readout once after enabling streaming and it is recommended to store the value. The next readout can lead to a BIST fail result which is expected behaviour.

11.3. Column Analog BIST

At the end of each phase.
Built-in self-test which checks the correct counting and range of the column ADCs.

Register	Pixel	Name	Description
0x14AE[0]	E026	ANALOG_FAIL_HOLD	Bit[0]: Result: 0 OK, 1 NG
0x14AB[0]		ANALOG_FAIL_CLR	Bit[0]: Set to 1 to clear ANALOG_FAIL_HOLD
0x3C30[7:0]		ANALOG_SETTING1	Bits[7:0]: Set to 0x06, min. 2.8ms after streaming
0x3C31[7:0]		ANALOG_SETTING2	Bits[7:0]: Set to 0x08, min. 2.8ms after streaming
0x3C32[7:0]		ANALOG_SETTING3	Bits[7:0]: Set to 0x06, min. 2.8ms after streaming
0x3C33[7:0]		ANALOG_SETTING4	Bits[7:0]: Set to 0x09, min. 2.8ms after streaming
0x3C34[7:0]		ANALOG_SETTING5	Bits[7:0]: Set to 0x06, min. 2.8ms after streaming
0x3C35[7:0]		ANALOG_SETTING6	Bits[7:0]: Set to 0x0A, min. 2.8ms after streaming
0x4C7A[7:0] 0x4C7B[7:0]		RAMP[15:8] RAMP[7:0]	0x4C7A[7:0]: Set to 0x01 0x4C7B[7:0]: Set to 0x35

Table 39: Column Analog BIST

In order to use Column Analog BIST please follow the procedure below:

- Enable streaming
- Set ANALOG_SETTING and RAMP registers
- Set ANALOG_FAIL_CLR to 1
- Wait for end of one acquisition
- Readout ANALOG_FAIL_HOLD using I2C or MetaData

11.4. PLL BIST

During streaming.
Built-in self-test which checks the frequency generated by PLLs.

Register	Pixel	Name	Description
0x1500[0]	E034	PLL_BIST_CORE	PLL #1 bist (frequency) result Bit[0]: Result: 0 OK, 1 NG Cleared by PLL_BISTCLR_CORE
0x1501[0]	E036	PLL_BIST_OUT	PLL #2 bist (frequency) result Bit[0]: Result: 0 OK, 1 NG Cleared by PLL_BISTCLR_OUT
0x1503[0]	E040	PLL_LOCK_CORE	PLL #1 bist (lock-detect) result Bit[0]: Result: 0 OK, 1 NG Cleared by PLL_BISTCLR_CORE
0x1504[0]	E042	PLL_LOCK_OUT	PLL #2 bist (lock-detect) result Bit[0]: Result: 0 OK, 1 NG Cleared by PLL_BISTCLR_OUT
0x10A0[0]		PLL_BISTCLR_CORE	PLL #1 bist (frequency) error clear Bit[0]: 1 = clear
0x10A1[0]		PLL_BISTCLR_OUT	PLL #2 bist (frequency) error clear Bit[0]: 1 = clear

Table 40: PLL BIST

In order to use PLL BIST please follow the procedure below:

- Enable streaming
- Set the following registers:

Communication Speed (Mbps)	Registers			
	0x10C2	0x10C3	0x10C4	0x10C5
300	0x001C	0x001C	0x013A	0x013A
600	0x000F	0x000F	0x009D	0x009D
704	0x000D	0x000D	0x0086	0x0086
800	0x000B	0x000B	0x0075	0x0075
904	0x000A	0x000A	0x0068	0x0068
960	0x000A	0x000A	0x0062	0x0062

Table 41: PLL Register Settings

- Set PLL_BISTCLR_CORE and PLL_BISTCLR_OUT to 1
- Readout PLL_BIST_CORE, PLL_BIST_OUT, PLL_LOCK_CORE, PLL_LOCK_OUT using I2c or MetaData

11.5. MIX FMOD BIST

At the start of each phase during streaming.
Built-in self-test validating the selected FMOD frequency.

Register	Pixel	Name	Description
0x1502[0]	E038	PLL_BIST_FMOD	PLL #3 MIX FMOD BIST (frequency) result Bit[0]: Result: 0 OK, 1 NG
0x1505[0]	E044	PLL_LOCK_FMOD	PLL #3 MIX FMOD BIST (lock) result Bit[0]: Result: 0 OK, 1 NG
0x10A2[0]		PLL_BISTCLR_FMOD	PLL #3 BIST (frequency) error clear Bit[0]: 1 = clear
0x10D0[3:0]		TPLLTESTDIV_FMOD	See example code for values
0x10D2[1:0] 0x10D3[7:0]		TPLLTESTOFFSET_FMOD[9:8] TPLLTESTOFFSET_FMOD[7:0]	0x10D2[1:0]: Set to 0x00 0x10D3[7:0]: Set to 0x10
0x10D4[7:0] 0x10D5[7:0]		TPLLTESTLO_FMOD[15:8] TPLLTESTLO_FMOD[7:0]	See example code for values

Table 42: MIX FMOD BIST

In order to use MIX FMOD BIST please follow the procedure below:

- Use the following code snippet to determine TPLLTESTDIV_FMOD and TPLLTESTLO_FMOD:

FMOD → Modulation frequency in MHz

tplltestdiv_mx[97] = {
0x07, 0x07, 0x07, 0x07, 0x08, 0x08, 0x08, 0x08, 0x08, 0x08, 0x08, 0x08, 0x09, 0x09, 0x09, 0x09, 0x09, 0x09, 0x09, 0x09,
0x09, 0x09, 0x09, 0x09, 0x09, 0x09, 0x09, 0x09, 0x09, 0x09, 0x0A, 0x0A, 0x0A, 0x0A, 0x0A, 0x0A, 0x0A, 0x0A, 0x0A, 0x0A,
0x0A, 0x0A, 0x0A, 0x0A, 0x0A, 0x0A, 0x0A, 0x0A, 0x0A, 0x0A, 0x0A, 0x0A, 0x0A, 0x0A, 0x0A, 0x0A, 0x0A, 0x0A, 0x0A, 0x0A,
0x0A, 0x0A, 0x0A, 0x0B, 0x0B, 0x0B, 0x0B, 0x0B, 0x0B, 0x0B, 0x0B, 0x0B, 0x0B, 0x0B, 0x0B, 0x0B, 0x0B, 0x0B, 0x0B, 0x0B,
0x0B, 0x0B, 0x0B, 0x0B, 0x0B, 0x0B, 0x0B, 0x0B, 0x0B, 0x0B, 0x0B, 0x0B, 0x0B, 0x0B, 0x0B, 0x0B, 0x0B}

TPLLTESTDIV_FMOD = *tplltestdiv_mx[FMOD-4]*

tplltestlo_mx[97] = {
0xF8, 0xC5, 0xA3, 0x8B, 0xF8, 0xDC, 0xC5, 0xB3, 0xA3, 0x96, 0x8B, 0x81, 0xF8, 0xE9, 0xDC, 0xD0, 0xC5, 0xBC, 0xB3, 0xAB,
0xA3, 0x9C, 0x96, 0x90, 0x8B, 0x86, 0x81, 0x7D, 0x78, 0x75, 0xE9, 0xE3, 0xDC, 0xD6, 0xD0, 0xCB, 0xC5, 0xC0, 0xBC, 0xB7,
0xB3, 0xAF, 0xAB, 0xA7, 0xA3, 0xA0, 0x9C, 0x99, 0x96, 0x93, 0x90, 0x8D, 0x8B, 0x88, 0x86, 0x83, 0x81, 0x7F, 0x7D, 0x7B,
0x78, 0x77, 0x75, 0xED, 0xE9, 0xE6, 0xE3, 0xDF, 0xDC, 0xD9, 0xD6, 0xD3, 0xD0, 0xCD, 0xCB, 0xC8, 0xC5, 0xC3, 0xC0, 0xBE,
0xBC, 0xB9, 0xB7, 0xB5, 0xB3, 0xB1, 0xAF, 0xAD, 0xAB, 0xA9. 0xA7, 0xA5, 0xA3, 0xA1, 0xA0, 0x9E, 0x9C}

TPLLTESTLO_FMOD[15:8]= *tplltestlo_mx[FMOD-4]*
TPLLTESTLO_FMOD[7:0]=0

- Enable streaming
- Set TPLLTESTDIV_FMOD, TPLLTESTOFFSET_FMOD, TPLLTESTLO_FMOD to the values which corresponds the modulation frequency value (see above)
- Set PLL_BISTCLR_FMOD to 1 to reset BIST result register
- Readout PLL_BIST_FMOD and PLL_LOCK_FMOD using I2C or MetaData

11.6. SRAM ECC BIST

Continuous, for every read during streaming.
Indicates an error was detected and corrected in the SRAM. Value is latched at start-up.

Register	Pixel	Name	Description
0x082C[2:0]	E006	LG_SRAM_ERR	LOGIC_SRAM ECC result Bit[2]: LOGIC_SRAM #2 ECC error result: 0 OK, 1 NG Bit[1]: LOGIC_SRAM #1 ECC error result: 0 OK, 1 NG Bit[0]: LOGIC_SRAM #1/#2 ECC error result: 0 OK, 1 NG All three cleared by RAMERR_CLR[0]
0x082E[0]	E010	IF_SRAM_ERR	INTERFACE_SRAM ECC result Bit[0]: Result: 0 OK, 1 NG Cleared by SRAM_ERR_CLR [1]
0x1083[1:0]		SRAM_ERR_CLR	SRAM ECC error clear Bit[1]: INTERFACE_SRAM ECC error clear: Set to 1 to clear Bit[0]: LOGIC_SRAM ECC error clear: Set to 1 to clear

Table 43: SRAM ECC BIST

In order to use SRAM ECC BIST please follow the procedure below:

- Enable streaming
- Set SRAM_ERR_CLR to 0x03
- Wait
- Readout LG_SRAM_ERR and IF_SRAM_ERR using I2C or MetaData

12. Package Information

12.1. MLX75027RTC (ceramic ball grid array)

12.1.1. Transmittance and Reflectance

The double sided anti-reflective coating covers the complete glass lid as seen in the Mechanical Dimensions.
The refractive index of the glass is: n=1.51.
This graph represents the transmittance and reflectivity of the combined glass and anti-reflective coatings.

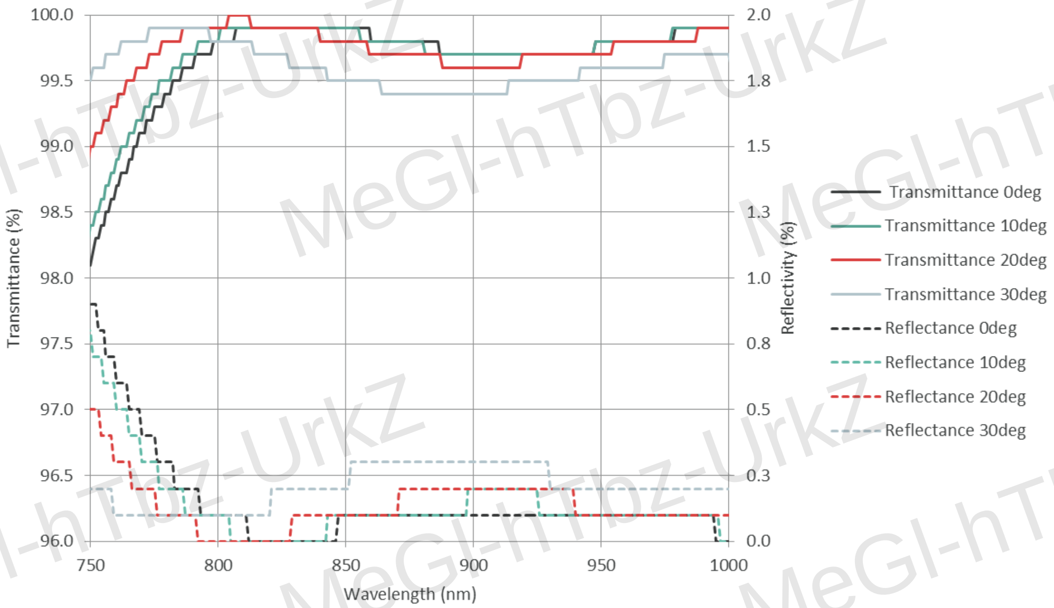


Figure 30: MLX75027RTC Transmittance and reflectance

12.1.2. Pinout & Equivalent I/O Circuitry (version -RTC)

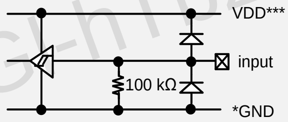
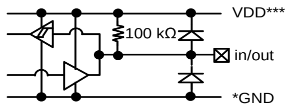
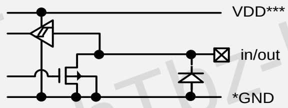
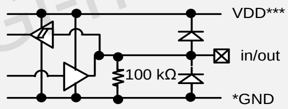
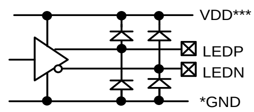
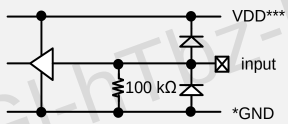
Designator	Pin	Function	Voltage Domain	Equivalent I/O Circuitry
SLASEL	A4	Slave select, choose between I²C slave address 0x57 or 0x67 (digital input)	0 - 1V8	
TRIGGERB	K11	Trigger I/O For more information consult section 8.2 (active low digital I/O)	0 - 1V8	
SCL	B5	I²C clock (digital I/O)	0 - 1V8	
SDA	A5	I²C data (digital I/O)	0 - 1V8	
LEDEN	K3	Optional external control signal (digital output)	0 - 1V8	
LEDP	L3	Positive differential illumination control signal	0 - 1V8	
LEDN	L4	Negative differential illumination control signal	0 - 1V8	
CLK	B3	Input clock of 8 MHz (digital input)	0 - 1V8	
RESETB	A2	Generic device reset (active low digital input)	0 - 1V8	
CSI_CLKN	G1	Digital output		MIPI D-PHY
CSI_CLKP	G2	Digital output		MIPI D-PHY
CSI_DAT1N	H2	Digital output		MIPI D-PHY
CSI_DAT1P	H1	Digital output		MIPI D-PHY
CSI_DAT2N	F1	Digital output		MIPI D-PHY
CSI_DAT2P	F2	Digital output		MIPI D-PHY
CSI_DAT3N	J2	Digital output		MIPI D-PHY
CSI_DAT3P	J1	Digital output		MIPI D-PHY
CSI_DAT4N	E1	Digital output		MIPI D-PHY
CSI_DAT4P	E2	Digital output		MIPI D-PHY

Table 44: MLX75027RTC Pinout 1

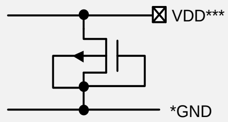
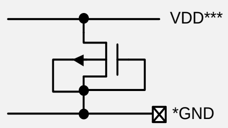
Designator	Pin	Function	Voltage Domain	I/O Equivalent Circuitry
VDDA	A7 B2 C12 E12 G12 M2 M11	Analog supply voltage	2V7	
VDDD	C2 C3 D1 K1 K2	Digital supply voltage	1V2	
VDDMIX	L5 L6 L7 L8 L9 L10	High current supply voltage for the mix driver	1V2	
VDDIF	A3 B6 L1 B12	Supply voltage for I/O interface	1V8	
VBO1	E11	Decoupled to AGND (4.7µF)	2V7	n/A
VBO2	G11	Decoupled to AGND (4.7µF)	2V7	n/A
VRSTL	F12	Decoupled to AGND (1µF)	0V[1] 0V5[2] 1V2[3]	n/A
VRL1	C11	Decoupled to AGND (4.7µF)	0V[1] 0V[2] -1.2V[3]	n/A
VRL2	F11	Decoupled to AGND (4.7µF)	0V[1] 0V[2] -1.2V[3]	n/A
AGND	B1 B8 B11 D11 D12 M5 M6 M7 M8 M9 M10	Analog ground	GND	
DGND	A8 A9 A10 A11 B9 B10 C1 C4	Digital ground	GND	

Table 45: MLX75027RTC Pinout 2

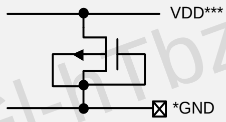
Designator	Pin	Function	Voltage Domain	I/O Equivalent Circuitry
DGND (continued)	C5 C6 C7 C8 C9 C10 D2 D3 D4 D5 D6 D7 D8 D9 D10 E3 E4 E5 E6 E7 E8 E9 E10 F3 F4 F5 F6 F7 F8 F9 F10 G3 G4 G5 G6 G7 G8 G9 G10 H3 H4 H5 H6 H7 H8 H9 H10 J3 J4 J5 J6	Digital ground	GND	

Table 46: MLX75027RTC Pinout 3

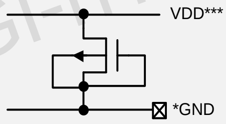
Designator	Pin	Function	Voltage Domain	I/O Equivalent Circuitry
DGND (continued)	J7 J8 J9 J10 K4 K5 K6 K7 K8 K9 K10 L11	Digital ground	GND	
n.c.	A1 A6 B4 B7 H11 H12 J11 J12 K12 L2 L12 M3 M4	Do not connect	Floating	n/A

Table 47: MLX75027RTC Pinout 4

Note[1] : During hardware standby
Note[2] : During software standby
Note[3] : After full initialization

An overlay of these pins and the package can be found here:

BOTTOM VIEW

	12	11	10	9	8	7	6	5	4	3	2	1
M		VDDA	AGND	AGND	AGND	AGND	AGND	AGND	n.c	n.c	VDDA	
L	n.c	DGND	VDDMIX	VDDMX	VDDMIX	VDDMIX	VDDMIX	VDDMIX	LEDN	LEDP	N.c.	VDDIF
K	n.c	TRIG GERB	DGND	DGND	DGND	DGND	DGND	DGND	DGND	LEDEN	VDDD	VDDD
J	n.c	n.c	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	CSI DAT3N	CSI DAT3P
H	n.c	n.c	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	CSI DAT1N	CSI DAT1P
G	VDDA	VBO2	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	CSI CLKP	CSI CLKN
F	VRSTL	VRL2	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	CSI DAT2P	CSI DAT2N
E	VDDA	VBO1	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	CSI DAT4P	CSI DAT4N
D	AGND	AGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	VDDD
C	VDDA	VRL1	DGND	DGND	DGND	DGND	DGND	DGND	DGND	VDDD	VDDD	DGND
B	VDDIF	AGND	DGND	DGND	AGND	n.c	VDDIF	SCL	n.c	CLK	VDDA	AGND
A		DGND	DGND	DGND	DGND	VDDA	n.c	SDA	SLASEL	VDDIF	RESETB	n.c

Figure 31: MLX75027RTC Package pinout

12.1.3. Mechanical Dimensions (version -RTC)

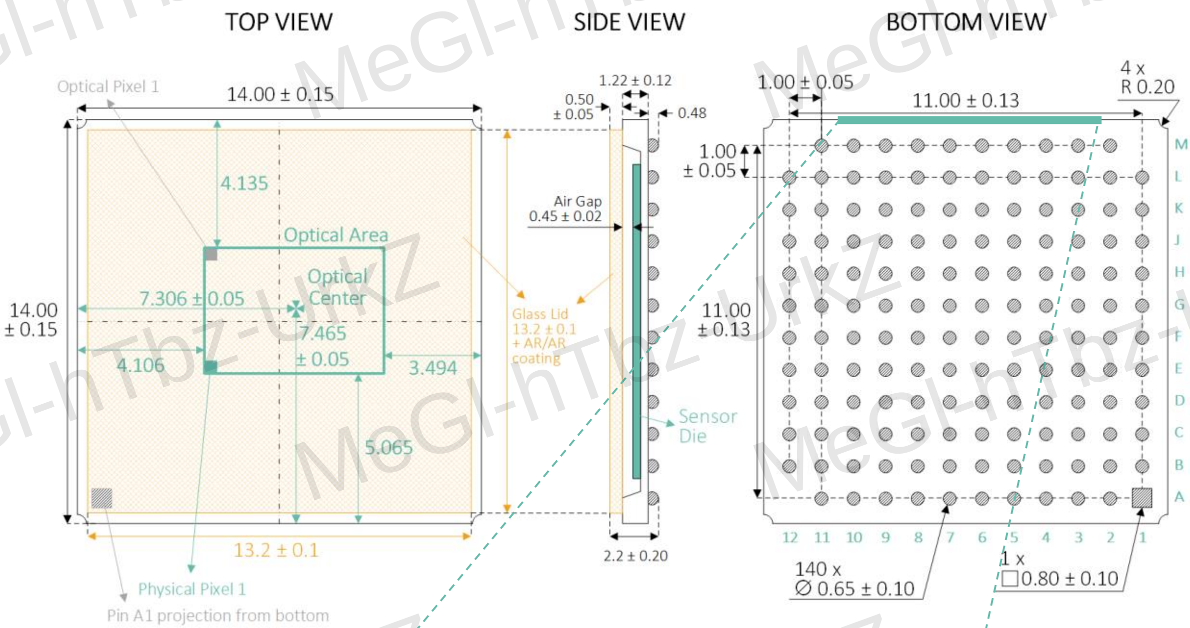


Figure 32: MLX75027RTC Mechanical Dimensions (in millimeter)

12.1.4. Package Marking (version -RTC)

MLX75027	12345678	YYWW
PRODUCT NAME	LOT CODE	DATE CODE

12.1.5. PCB Landing Pattern & Recommendations (version -RTC)

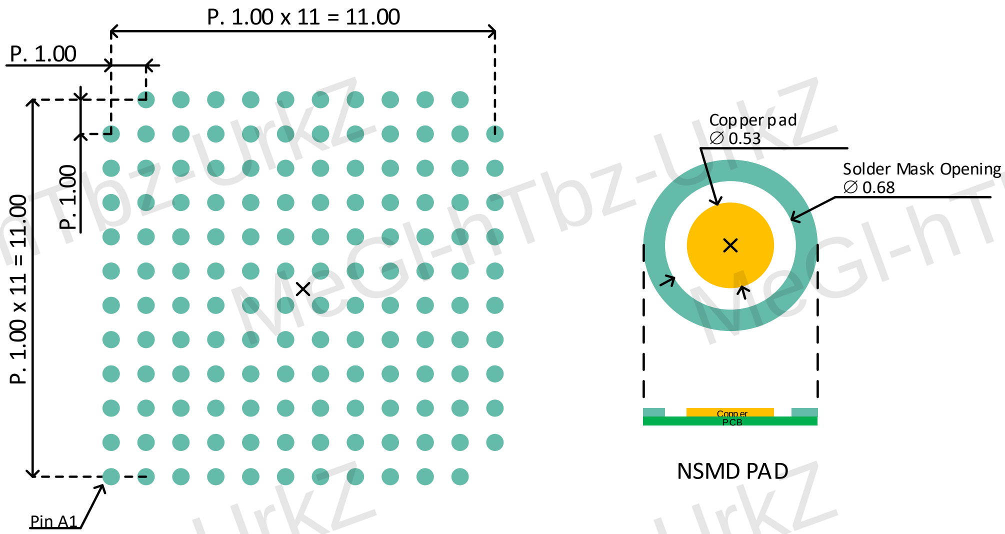


Figure 33: MLX75027RTC PCB landing pattern

*pin A1 is not a solderpad

- Exposed traces under the package should be should be covered by solder mask
- Via's close to the solder pads should be avoided to minimize solder wicking
- NSMD (non-solder mask defined) pads are recommended
- The solder ball composition is SAC305
- Underfill is not required

12.1.6. Cover Tape

Devices are available with an optional cover tape to protect the sensitive image area. For optimal protection from contamination or scratches the cover tape must be removed after PCB assembly & cleaning. The cover tape is able to withstand reflow profiles according to the solder profile specified in section 12.3.

12.1.6.1. Cover Tape Dimensions (version -RTC)

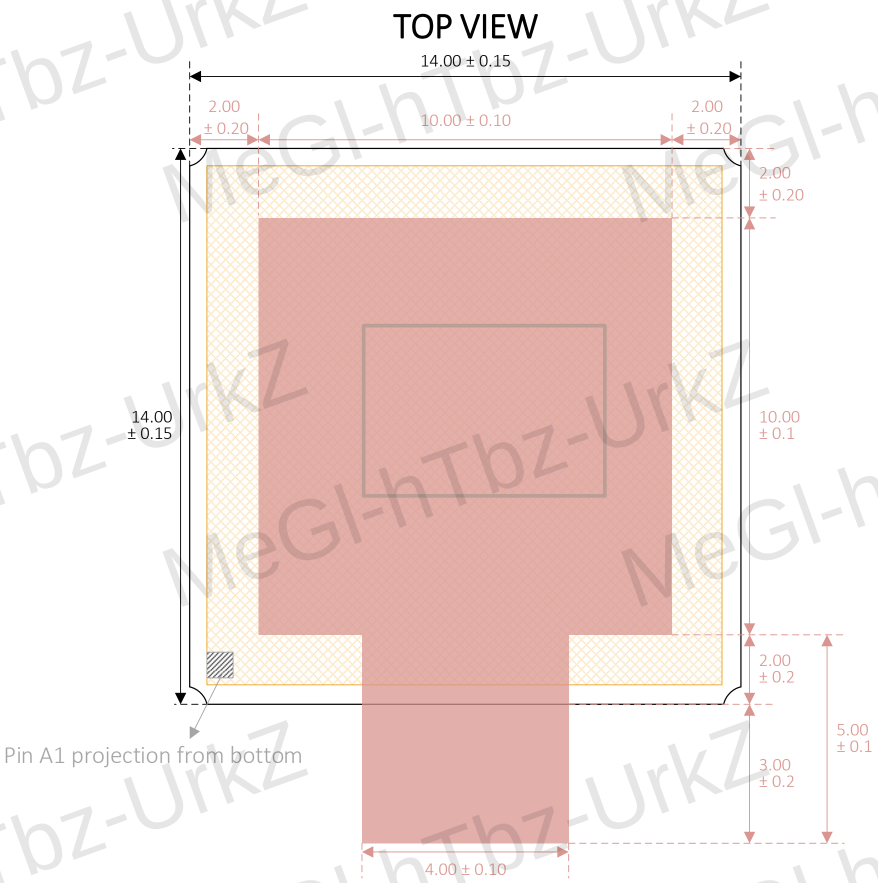


Figure 34: MLX75027RTC Cover Tape Dimensions (mm)

12.1.6.2. Cover Tape Removal

It is mandatory to avoid any horizontal removal to protect the optical sensor from glue residues.

Figure 35: Grab the flag of the covertape and peel it off in an angle of 180° as much as possible.

12.2. MLX75027RTI, MLX75027STI (interstitial ball grid array)

12.2.1. Transmittance and Reflectance

The double sided anti-reflective coating covers the complete glass lid as seen in the Mechanical Dimensions.
The refractive index of the glass is: n=1.5137.
This graph represents the transmittance and reflectivity of the combined glass and anti-reflective coatings.

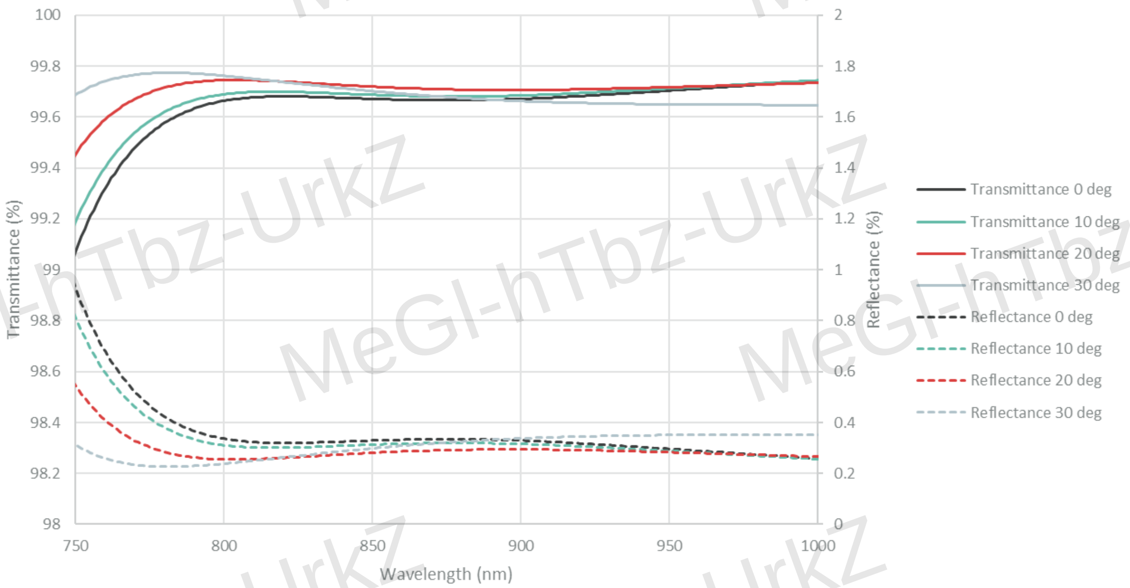


Figure 36: MLX75027RTI, MLX75027STI Transmittance and reflectance

12.2.2. Pinout & Equivalent I/O Circuitry (version –RTI, -STI)

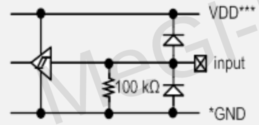
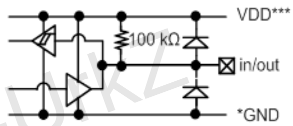
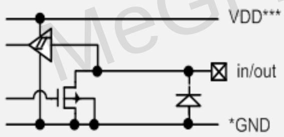
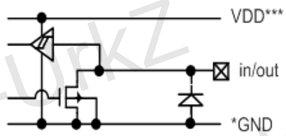
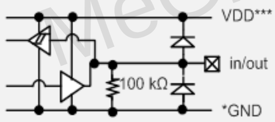
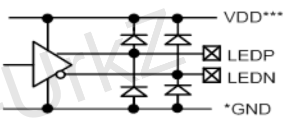
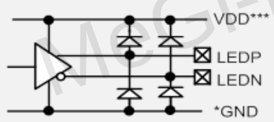
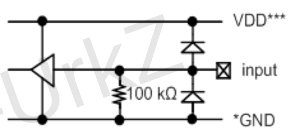
Designator	Pin	Function	Voltage Domain	Equivalent I/O Circuitry
SLASEL	E5	Slave select, choose between I²C slave address 0x57 or 0x67 (digital input)	0 - 1V8	
TRIGGERB	C12	Trigger input with MODE=0, trigger output indicator with MODE=1 (active low digital I/O)	0 - 1V8	
SCL	J6	I²C clock (digital I/O)	0 - 1V8	
SDA	K6	I²C data (digital I/O)	0 - 1V8	
LEDEN	D5	Optional external control signal (digital output)	0 - 1V8	
LEDP	C1	Positive differential illumination control signal	0 - 1V8	
LEDN	B2	Negative differential illumination control signal	0 - 1V8	
CLK	L4	Input clock of 8 MHz (digital input)	0 - 1V8	

Table 48: MLX75027RTI, MLX75027STI Pinout 1

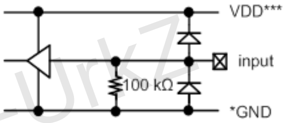
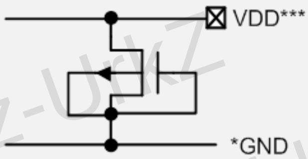
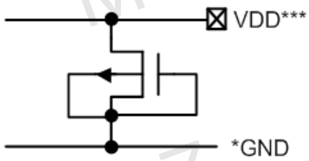
RESETB	J7	Generic device reset (active low digital input)	0 - 1V8	
CSI_CLKN	F1	Digital output		MIPI D-PHY
CSI_CLKP	F2	Digital output		MIPI D-PHY
CSI_DAT1N	E1	Digital output		MIPI D-PHY
CSI_DAT1P	E2	Digital output		MIPI D-PHY
CSI_DAT2N	G1	Digital output		MIPI D-PHY
CSI_DAT2P	G2	Digital output		MIPI D-PHY
CSI_DAT3N	D1	Digital output		MIPI D-PHY
CSI_DAT3P	D2	Digital output		MIPI D-PHY
CSI_DAT4N	H1	Digital output		MIPI D-PHY
CSI_DAT4P	H2	Digital output		MIPI D-PHY
VDDA	B5 B9 B11 C11 E11 E12 H5 H10 H13 J2 J10 K7 K9 K10	Analog supply voltage	2V7	

Table 49: MLX75027RTI, MLX75027STI Pinout 2

VDDD	C2 C6 D12 E3 E4 F4 F13 G3 G4 H4 J11 J13 K2 K8 L3 L6	Digital supply voltage	1V2	

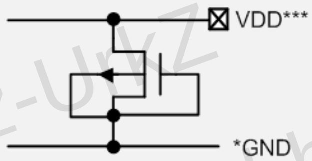
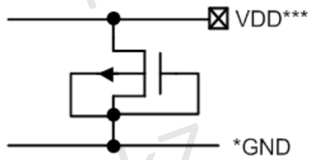
VDDMIX	A3 A5 A7 A9 A11 C7 C8	High current supply voltage for the mix driver	1V2	
VDDIF	B3 B6 D11 G5 H6 K11 L5 L9	Supply voltage for I/O interface	1V8	
VBO1	G13	Decoupled to AGND (4.7µF)	2V7	n/A
VBO2	D13	Decoupled to AGND (4.7µF)	2V7	n/A
VRSTL	G12	Decoupled to AGND (1µF)	0V[1] 0.5V[2] 1V2[3]	n/A
VRL1	H12	Decoupled to AGND (4.7µF)	0V[1] 0V[2] -1.2V[3]	n/A
VRL2	E13	Decoupled to AGND (4.7µF)	0V[1] 0V[2] -1.2V[3]	n/A

Table 50: MLX75027RTI, MLX75027STI Pinout 3

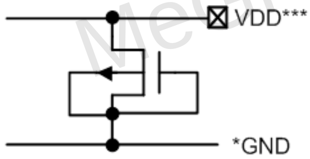
AGND	A1 A2 A4 A6 A8 A10 A12 A13 B1 B10 B12 B13 D7 D8 D9 E6 E7 E8 F5 F6 F7 F8 F9 F11 F12 G6 G7 G8 G10 H7 H11 J3 J4 J9 K1 K13 L1 L2 L7 L10 L11 L12 L13	Analog ground	GND	

Table 51: MLX75027RTI, MLX75027STI Pinout 4

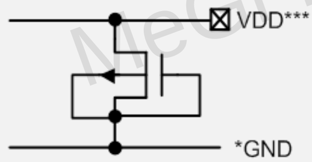
DGND	B4 C3 C4 C9 C13 D3 D4 D6 F3 F10 G11 H3 J1 J12 K3 K4 K5 K12 L8	Digital ground	GND	
n.c.	B7 B8 C5 C10 D10 E9 E10 G9 H8 H9 J5 J8	Do not connect	Floating	n/A

Table 52: MLX75027RTI, MLX75027STI Pinout 5

Note[1] : During hardware standby
Note[2] : During software standby
Note[3] : After full initialization

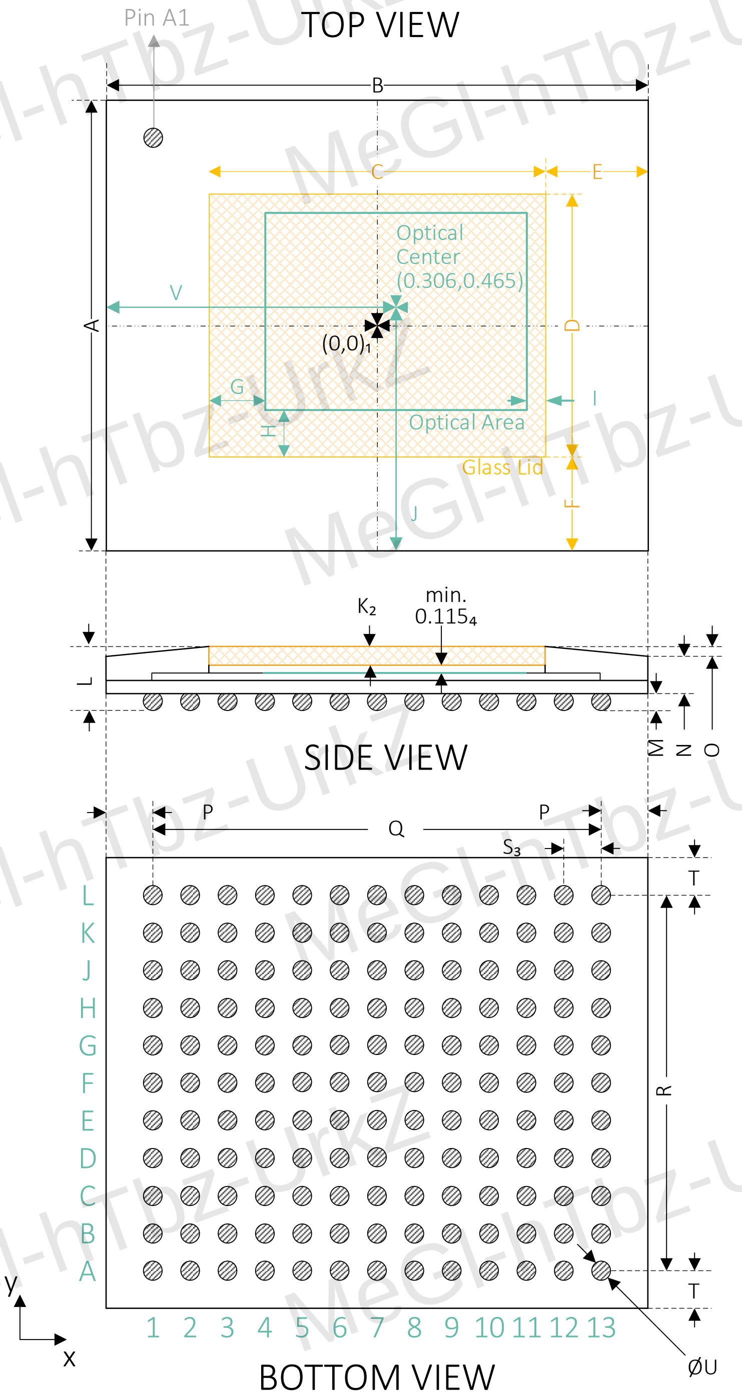
An overlay of these pins and the package can be found here:

TOP VIEW

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	AGND	AGND	VDDMIX	AGND	VDDMIX	AGND	VDDMIX	AGND	VDDMIX	AGND	VDDMIX	AGND	AGND
B	AGND	LEDN	VDDIF	DGND	VDDA	VDDIF	n.c.	n.c.	VDDA	AGND	VDDA	AGND	AGND
C	LEDP	VDDD	DGND	DGND	n.c.	VDDD	VDDMIX	VDDMIX	DGND	n.c.	VDDA	TRIG GERB	DGND
D	CSI_DAT3N	CSI_DAT3P	DGND	DGND	LEDEN	DGND	AGND	AGND	AGND	n.c.	VDDIF	VDDD	VBO2
E	CSI_DAT1N	CSI_DAT1P	VDDD	VDDD	SLASEL	AGND	AGND	AGND	n.c.	n.c.	VDDA	VDDA	VRL2
F	CSI_CLKN	CSI_CLKP	DGND	VDDD	AGND	AGND	AGND	AGND	AGND	DGND	AGND	AGND	VDDD
G	CSI_DAT2N	CSI_DAT2P	VDDD	VDDD	VDDIF	AGND	AGND	AGND	n.c.	AGND	DGND	VRSTL	VBO1
H	CSI_DAT4N	CSI_DAT4P	DGND	VDDD	VDDA	VDDIF	AGND	n.c.	n.c.	VDDA	AGND	VRL1	VDDA
J	DGND	VDDA	AGND	AGND	n.c.	SCL	RESETB	n.c.	AGND	VDDA	VDDD	DGND	VDDD
K	AGND	VDDD	DGND	DGND	DGND	SDA	VDDA	VDDD	VDDA	VDDA	VDDIF	DGND	AGND
L	AGND	AGND	VDDD	CLK	VDDIF	VDDD	AGND	DGND	VDDIF	AGND	AGND	AGND	AGND

Figure 37: MLX75027RTI, MLX75027STI Package pinout

12.2.3. Mechanical Dimensions (version –RTI, -STI)



	Typical
A	9.500
B	11.000
C	8.112
D	6.830
E	1.444
F	1.335
G	1.162
H	1.480
I	0.550
J	5.215
K	0.500
L	1.516
M	0.400
N	0.746
O	0.370
P	0.700
Q	9.600
R	8.000
S	0.800
T	0.750
U	0.520
V	5.806

All distances are in mm

Note:
1: glass,die and package center are the same. Optical center has an x-axis offset of 0.306 and y-axis offset of 0.465
2: equals the glass height
3: the solder ball pitch
4: air gap

Figure 38: MLX75027RTI, MLX75027STI Mechanical Dimensions (in millimeter)

12.2.4. Package Marking (version -RTI, -STI)

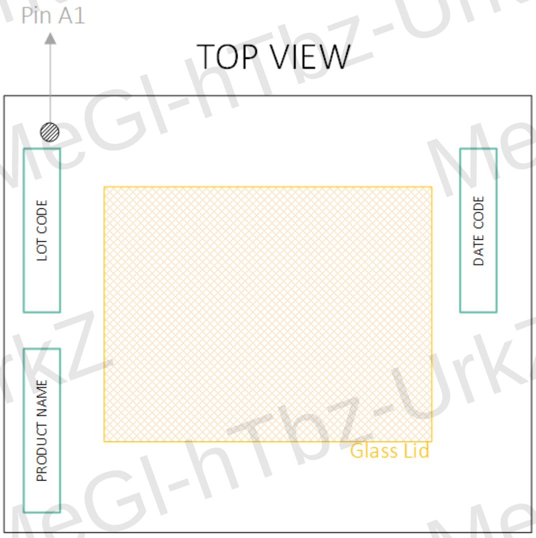


Figure 39: Package marking

12.2.5. PCB Landing Pattern & Recommendations (version -RTI, -STI)

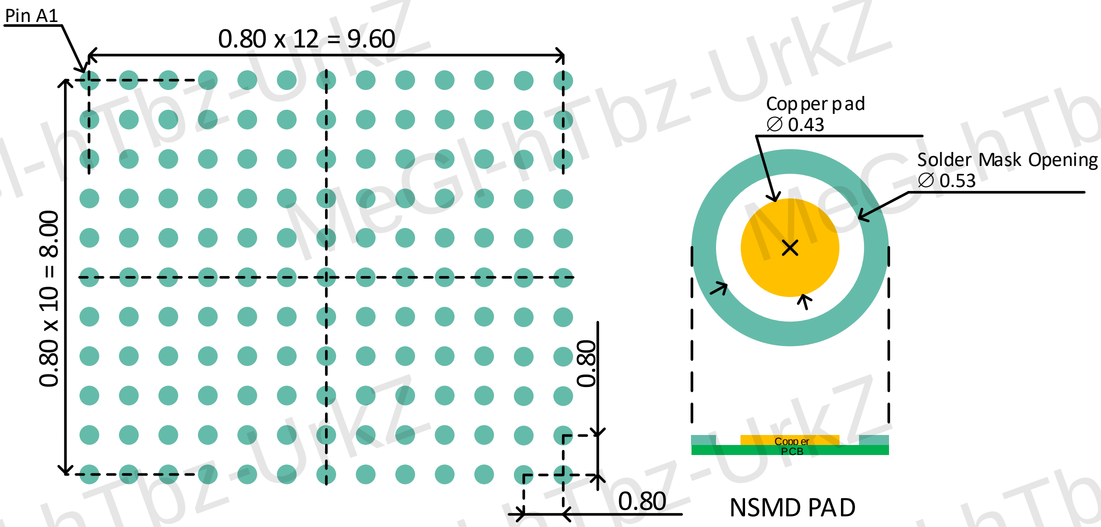


Figure 40: MLX75027RTI, MLX75027STI PCB landing pattern

- Exposed traces under the package should be should be covered by solder mask
- Via's close to the solder pads should be avoided to minimize solder wicking
- NSMD (non-solder mask defined) pads are recommended
- The solder ball composition is SAC305
- Underfill is not required

12.2.6. Cover Tape

Devices are available with an optional cover tape to protect the sensitive image area. For optimal protection from contamination or scratches the cover tape must be removed after PCB assembly & cleaning. The cover tape is able to withstand reflow profiles according to the solder profile specified in section 12.3.

12.2.6.1. Cover Tape Dimensions (version -RTI, -STI)

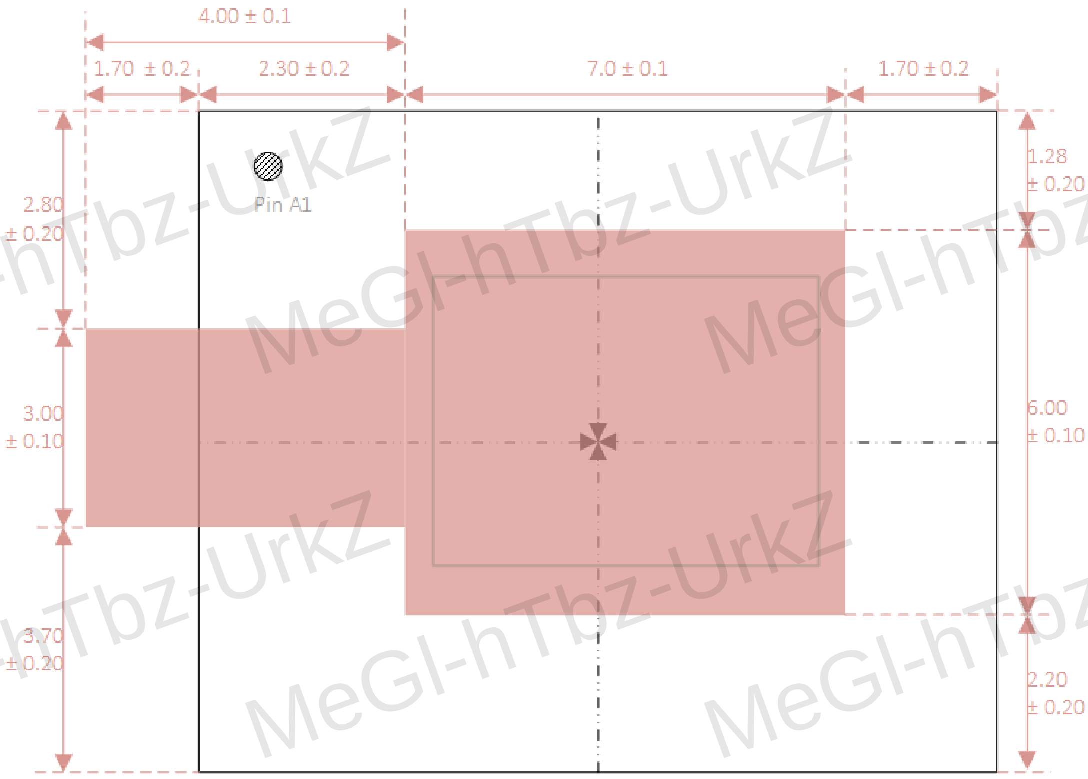


Figure 41: MLX75027RTI, MLX75027STI Cover Tape Dimensions (mm)

12.2.6.2. Cover Tape Removal

It is mandatory to avoid any horizontal removal to protect the optical sensor from glue residues.

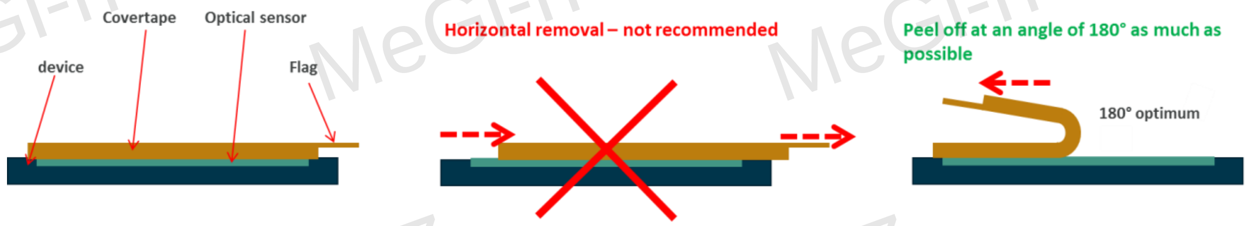


Figure 42: Grab the flag of the covertape and peel it off in an angle of 180° as much as possible.

12.3. Reflow Solder Profile

Melexis recommends either oven reflow or vapour phase soldering process (with linear temperature profile and a melting point of 218°C) for increased solder quality or reflow soldering according to JEDEC-J-STD-020D.

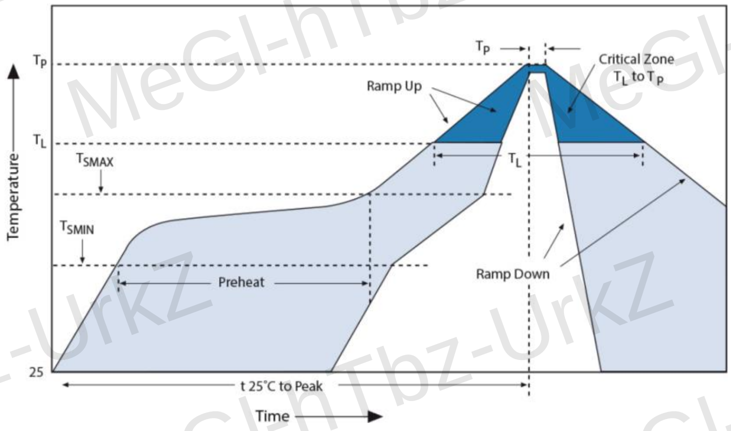


Figure 43: J-STD-020D reflow temperature profile

Profile feature	Standard Parameters	MLX Recommendation
Ramp-up rate	3°C/ sec. (Max.)	1.5°C ~ 2.5 °C / sec.
Preheat temp	150°C ~ 200°C	150°C ~ 200°C
Preheat time	60 ~ 180 sec.	60 ~ 180 sec.
Peak temp	245°C ~ 260°C	245°C
Liquidous time (TL)	60 ~ 150 sec.	60 sec.
Ramp down rate	6°C/sec (Max.)	2°C/sec.

Table 53: Reflow profile

12.4. Reflow Cleaning Instructions

Without using *no-clean* solder we recommend cleaning the sensor surface after component assembly with nitrogen gas, distilled water or isopropanol to remove any flux residues. Make sure to use distilled water or isopropanol in combination with an anti-static cleanroom wiper or clean room swab, never directly apply the distilled water or isopropanol directly to the glass. Do NOT use sodium hydroxide, other highly alkaline solutions or acetone as this would damage the anti-reflective coating on the glass surface.
Ultrasonic chip cleaning is prohibited, as it can result in dust emission from cut surfaces.

13. Tray and Shipping Information

13.1. MLX75027RTC (ceramic ball grid array)

MLX75027 sensors are delivered in trays. Each tray contains up to 119 sensors. The dimensions of the tray is shown in Figure 44: MLX75027RTC Tray Specification.

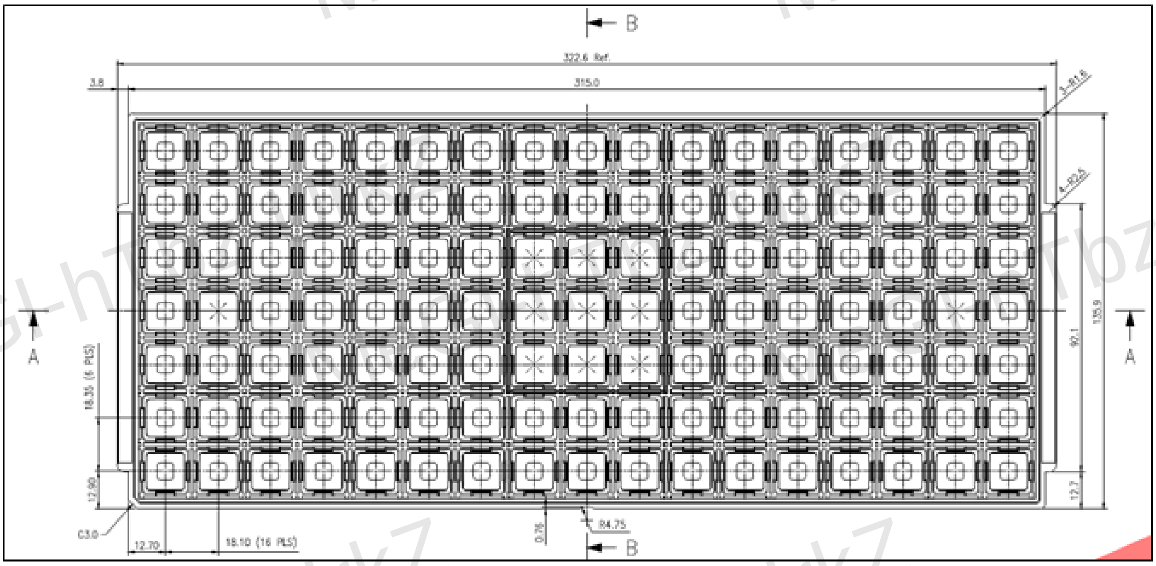


Figure 44: MLX75027RTC Tray Specification

Trays are filled according to: axis 1 and secondly axis 2 as seen in Figure 45: MLX75027RTC Tray Fill Order & Sensor Orientation. Looking at the tray from the top the A1 pin of the sensor is located in the bottom left corner.

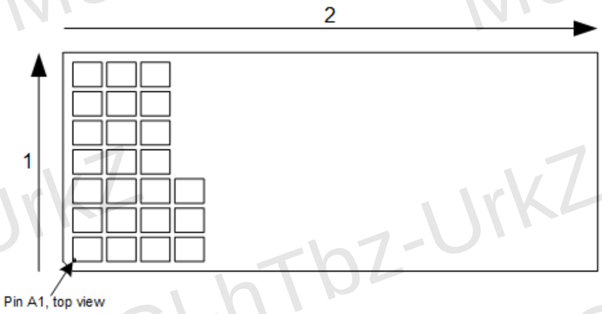


Figure 45: MLX75027RTC Tray Fill Order & Sensor Orientation

Each tray is delivered as part of a carton box. Each carton box contains a maximum amount of trays and sensors as specified in Table 54: MLX75027RTC Delivery Specification.

Packaging information	Amount	Unit
Box size	450x420x240	mm
Sensors/tray	119	/
Filled trays/box	60	/
Sensors/box	7140	/
Weight/box	19	kg

Table 54: MLX75027RTC Delivery Specification

13.2. MLX75027RTI, MLX75027STI (interstitial ball grid array)

MLX75027 sensors are delivered in trays. Each tray contains up to 168 sensors. The dimensions of the tray is shown in Figure 46: MLX75027RTI, MLX75027STI Tray Specification.

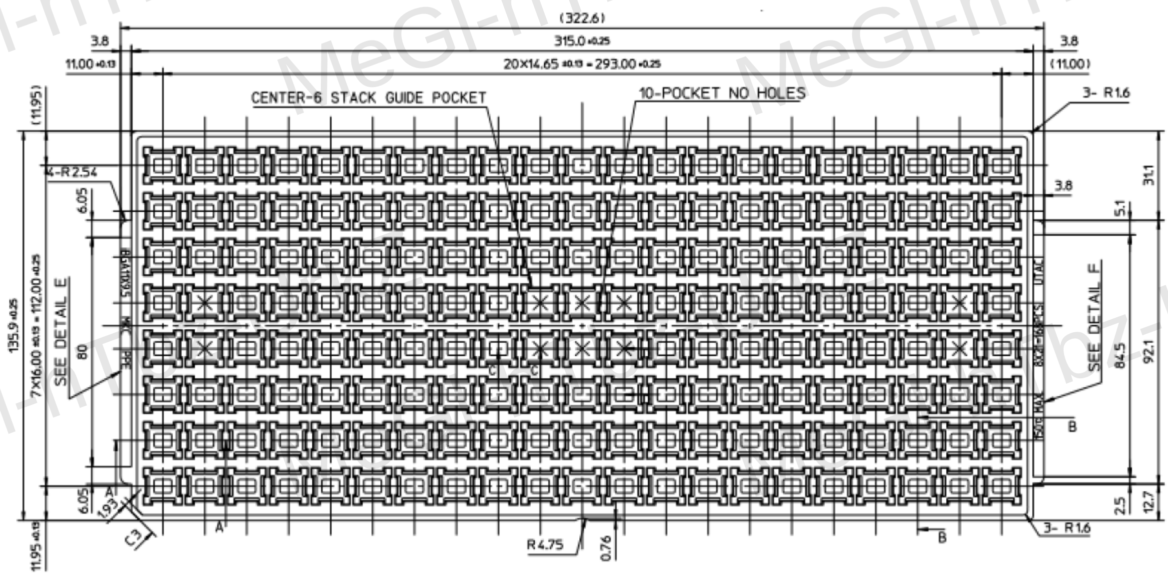


Figure 46: MLX75027RTI, MLX75027STI Tray Specification

Trays are filled according to: axis 1 and secondly axis 2 as seen in Figure 47: MLX75027RTI , MLX75027STI Tray Fill Order & Sensor Orientation. Looking at the tray from the top the A1 pin of the sensor is located in the bottom left corner.

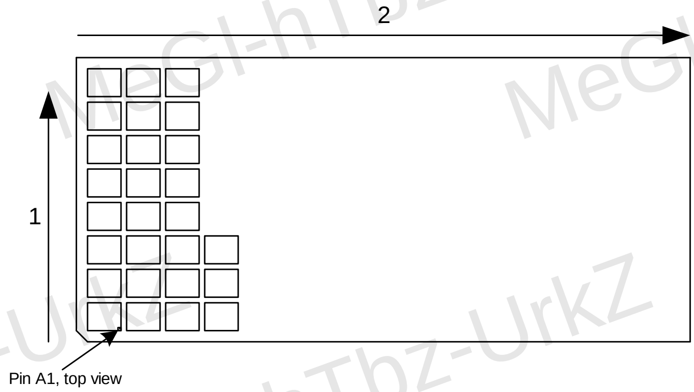


Figure 47: MLX75027RTI , MLX75027STI Tray Fill Order & Sensor Orientation

Each tray is delivered as part of a carton box. Each carton box contains a maximum amount of trays and sensors as specified in Table 55: MLX75027RTI, MLX75027STI Delivery Specification.

Packaging information	Amount	Unit
Box size	450x420x240	mm
Sensors/tray	168	/
Filled trays/box	60	/
Sensors/box	10080	/
Weight/box	14	kg

Table 55: MLX75027RTI, MLX75027STI Delivery Specification

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