# Digital microsystems design

### Outline

- Introduction
  - Prerequisites
  - Overview
  - Goal
  - Specific objectives
- Terms and definitions
- Technology
- Classification

- Design, build, use and program a digital system
  - Microprocessors (single, multiple)
    - Cores and threads
  - Mainboard
  - Buses
  - Memories
  - I/O interfaces

- Prerequisites
  - Programming languages
    - Native, not managed
  - Computer architecture
  - Digital logic
  - Digital circuits and signals

Hardware design track

LSD 
$$\Rightarrow$$
 LD  $\Rightarrow$  AC  $\Rightarrow$  OC  $\Rightarrow$  DMD  $\Rightarrow$  ES  $\Rightarrow$  IoT  $\Rightarrow$  CCIOT  $\Rightarrow$  FIC CE

- Prerequisites
  - C programming language
  - Registers, buffers, memories, decoders, multiplexers, buses
  - Logic gates
  - Pipelines, caches

- How is a computer program executed by hardware?
  - How is a C program executed by a desktop computer or an embedded device?
  - How is a Java program executed by a server or by a mobile device?
  - Is there any difference between them?

 Understand the terms used by computers and processors manufacturers

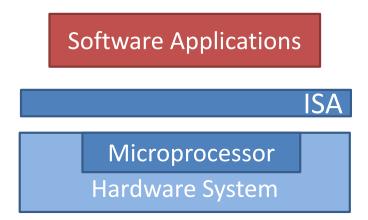
Product Collection	7th Generation Intel® Core™ i5 Processors
Code Name	Products formerly Kaby Lake
Vertical Segment	Mobile
Processor Number	i5-7200U
Status	Launched
Launch Date ?	Q3'16
Lithography ?	14 nm
Recommended Customer Price ?	\$281.00
Performance	
# of Cores ?	2
# of Threads ?	4
Processor Base Frequency ?	2.50 GHz
Max Turbo Frequency ?	3.10 GHz
Cache ?	3 MB SmartCache
Bus Speed ?	4 GT/s OPI
TDP ?	15 W
Configurable TDP-up Frequency ?	2.70 GHz
Configurable TDP-up 🔞	25 W
Configurable TDP-down Frequency 🔞	800 MHz
Configurable TDP-down ?	7.5 W

 What is the interface between software code and hardware components?

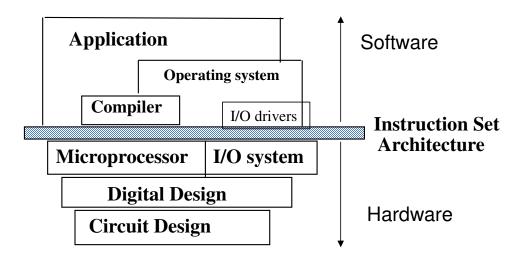
**Applications** 

**Physical System** 

 What is the interface between software code and hardware components?



 What is the glue (interface) between software code and hardware components?



- How would you describe to a friend, the role of the microprocessor in a computer system?
  - The processor is like the brain of a person, being able to take decisions or control the behavior of the system (HW)

- Microprocessors and microcontrollers are part of every type of modern electronic and computing devices: computers, mobile devices, TV sets, multimedia, automotive, etc.
  - Microprocessors general purpose
  - Microcontrollers application specific, application oriented,
     embedded

### Goal

 The discipline aims at providing students with knowledge needed to design a microprocessor-based system (both HW and low-level SW) and to understand how different systems' components are interconnected and application software are implemented and executed

## **Objectives**

### Specific objectives

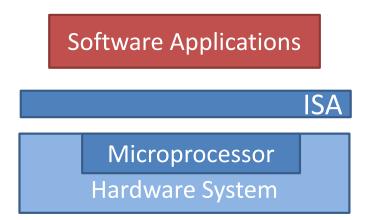
- Acquiring the overview over the microprocessor internal components and their behavior and their external interfaces to the system
- Acquiring the capacity to analyze and design microprocessor-based systems
- Acquiring the ability to implement and test low level applications for x86 ISA and how they will impact the efficiency of high-level algorithms

## Objectives

- x86, IA32, AMD64 processor architectures
- Specialized circuits
- Buses
- Memories
- Assembly language
- C language constraints and optimization

### **Terms**

- Microprocessor architecture, microarchitecture
  - Internal structure of a microprocessor
- Instruction set architecture
  - Programming interface of a microprocessor



- Moore's law
  - The number of transistors on a given piece of silicon would double every 18

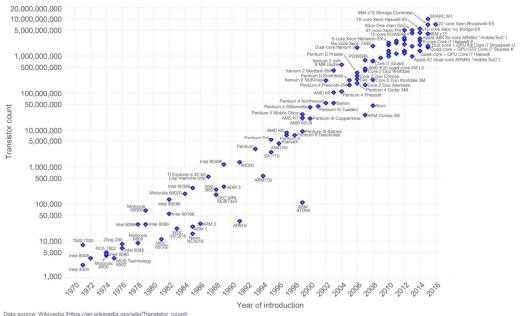
months (1965)

- 24 months (1975)

Moore's Law — The number of transistors on integrated circuit chips (1971-2016)

Moore's law describes the empirical regularity that the number of transistors on integrated circuits doubles approximately every two years.

This advancement is important as other aspects of technological progress — such as processing speed or the price of electronic products — are strongly linked to Moore's law.



• Which is the main factor that supported microprocessor advances?

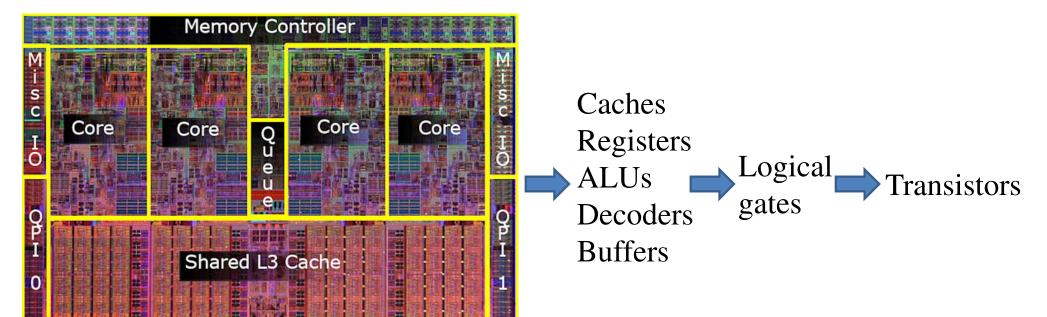
Processor	Year	Transistors count	Pins count	Technology [µm]	V <sub>DD</sub> [V]	F <sub>max</sub> [MHz]	P <sub>max</sub> [W]
4004	1971	2250	16	10	12	0.1	
8080	1974	4500	40	6	5	3	
8086	1978	29000	40	2	5	12	
80286	1982	134000	68	1.5	5	20	
80386	1985	275000	132	1	5	33	1.9
80486	1989	1200000	168	0.8	5 - 3.3	66	6
Pentium	1994	3100000	320	0.6 - 0.35	5 - 3.3	200	15
Pentium Pro	1997	5500000	387	0.35	3.3 - 2.9	300	47
Pentium 2	1998	7500000	242	0.25	3.3 - 2.1	500	27
Pentium 3	1999	9500000	242	0.18	3.3 - 1.3	1200	37
Pentium 4	2000	55000000	478	0.13	1.75 - 1.5	1500	57
Pentium 4	2001	55000000	478	0.13	1.75 - 1.5	2000	75
Itanium	2001	25000000		0.18	3.3	800	116
Pentium 4	2002	55000000	478	0.13	1.75 - 1.5	3000	81
Itanium 2	2002	220000000		0.18	3.3	1000	130

• Processor description on emag.ro

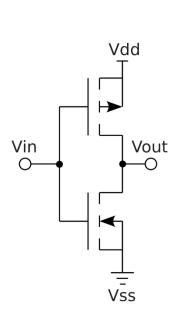
### **PROCESOR**

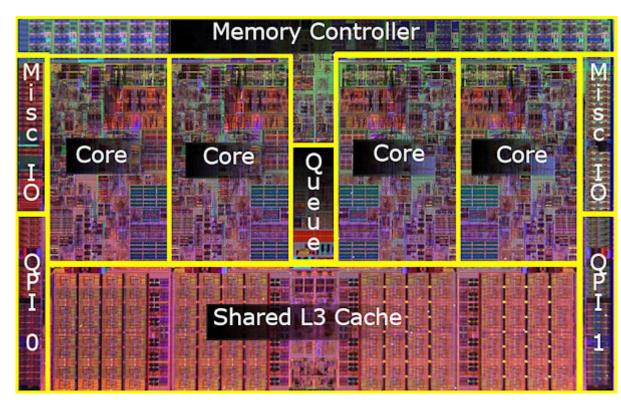
Producator procesor	Intel®
Tip procesor	i5
Model procesor	7400
Numar nuclee	4
Numar thread-uri	4
Arhitectura	Kaby Lake
Frecventa nominala	3000 MHz
Frecventa Turbo Boost	3500 MHz
Cache	6144 KB
Tehnologie procesor	14 nm

 Which is the smallest physical component used to design a circuit?

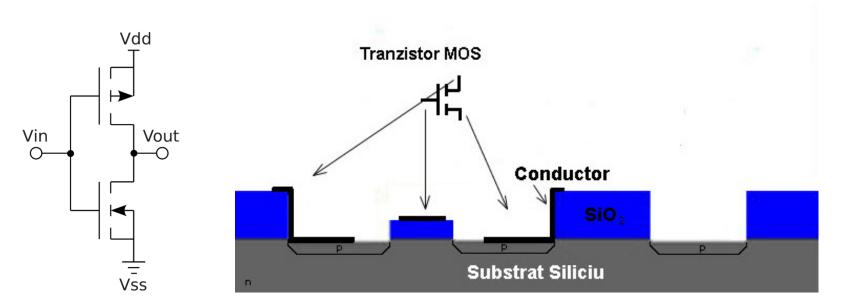


Manufacturing technology of VLSI

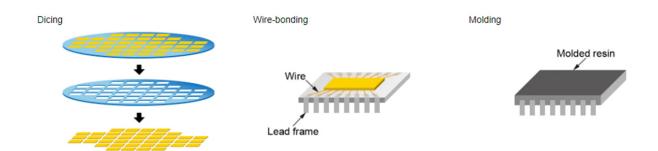




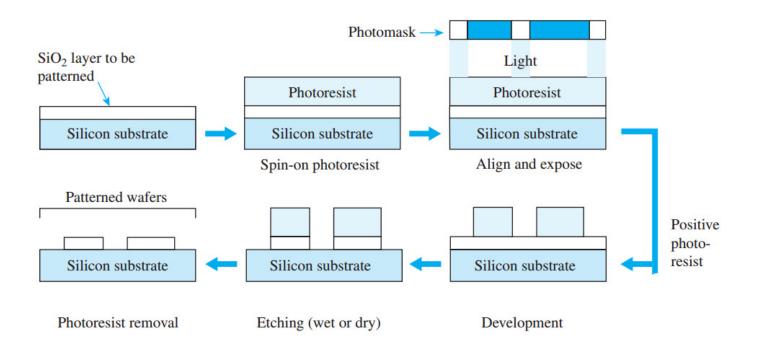
- Manufacturing technology of VLSI circuits
  - Cross section of a MOS transistor



Fabrication process



### Fabrication process



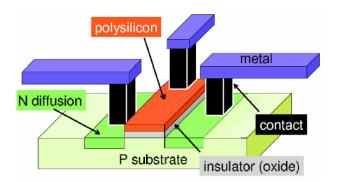
- Manufacturing technology of VLSI circuits
  - 3D view of a MOS transistor

# nMOS Transistor gate oxide (poly) drain source (diffusion) base

### Semiconductor manufacturing processes

```
10 μm – 1971
6 μm – 1974
3 μm – 1977
1.5 μm – 1981
1 μm – 1984
800 nm - 1987
600 nm - 1990
350 nm - 1993
250 nm - 1996
180 nm - 1999
130 nm - 2001
90 nm - 2003
65 nm - 2005
45 nm - 2007
32 nm - 2009
22 nm - 2012
14 nm - 2014
10 nm - 2016
7 nm - 2018
5 nm - 2020
Future
3 nm ~ 2022
2 nm ~ 2024
```

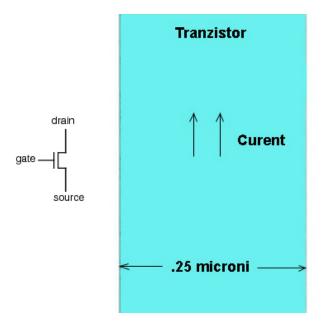
- Manufacturing technology of VLSI circuits
  - 3D view of a MOS transistor



### Semiconductor manufacturing processes

10 μm – 1971 6 μm – 1974 3 μm – 1977 1.5 μm – 1981 1 μm – 1984 800 nm - 1987 600 nm - 1990 350 nm - 1993 250 nm - 1996 180 nm - 1999 130 nm - 2001 90 nm - 2003 65 nm - 2005 45 nm - 2007 32 nm - 2009 22 nm - 2012 14 nm - 2014 10 nm - 2016 7 nm - 2018 5 nm - 2020 Future 3 nm ~ 2022 2 nm ~ 2024

- Manufacturing technology of VLSI circuits
  - Top-down view over a MOS transistor



### Semiconductor manufacturing processes

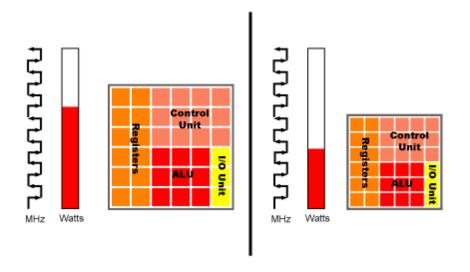
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Future
3 nm ~ 2022
2 nm ~ 2024
```

- Moore's law was a prediction of VLSI circuits development using the semiconductor scaling process
- Scaling is the process of shrinking the physical basic units of an integrated circuit – the transistors

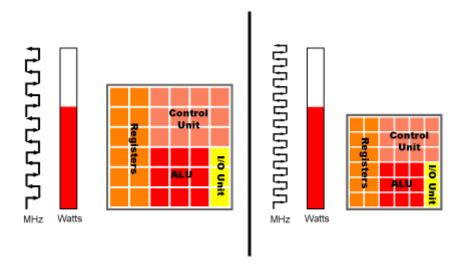
- Scaling objectives
  - Decrease the sizes of the transistors
  - Increase the frequency
  - Increase the number of transistors
- Consequence of increasing the number of transistors
  - Increase the power consumption
- As a solution to increasing power consumption
  - Decrease the circuit voltages
  - Decrease the threshold voltages

- Scaling benefits
  - Increase the number of transistors on the same area of the die
  - Decrease the power consumption of the circuit
  - Increase the operation frequency
- Technology scaling has been the mean by which Moore's Law was possible

- Scaling benefits
  - The same features at lower power consumption

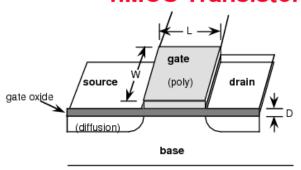


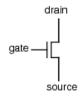
- Scaling benefits
  - Increasing processing speed at the same power consumption



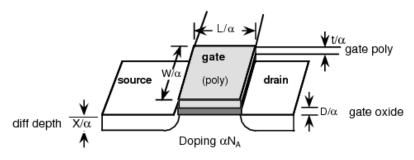
Scaling process

### **nMOS Transistor**

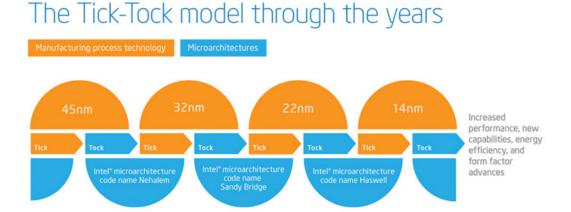




• Scaling factor  $\alpha$ :

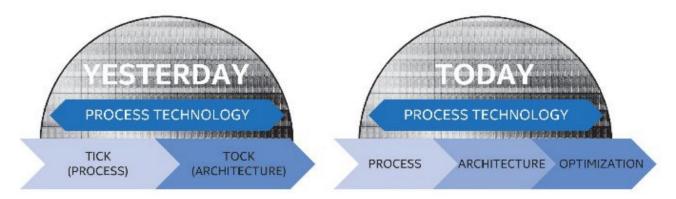


- Alternation of processor development steps
  - Scaling/technology changing (~1year)
  - Architectural advances (~1year)



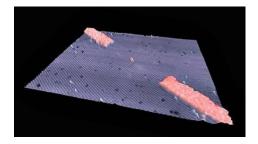
# Technology

- Moore's law limits
  - Prolongation of development cycle
    - Process
    - Architecture
    - Optimization



# Technology

- Moore's law limits
  - 2010 frequency
  - 2020 costs
  - 2025 size
    - Single atom transistor (University of New South Wales)
    - Validation of theoretical models



# Technology

- Moore's law risks
  - Companies took the prediction as a law to be competitive on the market
  - Push innovation in one direction increase the performance
  - Intel Israel Centrino technology optimize for low power

- A digital microsystem is a microprocessor or microcontrollerbased computing system.
  - Computer systems
  - Embedded systems
  - Mobile systems

- A microprocessor is a general purpose programmable logical circuit
  - Can be used in general purpose computing devices
  - Can be programmed to run any type of application
- A microcontroller is an application specific programmable logical circuit dedicated to real-time, embedded applications
  - Application oriented processor
  - Domain specific processor

- Mobile processors are low power processors used in mobile systems
  - General purpose, simple processors
  - Low power, energy efficient

- Other types of processors
  - DSP Digital Signal Processor
  - GPU Graphics Processing Unit
  - FPU Floating Point Unit
  - TPU Tensor Processing Unit
  - ASIC Application Specific Integrated Circuit
- Soft-processors (soft cores)
  - FPGA synthetized

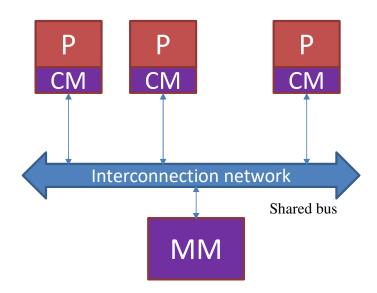
• What are the main parameters used to compare different systems?

#### Parameters

- Performance
- Number of processors
- Number of cores
- Interconnection network
- Memory hierarchies
- Granularity
  - Fine grain simple operations on large amount of data
  - Coarse grain complex operations on small amount of data

- Memory organization
  - UMA (Uniform Memory Access Model)
  - NORMA (No Remote Memory Access Model)
  - NUMA (Non-Uniform Memory Access Model)
  - COMA (Cache-Only Memory Access Model)

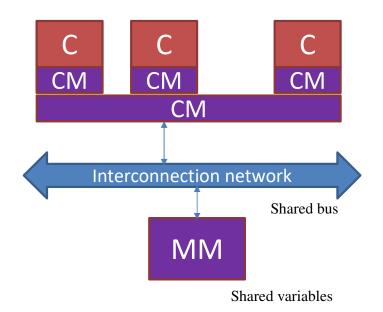
• UMA - Uniform Memory Access Model



P – CPU or CPU core CM – Cache memory MM – Main memory

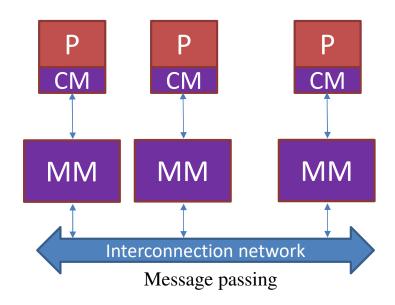
- UMA (Uniform Memory Access)
  - Shared memory / global memory
    - Shared variables
  - Uniform access
    - Equal access to memory
    - The same access time
    - No mater which processor
  - Unique physical address space
  - Symmetric multi-processors (SMP)

• UMA - Uniform Memory Access Model



C – CPU core CM – Cache memory MM – Main memory

NORMA - No Remote Memory Access Model

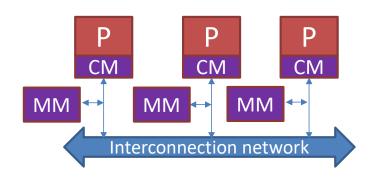


P – CPU or CPU core CM – Cache memory MM – Main memory

- NORMA (No Remote Memory Access)
  - Distributed memory
  - Access to local memory only
  - No access to remote memory
  - Distinct address spaces for every processor
  - Inter-processors communication using messages (network, I/O)

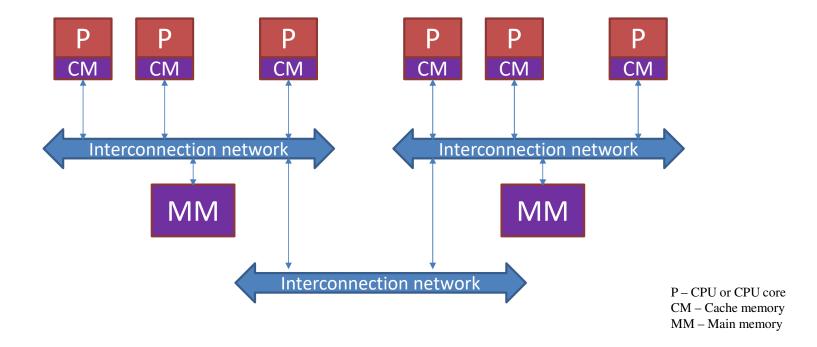
- NUMA (Non-Uniform Memory Access)
  - Distributed-shared memory
  - Each processor has access to both local memory and remote memory
  - Non-uniform access to memory
    - Local memory low access times
    - Remote memory high access times
  - Unique virtual address space

#### • NUMA



P – CPU or CPU core CM – Cache memory MM – Main memory

• Hybrid UMA/NUMA - general



- Flynn
  - Instructions stream
  - Data stream
- Flynn taxonomy:
  - SISD (Single Instruction stream Single Data stream)
  - SIMD (Single Instruction stream Multiple Data stream)
  - MISD (Multiple Instruction stream Single Data stream)
  - MIMD (Multiple Instruction stream Multiple Data stream)

#### SISD

- Instructions are executed sequentially
- Micro-operations parallelism allowed (pipeline)
- Multiple functional units (math-coprocesor, graphic processor, I/O processor)

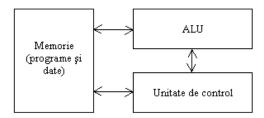


Figura 1.1 - Arhitectura von Neumann

#### • SISD

- UC command unit
- UE execution unit
- MM memory module
- SI instruction stream
- SD data stream

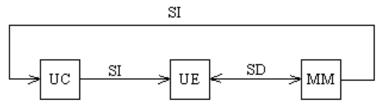


Figura 1.2 Arhitectura SISD

#### • SIMD

- One UC controls many UEs
- UEs execute simultaneously the same instruction on distinct data
- Large number of UEs (thousands)
- Applications having fine grain data processing

#### • SIMD

- Processors arrays
- Vector processors
- Graphical processors

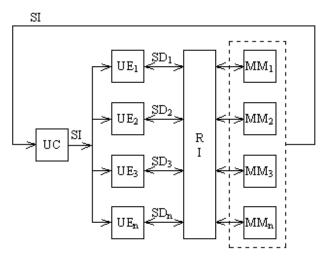


Figura 1.3 Arhitectura SIMD

- MISD
  - The same data is processed by different UEs
  - Macro-pipeline
- Systolic arrays

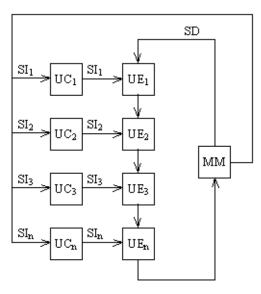


Figura 1.4 Arhitectura MISD

- MIMD
  - Each UE has its own UC
  - Every UE executes instructions on local data

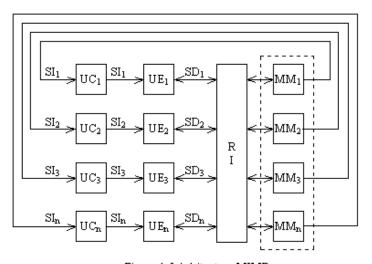
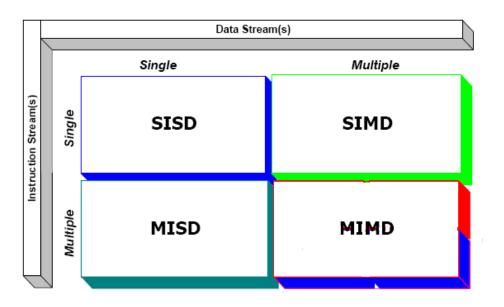


Figura 1.5 Arhitectura MIMD

- MIMD
  - Multi-processor servers
  - Multi-core processors
  - Computer networks
- Rack based servers
  - Blades
  - Hundreds of cores
  - Hundreds of GB of memory

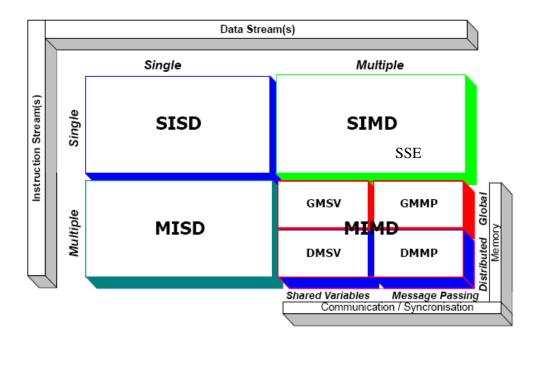


- Extension of Flynn taxonomy
  - MIMD



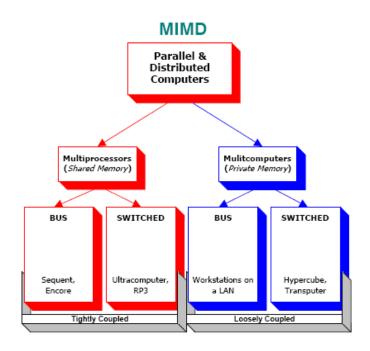
- MIMD architectures can be further classified based on:
  - Inter-processor communication:
    - Shared memory or messages
  - Interconnection network
    - Bus or crossbar
  - Memory organization:
    - Shared or distributed
  - Coupling level between the nodes
    - Loosely or tightly

Flynn-Johnson taxonomy



- GMSV Global Memory / Shared Variables.
  - Multi-core/ multi-processor
- GMMP Global Memory / Message Passing
  - virtualization
- DMSV Distributed Memory / Shared Variables.
  - Distributed-shared memory/ middleware
- DMMP Distributed Memory / Message Passing.
  - Computer networks, distributed computing, grid

Tanenbaum taxonomy



- Interconnection network topologies
  - Static (ring, tree, hypercube, mesh)
  - Dynamic (bus, switches/crossbar)
- Coupling
  - Tightly coupled systems
  - Loosely coupled systems

#### Administrative

- Lab B414/B413 2h / week
  - Iasmina Gruicin, Marius Marcu
- Project B414 1h / week
  - Marius Marcu

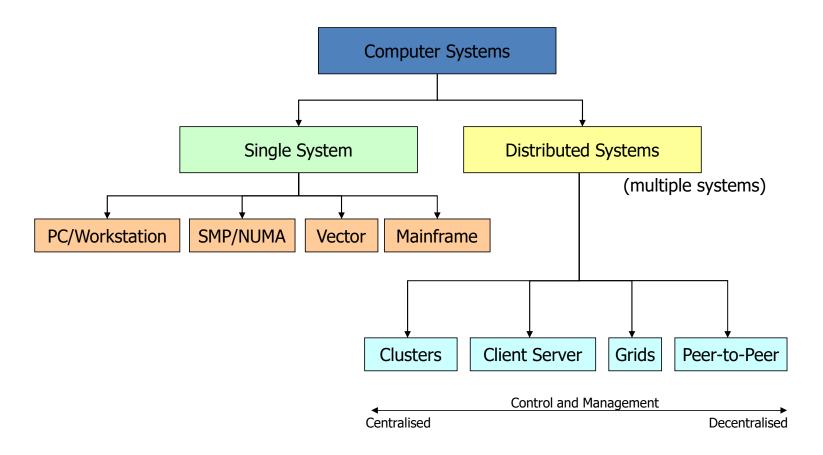
#### 10. Assessment

Activity type	10.1 Assessment criteria	10.2 Assessment methods	10.3 Weight in final mark
10.4 Lecture	Digital microsystem design fundaments	Written exam	25%
	Digital microsystem design applications	Written exam	25%
10.5 Seminar /labs	Solving the topics proposed during the laboratory	Laboratory deliverables presentation and questions	25%
	Semester project development and presentation	Project deliverables presentation and questions	25%

<sup>10.6</sup> Minimal performance standards (minimal specific knowledge required for passing the exam, the means to assess mastering the specific knowledge)

- Overall microprocessor architecture and behavior; overall microprocessor system architecture and behavior
- Memory decoding, I/O decoding
- Connecting memory to CPU
- Connecting I/O to CPU

# Summary



# Summary

- Memory organization
  - UMA
  - NUMA
  - NORMA

# Summary

- Flynn taxonomy
  - SISD
    - Harvard architecture
    - Princeton architecture
  - -SIMD
  - MISD
  - MIMD
    - GMSV
    - DMSV
    - GMMP
    - DMMP