Course 1
Large Scale Integrated CIrcuits

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September 28, 2017

Overview

Why this course

- Design and implementation of complex digital System-on-Chip(SoC)
- Main design principles for large SoC, that characterize today's semiconductor market
- RTL and system level description of todays SoC
- Prerequisites:
  - Digital Logic
  - Digital Circuits and Systems
  - Computer Architecture
- Complementary with Digital Microsystem Design
  - Digital Microsystem Design - targets mainly usage and programming of Digital Systems
  - Large Scale Integrated Circuit - low level design of Digital Systems

Course objectives

- Course has three main parts:
  1. Logic - Register Transfer Level - used for:
     - Processor core design
     - Hardware accelerators design
     - Communication interfaces design:
  2. Memory
  3. Interconnect
- The course does not cover Analogue and Mixed Signal components, that include: converters (ADC and DAC), sensors, PLLs, radio frequency (RF), etc.

Course outline

- Register Transfer Level (RTL) methodology - covers logic
  - Accelerating algorithms in hardware
  - Simple processor design
- Memory modules
  - Memory hierarchy
  - SRAM memory implementation and coding
- Interconnection infrastructure
  - Interconnection architectures
    - Bus based
    - Network-on Chip (NoC)
  - Bus architectures
    - AMBA AXI - proprietary to ARM
    - Wishbone bus - open source

Laboratory assignments

- Project based
- Design of a digital chronometer with memory function on a Digilent Nexys-2 FPGA board:
  - Clock frequency synthesis using Digital Clock Managers
  - Timer/counter and control finite state machine
  - Memory modules - using FPGA Block RAM (BRAM)
  - Wishbone bus usage

Evaluation

- Exam - 50%
  - Open book
  - Consists of two problems
- Laboratory/project - 50%

Historic perspective

- 1958 - First integrated circuit (IC) - Texas Instruments
  - 1 transistor + 1 R + 1 C oscillator
- 1959 - Planar manufacturing process for semiconductor devices (used until 2013-2015)
- 1960 - Metal Oxide Semiconductor Field Effect Transistor (MOS-FET) demonstrated
- 1963 - Complementary MOS gates are invented - there were too slow
- 1965 - First semiconductor memories (ROM memories)
- 1966 - First computer aided design tools for IC (IBM) - the start of the electronic design automation (EDA) industry
- 1966 - The first semiconductor RAM

Historic perspective

- 1969-1971 -Microprocessor Central Processing Unit (CPU) - integrated in a single chip
- 1971 - Reusable Programmable ROM - the start for non-volatile semiconductor memories (now used as Flash and SSD)
- 1974 - Texas Instruments TMS1000 - first microcontroller
- 1974 - Microma Digital Watch - first System on Chip
- 1978 - Introduction of Programmable Array Logic - precursors of Field Programmable Gate Arrays (FPGA)
- 1979 - Bell Labs DSP-1 - first chip dedicated Digital Signal Processor

Historic perspective

- 1981 - Berkeley RISC I - first RISC processor
- 1984-1985 - Altera EP300 and Xilinx XC2064 - first FPGAs
- 1985 - Acorn RISC Machine (ARM) processor
- 1996 - IBM Power4 - first dual-core processor
- 1996 - ARM Advanced Microcontroller Bus Architecture (AMBA) - first on-chip bus protocol
- 2004 - Intel and Tezzaron - first 3D integrated chips
- 2005 - Arteris - first commercial Network-on Chip (NoC) fabric

Transistor scaling - historic perspective

- Moore's Law - the number of transistors in an IC doubles every 18 months

Chip	Technology	Transistor count	Year
Intel 4004	PMOS 10 um	2300	1971
Intel 8008	PMOS 10 um	3500	1974
Intel 8080	NMOS 6 um	4300	1974
Intel 8086	NMOS 3 um	29000	1978
Intel 80286	NMOS 1.5 um	134 000	1982
Intel 80386	CMOS 1.5 um	275 000	1985
Intel 80486	CMOS 1 um	1 180 000	1989
Intel Pentium	CMOS 0.8 um	3 100 000	1993

Table: Intel CPU Evolution

Transistor scaling - historic perspective

- Moore's Law - the number of transistors in an IC doubles every 18 months

Chip	Technology	Transistor count	Year
Intel Pentium II Deschutes	CMOS 0.25 um	7 500 000	1998
Intel Pentium III Tualatin	CMOS 0.13 um	45 000 000	2001
Intel Pentium IV Prescott	CMOS 90 nm	112 000 000	2004
Intel Pentium D Presller	CMOS 65 nm	360 000 000	2006
Intel Core i7	CMOS 45 nm	731 000 000	2008
Intel Gulftown Core i7	CMOS 32 nm	1 170 000 000	2011
Intel Xeon Phi	CMOS 22 nm	5 000 000 000	2012
Intel Xeon Broadwell E5	CMOS 14 nm	7 200 000 000	2016

Table: Intel CPU Evolution

Transistor scaling - historic perspective

- Till around 2010 - planar (2D) devices - all the semiconductor devices within a die are built on a silicon plane
  - One die contains one silicon layer (for transistors) and multiple metal/dielectric layers (for connecting wires)
- Recent years - 3D ICs - multiple silicon layers - used for Flash and SSD memories
  - Problematic to use 3D ICs due to thermal issues (interior layers cannot be cooled efficiently)
- Recent years - 2.5D ICs - multiple silicon dies on a dielectric plane - used for processing (DSP, CPUs, GPUs and FPGAs) based IC

Future markets

Artificial Intelligence and Machine Learning

- "Software is eating the world, and AI is eating software" - NVIDIA CEO
- SoC with increased performance/power consumption ratio allows implementation of AI in both mobile and non-mobile applications:
  - Robotics and drones
  - Smartphones
  - Automotive and avionics
  - Data-centers
- Replacement of microcontroller by AI dedicated chips in a wide range of markets, such as automotive or robotics

Future markets

Artificial Intelligence and Machine Learning

- Typical SoCs targeting AI consist of:
  - CPU - usually 1 or 2 cores for control purposes
  - GPUs - multiple cores for acceleration of floating point multiplications and multiply-add (such as floating point implementation of NN)
  - FPGA fabric - reconfigurable hardware acceleration using integer operations
  - Custom DSP/image processing accelerators - for pre-processing purposes

Future markets

Telecom

- 100 Gbps wireless
- Internet everywhere (jungle, desert, Antarctica, middle of the ocean)
- Heavy DSP computation, based on integer operations:
  - Forward Error Correction, such as LDPC or Turbo
  - Fast Fourier Transforms, Dicrete Cosine Transforms
  - Modulation, channel estimation
  - MIMO (multiple input - multiple output) processors for multiple antenna arrays - 5G and beyond may use up to 256 antennas
  - Software Define Radios