List of Activities – Hardware Plan:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Activity** | **Description** | **Dependency** | **Time Estimate** | **Expected Time** |
|  | START | NULL |  |  |
|  | HW Planning phase | NULL |  |  |
|  | Design and test of clock division circuit design for quavers/semi-quavers | A |  |  |
|  | Design and test of circuit for outputting of relevant frequency waveforms to double integrator | C |  |  |
|  | Implementation of hardware circuit using components designed in C, and D for basic 60bpm tempo | C, D |  |  |
|  | **Demonstration of D on FPGA** | **C, D, E,** |  |  |
|  | Design and test circuit for tempo changing hardware | F |  |  |
|  | Interfacing with IR LED + remote control to control tempo changes | F |  |  |
|  | Implementation of circuit containing components designed in G, and H. | G, H, |  |  |
|  | **Demonstration of I on FPGA** | **G, H, I,** |  |  |
|  | Integration with SW … TBD |  |  |  |