Assignment.

1. Explain Master-slave flipflop.

It is a type of flip-flop that can be designed with two JK FFs by connecting in series one of these flipflop's, one flipflop works as the master and the other flipflop works as a slave. The connection of these flipflop's can be done like this, the master flipflop output can be connected to the inputs of the slave flip-flop. Here slave flipflop's outputs can be connected to the inputs of the master flip flop.

In this type of flipflop, an inverter ip also used addition to two flipflops. The inverter connection can be done in such a way that where the inverted CLK pulse can be connected to the slave flipflop. In other terms, if CLK pulse in 0 for a master flipflop, then CLK pulse will be 1 or for a slave flipflop. Similarly, when CLK pulse in 1 for master flipflop, then CLK pulse will be 0 for slave flipflop.

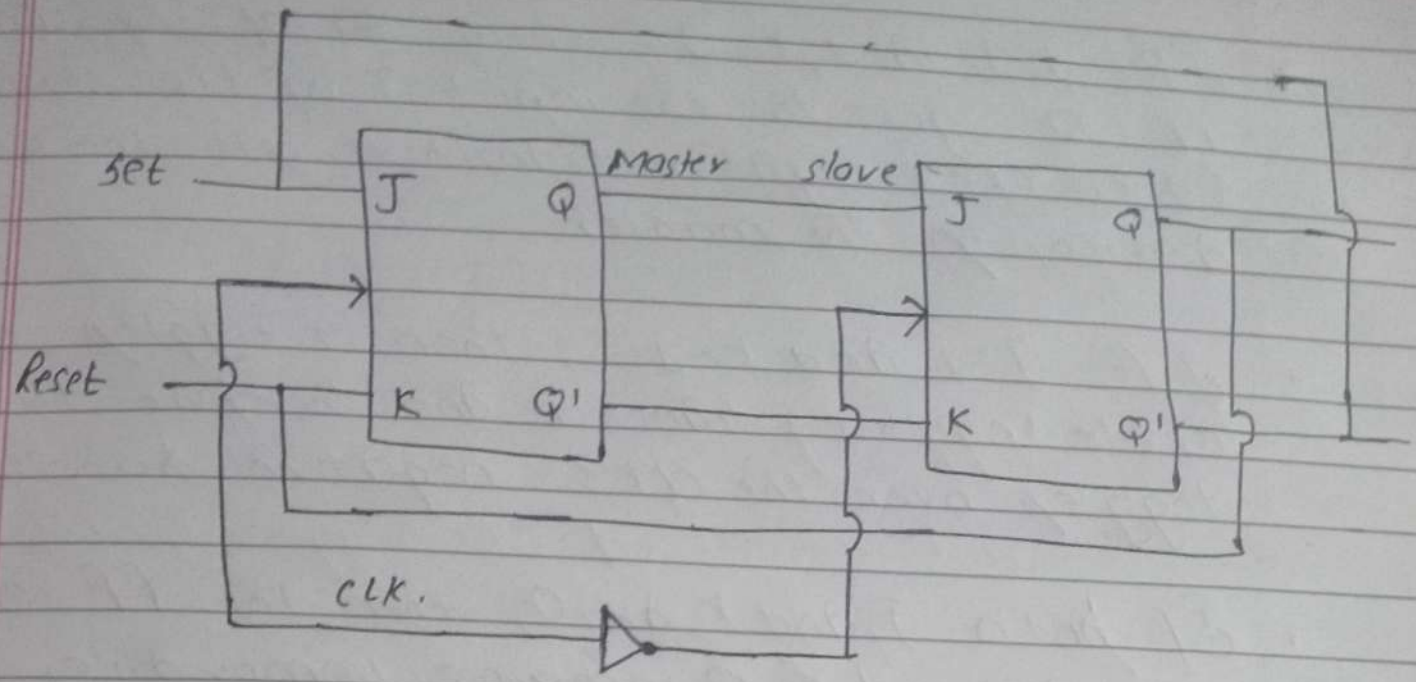


Fig: master - slave - flip - flop - circuit.

Master-slave flipflop working.

Whenever the CLK pulse goes to high which means 1, then the slave can separated; the inputs like J & K may change the condition of the system.

At first, the master ff will be triggered at a positive level whereas the slave ff will be triggered at a negative level. Due to this reason master ff responds first.

If J=0 & K=1, then the output of the master ff 'Q' goes to the input K of the slave ff and the CLK forces the slave ff to RST (reset) therefore the slave ff copies the master ff.

- If J=1 and K=0, then the of the master ff 'Q' goes to the input J of the slave ff & then clk's negative transition sets the slave ff and copies the master.
- If J=1 and K=1, then it toggles over the clk's positive transition and therefore the slave toggles over the clk's negative transition.
- If both J and K are 0, then the ff can be immobilized & Q remains unmovable.

Explain triggering.

In digital circuits, two methods of trigering are possible, namely edge triggering and level triggering, which ~~target~~ trigger that signal to switch from one state to the other.

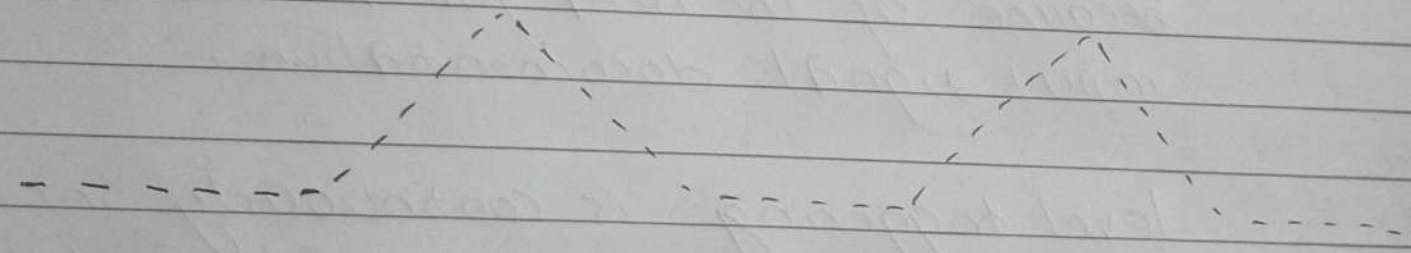
Edge triggering.

It is used wherever it is required to identify the transition in the state of the input signal from low to high or from high to low. It is commonly applied to synchronous circuits, including flip-flops and counters. More often, edge triggering is advantageous when high accuracy of timing is required.

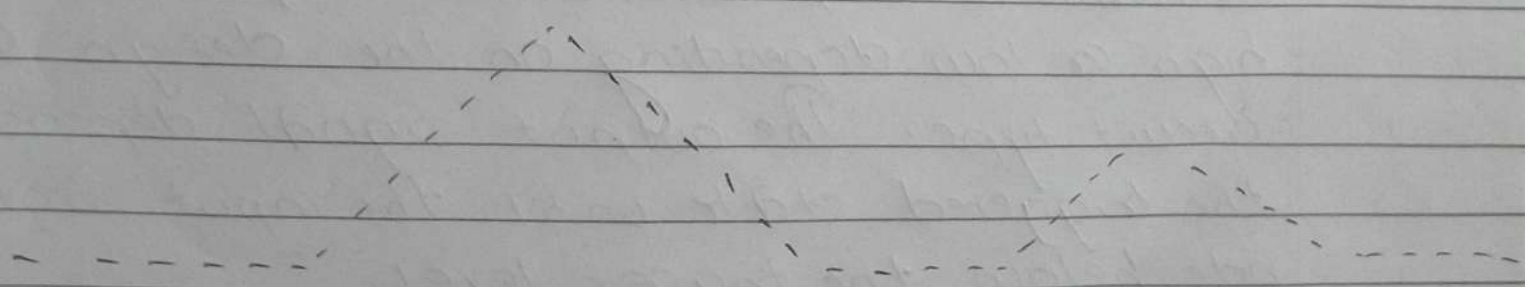
In edge triggering, the rapid change in the input signal that is sampled by the circuit's clock signal leads to a change in the signal. This edge, referred to as the ~~triggering~~ trigger edge of the pulse, may be rising, that is, from a low state to high, or falling, that is, from a high to low, depending on the circuit implementation. When the output signal crosses the trigger edge, the circuit changes the state of the output signal.

- Advantages of Edge triggering.

1) Precise timing
2) Reliability.



Fig; Positive Edge Trigger.



Fig; Negative Edge Trigger.

- Disadvantages of Edge triggering.

(a) Complex Design
(b) High sensitivity

2. Level Triggering.

It is a kind of triggering that determines a signal at a certain level rather than the change of its state. It gives some output when it is required to know the value of the signal at some point in time and not just a change in state. level triggering is commonly used in data acquisition and control systems because of the need for a constant level of input signal documentation.

level triggering is continuously included that checks for the input signal, and the output is produced when the input signal is at the determined level and above. This level can be high or low depending on the design of this circuit type. The output signal depends on the triggered state until the input signal descends below the trigger level.

- Advantages of level triggering.

(a) Continuous Monitoring.
(b) Simpler Circuit Design.

- Disadvantages of level triggering.

(a) less Precise.
(b) longer Trigger Duration.

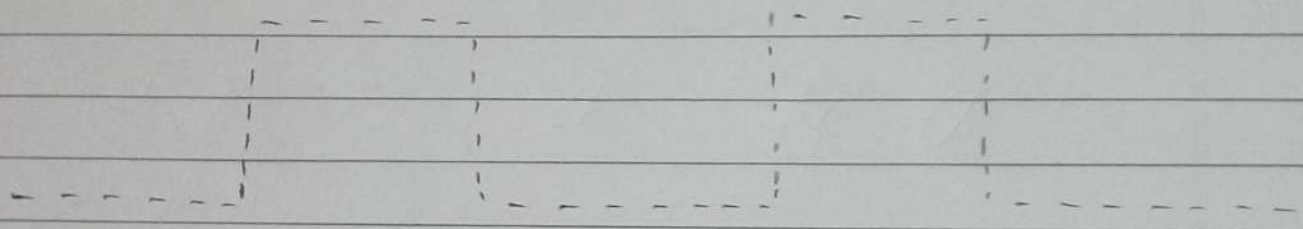


Fig: Positive level Trigger.

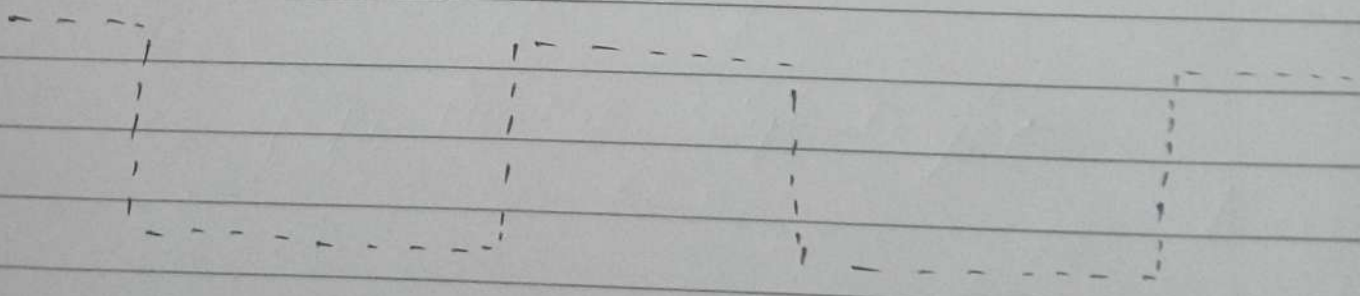


Fig: Negative level Trigger.