CS 2410 Project 1

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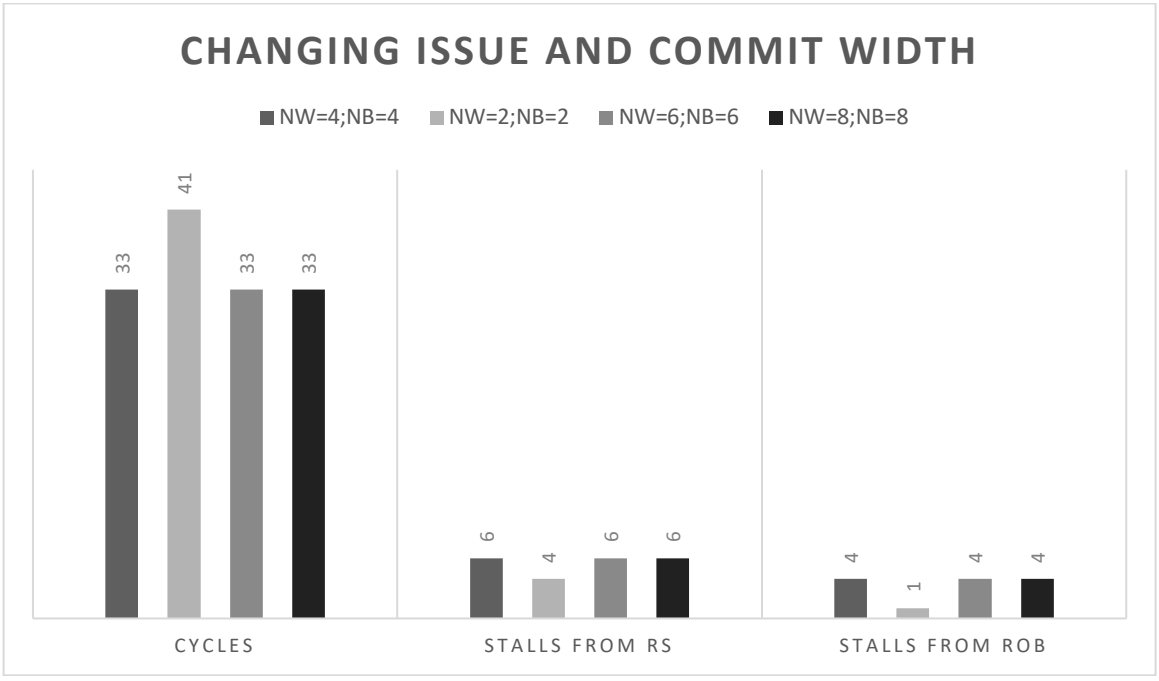
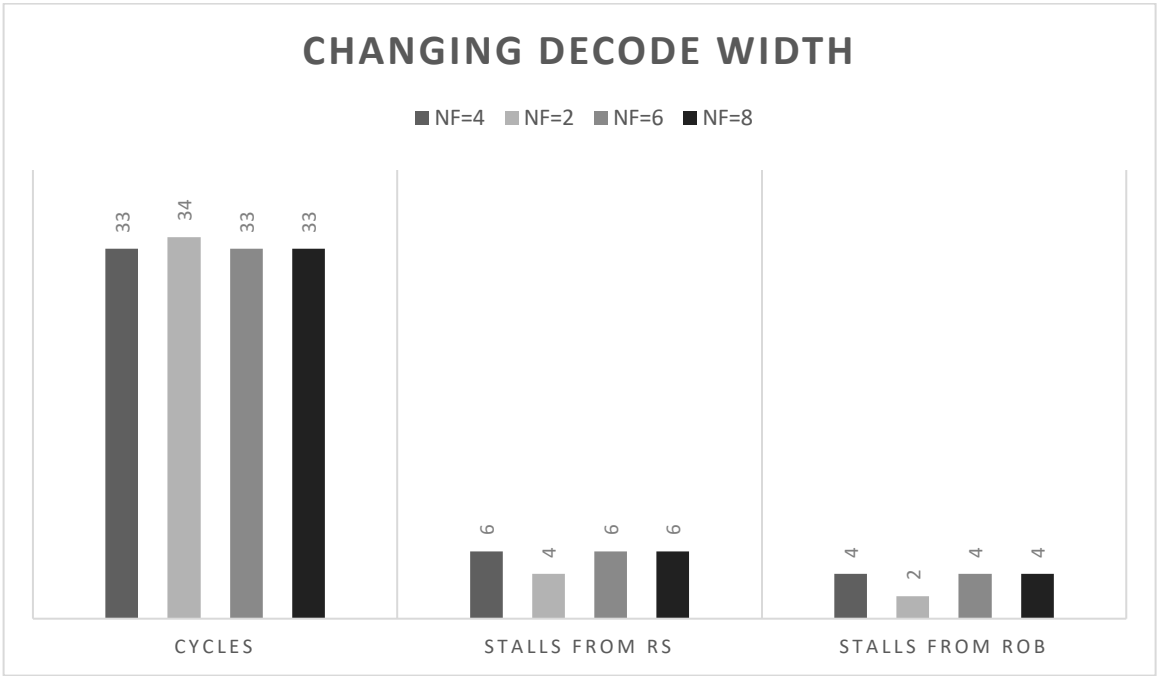
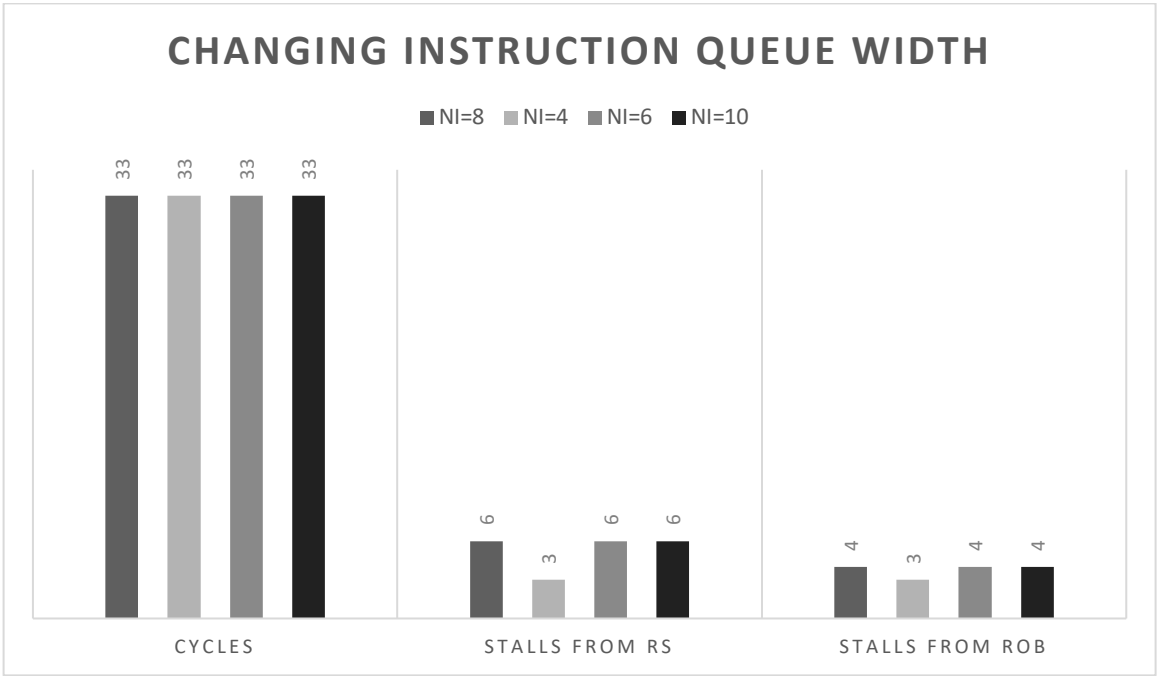
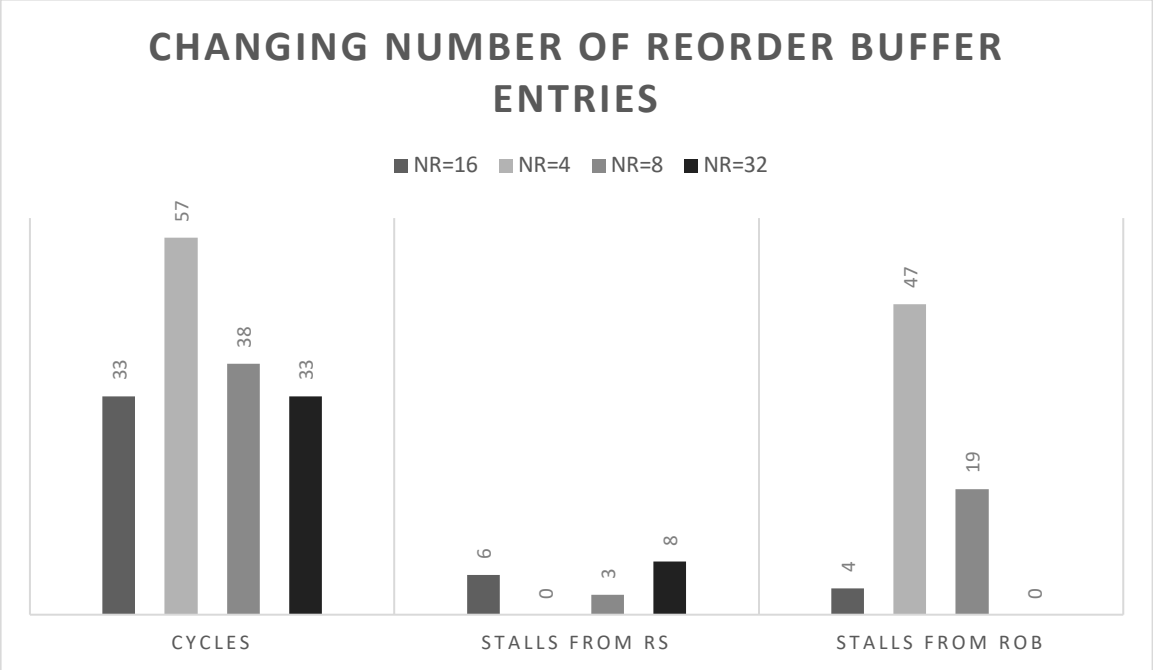
Test are run on the cluster oxygen.cs.pitt.edu

We tested our simulator with Test1.dat. Comparative analysis of NI, NW, NB, NF and NR is shown in figures below.




CHANGING DECODE WIDTH
NF=4
NF=2
NF=6
NF=8
33
34
33
33
6
4
6
6
4
2
4
4
CYCLES
STALLS FROM RS
STALLS FROM ROB

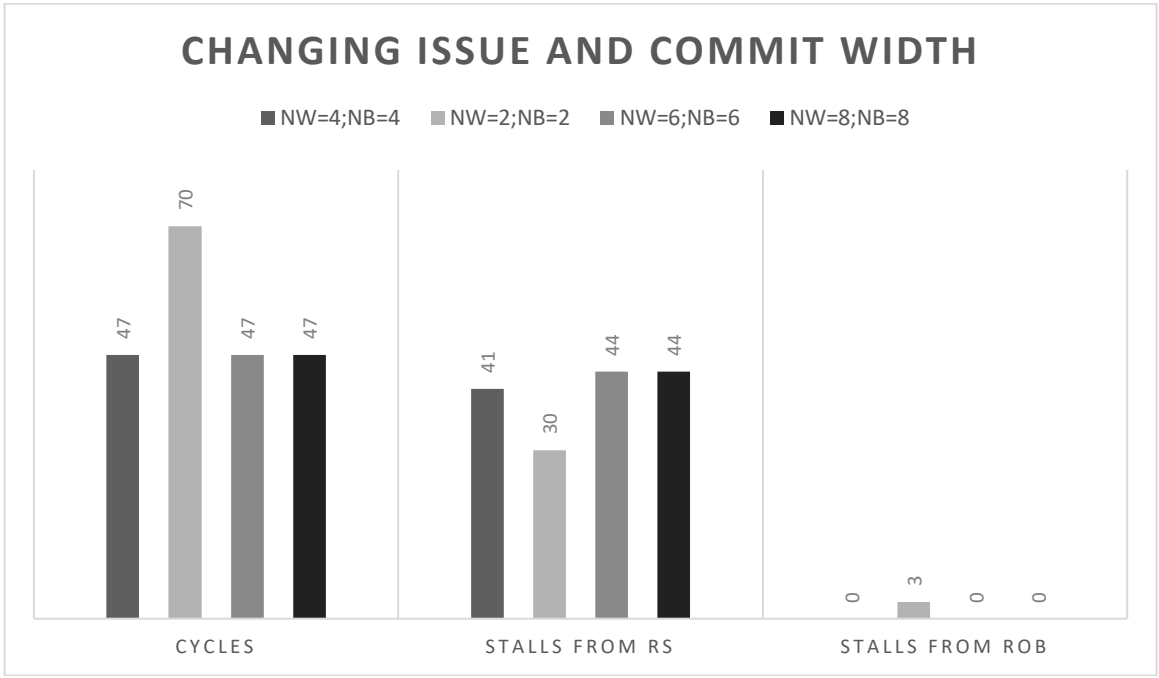

CHANGING INSTRUCTION QUEUE WIDTH
NI=8
NI=4
NI=6
NI=10
33
33
33
33
6
3
6
6
4
3
4
4
CYCLES
STALLS FROM RS
STALLS FROM ROB

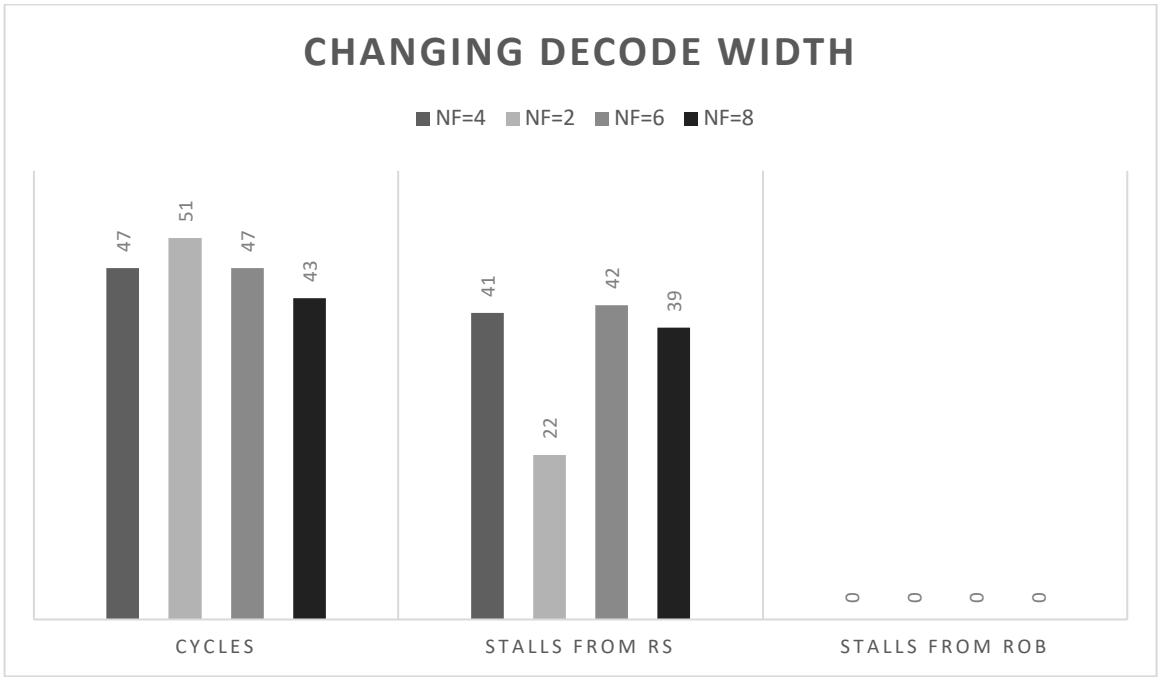


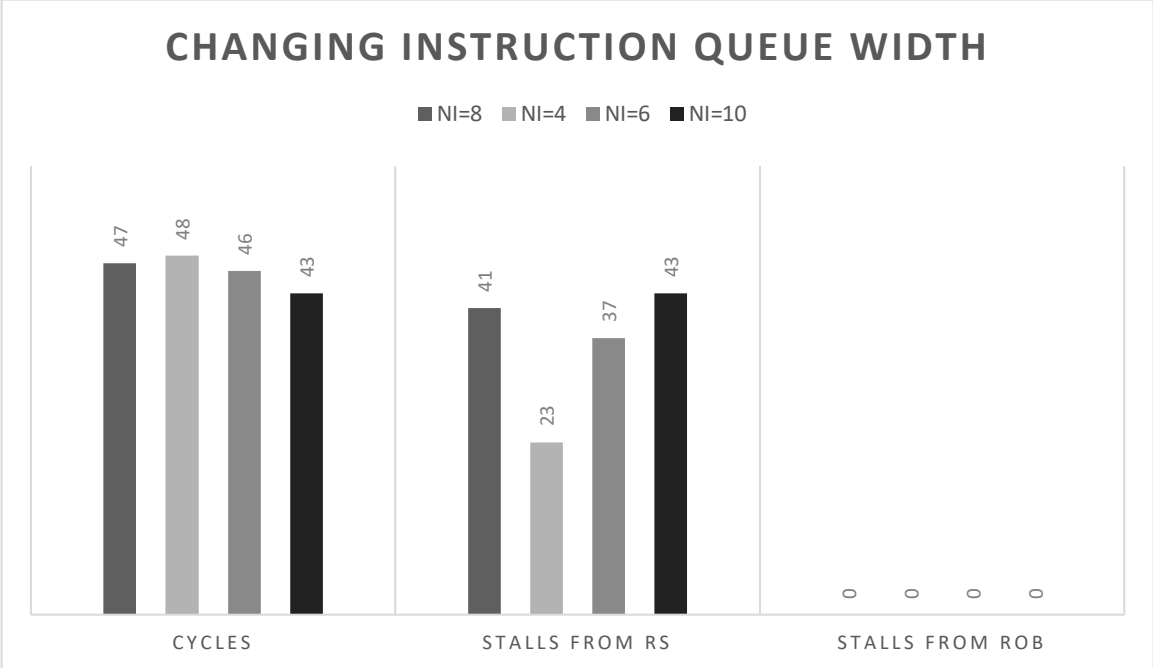
According to the comparative analysis above, we conclude that:

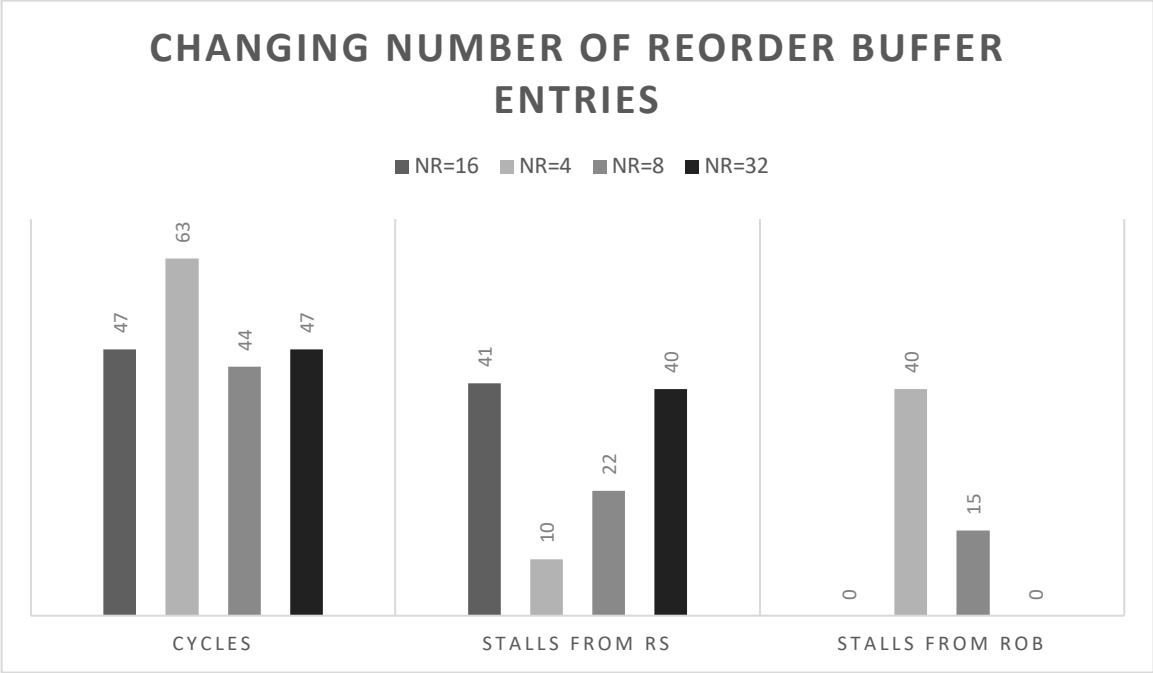
- Setting the issue and commit width equal to 4 is reasonable because if we set them less than 4 then the program will need more cycles to be completed and if we set them more than 4 then the total cycle remains.
- Neither fetch width nor instruction queue length is a bottleneck of the architecture.
- The length of reorder buffer is a bottleneck of the architecture, as shown in the figure with NR=4. Setting it to 16 is a good choice since setting NR to 32 doesn't help decreasing cycles.
- According to the basic configuration of these parameters, the average utilization of CDB is 43.000000 %, which shows that CDB is not the bottleneck when NB = 4. This is coherent with our experimentation before.

Part 2: SMT


CHANGING ISSUE AND COMMIT WIDTH
NW=4;NB=4
NW=2;NB=2
NW=6;NB=6
NW=8;NB=8
47
70
47
47
41
30
44
44
0
3
0
0
CYCLES
STALLS FROM RS
STALLS FROM ROB


CHANGING DECODE WIDTH
NF=4
NF=2
NF=6
NF=8
47
51
47
43
41
22
42
39
0
0
0
0
CYCLES
STALLS FROM RS
STALLS FROM ROB





Conclusion:

- If one thread, we need 33 cycles. In order to complete two test data in the same time, it should be 66. With SMT, it needs 47 for these two test data.
- Reservation station is the bottleneck of the architecture.