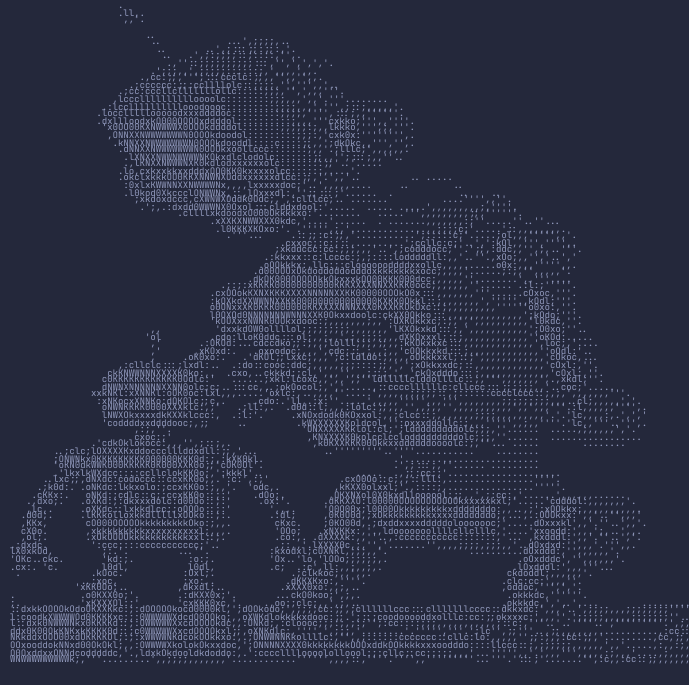


user@saahas-pc :~\$ neofetch --ascii\_colors 5 6 4



User	Saahas Yechuri
Location	San Francisco, CA
Contact	saahas@gatech.edu   484-983-4127
Links	github/Suputra   linkedin/saahas   youtube/@saahasY
Bio	Driven engineer working on the boundary between hardware and software. Experienced with designing and building mechatronic and robotic systems, building and scaling data analysis pipelines, and FPGA design. In my free time, I love to read (big fan of hard sci-fi and the future of humanity), bike, and hike!

\$ grep -A 2 "experience" ~/career.md | less

# Hardware/Software Engineer @ Zoox

Jan 2022 - Present | Foster City, CA

- > Designed and built a vehicle network emulator to simulate network traffic on real hardware. Developed hardware, firmware, and software for data collection, emulation, and validation.
- > Analyzed 100GB+ of vehicle network data using Python; extracted characteristics into 'streamdb' files that are now used company-wide for data flow analysis and network security investigations.
- > Designed a 4-layer passthrough board to inject errors into 100M/1G automotive Ethernet lines; matched BaseT impedance standards. Uncovered critical issues with missing data and fault detection.
- > Optimized network data analysis speed using the MapReduce paradigm and designed data pipelines for Zoox's compute cluster.
- > Utilized skills in hardware design, firmware development, software engineering (Python, C/C++), and network protocols to create the 'Network Systems Tester' (NST) emulator platform.
- > Designed Test setups and Test Cases to verify the whole Time Synchronization system on Vehicle - including the Grandleader, Boundary Clocks, and Endpoints. This involved creative test setups, packet analysis, and experimentation with plotting / data analysis.
- > Maintain scripts that verify functionality of Telecommunications and Time Synchronization on the manufacturing line.

# Undergraduate Researcher @ Bio-Robotics Lab

Aug 2022 - Sep 2023 | Atlanta, GA

- > Developed FPGA-based hardware accelerators for Homomorphic Encryption on a Xilinx Zynq ZC702, focusing on key generation, encryption, and large integer arithmetic. Created a novel key-switching scheme for faster homomorphic operations.
- > Designed and optimized Verilog modules, including an implementation of the Miller-Rabin primality test, pseudorandom number generators based on LFSRs, and efficient modular exponentiators.
- > Interfaced FPGA fabric with Zynq PS using AXI IP cores and C code. Integrated ADC modules to process real-world sensor data securely.
- > Extensively debugged and validated designs using Xilinx Vivado's Simulation Suite and Integrated Logic Analyzer (ILA) on both simulated and real hardware.

# Student Assistant @ STEM@GTRI

June 2021 - July 2021 | Atlanta, GA

- > Mentored 10 Students in the development of an autonomous robotic arm with computer vision and high level control.
- > Started from basic Python lessons, and got all the way to control using DH-parameters, Finite State Machines, and Computer Vision.
- > Wrote 25+ example scripts and 15+ lessons to help facilitate student understanding of various topics.
- > Wrote a ROS package to integrate computer vision, inverse kinematics, and control into a simple template stack for the students.

# R&D Engineering Intern @ nth Solutions LLC

Feb 2018 - Aug 2019 | Exton, PA

- > 3D Modeled and printed parts for a variety of applications, including product enclosures, accessories, and test rigs. Designed and maintained 25+ 3D printed models, each with 10+ iterations.
- > Wrote documentation and drew diagrams for patents. Experienced with technical writing and research.
- > Programmed and range tested ESP8266 and LoRa modules to add IoT functionality to a pre-existing product.

\$ skills list --format=compact | bat -p --style=grid

Programming	Domain Knowledge	Tools & Software
Python [██████████] E	Networking & OSI [██████████] A	Hardware Design [██████████] A
C [██████████] A	TCP/IP Stack [██████████] I	Vivado/Vitis [██████████] I
C++ [██████████] I	Ethernet LL-4 [██████████] I	Altium [██████████] I
Verilog [██████████] I	PTP/NTP [██████████] I	Simulation [██████████] I
CUDA [██████████] I	DDS [██████████] I	MATLAB/Simulink [██████████] I
Javascript [██████████] I	Robotics & Control [██████████] I	GTKWave [██████████] I
Julia [██████████] I	IK/FK [██████████] I	Isaac Lab/Sim [██████████] I
Scala [██████████] I	D-H Parameters [██████████] I	CAD/CAM [██████████] I
ROS [██████████] I	PID Control [██████████] I	Inventor [██████████] I
Linux/Unix [██████████] A	RL for Control [██████████] I	SolidWorks [██████████] I
bash [██████████] A	Computer Vision [██████████] I	Onshape [██████████] I
bazel [██████████] A	Calibration [██████████] I	
OpenCV [██████████] I	CNNs [██████████] I	
PyTorch [██████████] I	SLAM [██████████] I	
Polars [██████████] A	Data Processing [██████████] I	
Matplotlib [██████████] E	MapReduce [██████████] I	
SciPy [██████████] I	Distributed Systems [██████████] I	
Numpy [██████████] E		

\$ tree ~/projects --charset=ascii -L 3

```
/projects
├── FPGA Based Ethernet MAC/PHY
│   ├── description.txt
│   └── Designed and Tested Verilog modules for a Simple 10BaseT MAC and PHY following IEEE 802.3 to transmit fixed Layer 2 Ethernet packets. Debugged and Tested using Verilator and gtkwave. Working on expanding to Layer 3+
├── Chess Robot
│   ├── description.txt
│   └── Using an old 3d printer frame, built a chess robot. Designed motor control circuits, wrote Firmware for low level control, and code for move detection using fiducial markers (AprilTags) and generation. Demo videos on Youtube.
└── Gyro-Boat
    ├── description.txt
    └── Built a model boat stabilized by a gyroscope, inspired by Sperry's Gyro-Stabilizer. Demo videos on Youtube.
```

3 directories, 6 files

\$ cat ~/awards | column -t -s ';' | sed '1,2s/./-/g'

Awards & Recognition			
Year	Award	Organization	Details
2024	Hack for Social Impact (1st Place)	UNCCD	Developed "Arboren" to help UN analysts visualize and analyze desertification data. Presented at COP 16 in Riyadh.
2023	SII2024 Conference Paper	IEEE	FPGA-based sensor encryption system paper accepted to Symposium on System Integration in Ha Long Bay, Vietnam.
2022	President's Undergraduate Research Award (PURA)	Georgia Tech	Funded to do research on Homomorphic Encryption with FPGAs. Mentored a student on FPGA development, and presented findings at a research symposium.
2021	NASA SpaceApps Best Use of Technology	NASA	Developed novel space component separation system, used electromagnetic and hydraulic principles to apply a 16kN preload.
2020	MIT COVID-19 Challenge Winning Team	MIT	Created "COValert" SMS chatbot for rural COVID triage for areas without internet access.

\$ ssh guest@uspto ls -l ~/patents | grep -l "Saahas Yechuri" | bat --style=grid

File: US-11287348-B2.pdf
<b>Tire Balance Measurement:</b> Apparatus for measuring imbalance forces of a tire/hub assembly of a vehicle during motion of the vehicle (Issued Mar 29, 2022)
File: US-10701266-B2.pdf
<b>Video File Reader:</b> Method for reading out contents of a video file having a predefined video file format (Issued Jun 30, 2020)
File: US-10469750-B1.pdf
<b>Motion Data Embedding:</b> Method for embedding motion data of an object into a video file to allow for synchronized visualization of the motion data (Issued Nov 5, 2019)
File: US-10284752-B1.pdf
<b>Video-IMU Synchronization:</b> Method for determining a start offset between a video recording device and an inertial measurement unit (Issued May 7, 2019)

\$ cat education.yml

```
institution: Georgia Institute of Technology
degree: BS in Mechanical Engineering
gpa: 4.0
coursework:
  - Control of Dynamic Systems
  - Robotics
  - Mechatronics
  - Machine Design
  - System Dynamics
  - Thermal and Fluids Laboratory
  - Experimental Methods
  - Heat Transfer
  - Fluid Mechanics
  - Thermodynamics
  - Numerical Methods
  - Deformable Bodies
  - Dynamics
  - Statics
  - Digital/Analog Circuits
```