The University of Texas at Dallas

VLSI Design

Project 6

EECT 6325

20-Bit ALU

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

20 Bit Arithmetic Logic Unit

1. Description:

Arithmetic and logic unit is a digital circuit used to perform arithmetic and logic operations. It was first realized by John Von Neumann [1].

It performs arithmetic operations such as addition, subtraction, multiplication etc., It also performs logic operations such as AND, OR, NOT, XOR etc.,

The main use of ALU is its implementation in CPU of a computer [1]. It can perform both simple and complex operations. The various operations implemented are:

- Addition: Adds two numbers
- Subtraction: Subtracts one number from the other
- Multiplication: Multiplies two numbers
- MAC: Multiplies and accumulates the result
- OR: Performs logical OR of two inputs
- AND: Performs logical AND of two inputs
- NOT: Performs logical NOT of first input
- XOR: Performs logical XOR of two inputs
- Left shift: Shifts the first operand to the left by the number of places specified by the second operand
- Right shift: Shifts the first operand to the right by the number of places specified by the second operand
- Compare: The two operands are compared and the output is given as follows
    - If first operand is greater, output is 1
    - If second operand is greater, output is 2
    - If the two operands are equal, output is 3
- Palindrome: If the two numbers are palindrome of each other i.e., one number is the reverse of the other, then the output is 1, else it is zero
- Reduction AND: AND operation is performed on successive bits of the first operand
- Reduction OR: OR operation is performed on successive bits of the first operand
- Reduction XOR: XOR operation is performed on successive bits of the first operand
- NOR: Performs logical NOR of the 2 inputs
- NAND: Performs logical NAND of the 2 inputs

- XNOR: Performs logical XNOR of the 2 inputs
- Binary to gray conversion: The binary values are converted to gray scale through XOR operations
- Subtraction using 2's complement
- Negation of second input

In our design of ALU, the inputs 'a' and 'b' are 20 bit wide and the output 'out' is 40 bit. The operations are performed based on another input signal 'sel' during the edge of the clock signal transition. The width of the output signal is chosen to be double that of the input, to make room for the multiplication operation. As an example, the inputs are taken as a=18 and b=3. Table 1 summarizes the operations and corresponding outputs.

Sel value	Operation	O/p in decimal	O/p in binary
1	Addition	21	00…0010101
2	Subtraction	15	00…0001111
3	Multiplication	54	00…0110110
4	MAC	72	00…1001000
5	OR	19	00…0010011
6	AND	2	00…0000010
7	NOT	1099511627757	11…1101101
8	XOR	17	00…1110001
9	Left shift	144	00…10010000
10	Right shift	2	00…0000010
11	Compare	1	00…0000001
12	Palindrome	0	00…0000000
13	Reduction And	0	00…0000000
14	Reduction Or	1	00…0000001
15	Reduction Xor	0	00…0000000
16	NOR	1099511627756	11…1101100
17	NAND	1099511627773	11…1111101
18	XNOR	1099511627758	11…1101110
19	Binary to gray	27	00…0011011
20	Subtraction using 2's complement	15	00…0001111
21	Negation of 'b'	1099511627772	11…1111100
Default	-	0	00…0000000

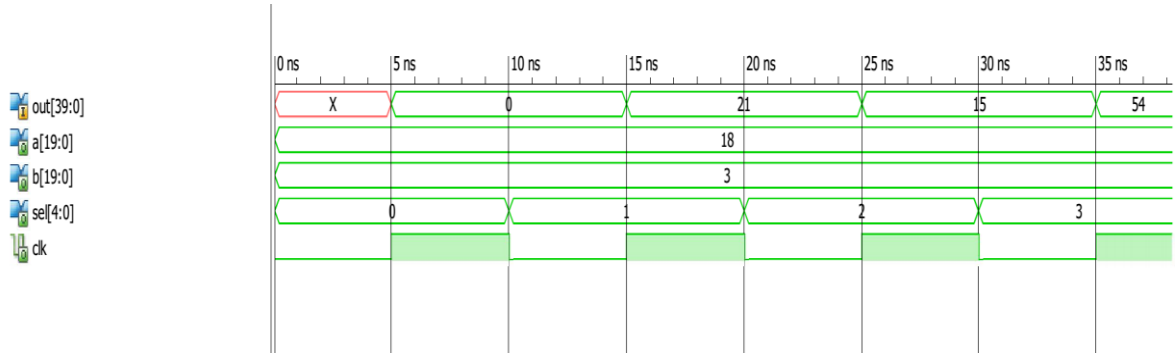
Table 1 ALU Operations

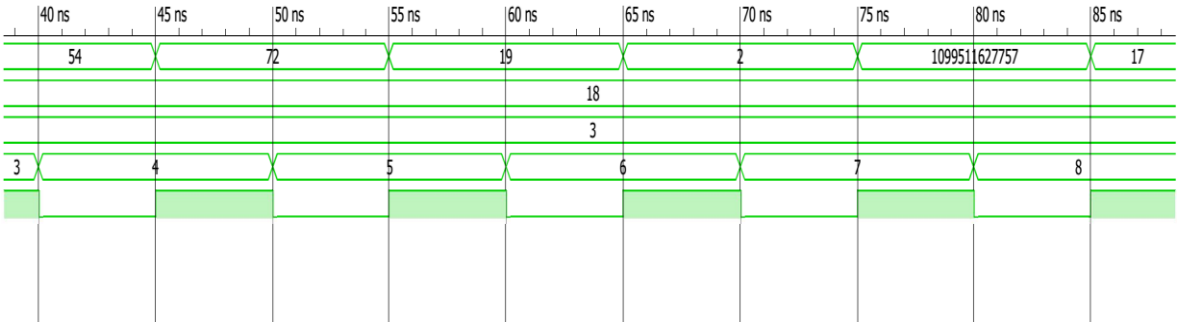
2. Design trade-offs:

- The width of the n-MOS and p-MOS are chosen in such a way as to get optimum Energy-delay product. However the width can be decreased furthermore but with a trade-off with the high EDP.
- While laying out the cells, the minimum distance between the external pin and the GR logic has to be 0.24um. However, in order to avoid the Design rule check error of distance between the RX and GRlogic(min of 0.1um), the GRLogic was extended according to the scale of 0.24+0.48*n, which increased the area of each cell.
- In order to minimize the number of diffusion breaks in individual cells of mux2 and D-flip flop, the height of the cells were increased which was a trade-off between number of breaks and area.

3. Simulation:

A Verilog code was written to describe the above functionalities and tested using a test bench code to obtain the below 5 graphs.





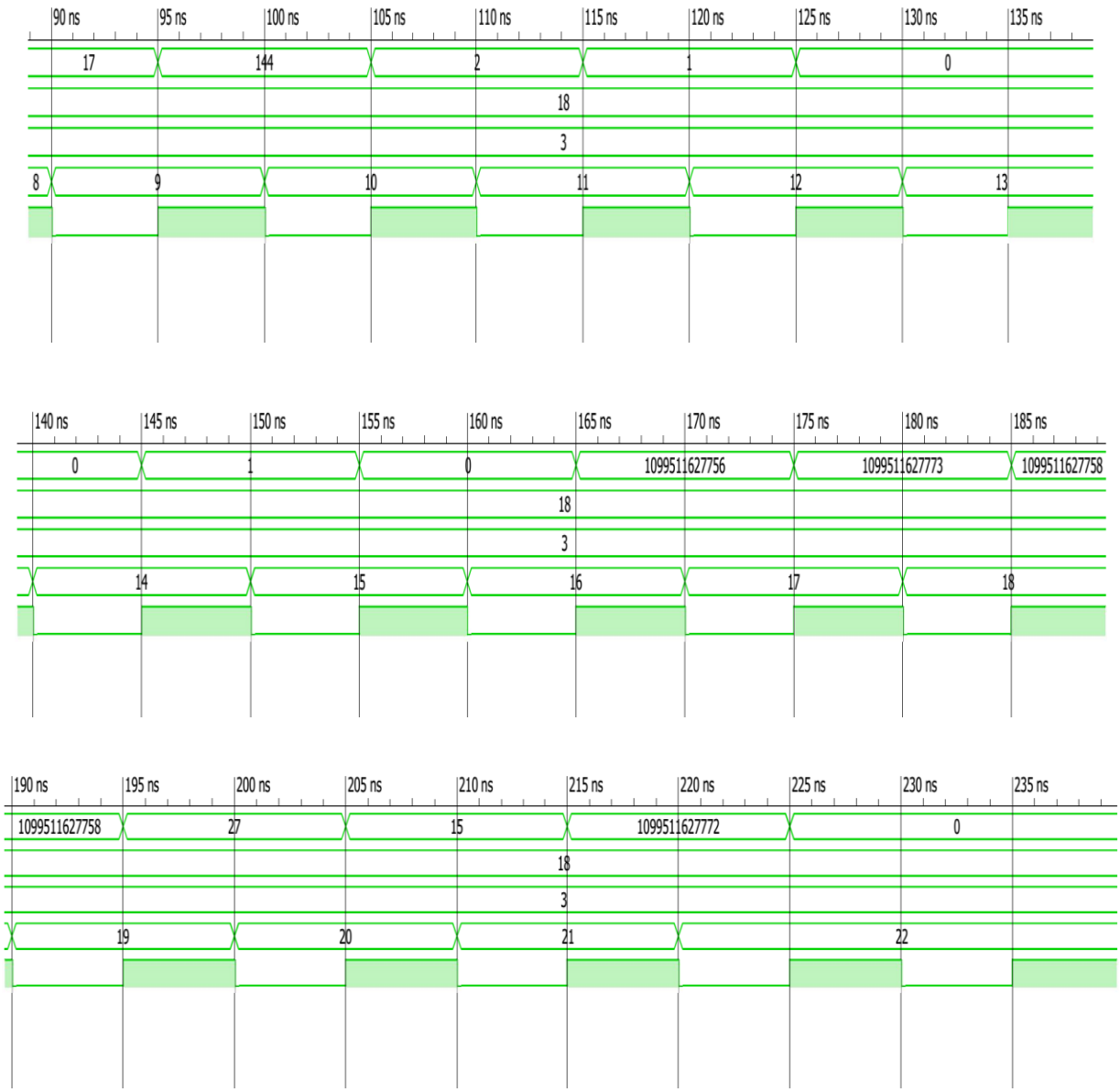


Figure 1 Simulation waveform of original code

The layouts of 8 cells were used to characterize the library. That .lib file was converted to .db file using design vision and the netlist for the Verilog code was regenerated using our library. The sample netlist is as shown below:

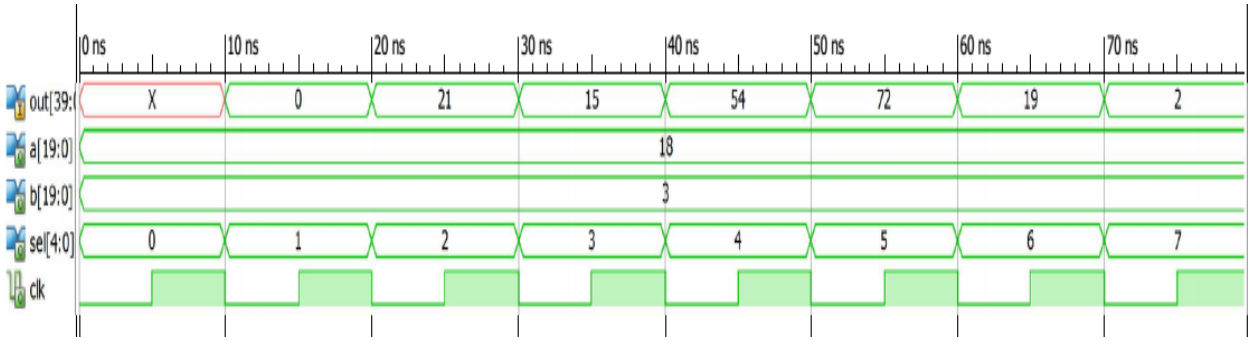
```
module alu_161 ( a, b, sel, clk, out );
  input [19:0] a;
  input [19:0] b;
  input [4:0] sel;
  output [39:0] out;
  input clk;
  wire   N45, N46, N180, N181, N222, N223, N426, N428, N429, N430, N431, N509,
       N510, N591, N592, N611, N612, N613, N614, N615, N616, N617, N618,
       N619, N620, N621, N622, N623, N624, N625, N626, N627, N628, N629,
       N630, n751, n752, n753, n754, n755, n756, n757, n758, n759, n760,
       n761, n762, n763, n764, n765, n766, n767, n768, n771, n772, n773,…….
```

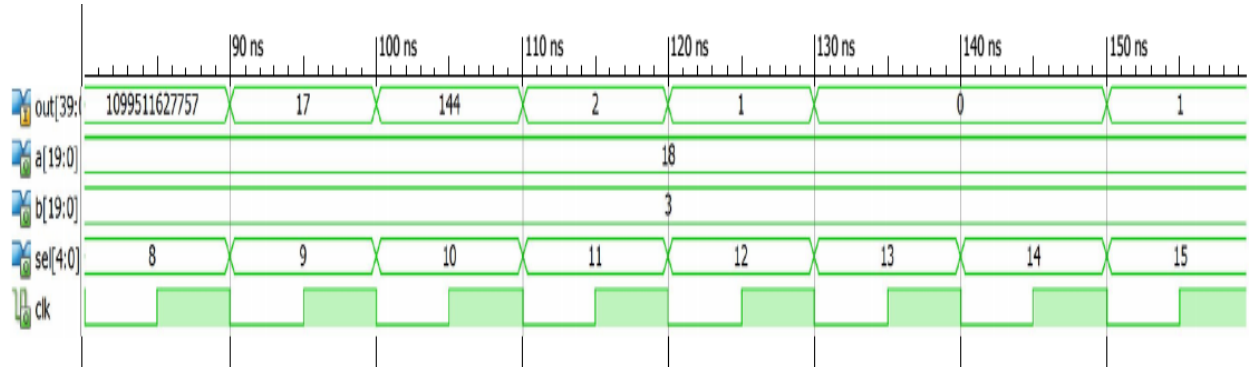
The cell list is as below:

Cell	Reference	Library	Area	Attributes
U727	xor2	op_cond	27.959999	mo
U728	xor2	op_cond	27.959999	mo
U729	xor2	op_cond	27.959999	mo
.				
.				
sll_57/M1_5_36	mux2	op_cond	34.939999	mo
sll_57/M1_5_37	mux2	op_cond	34.939999	mo
sll_57/M1_5_38	mux2	op_cond	34.939999	mo
sll_57/M1_5_39	mux2	op_cond	34.939999	mo
Total 4326 cells			98171.926731	

***** End Of Report *****

The netlist was tested using a testbench to obtain the below 3 graphs. It can be noted that the output here is obtained at the negative edge of the clock.





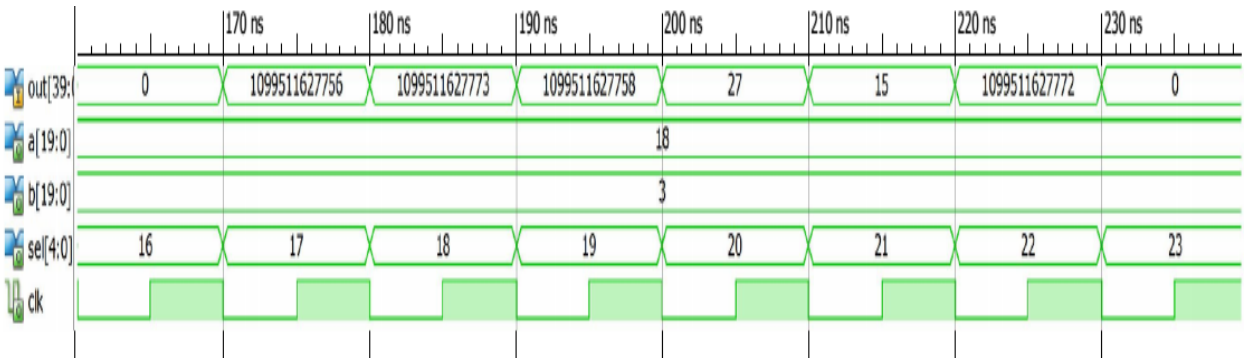


Figure 2 Simulation using our library

4. Abstract and LEF generation

A new layout for the 'filler' was created (Figure 3)without any I/O pins, with the height matched to the rest of the cells.

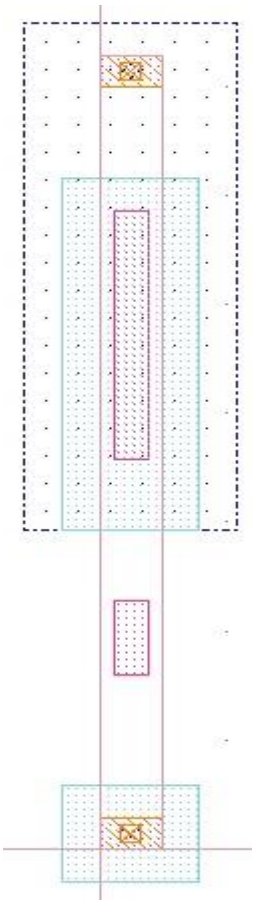
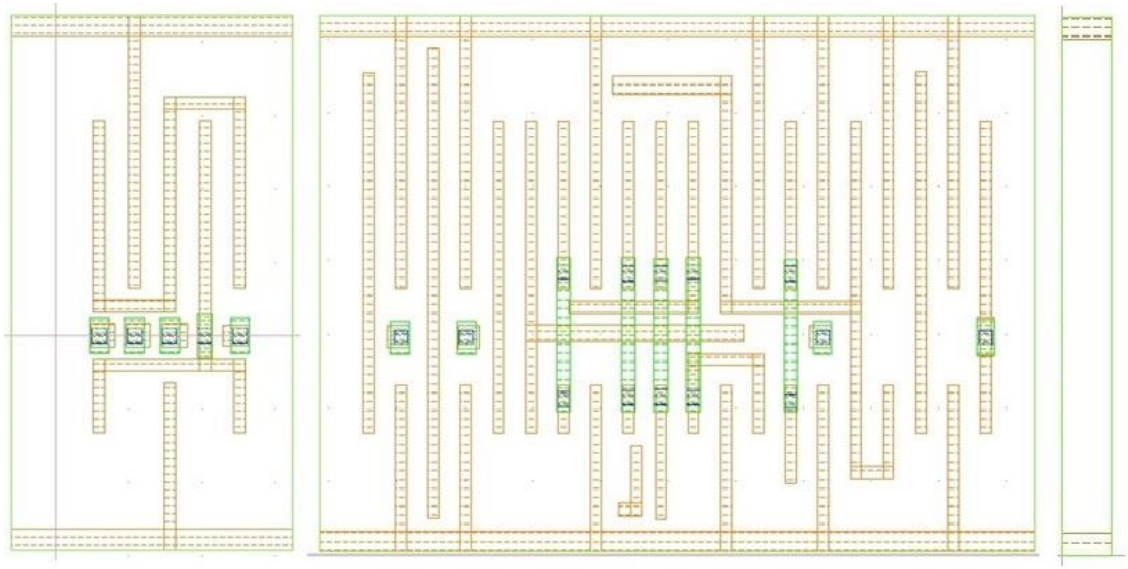
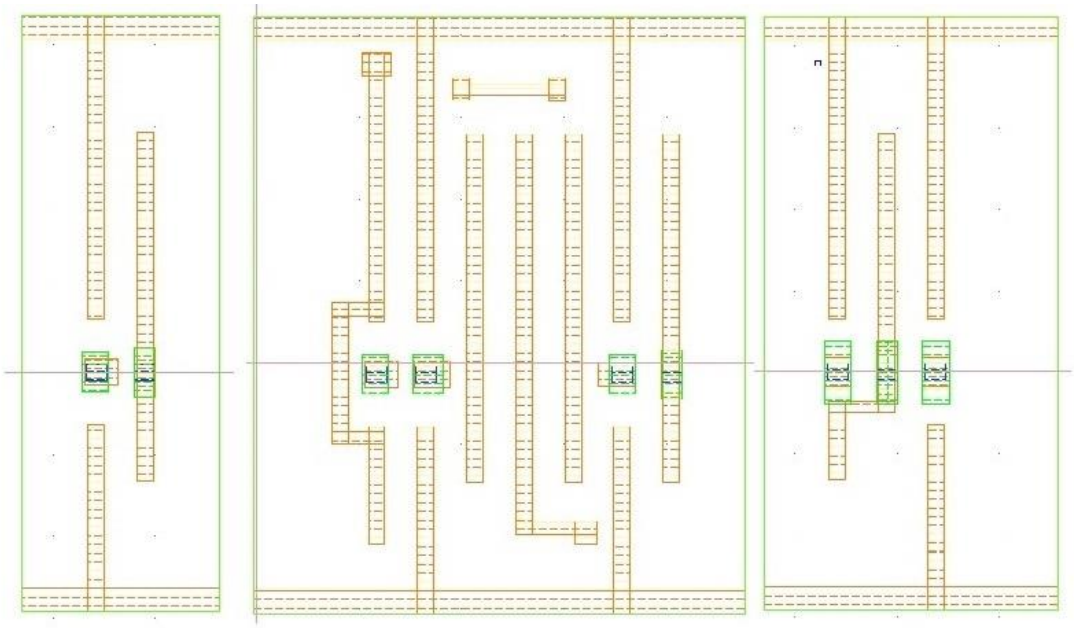


Figure 3 Filler layout

An abstract was created for each of the cells including filler. The abstracts are as shown below in figure 4.



aoi22 D flip flop filler



inverter mux2 nand2

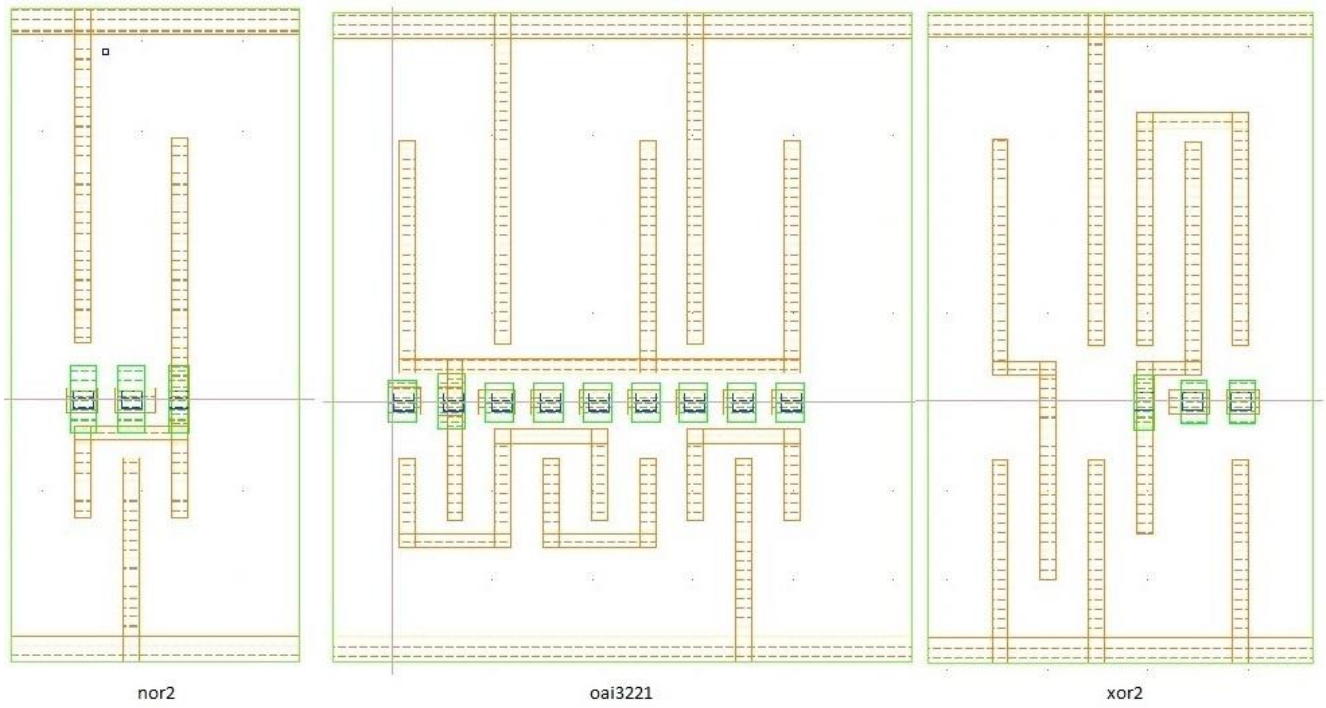


Figure 4 Abstracts

A LEF file was created and exported from cadence using our library. In this case, library proj6. A ASCII dump file named proj6_dump.asc was created from the LEF file. PERL script was run to convert the LEF file to Encounter readable version as proj6_out.lef.

5. Automatic routing and placement:

Using Encounter tool of Siliconsmart, the Verilog file and the output LEF files are imported. Floor planning, placement of standard cells, placement of fillers, supplying the power rings and stripes and routing is performed. The I/O metal pins are matched and the design is saved as a DEF file.

Using cadence, the DEF file is imported and the layout is obtained. The final layout of 20 bit ALU is as shown in the figure 5. This layout is checked for DRC errors.

The Verilog file is imported and the schematic is obtained as shown in figure 6. The schematic is checked for LVS errors. The symbol is shown in figure 7.

The windows showing DRC and LVS is in figure 8.

Figure 5 Layout of ALU

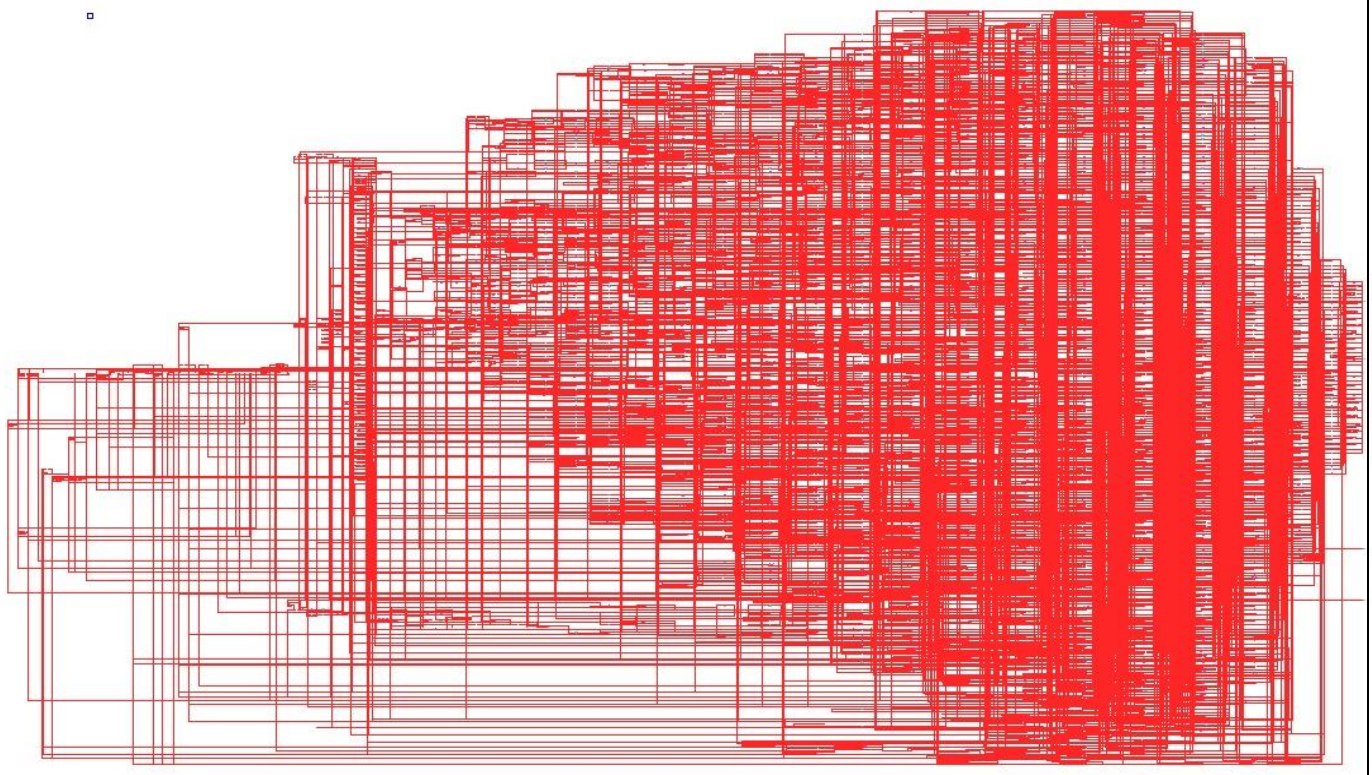


Figure 6 Schematic

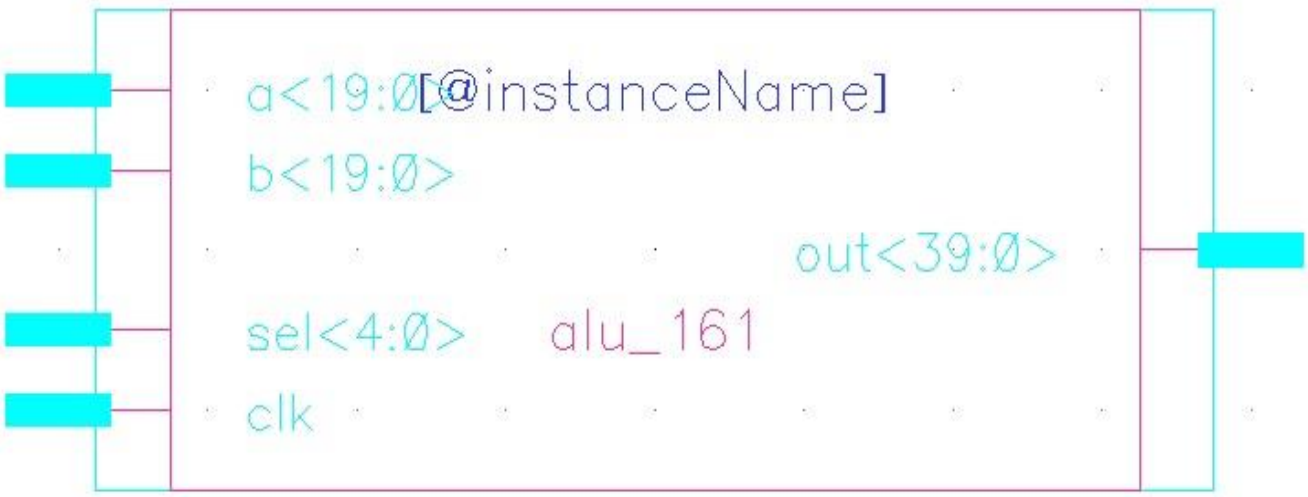


Figure 7 Symbol

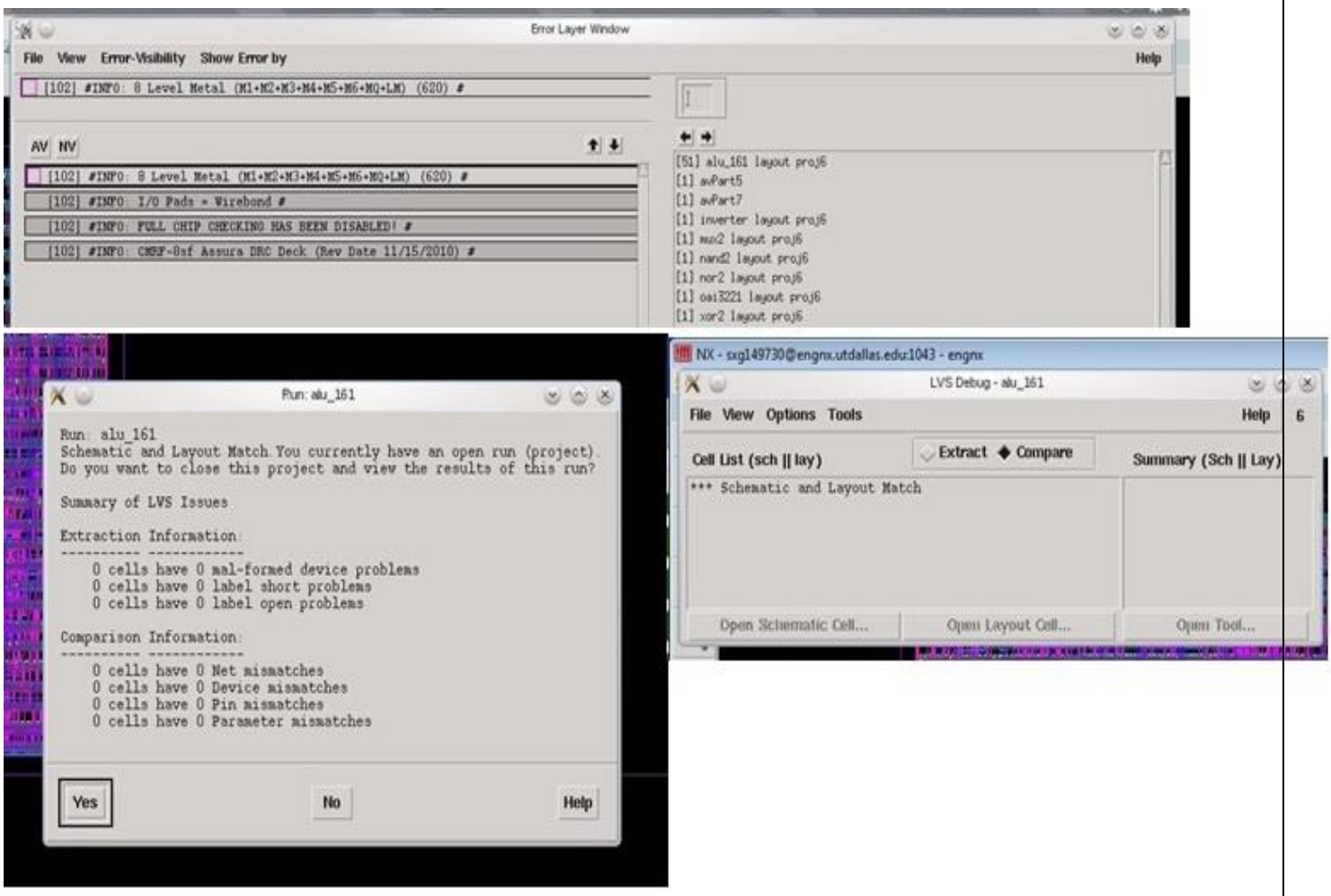


Figure 8 DRC and LVS error windows

6. Static timing analysis:

It was done using Primetime. The Verilog file and the primetime.script files were used to generate the report for area and maximum delay. The file 'Variables1' was changed as below:

set library_file "op_cond.db"
set 13erilog_file "alu_161_syn.v"
set input_transition 65
set load 25
set driving_cell "inverter"
set clock_pin_name "clk"
set clock_period 60
set reset_pin_name "r"

The maximum delay is obtained to be 20.97ns and the slack is not obtained, since we have only D-flip flop connected to the output register. The power is obtained to be 1.88mW.

Primetime report:

PrimeTime I
Version I-2013.12-SP3 for suse64 – Apr 17, 2014
Copyright I 1988-2014 Synopsys, Inc.
ALL RIGHTS RESERVED

This program is proprietary and confidential information of Synopsys, Inc.
and may be used and disclosed only as authorized in a license agreement
controlling such use and disclosure.
Define search path 13erilog file and library and variables

set search_path "* ~/cad/primetime"
* ~/cad/primetime
source variables1
r
r
link library

set link_library $library_file
op_cond.db
set target_library $library_file
op_cond.db
#set link_library [list $library_file]
#set target_library [list $library_file]

```
# link design
remove_design –all
Error: Nothing matched for designs: there are none loaded (SEL-005)
0
read_verilog $verilog_file
Loading 14erilog file '/home/eng/s/sxg149730/cad/primetime/alu_161_syn.v'
1
# Define IO parameters
set_driving_cell –lib_cell $driving_cell –input_transition_rise $input_transition –input_transition_fall
$input_transition [all_inputs]
Loading db file '/home/eng/s/sxg149730/cad/primetime/op_cond.db'
Linking design alu_161...
1
set_load $load [all_outputs]
1
#define the clock – for comb circuit we may not need to use any clock
create_clock –name clk –period $clock_period [get_ports $clock_pin_name]
1
set_clock_transition –rise –max $input_transition [get_clocks clk]
1
set_clock_transition –fall –max $input_transition [get_clocks clk]
1
# set condition
set timing_slew_propagation_mode worst_slew
worst_slew
set timing_report_unconstrained_paths true
true
set power_enable_analysis true
true
set_disable_timing [get_ports $reset_pin_name]
Warning: No port objects matched 'r' (SEL-004)
Error: Nothing matched for ports (SEL-005)
Error: Nothing matched for object_list (SEL-005)
0
# analyze delay and power
check_timing
Warning: Some timing arcs have been disabled for breaking timing loops
        or because of constant propagation. Use the 'report_disable_timing'
        command to get the list of these disabled timing arcs. (PTE-003)
Information: Checking 'no_input_delay'.
```

Information: Checking 'no_driving_cell'.
Information: Checking 'unconstrained_endpoints'.
Warning: There are 80 endpoints which are not constrained for maximum delay.

Information: Checking 'unexpandable_clocks'.
Information: Checking 'latch_fanout'.
Information: Checking 'no_clock'.
Information: Checking 'partial_input_delay'.
Information: Checking 'generic'.
Information: Checking 'loops'.
Information: Checking 'generated_clocks'.
Information: Checking 'pulse_clock_non_pulse_clock_merge'.
Information: Checking 'pll_configuration'.
0
update_timing
1
report_timing –transition_time –to out_reg[39]/d

Report : timing
-path_type full
-delay_type max
-max_paths 1
-transition_time
-sort_by slack
Design : alu_161
Version: I-2013.12-SP3
Date : Tue Dec 9 12:17:07 2014

Startpoint: sel[0] (input port)
Endpoint: out_reg[39]
(falling edge-triggered flip-flop clocked by clk')
Path Group: (none)
Path Type: max

Point	Trans	Incr	Path
input external delay		0.00	0.00 r
sel[0] (in)	12.67	11.67	11.67 r
U811/vout (nor2)	1.96	1.76	13.43 f
U4899/out (inverter)	0.47	0.50	13.94 r
U4898/out (nand2)	0.19	0.25	14.19 f
U4897/out (inverter)	0.21	0.22	14.41 r

U4889/out (nand2)	0.08	0.10	14.51	f
U4881/out (aoi22)	0.90	0.09	14.60	r
U4880/vout (xor2)	0.40	0.27	14.88	f
U4863/out (inverter)	0.09	0.09	14.97	r
U4862/out (nand2)	0.25	0.06	15.03	f
U4861/out (aoi22)	0.22	0.15	15.19	r
U3225/out (nand2)	0.08	0.10	15.29	f
U3224/out (aoi22)	0.23	0.10	15.38	r
U3212/out (nand2)	0.08	0.10	15.49	f
U3210/out (aoi22)	0.22	0.10	15.58	r
U3198/out (nand2)	0.08	0.10	15.69	f
U3196/out (aoi22)	0.24	0.10	15.78	r
U3185/out (nand2)	0.08	0.11	15.89	f
U3183/out (aoi22)	0.24	0.10	15.99	r
U3172/out (nand2)	0.08	0.11	16.09	f
U3170/out (aoi22)	0.24	0.10	16.19	r
U3159/out (nand2)	0.08	0.11	16.30	f
U3157/out (aoi22)	0.24	0.10	16.40	r
U3145/out (nand2)	0.08	0.11	16.50	f
U3143/out (aoi22)	0.24	0.10	16.60	r
U3131/out (nand2)	0.08	0.11	16.71	f
U3129/out (aoi22)	0.24	0.10	16.81	r
U3117/out (nand2)	0.08	0.11	16.91	f
U3115/out (aoi22)	0.24	0.10	17.01	r
U3102/out (nand2)	0.08	0.11	17.12	f
U3100/out (aoi22)	0.24	0.10	17.22	r
U3088/out (nand2)	0.08	0.11	17.33	f
U3086/out (aoi22)	0.24	0.10	17.42	r
U3074/out (nand2)	0.08	0.11	17.53	f
U3072/out (aoi22)	0.24	0.10	17.63	r
U3061/out (nand2)	0.08	0.11	17.73	f
U3059/out (aoi22)	0.24	0.10	17.83	r
U3047/out (nand2)	0.08	0.11	17.94	f
U3045/out (aoi22)	0.24	0.10	18.04	r
U3034/out (nand2)	0.08	0.11	18.14	f
U3032/out (aoi22)	0.24	0.10	18.24	r
U3020/out (nand2)	0.08	0.11	18.35	f
U3018/out (aoi22)	0.24	0.10	18.45	r
U3007/out (nand2)	0.08	0.11	18.55	f
U3005/out (aoi22)	0.25	0.10	18.65	r
U2993/out (nand2)	0.08	0.11	18.76	f
U2991/out (aoi22)	0.25	0.10	18.86	r

```
  U2980/out (nand2)                       0.08      0.11     18.97 f
  U2978/out (aoi22)                       0.27      0.11     19.08 r
  U2842/out (inverter)                    0.07      0.09     19.16 f
  U2841/vout (nor2)                       0.10      0.10     19.26 r
  U2705/out (nand2)                       0.08      0.09     19.35 f
  U2454/vout (nor2)                       0.10      0.10     19.45 r
  U2340/out (nand2)                       0.06      0.07     19.52 f
  U2339/out (inverter)                    0.05      0.05     19.57 r
  U2222/out (nand2)                       0.11      0.10     19.67 f
  U2022/vout (nor2)                       0.10      0.10     19.77 r
  U1938/out (nand2)                       0.09      0.10     19.88 f
  U1845/vout (nor2)                       0.12      0.12     20.00 r
  U1707/out (nand2)                       0.09      0.11     20.11 f
  U1645/vout (nor2)                       0.10      0.10     20.21 r
  U1585/out (nand2)                       0.11      0.12     20.33 f
  U1497/vout (nor2)                       0.10      0.10     20.44 r
  U1468/out (nand2)                       0.09      0.10     20.54 f
  U1433/vout (nor2)                       0.10      0.11     20.65 r
  U1422/out (nand2)                       0.07      0.08     20.73 f
  U1419/vout (xor2)                       0.06      0.12     20.85 f
  U1418/vout (nor2)                       0.06      0.05     20.91 r
  U1417/out (nand2)                       0.05      0.06     20.97 f
  out_reg[39]/d (dffl)                    0.05      0.00     20.97 f
  data arrival time                                          20.97
  --------------------------------------------------------------------------
  (Path is unconstrained)
1
update_power
Information: Checked out license 'PrimeTime-PX' (PT-019)
Warning: Neither event file or switching activity data present for power estimation. The command will
propagate switching activity values for power calculation.  (PWR-246)
Information: Running averaged power analysis... (PWR-601)
1

report_power
****************************************
Report : Averaged Power
Design : alu_161
Version: I-2013.12-SP3
Date   : Tue Dec  9 12:17:08 2014
****************************************
  Attributes
  ----------
    i  -  Including register clock pin internal power
```

u - User defined power group

Power Group	Internal Power	Switching Power	Leakage Power	Total Power	(%)	Attrs
clock_network	4.031e-04	2.994e-06	1.672e-10	4.061e-04	(21.60%)	i
register	8.565e-05	1.202e-03	7.184e-08	1.288e-03	(68.50%)	
combinational	1.147e-04	7.088e-05	5.867e-07	1.862e-04	(9.90%)	
sequential	0.0000	0.0000	0.0000	0.0000	(0.00%)	
memory	0.0000	0.0000	0.0000	0.0000	(0.00%)	
io_pad	0.0000	0.0000	0.0000	0.0000	(0.00%)	
black_box	0.0000	0.0000	0.0000	0.0000	(0.00%)	

Net Switching Power = 1.276e-03 (67.87%)
Cell Internal Power = 6.034e-04 (32.10%)
Cell Leakage Power = 6.587e-07 (0.04%)

Total Power = 1.880e-03 (100.00%)

1
1
Information: Defining new variable 'driving_cell'. (CMD-041)
Information: Defining new variable 'library_file'. (CMD-041)
Information: Defining new variable 'verilog_file'. (CMD-041)
Information: Defining new variable 'input_transition'. (CMD-041)
Information: Defining new variable 'timing_slew_propagation_mode'. (CMD-041)
Information: Defining new variable 'clock_period'. (CMD-041)
Information: Defining new variable 'load'. (CMD-041)
Information: Defining new variable 'reset_pin_name'. (CMD-041)
Information: Defining new variable 'clock_pin_name'. (CMD-041)
1
pt_shell> quit

7. Result:

The 20 bit ALU having area of 382463.5576 um^2 .

The total number of cells used are 4326

The worst case delay obtained is 20.97 time units and total power is 1.88mW