PROJECT #1

COMPUTER ARCHITECTURE

EE 6304

DESIGN OF CACHE

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1. Description and Aim of the project:

Description: Performance of a computer depends mostly on the performance of its memory and the speed. A most integral part of the memory hierarchy is the cache. Designing cache affects the architecture's performance. When a data is to be fetched, the cache is first accessed before the main memory. Thus the access speed to the cache should be minimized. For this reason, the cache is placed near to the processor. In the modern days, we can get multilevel caches with levels L1, L2, L3, etc., which facilitates faster access.

Aim: The aim of the project is to design a 2 level cache on a ALPHA microprocessor, by varying the unified cache properties, associativity and replacement policies. Simple scalar tool should be used to simulate the various parameters for 3 different benchmarks.

The CPI should be calculated and plotted for various configurations. The cost and performance should be calculated and optimized.

2. Approach for simulation:

Simulation is performed on Simple scalar 3.0 considering 3 different benchmarks i.e., GCC, Anagram and GO. The cache size of the 2 level design considered is L1:256KB, L2:1MB. The simulations are done considering both levels to have separate memory for instruction and data, both levels having unified memory and L1 having separate and L2 having unified memory. The following parameters are varied:

a. Block size: 32, 64 bytes
b. Associativity: Direct mapped, 2 way, 4 way, 8 way and fully associative.
c. Replacement policies: FIFO, Random, LRU

Simulations with design choices of permutations of these values for all benchmarks and making data and instruction cache unified. Below report shows the results for all these simulations. Based on the cost function, we use the above results to choose a appropriate design for each benchmark.

3. PART 1: BENCHMARKS USED:

- Gcc
- Anagram
- Go

The above Benchmarks are run and the output files thus obtained are verified with the input files. There was no deviation observed.

4. PART 2: FINDING THE CPI:

A separate 128 kb instruction and data cache for L1 and a unified 1MB L2 cache.
CPI is calculated as below:

CPI= 1+ Miss penalty of L1*total ((Miss rate of L1*Miss access of L1)/ number of instructions)+ Miss penalty of L2*total((Miss penalty of L2((Miss rate of L2*Miss access of L2)/ number of instructions) ….1)

where, Ideal CPI=1

Miss penalty of L1=4
Miss penalty of L2=70,

CPI= 1+ 4((inst level1 access*inst level1 miss rate + data level1 access*data levl1 miss rate)/# of inst) + 70((data level2 access* data level2 miss rate)# of inst)

1) CPI for GCC benchmark:

Total number of instructions used: 337327101
Instruction level1 accesses: 337327101
Instruction level1 miss rate: 0.0047
Data level1 accesses: 124102799
Data level1 miss rate: 0.0106
Data level2 accesses: 3330118
Data level2 miss rate: 0.1311

With these values substituting in equation 1)

.'.CPI= 1.124995

2) CPI for Anagram benchmark:

Total number of instructions used: 25593315
Instruction level1 accesses: 25593315
Instruction level1 miss rate: 0.0528
Data level1 accesses: 2021
Data level1 miss rate: 0.0787
Data level2 accesses: 425
Data level2 miss rate: 0.9953

.'.CPI= 1.2124

3) CPI for GO benchmark:

Total number of instructions used: 709783
Instruction level1 accesses: 709783
Instruction level1 miss rate: 0.0010
Data level1 accesses: 196785
Data level1 miss rate: 0.0264
Data level2 accesses: 9636
Data level2 miss rate: 0.5583

.'.CPI=1.5638

5. PART 3: OPTIMIZATION OF CPI FOR EVERY BENCHMARK:

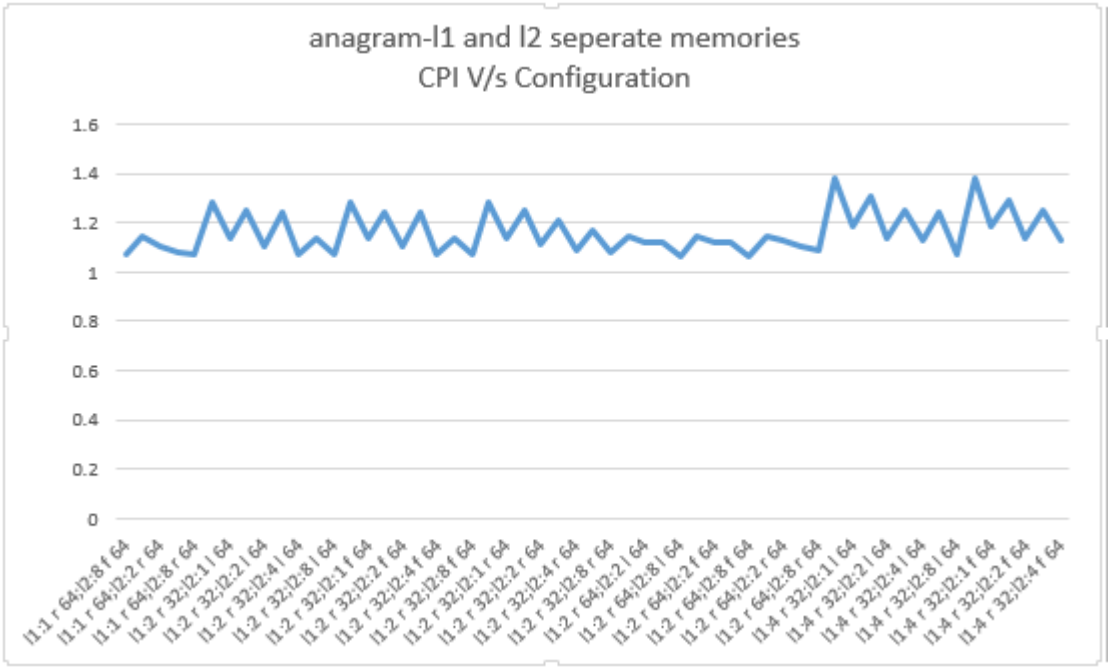
To optimize CPI for each benchmark, we have taken 2 caches, L1 cache of size 128KB and L2 cache of size 1MB. CPI of each benchmark is compared with the results :

- L1 separate Data and Instruction cache, L2 unified Data and Instruction cache
- L1 separate Data and Instruction cache, L2 separate Data and Instruction cache
- L1 unified Data and Instruction cache, L2 unified Data and Instruction cache
- Block size: 32 bytes, 64 bytes
- Associativity: 1-way, 2-way, 4-way and 8-way
- Replacement Policy: FIFO(f), Random(r), LRU(l)

The results for running the simulation on each benchmark is given below:

1. Anagram Benchmark:

   a) L1 and L2 with separate Data and Instruction cache:

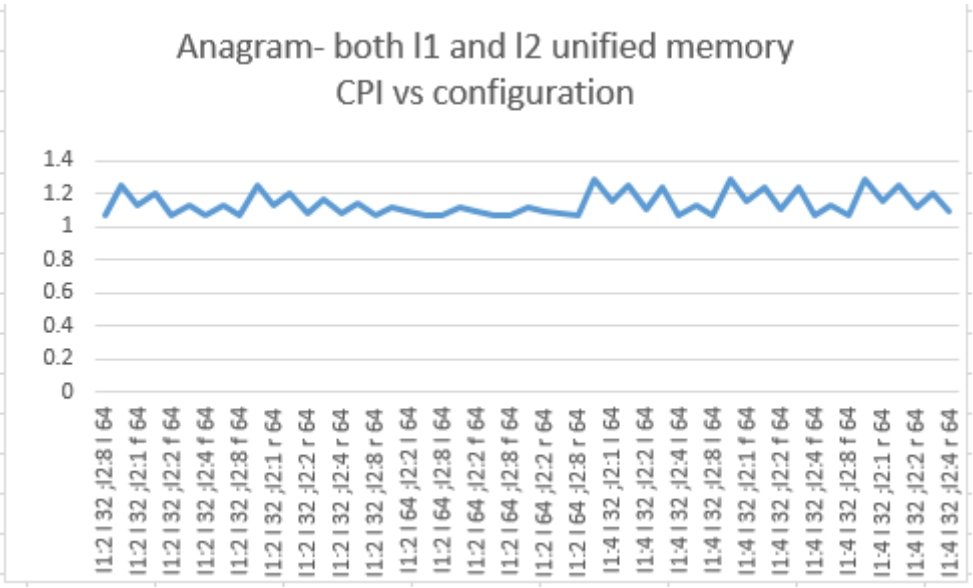


The above figure shows CPI as a function of various configurations. For the configuration l1:2 r 64;l2:8 l 64, lowest value of CPI=1.067148 where both L1 and L2 have separate data and instruction memory, L1:2-way associative, L2:8-way associative and the replacement policy for L1 is random and L2 is LRU.

The values are tabulated as below:

1	Configuration	# of instructior	dl1 acces	dl1 missrate	il1 access	il1 missrate	dl2 acces	dl2 missrate	il2 access	il2 missrate	CPI
2	I1:1 r 64;I2:8 f 64	25593315	11153944	0.0056	25593315	0	102180	0.2058	490	1	1.068767
3	I1:1 r 64;I2:1 r 64	25593315	11153944	0.0056	25593315	0	102180	0.4671	490	1	1.141799
4	I1:1 r 64;I2:2 r 64	25593315	11153944	0.0056	25593315	0	102180	0.3216	490	1	1.101115
5	I1:1 r 64;I2:4 r 64	25593315	11153944	0.0056	25593315	0	102180	0.2559	490	1	1.082765
6	I1:1 r 64;I2:8 r 64	25593315	11153944	0.0056	25593315	0	102180	0.2289	490	1	1.075205
7	I1:2 r 32;I2:1 I 32	25593315	11153944	0.0093	25593315	0	179226	0.5417	876	0.9726	1.284245
8	I1:2 r 32;I2:1 I 64	25593315	11153944	0.0093	25593315	0	179226	0.2452	876	0.5594	1.137926
9	I1:2 r 32;I2:2 I 32	25593315	11153944	0.0093	25593315	0	179226	0.4657	876	0.9726	1.246993
10	I1:2 r 32;I2:2 I 64	25593315	11153944	0.0093	25593315	0	179226	0.183	876	0.5594	1.10743
11	I1:2 r 32;I2:4 I 32	25593315	11153944	0.0093	25593315	0	179226	0.4477	876	0.9726	1.23817
12	I1:2 r 32;I2:4 I 64	25593315	11153944	0.0093	25593315	0	179226	0.1173	876	0.5594	1.075254
13	I1:2 r 32;I2:8 I 32	25593315	11153944	0.0093	25593315	0	179226	0.2342	876	0.9726	1.133512
14	I1:2 r 32;I2:8 I 64	25593315	11153944	0.0093	25593315	0	179226	0.1173	876	0.5594	1.075254
15	I1:2 r 32;I2:1 f 32	25593315	11153944	0.0093	25593315	0	179226	0.5417	876	0.9726	1.284245
16	I1:2 r 32;I2:1 f 64	25593315	11153944	0.0093	25593315	0	179226	0.2452	876	0.5594	1.137926
17	I1:2 r 32;I2:2 f 32	25593315	11153944	0.0093	25593315	0	179226	0.4635	876	0.9726	1.24594
18	I1:2 r 32;I2:2 f 64	25593315	11153944	0.0093	25593315	0	179226	0.1834	876	0.5594	1.107659
19	I1:2 r 32;I2:4 f 32	25593315	11153944	0.0093	25593315	0	179226	0.4528	876	0.9726	1.240672
20	I1:2 r 32;I2:4 f 64	25593315	11153944	0.0093	25593315	0	179226	0.1173	876	0.5594	1.075254
21	I1:2 r 32;I2:8 f 32	25593315	11153944	0.0093	25593315	0	179226	0.2342	876	0.9726	1.133512
22	I1:2 r 32;I2:8 f 64	25593315	11153944	0.0093	25593315	0	179226	0.1173	876	0.5594	1.075254
23	I1:2 r 32;I2:1 r 32	25593315	11153944	0.0093	25593315	0	179280	0.5424	876	0.9726	1.284681
24	I1:2 r 32;I2:1 r 64	25593315	11153944	0.0093	25593315	0	179352	0.2456	873	0.5613	1.13821
25	I1:2 r 32;I2:2 r 32	25593315	11153944	0.0093	25593315	0	179220	0.4792	874	0.9748	1.2536
26	I1:2 r 32;I2:2 r 64	25593315	11153944	0.0093	25593315	0	179347	0.1871	883	0.5549	1.109547
27	I1:2 r 32;I2:4 r 32	25593315	11153944	0.0093	25593315	0	179363	0.384	867	0.9827	1.207123
28	I1:2 r 32;I2:4 r 64	25593315	11153944	0.0093	25593315	0	179386	0.1472	862	0.5684	1.089957
29	I1:2 r 32;I2:8 r 32	25593315	11153944	0.0093	25593315	0	179339	0.3042	873	0.9759	1.167968
30	I1:2 r 32;I2:8 r 64	25593315	11153944	0.0093	25593315	0	179348	0.1305	870	0.5632	1.081767
31	I1:2 r 64;I2:1 I 64	25593315	11153944	0.0047	25593315	0	90260	0.5421	499	0.982	1.143454
32	I1:2 r 64;I2:2 I 64	25593315	11153944	0.0047	25593315	0	90260	0.4639	499	0.982	1.124158
33	I1:2 r 64;I2:4 I 64	25593315	11153944	0.0047	25593315	0	90260	0.4456	499	0.982	1.119629
34	**I1:2 r 64;I2:8 I 64**	25593315	**11153944**	**0.0047**	**25593315**	**0**	**90260**	**0.233**	**499**	**0.982**	**1.067148**
35	I1:2 r 64;I2:1 f 64	25593315	11153944	0.0047	25593315	0	90260	0.5421	499	0.982	1.143454
36	I1:2 r 64;I2:2 f 64	25593315	11153944	0.0047	25593315	0	90260	0.4614	499	0.982	1.123526
37	I1:2 r 64;I2:4 f 64	25593315	11153944	0.0047	25593315	0	90260	0.4504	499	0.982	1.120827
38	**I1:2 r 64;I2:8 f 64**	25593315	**11153944**	**0.0047**	**25593315**	**0**	**90260**	**0.233**	**499**	**0.982**	**1.067148**
39	I1:2 r 64;I2:1 r 64	25593315	11153944	0.0047	25593315	0	90200	0.5411	502	0.9761	1.143114
40	I1:2 r 64;I2:2 r 64	25593315	11153944	0.0047	25593315	0	90189	0.4791	502	0.9761	1.127798
41	I1:2 r 64;I2:4 r 64	25593315	11153944	0.0047	25593315	0	90255	0.3837	507	0.9665	1.104337
42	I1:2 r 64;I2:8 r 64	25593315	11153944	0.0047	25593315	0	90221	0.3027	500	0.98	1.08432
43	I1:4 r 32;I2:1 I 32	25593315	11153944	0.0093	25593315	0	178679	0.7469	867	0.9827	1.383635
44	I1:4 r 32;I2:1 I 64	25593315	11153944	0.0093	25593315	0	178679	0.348	867	0.5652	1.187707
45	I1:4 r 32;I2:2 I 32	25593315	11153944	0.0093	25593315	0	178679	0.5847	867	0.9827	1.304405
46	I1:4 r 32;I2:2 I 64	25593315	11153944	0.0093	25593315	0	178679	0.243	867	0.5652	1.136402
47	I1:4 r 32;I2:4 I 32	25593315	11153944	0.0093	25593315	0	178679	0.4727	867	0.9827	1.249676
48	I1:4 r 32;I2:4 I 64	25593315	11153944	0.0093	25593315	0	178679	0.2219	867	0.5652	1.126088
49	I1:4 r 32;I2:8 I 32	25593315	11153944	0.0093	25593315	0	178679	0.4497	867	0.9827	1.238399
50	I1:4 r 32;I2:8 I 64	25593315	11153944	0.0093	25593315	0	178679	0.1177	867	0.5652	1.075178
51	I1:4 r 32;I2:1 f 32	25593315	11153944	0.0093	25593315	0	178679	0.7469	867	0.9827	1.383635
52	I1:4 r 32;I2:1 f 64	25593315	11153944	0.0093	25593315	0	178679	0.348	867	0.5652	1.187707
53	I1:4 r 32;I2:2 f 32	25593315	11153944	0.0093	25593315	0	178679	0.5622	867	0.9827	1.293377
54	I1:4 r 32;I2:2 f 64	25593315	11153944	0.0093	25593315	0	178679	0.2406	867	0.5652	1.135251
55	I1:4 r 32;I2:4 f 32	25593315	11153944	0.0093	25593315	0	178679	0.467	867	0.9827	1.246862

b)Both L1 and L2 unified Cache:



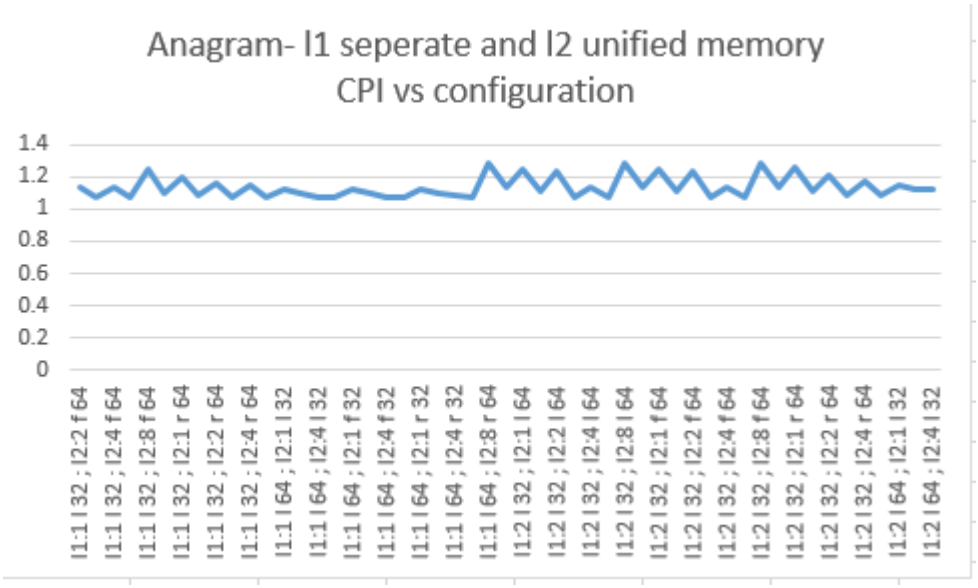
The above figure shows CPI as a function of various configurations. For the configuration l1:2 l 64 ;l2:4 l 64, lowest value of CPI observed is 1.066071. L1 is 2-way associative and L2 is 4-way associative and replacement policy for both L1 and L2 is LRU.

The values are tabulated as below:

	Configuration	#of instruction	ul1 access	ul1 missrate	ul2 access	ul2 missrate	CPI
2	l1:2 l 32 ;l2:8 l 64	25593315	36747259	0.0025	165565	0.13	1.073094
3	l1:2 l 32 ;l2:1 f 32	25593315	36747259	0.0025	165565	0.5097	1.24503
4	l1:2 l 32 ;l2:1 f 64	25593315	36747259	0.0025	165565	0.2423	1.12395
5	l1:2 l 32 ;l2:2 f 32	25593315	36747259	0.0025	165565	0.4024	1.196438
6	l1:2 l 32 ;l2:2 f 64	25593315	36747259	0.0025	165565	0.1311	1.073605
7	l1:2 l 32 ;l2:4 f 32	25593315	36747259	0.0025	165565	0.2586	1.131351
8	l1:2 l 32 ;l2:4 f 64	25593315	36747259	0.0025	165565	0.13	1.073094
9	l1:2 l 32 ;l2:8 f 32	25593315	36747259	0.0025	165565	0.2586	1.131351
10	l1:2 l 32 ;l2:8 f 64	25593315	36747259	0.0025	165565	0.13	1.073094
11	l1:2 l 32 ;l2:1 r 32	25593315	36747259	0.0025	165565	0.5097	1.24503
12	l1:2 l 32 ;l2:1 r 64	25593315	36747259	0.0025	165565	0.2423	1.12395
13	l1:2 l 32 ;l2:2 r 32	25593315	36747259	0.0025	165565	0.4034	1.196928
14	l1:2 l 32 ;l2:2 r 64	25593315	36747259	0.0025	165565	0.1537	1.083824
15	l1:2 l 32 ;l2:4 r 32	25593315	36747259	0.0025	165565	0.3219	1.160015
16	l1:2 l 32 ;l2:4 r 64	25593315	36747259	0.0025	165565	0.1384	1.076918
17	l1:2 l 32 ;l2:8 r 32	25593315	36747259	0.0025	165565	0.2873	1.144327
18	l1:2 l 32 ;l2:8 r 64	25593315	36747259	0.0025	165565	0.1335	1.074697
19	l1:2 l 64 ;l2:1 l 64	25593315	36747259	0.0013	83346	0.5092	1.123274
20	l1:2 l 64 ;l2:2 l 64	25593315	36747259	0.0013	83346	0.4019	1.098819
21	**l1:2 l 64 ;l2:4 l 64**	**25593315**	**36747259**	**0.0013**	**83346**	**0.2582**	**1.066061**
22	l1:2 l 64 ;l2:8 l 64	25593315	36747259	0.0013	83346	0.2582	1.066058
23	l1:2 l 64 ;l2:1 f 64	25593315	36747259	0.0013	83346	0.5092	1.123274
24	l1:2 l 64 ;l2:2 f 64	25593315	36747259	0.0013	83346	0.4019	1.098819
25	l1:2 l 64 ;l2:4 f 64	25593315	36747259	0.0013	83346	0.2582	1.066058
26	l1:2 l 64 ;l2:8 f 64	25593315	36747259	0.0013	83346	0.2582	1.066058

27	l1:2 l 64 ;l2:1 r 64	25593315	36747259	0.0013	83346	0.5092	1.123274
28	l1:2 l 64 ;l2:2 r 64	25593315	36747259	0.0013	83346	0.4024	1.098923
29	l1:2 l 64 ;l2:4 r 64	25593315	36747259	0.0013	83346	0.3231	1.080847
30	l1:2 l 64 ;l2:8 r 64	25593315	36747259	0.0013	83346	0.2864	1.072478
31	l1:4 l 32 ;l2:1 l 32	25593315	36747259	0.0026	169952	0.5927	1.290426
32	l1:4 l 32 ;l2:1 l 64	25593315	36747259	0.0026	169952	0.2901	1.149744
33	l1:4 l 32 ;l2:2 l 32	25593315	36747259	0.0026	169952	0.4952	1.245106
34	l1:4 l 32 ;l2:2 l 64	25593315	36747259	0.0026	169952	0.1973	1.106612
35	l1:4 l 32 ;l2:4 l 32	25593315	36747259	0.0026	169952	0.4835	1.23966
36	l1:4 l 32 ;l2:4 l 64	25593315	36747259	0.0026	169952	0.1266	1.073774
37	l1:4 l 32 ;l2:8 l 32	25593315	36747259	0.0026	169952	0.252	1.132029
38	l1:4 l 32 ;l2:8 l 64	25593315	36747259	0.0026	169952	0.1266	1.073772
39	l1:4 l 32 ;l2:1 f 32	25593315	36747259	0.0026	169952	0.5927	1.290426
40	l1:4 l 32 ;l2:1 f 64	25593315	36747259	0.0026	169952	0.2901	1.149744
41	l1:4 l 32 ;l2:2 f 32	25593315	36747259	0.0026	169952	0.4938	1.24446
42	l1:4 l 32 ;l2:2 f 64	25593315	36747259	0.0026	169952	0.1972	1.106593
43	l1:4 l 32 ;l2:4 f 32	25593315	36747259	0.0026	169952	0.4835	1.239657
44	l1:4 l 32 ;l2:4 f 64	25593315	36747259	0.0026	169952	0.1266	1.073772
45	l1:4 l 32 ;l2:8 f 32	25593315	36747259	0.0026	169952	0.252	1.132029
46	l1:4 l 32 ;l2:8 f 64	25593315	36747259	0.0026	169952	0.1266	1.073772
47	l1:4 l 32 ;l2:1 r 32	25593315	36747259	0.0026	169952	0.5927	1.290426
48	l1:4 l 32 ;l2:1 r 64	25593315	36747259	0.0026	169952	0.2901	1.149744
49	l1:4 l 32 ;l2:2 r 32	25593315	36747259	0.0026	169952	0.5165	1.255012
50	l1:4 l 32 ;l2:2 r 64	25593315	36747259	0.0026	169952	0.21	1.112522

c)L1 separate and L2 unified memory:



The above figure shows CPI as a function of various configurations. For the configuration l1:1 l 64 ; l2:8 l 32 the Lowest value of CPI observed is 1.067255. L1 is 1-way associative, L2 is 8-way associative and the replacement policy for both is LRU.

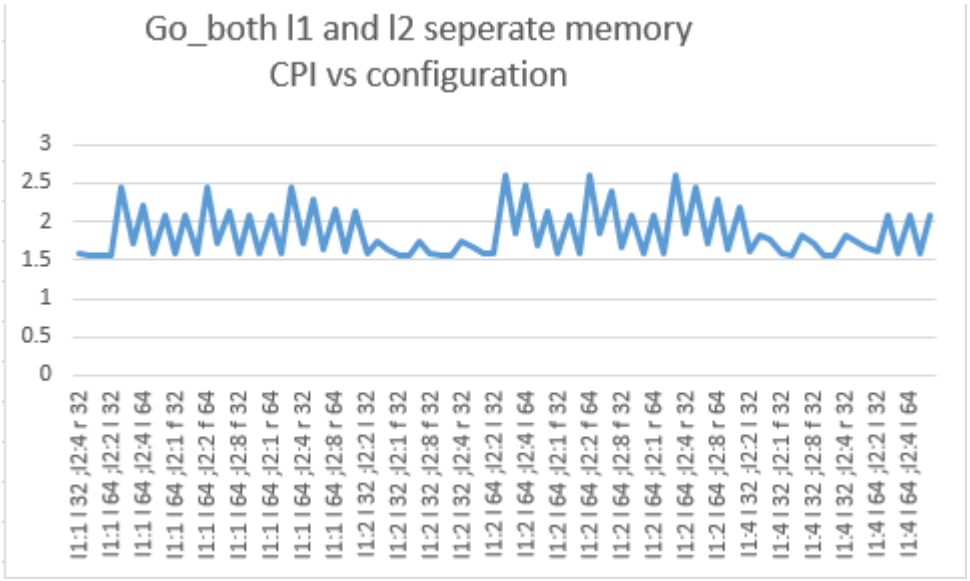
The values are tabulated as below:

	A	B	C	D	E	F	G	H	I
1	Configuration	# of instructions	dl1 access	dl1 missrate	il1 access	il1 missrate	dl2 access	dl2 missrate	CPI
2	I1:1 I 32 ; I2:2 f 64	25593315	11153944	0.0095	25593315	0	181827	0.2355	1.133805
3	I1:1 I 32 ; I2:4 f 32	25593315	11153944	0.0095	25593315	0	181827	0.1184	1.075548
4	I1:1 I 32 ; I2:4 f 64	25593315	11153944	0.0095	25593315	0	181827	0.2355	1.133805
5	I1:1 I 32 ; I2:8 f 32	25593315	11153944	0.0095	25593315	0	181827	0.1184	1.075548
6	I1:1 I 32 ; I2:8 f 64	25593315	11153944	0.0095	25593315	0	181827	0.4606	1.245763
7	I1:1 I 32 ; I2:1 r 32	25593315	11153944	0.0095	25593315	0	181827	0.1624	1.097445
8	I1:1 I 32 ; I2:1 r 64	25593315	11153944	0.0095	25593315	0	181827	0.3656	1.19852
9	I1:1 I 32 ; I2:2 r 32	25593315	11153944	0.0095	25593315	0	181827	0.1348	1.083748
10	I1:1 I 32 ; I2:2 r 64	25593315	11153944	0.0095	25593315	0	181827	0.293	1.162414
11	I1:1 I 32 ; I2:4 r 32	25593315	11153944	0.0095	25593315	0	181827	0.1254	1.079032
12	I1:1 I 32 ; I2:4 r 64	25593315	11153944	0.0095	25593315	0	181827	0.2615	1.14672
13	I1:1 I 32 ; I2:8 r 32	25593315	11153944	0.0095	25593315	0	181827	0.1213	1.077008
14	I1:1 I 64 ; I2:1 I 32	25593315	11153944	0.0048	25593315	0	91316	0.4604	1.123382
15	I1:1 I 64 ; I2:2 I 32	25593315	11153944	0.0048	25593315	0	91316	0.3655	1.099672
16	I1:1 I 64 ; I2:4 I 32	25593315	11153944	0.0048	25593315	0	91316	0.2357	1.067255
17	**I1:1 I 64 ; I2:8 I 32**	**25593315**	**11153944**	**0.0048**	**25593315**	**0**	**91316**	**0.2357**	**1.067255**
18	I1:1 I 64 ; I2:1 f 32	25593315	11153944	0.0048	25593315	0	91316	0.4604	1.123382
19	I1:1 I 64 ; I2:2 f 32	25593315	11153944	0.0048	25593315	0	91316	0.3655	1.099672
20	I1:1 I 64 ; I2:4 f 32	25593315	11153944	0.0048	25593315	0	91316	0.2357	1.067255
21	I1:1 I 64 ; I2:8 f 32	25593315	11153944	0.0048	25593315	0	91316	0.2357	1.067255
22	I1:1 I 64 ; I2:1 r 32	25593315	11153944	0.0048	25593315	0	91316	0.4604	1.123382
23	I1:1 I 64 ; I2:2 r 32	25593315	11153944	0.0048	25593315	0	91316	0.3657	1.099737

	A	B	C	D	E	F	G	H	I
24	I1:1 I 64 ; I2:4 r 32	25593315	11153944	0.0048	25593315	0	91316	0.2922	1.081374
25	I1:1 I 64 ; I2:8 r 32	25593315	11153944	0.0048	25593315	0	91316	0.2612	1.073631
26	I1:1 I 64 ; I2:8 r 64	25593315	11153944	0.0095	25593315	0	181555	0.5456	1.28759
27	I1:2 I 32 ; I2:1 I 32	25593315	11153944	0.0095	25593315	0	181555	0.2318	1.131767
28	I1:2 I 32 ; I2:1 I 64	25593315	11153944	0.0095	25593315	0	181555	0.4605	1.245303
29	I1:2 I 32 ; I2:2 I 32	25593315	11153944	0.0095	25593315	0	181555	0.1839	1.10798
30	I1:2 I 32 ; I2:2 I 64	25593315	11153944	0.0095	25593315	0	181555	0.4517	1.240941
31	I1:2 I 32 ; I2:4 I 32	25593315	11153944	0.0095	25593315	0	181555	0.1185	1.075517
32	I1:2 I 32 ; I2:4 I 64	25593315	11153944	0.0095	25593315	0	181555	0.2359	1.133775
33	I1:2 I 32 ; I2:8 I 32	25593315	11153944	0.0095	25593315	0	181555	0.1185	1.075517
34	I1:2 I 32 ; I2:8 I 64	25593315	11153944	0.0095	25593315	0	181555	0.5456	1.28759
35	I1:2 I 32 ; I2:1 f 32	25593315	11153944	0.0095	25593315	0	181555	0.2318	1.131767
36	I1:2 I 32 ; I2:1 f 64	25593315	11153944	0.0095	25593315	0	181555	0.4603	1.245208
37	I1:2 I 32 ; I2:2 f 32	25593315	11153944	0.0095	25593315	0	181555	0.1839	1.10798
38	I1:2 I 32 ; I2:2 f 64	25593315	11153944	0.0095	25593315	0	181555	0.4517	1.240938
39	I1:2 I 32 ; I2:4 f 32	25593315	11153944	0.0095	25593315	0	181555	0.1185	1.075517
40	I1:2 I 32 ; I2:4 f 64	25593315	11153944	0.0095	25593315	0	181555	0.2359	1.133775
41	I1:2 I 32 ; I2:8 f 32	25593315	11153944	0.0095	25593315	0	181555	0.1185	1.075517
42	I1:2 I 32 ; I2:8 f 64	25593315	11153944	0.0095	25593315	0	181555	0.5456	1.28759
43	I1:2 I 32 ; I2:1 r 32	25593315	11153944	0.0095	25593315	0	181555	0.2318	1.131767
44	I1:2 I 32 ; I2:1 r 64	25593315	11153944	0.0095	25593315	0	181555	0.4794	1.254723
45	I1:2 I 32 ; I2:2 r 32	25593315	11153944	0.0095	25593315	0	181555	0.1846	1.108305
46	I1:2 I 32 ; I2:2 r 64	25593315	11153944	0.0095	25593315	0	181555	0.3849	1.207802

2) For GO benchmark:

a) Both L1 and L2 separate memory:

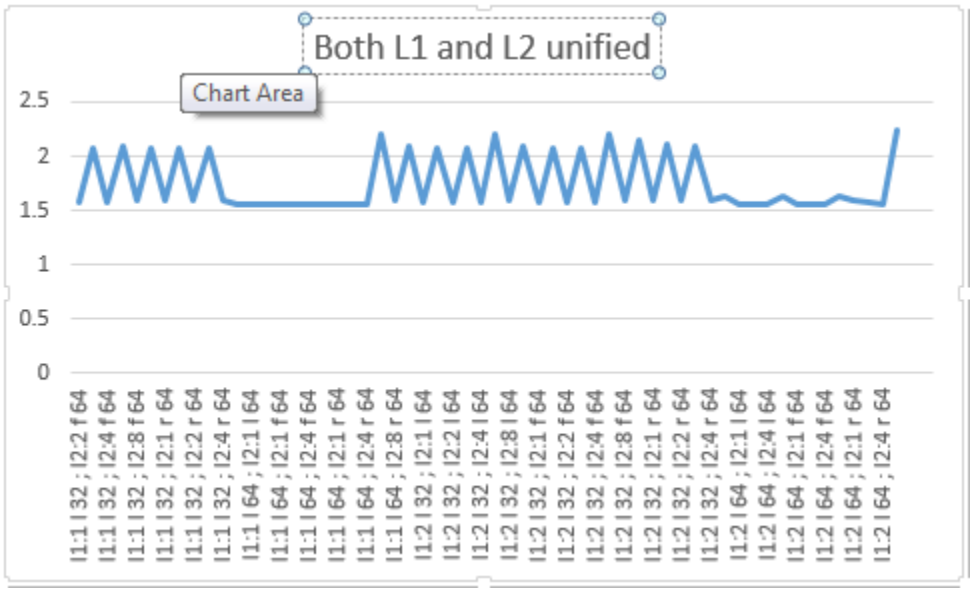


The above figure shows CPI as a function of various configurations. For the configuration **l1:2 l 32 ;l2:1 f 32,** the Lowest value of CPI observed is 1.555089. L1 is 2-way associative, L2 is 1-way associative and the replacement policy for L1 is LRU and L2 is FIFO.

The values are tabulated as below:

	A	B	C	D	E	F	G	H	I	J	K
1	Configuration	# of instru	dl1 access	dl1 missra	il1 access	il1 missrat	dl2 access	dl2 missra	il2 access	il2 missrat	CPI
2	l1:1 l 32 ;l2:4 r 32	718216	200572	0.025	718216	0.0006	7690	0.6848	454	1	1.587985
3	l1:1 l 32 ;l2:8 r 32	718216	200572	0.025	718216	0.0006	7690	0.6581	454	1	1.568005
4	l1:1 l 64 ;l2:1 l 32	718216	200572	0.025	718216	0.0006	7690	0.6473	454	1	1.559915
5	l1:1 l 64 ;l2:2 l 32	718216	200572	0.025	718216	0.0006	7690	0.644	454	1	1.557381
6	l1:1 l 64 ;l2:2 l 64	718216	200572	0.0489	718216	0.0011	15013	0.9011	801	1	2.455604
7	l1:1 l 64 ;l2:4 l 32	718216	200572	0.0489	718216	0.0011	15013	0.4116	801	0.568	1.705718
8	l1:1 l 64 ;l2:4 l 64	718216	200572	0.0489	718216	0.0011	15013	0.74	801	1	2.219937
9	l1:1 l 64 ;l2:8 l 32	718216	200572	0.0489	718216	0.0011	15013	0.3283	801	0.5668	1.583693
10	l1:1 l 64 ;l2:8 l 64	718216	200572	0.0489	718216	0.0011	15013	0.6439	801	1	2.079296
11	l1:1 l 64 ;l2:1 f 32	718216	200572	0.0489	718216	0.0011	15013	0.3283	801	0.5668	1.583693
12	l1:1 l 64 ;l2:1 f 64	718216	200572	0.0489	718216	0.0011	15013	0.6439	801	1	2.079296
13	l1:1 l 64 ;l2:2 f 32	718216	200572	0.0489	718216	0.0011	15013	0.3283	801	0.5668	1.583693
14	l1:1 l 64 ;l2:2 f 64	718216	200572	0.0489	718216	0.0011	15013	0.9011	801	1	2.455604
15	l1:1 l 64 ;l2:4 f 32	718216	200572	0.0489	718216	0.0011	15013	0.4116	801	0.568	1.705718
16	l1:1 l 64 ;l2:4 f 64	718216	200572	0.0489	718216	0.0011	15013	0.6797	801	1	2.131634
17	l1:1 l 64 ;l2:8 f 32	718216	200572	0.0489	718216	0.0011	15013	0.3283	801	0.5668	1.583693
18	l1:1 l 64 ;l2:8 f 64	718216	200572	0.0489	718216	0.0011	15013	0.6439	801	1	2.079296
19	l1:1 l 64 ;l2:1 r 32	718216	200572	0.0489	718216	0.0011	15013	0.3283	801	0.5668	1.583693
20	l1:1 l 64 ;l2:1 r 64	718216	200572	0.0489	718216	0.0011	15013	0.6439	801	1	2.079296
21	l1:1 l 64 ;l2:2 r 32	718216	200572	0.0489	718216	0.0011	15013	0.3283	801	0.5668	1.583693
22	l1:1 l 64 ;l2:2 r 64	718216	200572	0.0489	718216	0.0011	15013	0.9011	801	1	2.455604
23	l1:1 l 64 ;l2:4 r 32	718216	200572	0.0489	718216	0.0011	15013	0.4116	801	0.568	1.705718
24	l1:1 l 64 ;l2:4 r 64	718216	200572	0.0489	718216	0.0011	15013	0.7803	801	1	2.278805
25	l1:1 l 64 ;l2:8 r 32	718216	200572	0.0489	718216	0.0011	15013	0.3609	801	0.5668	1.631353
26	l1:1 l 64 ;l2:8 r 64	718216	200572	0.0489	718216	0.0011	15013	0.7078	801	1	2.172764
27	l1:2 l 32 ;l2:1 l 32	718216	200572	0.0489	718216	0.0011	15013	0.3426	801	0.5668	1.604648
28	l1:2 l 32 ;l2:1 l 64	718216	200572	0.0489	718216	0.0011	15013	0.6737	801	1	2.12296
29	l1:2 l 32 ;l2:2 l 32	718216	200572	0.0489	718216	0.0011	15013	0.3353	801	0.5668	1.593927
30	l1:2 l 32 ;l2:4 l 32	718216	200572	0.025	718216	0.0006	7680	0.9018	454	1	1.749724
31	l1:2 l 32 ;l2:8 l 32	718216	200572	0.025	718216	0.0006	7680	0.7392	454	1	1.627992
32	**l1:2 l 32 ;l2:1 f 32**	**718216**	**200572**	**0.025**	**718216**	**0.0006**	**7680**	**0.6418**	**454**	**1**	**1.555089**
33	l1:2 l 32 ;l2:2 f 32	718216	200572	0.025	718216	0.0006	7680	0.6418	454	1	1.555089
34	l1:2 l 32 ;l2:4 f 32	718216	200572	0.025	718216	0.0006	7680	0.9018	454	1	1.749724
35	l1:2 l 32 ;l2:8 f 32	718216	200572	0.025	718216	0.0006	7680	0.679	454	1	1.582964
36	l1:2 l 32 ;l2:1 r 32	718216	200572	0.025	718216	0.0006	7680	0.6418	454	1	1.555089
37	l1:2 l 32 ;l2:2 r 32	718216	200572	0.025	718216	0.0006	7680	0.6418	454	1	1.555089
38	l1:2 l 32 ;l2:4 r 32	718216	200572	0.025	718216	0.0006	7680	0.9018	454	1	1.749724
39	l1:2 l 32 ;l2:8 r 32	718216	200572	0.025	718216	0.0006	7680	0.7785	454	1	1.657426
40	l1:2 l 64 ;l2:1 l 32	718216	200572	0.025	718216	0.0006	7680	0.7013	454	1	1.59963
41	l1:2 l 64 ;l2:2 l 32	718216	200572	0.025	718216	0.0006	7680	0.6749	454	1	1.579845
42	l1:2 l 64 ;l2:2 l 64	718216	200572	0.0489	718216	0.0011	15015	0.9945	801	1	2.592552
43	l1:2 l 64 ;l2:4 l 32	718216	200572	0.0489	718216	0.0011	15015	0.5112	801	0.568	1.851437
44	l1:2 l 64 ;l2:4 l 64	718216	200572	0.0489	718216	0.0011	15015	0.9139	801	1	2.474523
45	l1:2 l 64 ;l2:8 l 32	718216	200572	0.0489	718216	0.0011	15015	0.4	801	0.5668	1.688673
46	l1:2 l 64 ;l2:8 l 64	718216	200572	0.0489	718216	0.0011	15015	0.6831	801	1	2.136714

c)Both L1 and L2 unified memory:



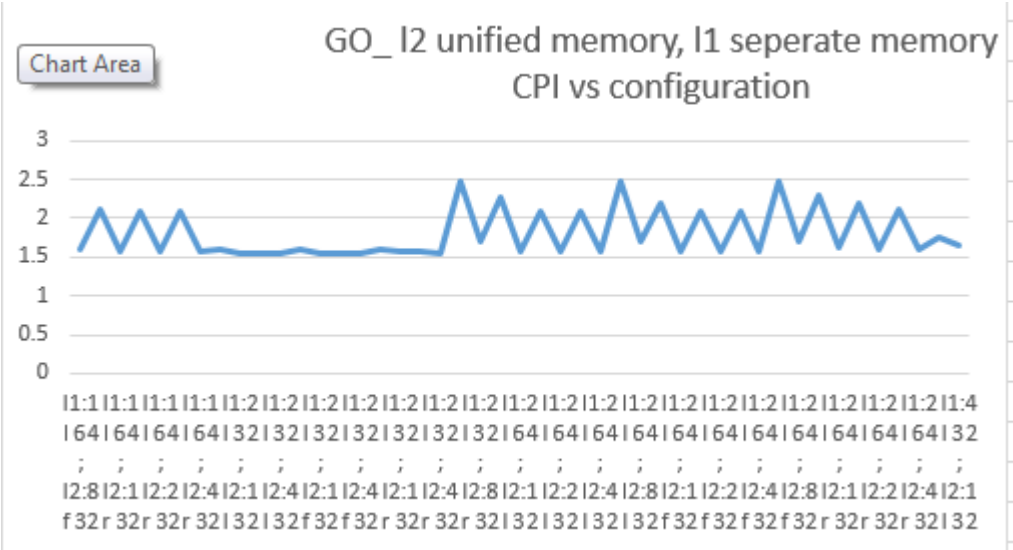
The above figure shows CPI as a function of various configurations. For the configuration **l1:1 l 64 ; l2:1 l 64,** the lowest CPI observed is 1.555022. L1 is 1-way associative and L2 is 2-way associative. The replacement policy for both L1 and L2 is LRU.

The values are tabulated as below:

1	configuration	#of instructions	ul1 access	ul1 missrate	ul2 access	ul2 missrate	CPI
2	l1:1 l 32 ; l2:2 f 64	718216	918788	0.0115	12979	0.4147	1.58346
3	l1:1 l 32 ; l2:4 f 32	718216	918788	0.0115	12979	0.8065	2.079063
4	l1:1 l 32 ; l2:4 f 64	718216	918788	0.0115	12979	0.4147	1.58346
5	l1:1 l 32 ; l2:8 f 32	718216	918788	0.0115	12979	0.8127	2.08686
6	l1:1 l 32 ; l2:8 f 64	718216	918788	0.0115	12979	0.4284	1.600711
7	l1:1 l 32 ; l2:1 r 32	718216	918788	0.0115	12979	0.8093	2.082571
8	l1:1 l 32 ; l2:1 r 64	718216	918788	0.0115	12979	0.4208	1.591159
9	l1:1 l 32 ; l2:2 r 32	718216	918788	0.0115	12979	0.8072	2.07994
10	l1:1 l 32 ; l2:2 r 64	718216	918788	0.0115	12979	0.4177	1.587163
11	l1:1 l 32 ; l2:4 r 32	718216	918788	0.0115	12979	0.8068	2.079452
12	l1:1 l 32 ; l2:4 r 64	718216	918788	0.0115	12979	0.4159	1.584922
13	l1:1 l 32 ; l2:8 r 64	718216	918788	0.0059	6744	0.8072	1.560968
14	**l1:1 l 64 ; l2:1 l 64**	**718216**	**918788**	**0.0059**	**6744**	**0.7982**	**1.555022**
15	l1:1 l 64 ; l2:2 l 64	718216	918788	0.0059	6744	0.7982	1.555022
16	l1:1 l 64 ; l2:4 l 64	718216	918788	0.0059	6744	0.7982	1.555022
17	l1:1 l 64 ; l2:8 l 64	718216	918788	0.0059	6744	0.8072	1.560968
18	l1:1 l 64 ; l2:1 f 64	718216	918788	0.0059	6744	0.7982	1.555022
19	l1:1 l 64 ; l2:2 f 64	718216	918788	0.0059	6744	0.7982	1.555022
20	l1:1 l 64 ; l2:4 f 64	718216	918788	0.0059	6744	0.7982	1.555022
21	l1:1 l 64 ; l2:8 f 64	718216	918788	0.0059	6744	0.8072	1.560968
22	l1:1 l 64 ; l2:1 r 64	718216	918788	0.0059	6744	0.8023	1.557751

23	l1:1 l 64 ; l2:2 r 64	718216	918788	0.0059	6744	0.8009	1.556777
24	l1:1 l 64 ; l2:4 r 64	718216	918788	0.0059	6744	0.7995	1.5559
25	l1:1 l 64 ; l2:8 r 32	718216	918788	0.0115	12326	0.9489	2.198949
26	l1:1 l 64 ; l2:8 r 64	718216	918788	0.0115	12326	0.446	1.594771
27	l1:2 l 32 ; l2:1 l 32	718216	918788	0.0115	12326	0.8549	2.085988
28	l1:2 l 32 ; l2:1 l 64	718216	918788	0.0115	12326	0.4367	1.58366
29	l1:2 l 32 ; l2:2 l 32	718216	918788	0.0115	12326	0.8493	2.079263
30	l1:2 l 32 ; l2:2 l 64	718216	918788	0.0115	12326	0.4367	1.58366
31	l1:2 l 32 ; l2:4 l 32	718216	918788	0.0115	12326	0.8493	2.079263
32	l1:2 l 32 ; l2:4 l 64	718216	918788	0.0115	12326	0.4367	1.58366
33	l1:2 l 32 ; l2:8 l 32	718216	918788	0.0115	12326	0.9489	2.198949
34	l1:2 l 32 ; l2:8 l 64	718216	918788	0.0115	12326	0.446	1.594771
35	l1:2 l 32 ; l2:1 f 32	718216	918788	0.0115	12326	0.8545	2.085501
36	l1:2 l 32 ; l2:1 f 64	718216	918788	0.0115	12326	0.4367	1.58366
37	l1:2 l 32 ; l2:2 f 32	718216	918788	0.0115	12326	0.8493	2.079263
38	l1:2 l 32 ; l2:2 f 64	718216	918788	0.0115	12326	0.4367	1.58366
39	l1:2 l 32 ; l2:4 f 32	718216	918788	0.0115	12326	0.8493	2.079263
40	l1:2 l 32 ; l2:4 f 64	718216	918788	0.0115	12326	0.4367	1.58366
41	l1:2 l 32 ; l2:8 f 32	718216	918788	0.0115	12326	0.9489	2.198949
42	l1:2 l 32 ; l2:8 f 64	718216	918788	0.0115	12326	0.446	1.594771
43	l1:2 l 32 ; l2:1 r 32	718216	918788	0.0115	12326	0.9011	2.141542
44	l1:2 l 32 ; l2:1 r 64	718216	918788	0.0115	12326	0.4406	1.588338
45	l1:2 l 32 ; l2:2 r 32	718216	918788	0.0115	12326	0.8764	2.111913

b) L1 separate memory and L2 unified memory:



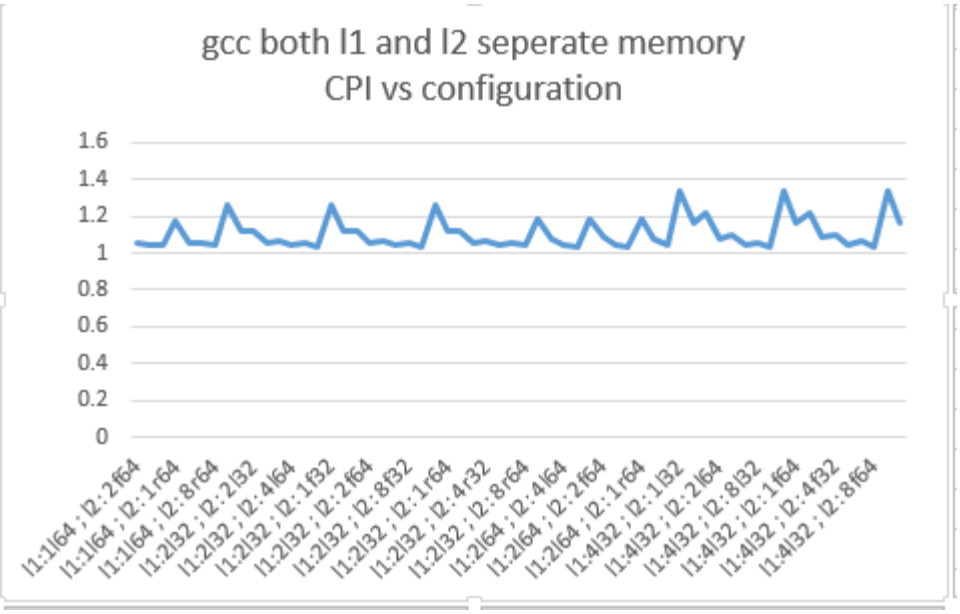
The above figure shows CPI as a function of various configurations. For the configuration **l1:2 l 32 ;l2:4 l 32,** the lowest value of CPI observed is 1.555089. L1and L2 is 2-way associative . The replacement policy for L1 is LRU and for L2 is FIFO.

The values are tabulated as below:

1	Configuration	# of instructions	dl1 access	dl1 missrate	il1 access	il1 missrate	dl2 access	dl2 missrate	CPI
2	I1:1 I 32 ; I2:8 r 64	718216	200572	0.0489	718216	0.0011	15814	0.6621	2.079491
3	I1:1 I 64 ; I2:1 I 32	718216	200572	0.0489	718216	0.0011	15814	0.3404	1.583693
4	I1:1 I 64 ; I2:1 I 64	718216	200572	0.0489	718216	0.0011	15814	0.6619	2.079296
5	I1:1 I 64 ; I2:2 I 32	718216	200572	0.0489	718216	0.0011	15814	0.3404	1.583693
6	I1:1 I 64 ; I2:2 I 64	718216	200572	0.0489	718216	0.0011	15814	0.6619	2.079296
7	I1:1 I 64 ; I2:4 I 32	718216	200572	0.0489	718216	0.0011	15814	0.3404	1.583693
8	I1:1 I 64 ; I2:4 I 64	718216	200572	0.0489	718216	0.0011	15814	0.729	2.182608
9	I1:1 I 64 ; I2:8 I 32	718216	200572	0.0489	718216	0.0011	15814	0.3429	1.587495
10	I1:1 I 64 ; I2:8 I 64	718216	200572	0.0489	718216	0.0011	15814	0.662	2.079394
11	I1:1 I 64 ; I2:1 f 32	718216	200572	0.0489	718216	0.0011	15814	0.3404	1.583693
12	I1:1 I 64 ; I2:1 f 64	718216	200572	0.0489	718216	0.0011	15814	0.6619	2.079296
13	I1:1 I 64 ; I2:2 f 32	718216	200572	0.0489	718216	0.0011	15814	0.3404	1.583693
14	I1:1 I 64 ; I2:2 f 64	718216	200572	0.0489	718216	0.0011	15814	0.6619	2.079296
15	I1:1 I 64 ; I2:4 f 32	718216	200572	0.0489	718216	0.0011	15814	0.3404	1.583693
16	I1:1 I 64 ; I2:4 f 64	718216	200572	0.0489	718216	0.0011	15814	0.729	2.182608
17	I1:1 I 64 ; I2:8 f 32	718216	200572	0.0489	718216	0.0011	15814	0.3429	1.587495
18	I1:1 I 64 ; I2:8 f 64	718216	200572	0.0489	718216	0.0011	15814	0.6904	2.123155
19	I1:1 I 64 ; I2:1 r 32	718216	200572	0.0489	718216	0.0011	15814	0.3414	1.585253
20	I1:1 I 64 ; I2:1 r 64	718216	200572	0.0489	718216	0.0011	15814	0.6754	2.100056
21	I1:1 I 64 ; I2:2 r 32	718216	200572	0.0489	718216	0.0011	15814	0.341	1.584571
22	I1:1 I 64 ; I2:2 r 64	718216	200572	0.0489	718216	0.0011	15814	0.669	2.090212
23	I1:1 I 64 ; I2:4 r 32	718216	200572	0.0489	718216	0.0011	15814	0.3406	1.583986
24	I1:1 I 64 ; I2:8 r 32	718216	200572	0.025	718216	0.0006	8134	0.729	1.608402
25	I1:2 I 32 ; I2:1 I 32	718216	200572	0.025	718216	0.0006	8134	0.6622	1.555382
26	I1:2 I 32 ; I2:2 I 32	718216	200572	0.025	718216	0.0006	8134	0.6618	1.555089
27	**I1:2 I 32 ; I2:4 I 32**	**718216**	**200572**	**0.025**	**718216**	**0.0006**	**8134**	**0.6618**	**1.555089**
28	I1:2 I 32 ; I2:8 I 32	718216	200572	0.025	718216	0.0006	8134	0.729	1.608402
29	I1:2 I 32 ; I2:1 f 32	718216	200572	0.025	718216	0.0006	8134	0.6622	1.555382
30	I1:2 I 32 ; I2:2 f 32	718216	200572	0.025	718216	0.0006	8134	0.6618	1.555089
31	I1:2 I 32 ; I2:4 f 32	718216	200572	0.025	718216	0.0006	8134	0.6618	1.555089
32	I1:2 I 32 ; I2:8 f 32	718216	200572	0.025	718216	0.0006	8134	0.729	1.608402
33	I1:2 I 32 ; I2:1 r 32	718216	200572	0.025	718216	0.0006	8134	0.6906	1.577896
34	I1:2 I 32 ; I2:2 r 32	718216	200572	0.025	718216	0.0006	8134	0.6751	1.565615
35	I1:2 I 32 ; I2:4 r 32	718216	200572	0.025	718216	0.0006	8134	0.6666	1.55889
36	I1:2 I 32 ; I2:4 r 64	718216	200572	0.0489	718216	0.0011	15816	0.9237	2.482905
37	I1:2 I 32 ; I2:8 r 32	718216	200572	0.0489	718216	0.0011	15816	0.4167	1.701343
38	I1:2 I 32 ; I2:8 r 64	718216	200572	0.0489	718216	0.0011	15816	0.7911	2.278523
39	I1:2 I 64 ; I2:1 I 32	718216	200572	0.0489	718216	0.0011	15816	0.3413	1.585167
40	I1:2 I 64 ; I2:1 I 64	718216	200572	0.0489	718216	0.0011	15816	0.6619	2.079308
41	I1:2 I 64 ; I2:2 I 32	718216	200572	0.0489	718216	0.0011	15816	0.3404	1.583705
42	I1:2 I 64 ; I2:2 I 64	718216	200572	0.0489	718216	0.0011	15816	0.6619	2.079308
43	I1:2 I 64 ; I2:4 I 32	718216	200572	0.0489	718216	0.0011	15816	0.3404	1.583705
44	I1:2 I 64 ; I2:4 I 64	718216	200572	0.0489	718216	0.0011	15816	0.9237	2.482905
45	I1:2 I 64 ; I2:8 I 32	718216	200572	0.0489	718216	0.0011	15816	0.4167	1.701343
46	I1:2 I 64 ; I2:8 I 64	718216	200572	0.0489	718216	0.0011	15816	0.7282	2.181645

3)For GCC benchmark:

a) Both L1 and L2 have separate memory:

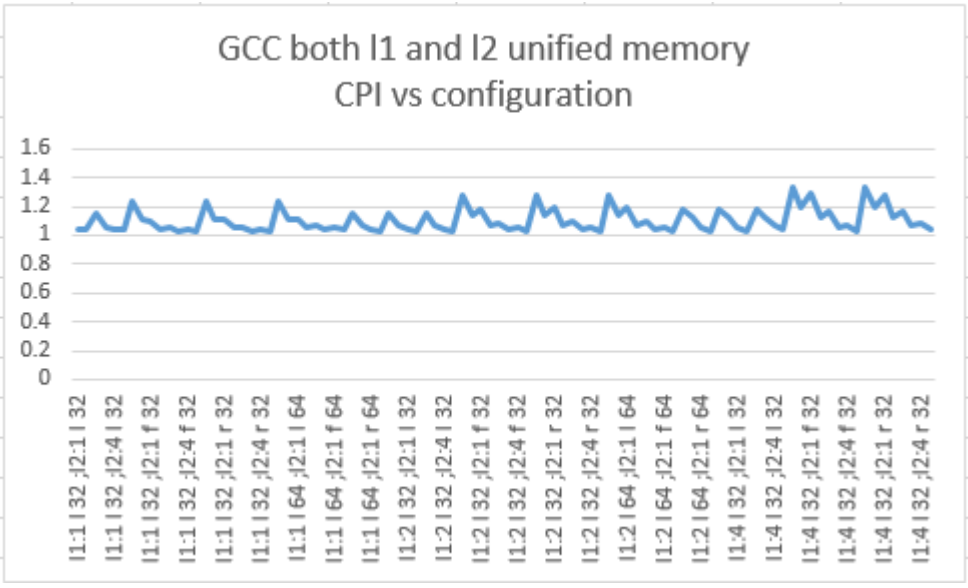


The above figure shows CPI as a function of various configurations. For the configuration **l1:2l32 ; l2: 8l64** the lowest value of CPI observed is 1.0365646. L1 is 2-way set associative and L2 is 8-way set associative. The replacement policy for L1 and L2 is LRU.

The values are tabulated as below:

	A	B	C	D	E	F	G	H	I	J	K
1	configuration	# of instructi	dl1 accesses	dl1 missra	dl2 access	dl2 missra	il1 access	il1 missrate	il2 access	il2 missrat	CPI
2	I1:1l64 ; I2: 2f64	337327098	124102798	0.0099	1613361	0.0613	337327098	0.004	1363326	0.024	1.057997
3	I1:1l64 ; I2: 4f64	337327098	124102798	0.0099	1613361	0.0447	337327098	0.004	1363326	0.008	1.04789
4	I1:1l64 ; I2: 8f64	337327098	124102798	0.0099	1613361	0.0308	337327098	0.004	1363326	0.008	1.043254
5	I1:1l64 ; I2: 1r64	337327098	124102798	0.0099	1613361	0.1913	337327098	0.004	1363326	0.2815	1.174359
6	I1:1l64 ; I2: 2r64	337327098	124102798	0.0099	1613361	0.0657	337327098	0.004	1363326	0.0241	1.059474
7	I1:1l64 ; I2: 4r64	337327098	124102798	0.0099	1613361	0.0475	337327098	0.004	1363326	0.0089	1.049085
8	I1:1l64 ; I2: 8r64	337327098	124102798	0.0099	1613361	0.0392	337327098	0.004	1363326	0.0084	1.046182
9	I1:2l32 ; I2: 1l32	337327098	124102798	0.0075	1348871	0.4056	337327098	0.0032	1095234	0.5633	1.265528
10	I1:2l32 ; I2: 1l64	337327098	124102798	0.0075	1348871	0.1752	337327098	0.0032	1095234	0.1893	1.116037
11	I1:2l32 ; I2: 2l32	337327098	124102798	0.0075	1348871	0.1823	337327098	0.0032	1095234	0.1943	1.119155
12	I1:2l32 ; I2: 2l64	337327098	124102798	0.0075	1348871	0.07	337327098	0.0032	1095234	0.0293	1.050218
13	I1:2l32 ; I2: 4l32	337327098	124102798	0.0075	1348871	0.1227	337327098	0.0032	1095234	0.0264	1.064302
14	I1:2l32 ; I2: 4l64	337327098	124102798	0.0075	1348871	0.0521	337327098	0.0032	1095234	0.01	1.040805
15	I1:2l32 ; I2: 8l32	337327098	124102798	0.0075	1348871	0.0989	337327098	0.0032	1095234	0.018	1.055753
16	**I1:2l32 ; I2: 8l64**	**337327098**	**124102798**	**0.0075**	**1348871**	**0.0369**	**337327098**	**0.0032**	**1095234**	**0.01**	**1.036546**
17	I1:2l32 ; I2: 1f32	337327098	124102798	0.0075	1348871	0.4056	337327098	0.0032	1095234	0.5633	1.265528
18	I1:2l32 ; I2: 1f64	337327098	124102798	0.0075	1348871	0.1752	337327098	0.0032	1095234	0.1893	1.116037
19	I1:2l32 ; I2: 2f32	337327098	124102798	0.0075	1348871	0.191	337327098	0.0032	1095234	0.1956	1.121902
20	I1:2l32 ; I2: 2f64	337327098	124102798	0.0075	1348871	0.0733	337327098	0.0032	1095234	0.0297	1.051233
21	I1:2l32 ; I2: 4f32	337327098	124102798	0.0075	1348871	0.1298	337327098	0.0032	1095234	0.0267	1.066357
22	I1:2l32 ; I2: 4f64	337327098	124102798	0.0075	1348871	0.0534	337327098	0.0032	1095234	0.01	1.041191
23	I1:2l32 ; I2: 8f32	337327098	124102798	0.0075	1348871	0.1014	337327098	0.0032	1095234	0.018	1.056446
24	I1:2l32 ; I2: 8f64	337327098	124102798	0.0075	1348871	0.0369	337327098	0.0032	1095234	0.01	1.036548
25	I1:2l32 ; I2: 1r32	337327098	124102798	0.0075	1348871	0.4056	337327098	0.0032	1095234	0.5633	1.265528
26	I1:2l32 ; I2: 1r64	337327098	124102798	0.0075	1348871	0.1752	337327098	0.0032	1095234	0.1893	1.116037
27	I1:2l32 ; I2: 2r32	337327098	124102798	0.0075	1348871	0.2063	337327098	0.0032	1095234	0.1799	1.122584
28	I1:2l32 ; I2: 2r64	337327098	124102798	0.0075	1348871	0.0791	337327098	0.0032	1095234	0.0287	1.052624
29	I1:2l32 ; I2: 4r32	337327098	124102798	0.0075	1348871	0.1386	337327098	0.0032	1095234	0.0304	1.069685
30	I1:2l32 ; I2: 4r64	337327098	124102798	0.0075	1348871	0.057	337327098	0.0032	1095234	0.0111	1.04244
31	I1:2l32 ; I2: 8r32	337327098	124102798	0.0075	1348871	0.1093	337327098	0.0032	1095234	0.0203	1.059171
32	I1:2l32 ; I2: 8r64	337327098	124102798	0.0075	1348871	0.0469	337327098	0.0032	1095234	0.0104	1.039462
33	I1:2l64 ; I2: 1l64	337327098	124102798	0.0055	958736	0.3929	337327098	0.0023	759280	0.5613	1.183757
34	I1:2l64 ; I2: 2l64	337327098	124102798	0.0055	958736	0.1552	337327098	0.0023	759280	0.1982	1.079257
35	I1:2l64 ; I2: 4l64	337327098	124102798	0.0055	958736	0.0935	337327098	0.0023	759280	0.0254	1.039758
36	I1:2l64 ; I2: 8l64	337327098	124102798	0.0055	958736	0.0723	337327098	0.0023	759280	0.0144	1.033797
37	I1:2l64 ; I2: 1f64	337327098	124102798	0.0055	958736	0.3929	337327098	0.0023	759280	0.5613	1.183757
38	I1:2l64 ; I2: 2f64	337327098	124102798	0.0055	958736	0.1637	337327098	0.0023	759280	0.2011	1.08141
39	I1:2l64 ; I2: 4f64	337327098	124102798	0.0055	958736	0.1008	337327098	0.0023	759280	0.0259	1.041276
40	I1:2l64 ; I2: 8f64	337327098	124102798	0.0055	958736	0.0744	337327098	0.0023	759280	0.0144	1.034213
41	I1:2l64 ; I2: 1r64	337327098	124102798	0.0055	958736	0.3929	337327098	0.0023	759280	0.5613	1.183757
42	I1:2l64 ; I2: 2r64	337327098	124102798	0.0055	958736	0.1773	337327098	0.0023	759280	0.1834	1.081325
43	I1:2l64 ; I2: 4r64	337327098	124102798	0.0055	958736	0.1088	337327098	0.0023	759280	0.0284	1.043264
44	I1:4l32 ; I2: 1l32	337327098	124102798	0.0063	1179975	0.6681	337327098	0.0025	850527	0.8651	1.335697
45	I1:4l32 ; I2: 1l64	337327098	124102798	0.0063	1179975	0.3069	337327098	0.0025	850527	0.401	1.165357
46	I1:4l32 ; I2: 2l32	337327098	124102798	0.0063	1179975	0.3777	337327098	0.0025	850527	0.6009	1.217968

b) Both L1 and L2 are unified memory:

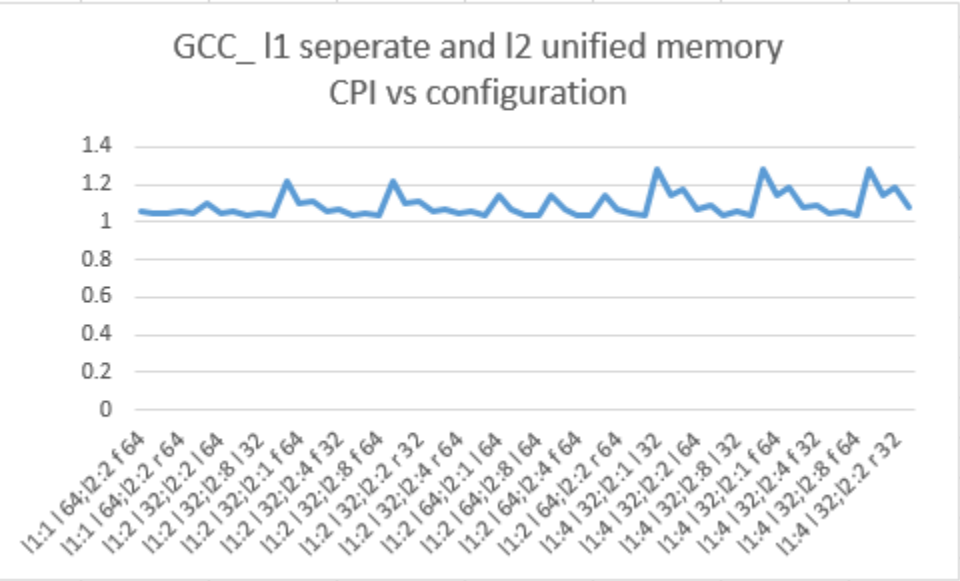


The above figure shows CPI as a function of various configurations. For the configuration **l1:1 l 32 ;l2:4 f 64**, the lowest value of CPI observed is L1 is 1.032631. L1 is 1-way set associative and L2 4-way associative. The replacement policy for L1 is LRU and L2 is FIFO.

The values are tabulated as below:

1	configuration	# of instruction	ul1 accesses	ul1 missrate	ul2 access	ul2 missra	CPI
2	l1:1 l 32 ;l2:1 l 32	337327098	461429896	0.0051	2769945	0.0227	1.041196
3	l1:1 l 32 ;l2:1 l 64	337327098	461429896	0.0051	2769945	0.0219	1.040696
4	l1:1 l 32 ;l2:2 l 32	337327098	461429896	0.0051	2769945	0.2211	1.155212
5	l1:1 l 32 ;l2:2 l 64	337327098	461429896	0.0051	2769945	0.0527	1.058429
6	l1:1 l 32 ;l2:4 l 32	337327098	461429896	0.0051	2769945	0.0295	1.045087
7	l1:1 l 32 ;l2:4 l 64	337327098	461429896	0.0051	2769945	0.0254	1.042709
8	l1:1 l 32 ;l2:8 l 32	337327098	461429896	0.0037	2128973	0.4723	1.228703
9	l1:1 l 32 ;l2:8 l 64	337327098	461429896	0.0037	2128973	0.2082	1.112034
10	l1:1 l 32 ;l2:1 f 32	337327098	461429896	0.0037	2128973	0.1875	1.102909
11	l1:1 l 32 ;l2:1 f 64	337327098	461429896	0.0037	2128973	0.0604	1.046727
12	l1:1 l 32 ;l2:2 f 32	337327098	461429896	0.0037	2128973	0.0798	1.05532
13	l1:1 l 32 ;l2:2 f 64	337327098	461429896	0.0037	2128973	0.0293	1.032989
14	l1:1 l 32 ;l2:4 f 32	337327098	461429896	0.0037	2128973	0.0558	1.044728
15	**l1:1 l 32 ;l2:4 f 64**	**337327098**	**461429896**	**0.0037**	**2128973**	**0.0285**	**1.032631**
16	l1:1 l 32 ;l2:8 f 32	337327098	461429896	0.0037	2128973	0.4723	1.228703
17	l1:1 l 32 ;l2:8 f 64	337327098	461429896	0.0037	2128973	0.2082	1.112034
18	l1:1 l 32 ;l2:1 r 32	337327098	461429896	0.0037	2128973	0.1969	1.107059
19	l1:1 l 32 ;l2:1 r 64	337327098	461429896	0.0037	2128973	0.064	1.048329
20	l1:1 l 32 ;l2:2 r 32	337327098	461429896	0.0037	2128973	0.0857	1.057909
21	l1:1 l 32 ;l2:2 r 64	337327098	461429896	0.0037	2128973	0.0296	1.033136
22	l1:1 l 32 ;l2:4 r 32	337327098	461429896	0.0037	2128973	0.0561	1.044843
23	l1:1 l 32 ;l2:4 r 64	337327098	461429896	0.0037	2128973	0.0285	1.032631
24	l1:1 l 32 ;l2:8 r 32	337327098	461429896	0.0037	2128973	0.4723	1.228703
25	l1:1 l 32 ;l2:8 r 64	337327098	461429896	0.0037	2128973	0.2082	1.112034
26	l1:1 l 64 ;l2:1 l 64	337327098	461429896	0.0037	2128973	0.2052	1.110734
27	l1:1 l 64 ;l2:2 l 64	337327098	461429896	0.0037	2128973	0.0696	1.050785
28	l1:1 l 64 ;l2:4 l 64	337327098	461429896	0.0037	2128973	0.0981	1.06341
29	l1:1 l 64 ;l2:8 l 64	337327098	461429896	0.0037	2128973	0.0385	1.037083
30	l1:1 l 64 ;l2:1 f 64	337327098	461429896	0.0037	2128973	0.0735	1.052528
31	l1:1 l 64 ;l2:2 f 64	337327098	461429896	0.0037	2128973	0.0329	1.034608
32	l1:1 l 64 ;l2:4 f 64	337327098	461429896	0.0027	1504835	0.46	1.158228
33	l1:1 l 64 ;l2:8 f 64	337327098	461429896	0.0027	1504835	0.1703	1.06778
34	l1:1 l 64 ;l2:1 r 64	337327098	461429896	0.0027	1504835	0.062	1.033962
35	l1:1 l 64 ;l2:2 r 64	337327098	461429896	0.0027	1504835	0.0414	1.027523
36	l1:1 l 64 ;l2:4 r 64	337327098	461429896	0.0027	1504835	0.46	1.158228
37	l1:1 l 64 ;l2:8 r 64	337327098	461429896	0.0027	1504835	0.1797	1.070714
38	l1:2 l 32 ;l2:1 l 32	337327098	461429896	0.0027	1504835	0.0681	1.035872
39	l1:2 l 32 ;l2:1 l 64	337327098	461429896	0.0027	1504835	0.0417	1.027626
40	l1:2 l 32 ;l2:2 l 32	337327098	461429896	0.0027	1504835	0.46	1.158228
41	l1:2 l 32 ;l2:2 l 64	337327098	461429896	0.0027	1504835	0.1863	1.072771
42	l1:2 l 32 ;l2:4 l 32	337327098	461429896	0.0027	1504835	0.0785	1.039108
43	l1:2 l 32 ;l2:4 l 64	337327098	461429896	0.0027	1504835	0.0556	1.031964
44	l1:2 l 32 ;l2:8 l 32	337327098	461429896	0.003	1760696	0.7305	1.283054

c) L1 separate memory and L2 unified memory:



The above figure shows CPI as a function of various configurations. For the configuration **l1:1 l 32;l2:4 r 32** the lowest value of CPI observed is 1.063657. L1 is 1-way set associative and L2 is 4-way set associative. The replacement policy used for L1 is LRU and L2 is Random.

The values are tabulated as below:

	A	B	C	D	E	F	G	H	I
1	Configuration	# of instructions	dl1 access	dl1 missra	il1 access	il1 missrat	dl2 access	dl2 missra	CPI
2	l1:1 l 32;l2:1 l 32	337327098	1.24E+08	0.012	3992178	0.0208	3.37E+08	0.0058	1.057966
3	l1:1 l 32;l2:1 l 64	337327098	1.24E+08	0.012	3992178	0.0382	3.37E+08	0.0058	1.072447
4	l1:1 l 32;l2:2 l 32	337327098	1.24E+08	0.012	3992178	0.0176	3.37E+08	0.0058	1.055348
5	l1:1 l 32;l2:2 l 64	337327098	1.24E+08	0.012	3992178	0.0335	3.37E+08	0.0058	1.068506
6	l1:1 l 32;l2:4 l 32	337327098	1.24E+08	0.012	3992178	0.0163	3.37E+08	0.0058	1.054257
7	l1:1 l 32;l2:4 l 64	337327098	1.24E+08	0.0099	2976687	0.1459	3.37E+08	0.004	1.120814
8	l1:1 l 32;l2:8 l 32	337327098	1.24E+08	0.0099	2976687	0.0422	3.37E+08	0.004	1.05673
9	l1:1 l 32;l2:8 l 64	337327098	1.24E+08	0.0099	2976687	0.0209	3.37E+08	0.004	1.043597
10	l1:1 l 32;l2:1 f 32	337327098	1.24E+08	0.0099	2976687	0.0204	3.37E+08	0.004	1.043244
11	l1:1 l 32;l2:1 f 64	337327098	1.24E+08	0.0099	2976687	0.1459	3.37E+08	0.004	1.120814
12	l1:1 l 32;l2:2 f 32	337327098	1.24E+08	0.0099	2976687	0.0446	3.37E+08	0.004	1.05819
13	l1:1 l 32;l2:2 f 64	337327098	1.24E+08	0.0099	2976687	0.0212	3.37E+08	0.004	1.043735
14	l1:1 l 32;l2:4 f 32	337327098	1.24E+08	0.0099	2976687	0.0204	3.37E+08	0.004	1.043244
15	l1:1 l 32;l2:4 f 64	337327098	1.24E+08	0.0099	2976687	0.0477	3.37E+08	0.004	1.060124
16	l1:1 l 32;l2:8 f 32	337327098	1.24E+08	0.0099	2976687	0.0235	3.37E+08	0.004	1.045191
17	l1:1 l 32;l2:8 f 64	337327098	1.24E+08	0.0075	2444105	0.1534	3.37E+08	0.0032	1.101774
18	l1:1 l 32;l2:1 r 32	337327098	1.24E+08	0.0075	2444105	0.0518	3.37E+08	0.0032	1.050233
19	l1:1 l 32;l2:1 r 64	337327098	1.24E+08	0.0075	2444105	0.0698	3.37E+08	0.0032	1.059355
20	l1:1 l 32;l2:2 r 32	337327098	1.24E+08	0.0075	2444105	0.0255	3.37E+08	0.0032	1.036892
21	l1:1 l 32;l2:2 r 64	337327098	1.24E+08	0.0075	2444105	0.0486	3.37E+08	0.0032	1.048632
22	**l1:1 l 32;l2:4 r 32**	**337327098**	**1.24E+08**	**0.0075**	**2444105**	**0.0248**	**3.37E+08**	**0.0032**	**1.036537**
23	l1:1 l 32;l2:4 r 64	337327098	1.24E+08	0.0075	2444105	0.3724	3.37E+08	0.0032	1.212847
24	l1:1 l 32;l2:8 r 32	337327098	1.24E+08	0.0075	2444105	0.1534	3.37E+08	0.0032	1.101774

25	l1:1 l 32;l2:8 r 64	337327098	1.24E+08	0.0075	2444105	0.1636	3.37E+08	0.0032	1.106947
26	l1:1 l 64;l2:1 l 64	337327098	1.24E+08	0.0075	2444105	0.0541	3.37E+08	0.0032	1.051411
27	l1:1 l 64;l2:2 l 64	337327098	1.24E+08	0.0075	2444105	0.0745	3.37E+08	0.0032	1.061731
28	l1:1 l 64;l2:4 l 64	337327098	1.24E+08	0.0075	2444105	0.0258	3.37E+08	0.0032	1.037031
29	l1:1 l 64;l2:8 l 64	337327098	1.24E+08	0.0075	2444105	0.0488	3.37E+08	0.0032	1.048738
30	l1:1 l 64;l2:1 f 64	337327098	1.24E+08	0.0075	2444105	0.0248	3.37E+08	0.0032	1.036537
31	l1:1 l 64;l2:2 f 64	337327098	1.24E+08	0.0075	2444105	0.3724	3.37E+08	0.0032	1.212847
32	l1:1 l 64;l2:4 f 64	337327098	1.24E+08	0.0075	2444105	0.1534	3.37E+08	0.0032	1.101774
33	l1:1 l 64;l2:8 f 64	337327098	1.24E+08	0.0075	2444105	0.1699	3.37E+08	0.0032	1.110116
34	l1:1 l 64;l2:2 r 64	337327098	1.24E+08	0.0075	2444105	0.0582	3.37E+08	0.0032	1.053496
35	l1:1 l 64;l2:8 r 64	337327098	1.24E+08	0.0075	2444105	0.085	3.37E+08	0.0032	1.067086
36	l1:2 l 32;l2:1 l 64	337327098	1.24E+08	0.0075	2444105	0.0337	3.37E+08	0.0032	1.041058
37	l1:2 l 32;l2:2 l 64	337327098	1.24E+08	0.0075	2444105	0.0641	3.37E+08	0.0032	1.056449
38	l1:2 l 32;l2:4 l 32	337327098	1.24E+08	0.0075	2444105	0.0287	3.37E+08	0.0032	1.038517
39	l1:2 l 32;l2:4 l 64	337327098	1.24E+08	0.0055	1718016	0.3533	3.37E+08	0.0023	1.14309
40	l1:2 l 32;l2:8 l 32	337327098	1.24E+08	0.0055	1718016	0.1415	3.37E+08	0.0023	1.067606
41	l1:2 l 32;l2:8 l 64	337327098	1.24E+08	0.0055	1718016	0.0546	3.37E+08	0.0023	1.0366
42	l1:2 l 32;l2:1 f 32	337327098	1.24E+08	0.0055	1718016	0.0363	3.37E+08	0.0023	1.030081
43	l1:2 l 32;l2:1 f 64	337327098	1.24E+08	0.0055	1718016	0.3533	3.37E+08	0.0023	1.14309
44	l1:2 l 32;l2:2 f 32	337327098	1.24E+08	0.0055	1718016	0.1485	3.37E+08	0.0023	1.070108
45	l1:2 l 32;l2:2 f 64	337327098	1.24E+08	0.0055	1718016	0.0595	3.37E+08	0.0023	1.038362
46	l1:2 l 32;l2:4 f 32	337327098	1.24E+08	0.0055	1718016	0.0365	3.37E+08	0.0023	1.030177

6. PART 4: Cost function definition:

In this section, we have taken arbitrary weights for different parameters of cache and defined the cost function. The design choice has to be made based on this cost function.
The weights of different parameters are:

- Performance:
    - Replacement policy: As the system is less complex, the cost is less
        - LRU-l = 20
        - FIFI-f= 10
        - Random= 5
    - Block size: As the size of the block increases, the cost increases
        - 32 bytes=10
        - 64 bytes=20
    - Associativity: It is given by A'=2*ln(A+1), where A is the associativity
        - 1-way
        - 2-way
        - 4-way
        - 8-way
    - CPI: It is taken from the previous table
- Overhead of the cache: The size of cache levels are considered
    - L1:
        - 128KB=12.5
        - 256KB= 25
    - L2:
        - 512KB=15
        - 1MB=30

The cost function is given by:

Cost function=Cost weights(performance+overhead due to size)

i.e., Cost function= ((Cost weights(block size)+Cost weights(replacement policy)+A')/CPI) + (overhead of L1 cache+ overhead of L2 cache)

7: PART 5: Optimization of cache based on performance and cache:

Using the above formula, the values of cost function for different configuration for all the 3 benchmarks are calculated and tabulated. The graphs for CPI vs Configuration and Cost function vs Configuration are compared to find the optimal cost value.

It can be found that not in all cases the minimum cost is the optimum cost of the system.

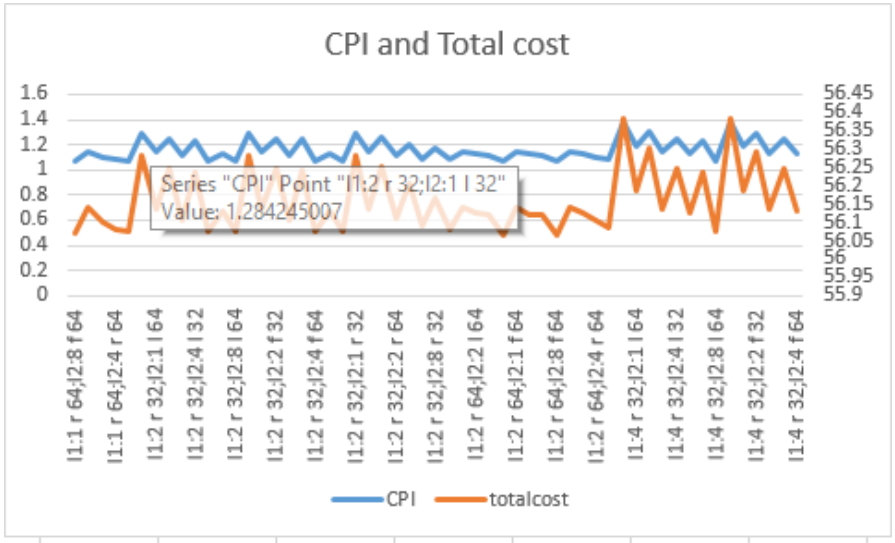
The optimum value is taken such that both CPI and total cost are near minimum hence reducing the CPI cost product.

The table and graphs for various benchmarks are as follows:

1) Anagram:

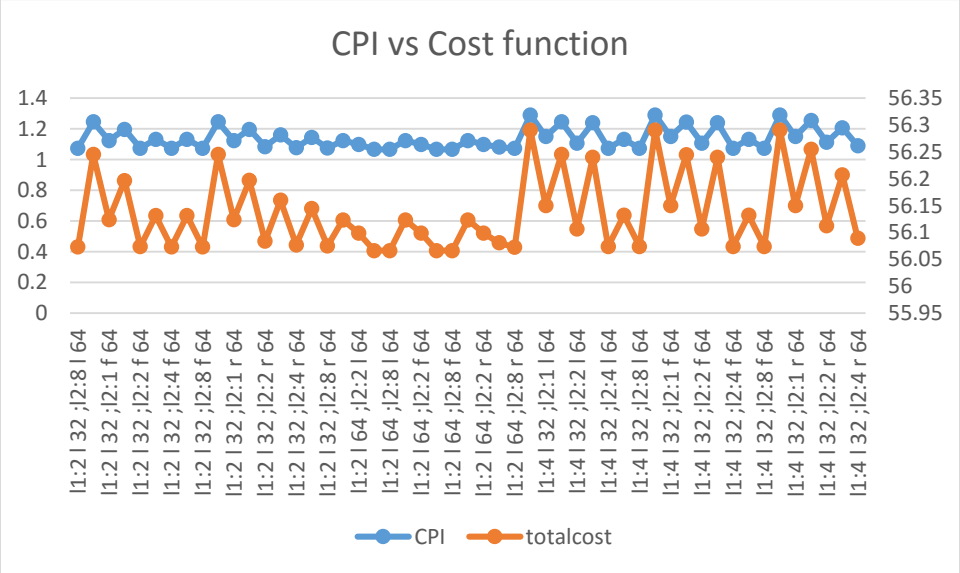
a) Both L1 and L2 separate memories: It is found that the optimal cost with minimum CPI is obtained at configuration l1:4 r 32;l2:1 l 64. The 4 way associative L1 cache has random replacement policy and 1 way associative L2 has LRU with CPI=1.1877 and optimal total cost =56.18771.

Configuration	CPI	totalcost
l1:1 r 64;l2:8 f 64	1.068767	56.06877
l1:1 r 64;l2:1 r 64	1.141799	56.1418
l1:1 r 64;l2:2 r 64	1.101115	56.10111
l1:1 r 64;l2:4 r 64	1.082765	56.08276
l1:1 r 64;l2:8 r 64	1.075205	56.07521
l1:2 r 32;l2:1 l 32	1.284245	56.28425
l1:2 r 32;l2:1 l 64	1.137926	56.13793
l1:2 r 32;l2:2 l 32	1.246993	56.24699
l1:2 r 32;l2:2 l 64	1.10743	56.10743
l1:2 r 32;l2:4 l 32	1.23817	56.23817
l1:2 r 32;l2:4 l 64	1.075254	56.07525
l1:2 r 32;l2:8 l 32	1.133512	56.13351
l1:2 r 32;l2:8 l 64	1.075254	56.07525
l1:2 r 32;l2:1 f 32	1.284245	56.28425
l1:2 r 32;l2:1 f 64	1.137926	56.13793
l1:2 r 32;l2:2 f 32	1.24594	56.24594
l1:2 r 32;l2:2 f 64	1.107659	56.10766
l1:2 r 32;l2:4 f 32	1.240672	56.24067
l1:2 r 32;l2:4 f 64	1.075254	56.07525
l1:2 r 32;l2:8 f 32	1.133512	56.13351
l1:2 r 32;l2:8 f 64	1.075254	56.07525
l1:2 r 32;l2:1 r 32	1.284681	56.28468
l1:2 r 32;l2:1 r 64	1.13821	56.13821
l1:2 r 32;l2:2 r 32	1.2536	56.2536
l1:2 r 32;l2:2 r 32	1.2536	56.2536
l1:2 r 32;l2:2 r 64	1.109547	56.10955
l1:2 r 32;l2:4 r 32	1.207123	56.20712
l1:2 r 32;l2:4 r 64	1.089957	56.08996
l1:2 r 32;l2:8 r 32	1.167968	56.16797
l1:2 r 32;l2:8 r 64	1.081767	56.08177
l1:2 r 64;l2:1 l 64	1.143454	56.14345
l1:2 r 64;l2:2 l 64	1.124158	56.12416
l1:2 r 64;l2:4 l 64	1.119629	56.11963
l1:2 r 64;l2:8 l 64	1.067148	56.06715
l1:2 r 64;l2:1 f 64	1.143454	56.14345
l1:2 r 64;l2:2 f 64	1.123526	56.12353
l1:2 r 64;l2:4 f 64	1.120827	56.12083
l1:2 r 64;l2:8 f 64	1.067148	56.06715
l1:2 r 64;l2:1 r 64	1.143114	56.14311
l1:2 r 64;l2:2 r 64	1.127798	56.1278
l1:2 r 64;l2:4 r 64	1.104337	56.10434
l1:2 r 64;l2:8 r 64	1.08432	56.08432
l1:4 r 32;l2:1 l 32	1.383635	56.38364
l1:4 r 32;l2:1 l 64	**1.187707**	**56.18771**
l1:4 r 32;l2:2 l 32	1.304405	56.30441
l1:4 r 32;l2:2 l 64	1.136402	56.1364
l1:4 r 32;l2:4 l 32	1.249676	56.24968
l1:4 r 32;l2:4 l 64	1.126088	56.12609
l1:4 r 32;l2:8 l 32	1.238399	56.2384



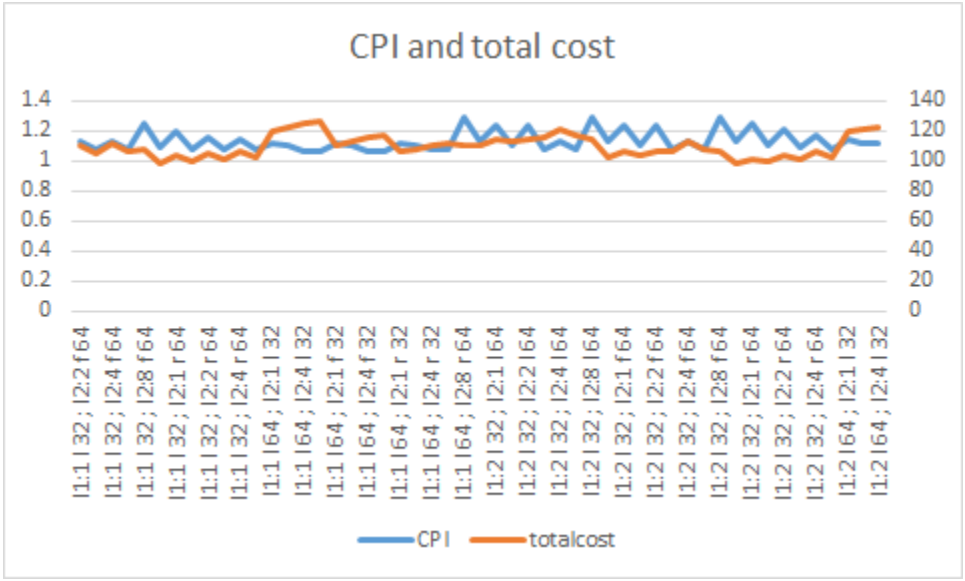
b) Both L1 and L2 unified memory: It is found that the optimal cost is obtained for the configuration L1:2 way associative with LRU policy and L2 4way associative with FIFO policy. The configuration is highlighted with CPI=1.066058 and optimal cost is 56.06606.

Configuration	CPI	totalcost
l1:2 l 32 ;l2:8 l 64	1.073094	56.07309
l1:2 l 32 ;l2:1 f 32	1.24503	56.24503
l1:2 l 32 ;l2:1 f 64	1.12395	56.12395
l1:2 l 32 ;l2:2 f 32	1.196438	56.19644
l1:2 l 32 ;l2:2 f 64	1.073605	56.07361
l1:2 l 32 ;l2:4 f 32	1.131351	56.13135
l1:2 l 32 ;l2:4 f 64	1.073094	56.07309
l1:2 l 32 ;l2:8 f 32	1.131351	56.13135
l1:2 l 32 ;l2:8 f 64	1.073094	56.07309
l1:2 l 32 ;l2:1 r 32	1.24503	56.24503
l1:2 l 32 ;l2:1 r 64	1.12395	56.12395
l1:2 l 32 ;l2:2 r 32	1.196928	56.19693
l1:2 l 32 ;l2:2 r 64	1.083824	56.08382
l1:2 l 32 ;l2:4 r 32	1.160015	56.16001
l1:2 l 32 ;l2:4 r 64	1.076918	56.07692
l1:2 l 32 ;l2:8 r 32	1.144327	56.14433
l1:2 l 32 ;l2:8 r 64	1.074697	56.0747
l1:2 l 64 ;l2:1 l 64	1.123274	56.12327
l1:2 l 64 ;l2:2 l 64	1.098819	56.09882
l1:2 l 64 ;l2:4 l 64	1.066061	56.06606
l1:2 l 64 ;l2:8 l 64	1.066058	56.06606
l1:2 l 64 ;l2:1 f 64	1.123274	56.12327
l1:2 l 64 ;l2:2 f 64	1.098819	56.09882
l1:2 l 64 ;l2:4 f 64	**1.066058**	**56.06606**
l1:2 l 64 ;l2:8 f 64	1.066058	56.06606
l1:2 l 64 ;l2:1 r 64	1.123274	56.12327
l1:2 l 64 ;l2:2 r 64	1.098923	56.09892
l1:2 l 64 ;l2:4 r 64	1.080847	56.08085
l1:2 l 64 ;l2:8 r 64	1.072478	56.07248
l1:4 l 32 ;l2:1 l 32	1.290426	56.29043
l1:4 l 32 ;l2:1 l 64	1.149744	56.14974
l1:4 l 32 ;l2:2 l 32	1.245106	56.24511
l1:4 l 32 ;l2:2 l 64	1.106612	56.10661
l1:4 l 32 ;l2:4 l 32	1.23966	56.23966
l1:4 l 32 ;l2:4 l 64	1.073774	56.07377
l1:4 l 32 ;l2:8 l 32	1.132029	56.13203
l1:4 l 32 ;l2:8 l 64	1.073772	56.07377
l1:4 l 32 ;l2:1 f 32	1.290426	56.29043
l1:4 l 32 ;l2:1 f 64	1.149744	56.14974
l1:4 l 32 ;l2:2 f 32	1.24446	56.24446
l1:4 l 32 ;l2:2 f 64	1.106593	56.10659
l1:4 l 32 ;l2:4 f 32	1.239657	56.23966
l1:4 l 32 ;l2:4 f 64	1.073772	56.07377
l1:4 l 32 ;l2:8 f 32	1.132029	56.13203
l1:4 l 32 ;l2:8 f 64	1.073772	56.07377
l1:4 l 32 ;l2:1 r 32	1.290426	56.29043
l1:4 l 32 ;l2:1 r 64	1.149744	56.14974
l1:4 l 32 ;l2:2 r 32	1.255012	56.25501



c) L1 separate and L2 unified memory: The optimum value for cost and CPI combined is obtained at configuration l1:1 l 32; l2: 1 r 32. L1 cache is 1 way associative with LRU policy and L2 is 1 way associative with Random policy. The CPI obtained at this point is 1.097445 and optimal total cost is 98.53074

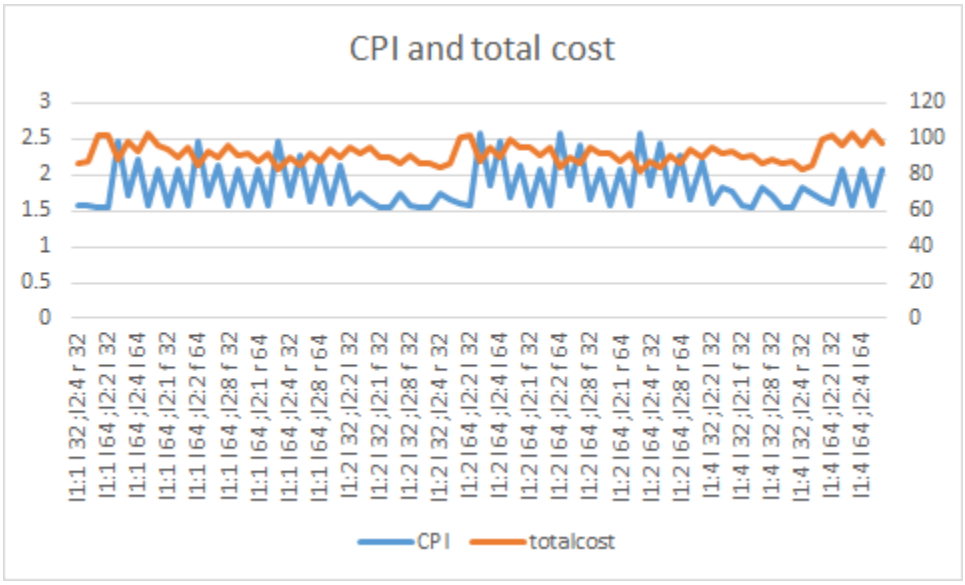
Configuration	CPI	totalcost
l1:1 l 32 ; l2:2 f 64	1.133805	111.0798
l1:1 l 32 ; l2:4 f 32	1.075548	105.7696
l1:1 l 32 ; l2:4 f 64	1.133805	111.9808
l1:1 l 32 ; l2:8 f 32	1.075548	106.8626
l1:1 l 32 ; l2:8 f 64	1.245763	107.8036
l1:1 l 32 ; l2:1 r 32	**1.097445**	**98.53074**
l1:1 l 32 ; l2:1 r 64	1.19852	103.2033
l1:1 l 32 ; l2:2 r 32	1.083748	99.82918
l1:1 l 32 ; l2:2 r 64	1.162414	105.3981
l1:1 l 32 ; l2:4 r 32	1.079032	100.9719
l1:1 l 32 ; l2:4 r 64	1.14672	106.9788
l1:1 l 32 ; l2:8 r 32	1.077008	102.1498
l1:1 l 64 ; l2:1 l 32	1.123382	119.7799
l1:1 l 64 ; l2:2 l 32	1.099672	121.9141
l1:1 l 64 ; l2:4 l 32	1.067255	124.9038
l1:1 l 64 ; l2:8 l 32	1.067255	126.0053
l1:1 l 64 ; l2:1 f 32	1.123382	110.8782
l1:1 l 64 ; l2:2 f 32	1.099672	112.8205
l1:1 l 64 ; l2:4 f 32	1.067255	115.5339
l1:1 l 64 ; l2:8 f 32	1.067255	116.6354
l1:1 l 64 ; l2:1 r 32	1.123382	106.4274
l1:1 l 64 ; l2:2 r 32	1.099737	108.2705
l1:1 l 64 ; l2:4 r 32	1.081374	110.1198
l1:1 l 64 ; l2:8 r 32	1.073631	111.6123
l1:1 l 64 ; l2:8 r 64	1.28759	109.9715
l1:2 l 32 ; l2:1 l 32	1.131767	111.1808
l1:2 l 32 ; l2:1 l 64	1.245303	114.0888
l1:2 l 32 ; l2:2 l 32	1.10798	113.1188
l1:2 l 32 ; l2:2 l 64	1.240941	114.95
l1:2 l 32 ; l2:4 l 32	1.075517	115.8229
l1:2 l 32 ; l2:4 l 64	1.133775	121.5177
l1:2 l 32 ; l2:8 l 32	1.075517	116.916
l1:2 l 32 ; l2:8 l 64	1.28759	114.4845
l1:2 l 32 ; l2:1 f 32	1.131767	102.345
l1:2 l 32 ; l2:1 f 64	1.245208	106.0626



3) GO:

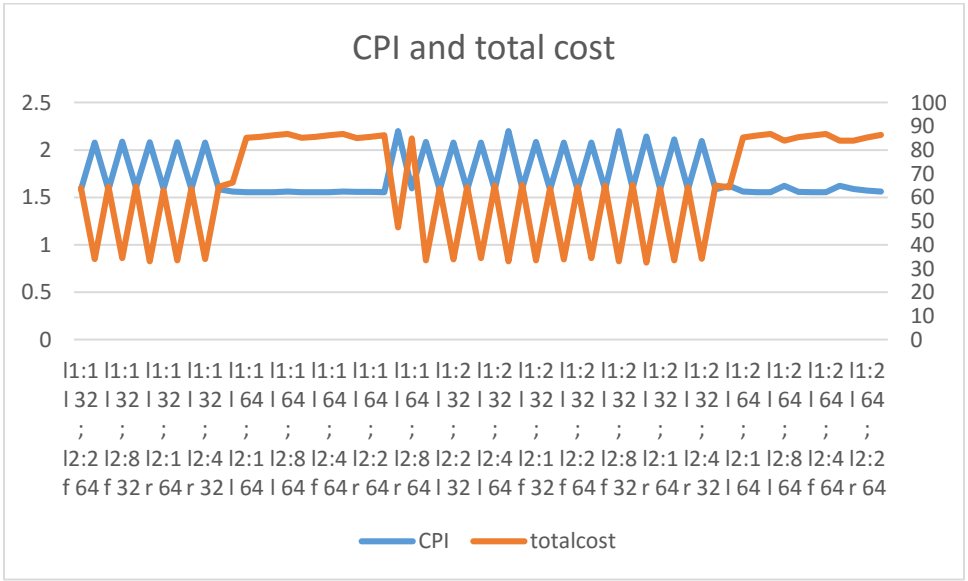
a) Both L1 and L2 separate memory: The optimum value of both CPI and cost is highlighted and is for the configuration l1:2 l 32 ;l2:1 f 32. Where, L1 is 2 way associative with LRU policy and L2 is 1 way with FIFO. The CPI is obtained as 1.55089277 and cost 89.456876

Configuration	CPI	totalcost
l1:1 l 32 ;l2:4 r 32	1.587984673	86.23781421
l1:1 l 32 ;l2:8 r 32	1.568004611	87.38558302
l1:1 l 64 ;l2:1 l 32	1.559915123	101.6516336
l1:1 l 64 ;l2:2 l 32	1.557381066	102.2482429
l1:1 l 64 ;l2:2 l 64	2.455603885	89.0378672
l1:1 l 64 ;l2:4 l 32	1.705718057	98.73827778
l1:1 l 64 ;l2:4 l 64	2.219936621	93.11152507
l1:1 l 64 ;l2:8 l 32	1.583693485	102.8506379
l1:1 l 64 ;l2:8 l 64	2.079296479	96.2546957
l1:1 l 64 ;l2:1 f 32	1.583693485	94.63682955
l1:1 l 64 ;l2:1 f 64	2.079296479	89.99865914
l1:1 l 64 ;l2:2 f 32	1.583693485	95.14887953
l1:1 l 64 ;l2:2 f 64	2.455603885	84.96554916
l1:1 l 64 ;l2:4 f 32	1.705718057	92.87564417
l1:1 l 64 ;l2:4 f 64	2.131634494	89.99904434
l1:1 l 64 ;l2:8 f 32	1.583693485	96.53628473
l1:1 l 64 ;l2:8 f 64	2.079296479	91.44537673
l1:1 l 64 ;l2:1 r 32	1.583693485	91.47965296
l1:1 l 64 ;l2:1 r 64	2.079296479	87.59399966
l1:1 l 64 ;l2:2 r 32	1.583693485	91.99170294
l1:1 l 64 ;l2:2 r 64	2.455603885	82.92939014
l1:1 l 64 ;l2:4 r 32	1.705718057	89.94432737
l1:1 l 64 ;l2:4 r 64	2.278804705	85.54459649
l1:1 l 64 ;l2:8 r 32	1.631353242	92.25786786
l1:1 l 64 ;l2:8 r 64	2.172764182	87.57635784
l1:2 l 32 ;l2:1 l 32	1.604648184	94.62458536
l1:2 l 32 ;l2:1 l 64	2.122960224	89.66080905
l1:2 l 32 ;l2:2 l 32	1.593927175	95.39986905
l1:2 l 32 ;l2:4 l 32	1.749724317	92.38651842
l1:2 l 32 ;l2:8 l 32	1.627992136	95.90417408
l1:2 l 32 ;l2:1 f 32	**1.555089277**	**89.45687636**
l1:2 l 32 ;l2:2 f 32	1.555089277	89.97834495
l1:2 l 32 ;l2:4 f 32	1.749724317	86.67133237
l1:2 l 32 ;l2:8 f 32	1.582963899	90.75045126
l1:2 l 32 ;l2:1 r 32	1.555089277	86.24162687



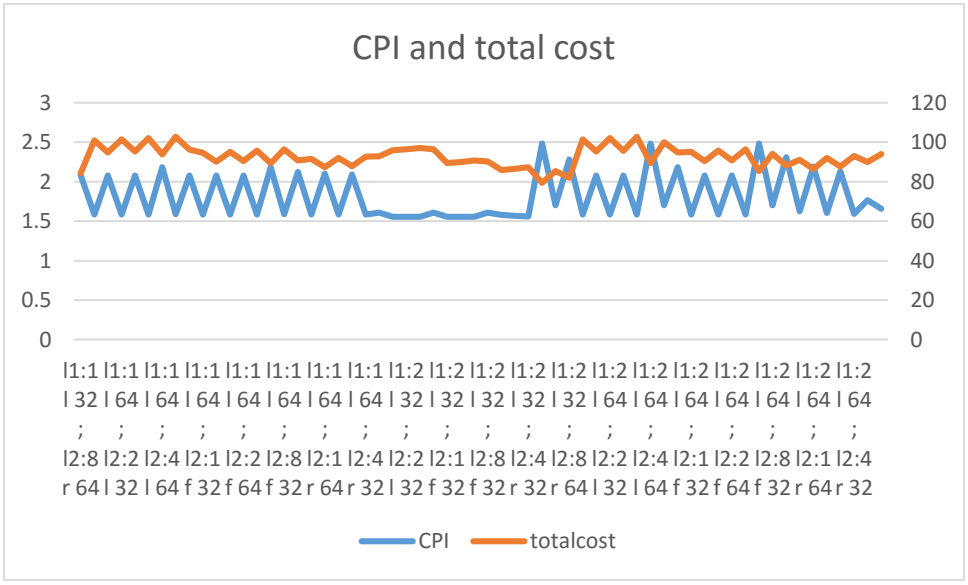
b) Both L1 and L2 unified: The optimal value for CPI and cost together is obtained for the configuration l1:1 l 32 ; l2:8 r 64. L1 is 1 way associative with LRU policy and L2 is 8 way associative with CPI 1.560968 and cost is 66.20362.

configuration	CPI	totalcost
l1:1 l 32 ; l2:2 f 64	1.58346	63.88984
l1:1 l 32 ; l2:4 f 32	2.079063	33.99813
l1:1 l 32 ; l2:4 f 64	1.58346	64.53504
l1:1 l 32 ; l2:8 f 32	2.08686	34.43816
l1:1 l 32 ; l2:8 f 64	1.600711	64.58472
l1:1 l 32 ; l2:1 r 32	2.082571	33.06257
l1:1 l 32 ; l2:1 r 64	1.591159	63.07587
l1:1 l 32 ; l2:2 r 32	2.07994	33.49302
l1:1 l 32 ; l2:2 r 64	1.587163	63.74309
l1:1 l 32 ; l2:4 r 32	2.079452	33.99194
l1:1 l 32 ; l2:4 r 64	1.584922	64.47644
l1:1 l 32 ; l2:8 r 64	**1.560968**	**66.20362**
l1:1 l 64 ; l2:1 l 64	1.555022	85.09691
l1:1 l 64 ; l2:2 l 64	1.555022	85.6184
l1:1 l 64 ; l2:4 l 64	1.555022	86.27541
l1:1 l 64 ; l2:8 l 64	1.560968	86.70372
l1:1 l 64 ; l2:1 f 64	1.555022	85.09691
l1:1 l 64 ; l2:2 f 64	1.555022	85.6184
l1:1 l 64 ; l2:4 f 64	1.555022	86.27541
l1:1 l 64 ; l2:8 f 64	1.560968	86.70372
l1:1 l 64 ; l2:1 r 64	1.557751	84.94959
l1:1 l 64 ; l2:2 r 64	1.556777	85.52305
l1:1 l 64 ; l2:4 r 64	1.5559	86.22733
l1:1 l 64 ; l2:8 r 32	2.198949	47.2861
l1:1 l 64 ; l2:8 r 64	1.594771	84.88712
l1:2 l 32 ; l2:1 l 32	2.085988	33.3988
l1:2 l 32 ; l2:1 l 64	1.58366	63.88188
l1:2 l 32 ; l2:2 l 32	2.079263	33.8936
l1:2 l 32 ; l2:2 l 64	1.58366	64.39394
l1:2 l 32 ; l2:4 l 32	2.079263	34.38495
l1:2 l 32 ; l2:4 l 64	1.58366	65.03906
l1:2 l 32 ; l2:8 l 32	2.198949	33.10247
l1:2 l 32 ; l2:8 l 64	1.594771	65.33004
l1:2 l 32 ; l2:1 f 32	2.085501	33.40637
l1:2 l 32 ; l2:1 f 64	1.58366	63.88188
l1:2 l 32 ; l2:2 f 32	2.079263	33.8936
l1:2 l 32 ; l2:2 f 64	1.58366	64.39394
l1:2 l 32 ; l2:4 f 32	2.079263	34.38495
l1:2 l 32 ; l2:4 f 64	1.58366	65.03906
l1:2 l 32 ; l2:8 f 32	2.198949	33.10247
l1:2 l 32 ; l2:8 f 64	1.594771	65.33004
l1:2 l 32 ; l2:1 r 32	2.141542	32.55834
l1:2 l 32 ; l2:1 r 64	1.588338	63.69667
l1:2 l 32 ; l2:2 r 32	2.111913	33.38506
l1:2 l 32 ; l2:2 r 64	1.585902	64.30433
l1:2 l 32 ; l2:4 r 32	2.094272	34.14569
l1:2 l 32 ; l2:4 r 64	1.585025	64.98393
l1:2 l 32 ; l2:8 r 64	1.622011	64.24969
l1:2 l 64 ; l2:1 l 64	1.560219	85.33659
l1:2 l 64 ; l2:2 l 64	1.555151	86.13288



c) L1 separate and L2 unified memory: The optimum value for both CPI and total cost is obtained for the configuration l1:2 l 32 ; l2:4 f 32. L1 is 2 way associative with LRU and L2 is 4 way associative with FIFO policy. The optimal CPI is 1.555089 and cost is 90.6353.

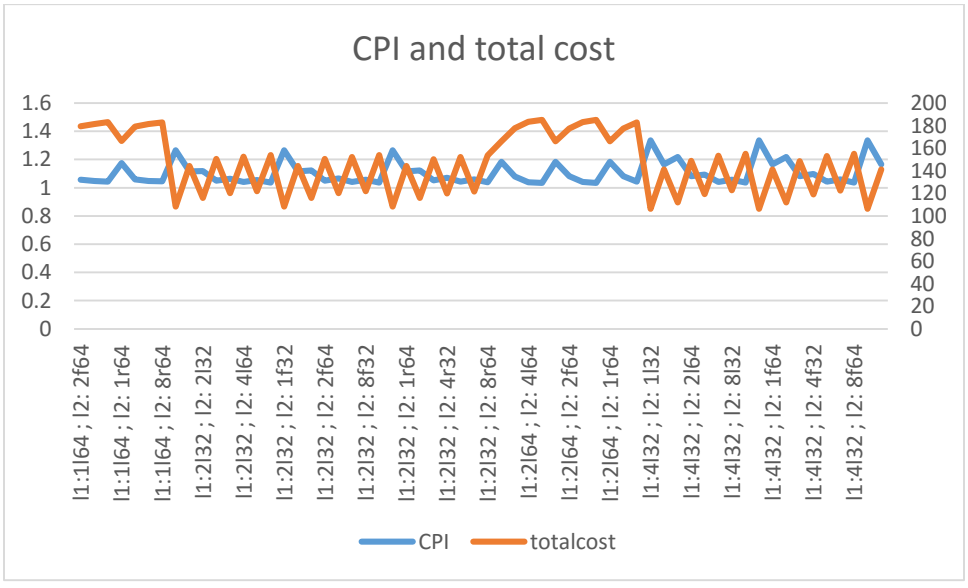
Configuration	CPI	totalcost
l1:1 l 32 ; l2:8 r 64	2.079491	84.22866
l1:1 l 64 ; l2:1 l 32	1.583693	100.9512
l1:1 l 64 ; l2:1 l 64	2.079296	94.80798
l1:1 l 64 ; l2:2 l 32	1.583693	101.4632
l1:1 l 64 ; l2:2 l 64	2.079296	95.19798
l1:1 l 64 ; l2:4 l 32	1.583693	102.1083
l1:1 l 64 ; l2:4 l 64	2.182608	93.76334
l1:1 l 64 ; l2:8 l 32	1.587495	102.7361
l1:1 l 64 ; l2:8 l 64	2.079394	96.25276
l1:1 l 64 ; l2:1 f 32	1.583693	94.63683
l1:1 l 64 ; l2:1 f 64	2.079296	89.99866
l1:1 l 64 ; l2:2 f 32	1.583693	95.14888
l1:1 l 64 ; l2:2 f 64	2.079296	90.38866
l1:1 l 64 ; l2:4 f 32	1.583693	95.79399
l1:1 l 64 ; l2:4 f 64	2.182608	89.18166
l1:1 l 64 ; l2:8 f 32	1.587495	96.43683
l1:1 l 64 ; l2:8 f 64	2.123155	90.69251
l1:1 l 64 ; l2:1 r 32	1.585253	91.44377
l1:1 l 64 ; l2:1 r 64	2.100056	87.2718
l1:1 l 64 ; l2:2 r 32	1.584571	91.97123
l1:1 l 64 ; l2:2 r 64	2.090212	87.81175
l1:1 l 64 ; l2:4 r 32	1.583986	92.62986
l1:1 l 64 ; l2:8 r 32	1.608402	92.78952
l1:2 l 32 ; l2:1 l 32	1.555382	95.87969
l1:2 l 32 ; l2:2 l 32	1.555089	96.40884
l1:2 l 32 ; l2:4 l 32	1.555089	97.06582
l1:2 l 32 ; l2:8 l 32	1.608402	96.40238
l1:2 l 32 ; l2:1 f 32	1.555382	89.4504
l1:2 l 32 ; l2:2 f 32	1.555089	89.97834
l1:2 l 32 ; l2:4 f 32	**1.555089**	**90.63532**
l1:2 l 32 ; l2:8 f 32	1.608402	90.18503
l1:2 l 32 ; l2:1 r 32	1.577896	85.79007
l1:2 l 32 ; l2:2 r 32	1.565615	86.54954
l1:2 l 32 ; l2:4 r 32	1.55889	87.34102
l1:2 l 32 ; l2:4 r 64	2.482905	79.33283
l1:2 l 32 ; l2:8 r 32	1.701343	85.32408
l1:2 l 32 ; l2:8 r 64	2.278523	82.0314
l1:2 l 64 ; l2:1 l 32	1.585167	101.4201
l1:2 l 64 ; l2:1 l 64	2.079308	95.19776
l1:2 l 64 ; l2:2 l 32	1.583705	101.975
l1:2 l 64 ; l2:2 l 64	2.079308	95.58777
l1:2 l 64 ; l2:4 l 32	1.583705	102.6201
l1:2 l 64 ; l2:4 l 64	2.482905	89.40168
l1:2 l 64 ; l2:8 l 32	1.701343	100.0184
l1:2 l 64 ; l2:8 l 64	2.181645	94.69101
l1:2 l 64 ; l2:1 f 32	1.585069	95.11404
l1:2 l 64 ; l2:1 f 64	2.079308	90.38847
l1:2 l 64 ; l2:2 f 32	1.583705	95.66064
l1:2 l 64 ; l2:2 f 64	2.079308	90.77847
l1:2 l 64 ; l2:4 f 32	1.583705	96.30575
l1:2 l 64 ; l2:4 f 64	2.482905	85.37414
l1:2 l 64 ; l2:8 f 32	1.701343	94.14064
l1:2 l 64 ; l2:8 f 64	2.309127	88.1691



3)GCC:

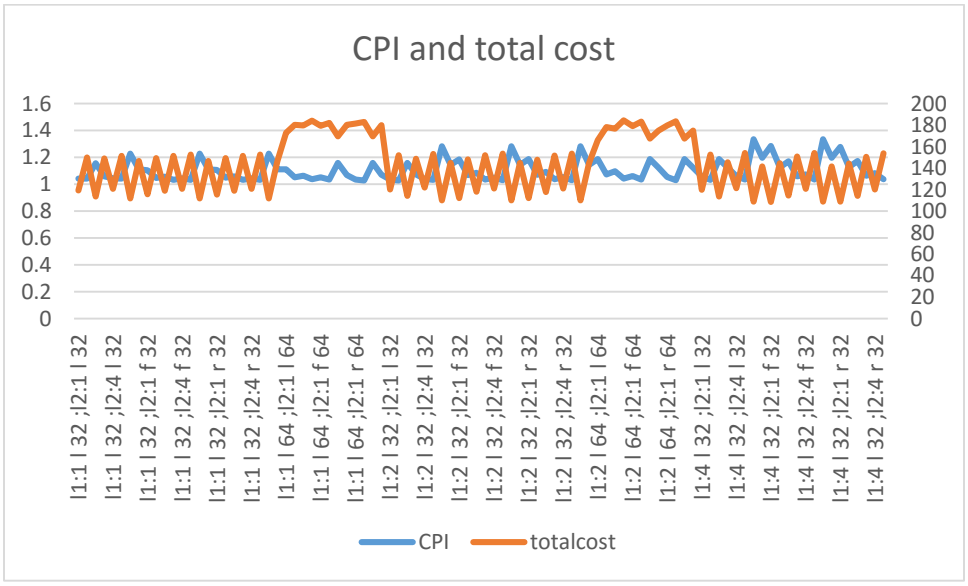
a) Both L1 and L2 separate memory: The optimized value for both CPI and cost is obtained at the configuration l1:2l32 ; l2: 4f32 . L1 is 2 way associative with LRU policy and L2 is 4 way associative with FIFO policy. The CPI for this configuration is 1.066357 and total cost= 120.0965.

configuration	CPI	totalcost
l1:1l64 ; l2: 2f64	1.057997	179.3705
l1:1l64 ; l2: 4f64	1.04789	181.545
l1:1l64 ; l2: 8f64	1.043254	183.2341
l1:1l64 ; l2: 1r64	1.174359	166.3566
l1:1l64 ; l2: 2r64	1.059474	179.197
l1:1l64 ; l2: 4r64	1.049085	181.4008
l1:1l64 ; l2: 8r64	1.046182	182.8752
l1:2l32 ; l2: 1l32	1.265528	108.4034
l1:2l32 ; l2: 1l64	1.116037	144.2296
l1:2l32 ; l2: 2l32	1.119155	116.1126
l1:2l32 ; l2: 2l64	1.050218	150.5939
l1:2l32 ; l2: 4l32	1.064302	120.2222
l1:2l32 ; l2: 4l64	1.040805	152.4401
l1:2l32 ; l2: 8l32	1.055753	121.8638
l1:2l32 ; l2: 8l64	1.036546	153.9745
l1:2l32 ; l2: 1f32	1.265528	108.4034
l1:2l32 ; l2: 1f64	1.116037	144.2296
l1:2l32 ; l2: 2f32	1.121902	115.963
l1:2l32 ; l2: 2f64	1.051233	150.5016
l1:2l32 ; l2: 4f32	**1.066357**	**120.0965**
l1:2l32 ; l2: 4f64	1.041191	152.4039
l1:2l32 ; l2: 8f32	1.056446	121.82
l1:2l32 ; l2: 8f64	1.036548	153.9744
l1:2l32 ; l2: 1r32	1.265528	108.4034
l1:2l32 ; l2: 1r64	1.116037	144.2296
l1:2l32 ; l2: 2r32	1.122584	115.9259
l1:2l32 ; l2: 2r64	1.052624	150.3754
l1:2l32 ; l2: 4r32	1.069685	119.894
l1:2l32 ; l2: 4r64	1.04244	152.2872
l1:2l32 ; l2: 8r32	1.059171	121.6481
l1:2l32 ; l2: 8r64	1.039462	153.6969
l1:2l64 ; l2: 1l64	1.183757	166.1576
l1:2l64 ; l2: 2l64	1.079257	177.6718
l1:2l64 ; l2: 4l64	1.039758	183.3146
l1:2l64 ; l2: 8l64	1.033797	185.1916



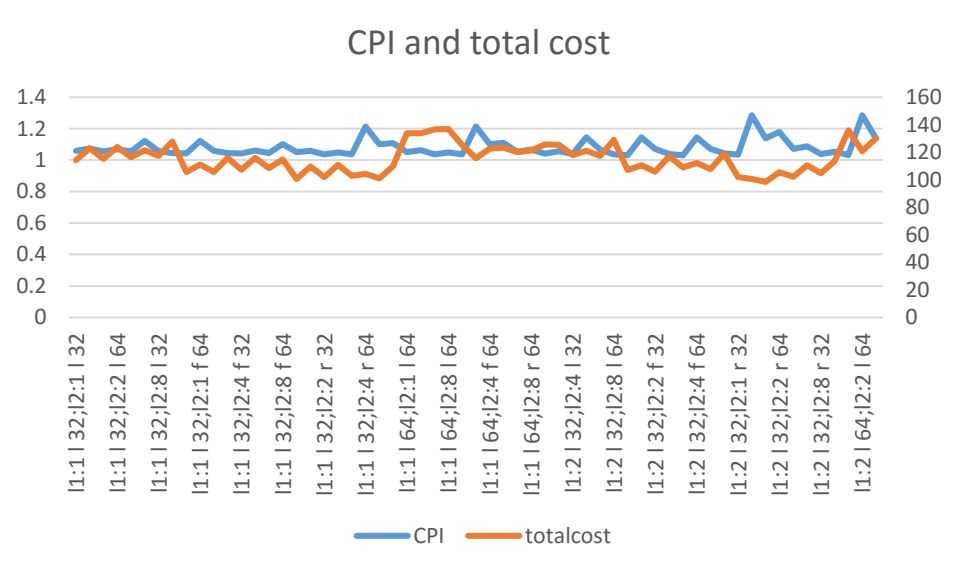
b) Both L1 and L2 unified: The optimized value for CPI and Cost is obtained for the configuration l1:1 l 32 ;l2:1 l 32. L1 is 1 way associative with LRU replacement policy and L2 is 1 way associative with LRU policy. The Optimized CPI value is 1.041195 and optimal total cost is 119.130683

configuration	CPI	totalcost
l1:1 l 32 ;l2:1 l 32	**1.041195659**	**119.130683**
l1:1 l 32 ;l2:1 l 64	1.040696173	149.9101104
l1:1 l 32 ;l2:2 l 32	1.155211788	113.5031417
l1:1 l 32 ;l2:2 l 64	1.058428635	149.0861912
l1:1 l 32 ;l2:4 l 32	1.045086748	120.6454311
l1:1 l 32 ;l2:4 l 64	1.042709264	151.4843928
l1:1 l 32 ;l2:8 l 32	1.22870267	111.7922128
l1:1 l 32 ;l2:8 l 64	1.112033685	146.526673
l1:1 l 32 ;l2:1 f 32	1.102909307	115.5422298
l1:1 l 32 ;l2:1 f 64	1.046727251	149.3632533
l1:1 l 32 ;l2:2 f 32	1.055319979	119.0407841
l1:1 l 32 ;l2:2 f 64	1.032988598	151.4033089
l1:1 l 32 ;l2:4 f 32	1.044728479	120.667943
l1:1 l 32 ;l2:4 f 64	1.032630637	152.4260947
l1:1 l 32 ;l2:8 f 32	1.22870267	111.7922128
l1:1 l 32 ;l2:8 f 64	1.112033685	146.526673
l1:1 l 32 ;l2:1 r 32	1.107059374	115.3152733
l1:1 l 32 ;l2:1 r 64	1.048329464	149.2190333
l1:1 l 32 ;l2:2 r 32	1.057909128	118.8840494
l1:1 l 32 ;l2:2 r 64	1.033135518	151.3895997
l1:1 l 32 ;l2:4 r 32	1.044842611	120.6607698
l1:1 l 32 ;l2:4 r 64	1.032630637	152.4260947
l1:1 l 32 ;l2:8 r 32	1.22870267	111.7922128
l1:1 l 32 ;l2:8 r 64	1.112033685	146.526673
l1:1 l 64 ;l2:1 l 64	1.110734027	172.7352863
l1:1 l 64 ;l2:2 l 64	1.050784767	180.224045
l1:1 l 64 ;l2:4 l 64	1.063409694	179.6981017
l1:1 l 64 ;l2:8 l 64	1.037083051	183.9971361
l1:1 l 64 ;l2:1 f 64	1.052527674	179.2462235
l1:1 l 64 ;l2:2 f 64	1.034607827	182.1820254
l1:1 l 64 ;l2:4 f 64	1.158227614	169.4897329
l1:1 l 64 ;l2:8 f 64	1.067779856	180.2886939
l1:1 l 64 ;l2:1 r 64	1.033962175	181.4771496
l1:1 l 64 ;l2:2 r 64	1.02752261	183.0590011
l1:1 l 64 ;l2:4 r 64	1.158227614	169.4897329



c) L1 separate and L2 unified memory: Here, the optimal value for both CPI and cost is obtained at the configuration l1:1 l 32;l2:4 r 32. L1 is 1 way associative with LRU replacement policy and L2 is 4 way associative with Random replacement. The optimal CPI=1.03653 and optimal total cost=102.8566

Configuration	CPI	totalcost
l1:1 l 32;l2:1 l 32	1.05796593	114.3333
l1:1 l 32;l2:1 l 64	1.07244748	122.8566
l1:1 l 32;l2:2 l 32	1.05534752	115.2489
l1:1 l 32;l2:2 l 64	1.06850638	123.8658
l1:1 l 32;l2:4 l 32	1.05425703	116.2803
l1:1 l 32;l2:4 l 64	1.12081409	121.5634
l1:1 l 32;l2:8 l 32	1.05673033	117.2493
l1:1 l 32;l2:8 l 64	1.04359741	127.6149
l1:1 l 32;l2:1 f 32	1.0432436	105.5851
l1:1 l 32;l2:1 f 64	1.12081409	111.0062
l1:1 l 32;l2:2 f 32	1.05818978	105.637
l1:1 l 32;l2:2 f 64	1.04373541	115.9192
l1:1 l 32;l2:4 f 32	1.0432436	107.3417
l1:1 l 32;l2:4 f 64	1.0601236	115.9412
l1:1 l 32;l2:8 f 32	1.04519132	108.3689
l1:1 l 32;l2:8 f 64	1.10177357	114.7044
l1:1 l 32;l2:1 r 32	1.05023318	100.4876
l1:1 l 32;l2:1 r 64	1.05935465	109.5356
l1:1 l 32;l2:2 r 32	1.03689212	101.8549
l1:1 l 32;l2:2 r 64	1.048632	110.8666
l1:1 l 32;l2:4 r 32	**1.03653748**	**102.8566**
l1:1 l 32;l2:4 r 64	1.21284674	104.1448
l1:1 l 32;l2:8 r 32	1.10177357	101.09
l1:1 l 32;l2:8 r 64	1.10694688	109.9085
l1:1 l 64;l2:1 l 64	1.05141123	133.7252
l1:1 l 64;l2:2 l 64	1.06173131	133.7238
l1:1 l 64;l2:4 l 64	1.03703115	136.584
l1:1 l 64;l2:8 l 64	1.04873846	136.7942
l1:1 l 64;l2:1 f 64	1.03653748	125.2074
l1:1 l 64;l2:2 f 64	1.21284674	115.6701
l1:1 l 64;l2:4 f 64	1.10177357	122.7137
l1:1 l 64;l2:8 f 64	1.11011603	123.2638
l1:1 l 64;l2:2 r 64	1.05349612	120.1009
l1:1 l 64;l2:8 r 64	1.0670864	121.3308
l1:2 l 32;l2:1 l 64	1.04105775	125.6815



8) CONCLUSION:

In this project, based on the optimal cache configuration for each benchmark, CPI is calculated. Simple scalar tool is used to simulate the various parameters for 3 different benchmarks- Anagram, GO and

GCC..Also, the cost function is measured and most optimum value for CPI and cost considered together is taken as the value of optimum cache.

It is seen that for each benchmark, FIFO is less expensive than LRU and Random less expensive than FIFO. Thus, the measurement of optimal cost for different designs of cache is an approximation based on the assumptions of cost weights made in this project.