ADVANCED VLSI DESIGN

SRAM DESIGN AND LAYOUT

(256 words)

Area of Memory cell	3.400um x 2.380 um =8.092 squm
Aspect Ratio of Memory cell	1.428
Memory array area	100.440 x 152.320= 15299.02squm
Memory area per bit	7.47022 squm (15299.02/(256*8))
Total Memory area	40035.4656 squm (258.36umx 154.96um)
Height of the total memory	154.96um
Width of the total memory	258.36um
Total Memory area per bit	19.5485 squm (40035.4656/256*8)
Aspect Ratio of total memory	0.6001
Worst case Write time	For '0' =425ps For '1' = 560ps
Worst case Read time	For '0'= 908ps, For '1' =1.18ns

CONTENTS

1. INTRODUCTION

1.1 Introduction to SRAM

A 256 word 8T-SRAM with word size 8 bits is designed and layout using IBM 130nm process. Design Rule checking(DRC), Layout versus schematic(LVS) and finally circuit simulation is done for finding the worst read/write times for an output capacitance of 25fF.

The memory cell consists of the following blocks:

1)8T (8 transistor) Memory cell
2)Row decoder
3)Column decoder
4)Precharger
5) Sense Amplifier
6) Clock buffer
7)T gate

1.2 SRAM Architecture

The designed SRAM array consists of 2048 bits with word size 8 bits. Number of row address bits is 5 and column address bits is 3 requiring 32x5 decoder. Each memory cell stores 2^5=32 words with 2^3=8 bits each.
8T-SRAM memory cell consists of cross-coupled inverters to store a bit, 2 bit lines for bit line conditioning, 2 wordlines both lines used to select appropriate memory cell

The schematic and layout of 8T memory cell is given below

1.3 Schematic of a single memory cell

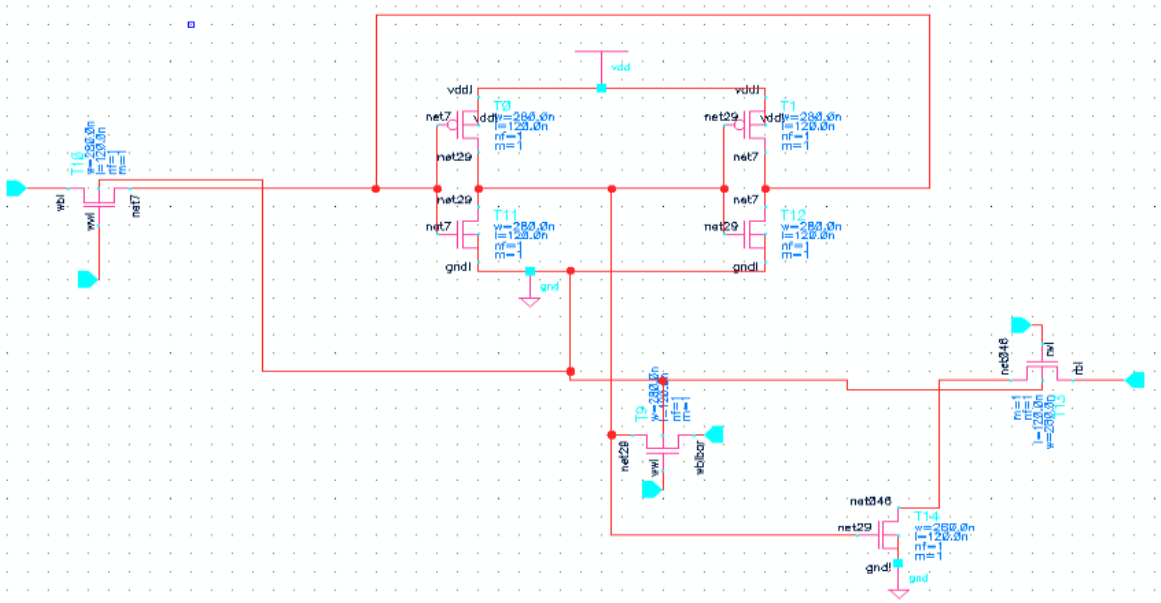


Fig 1. Schematic of single memory cell

1.4) Layout of a memory cell

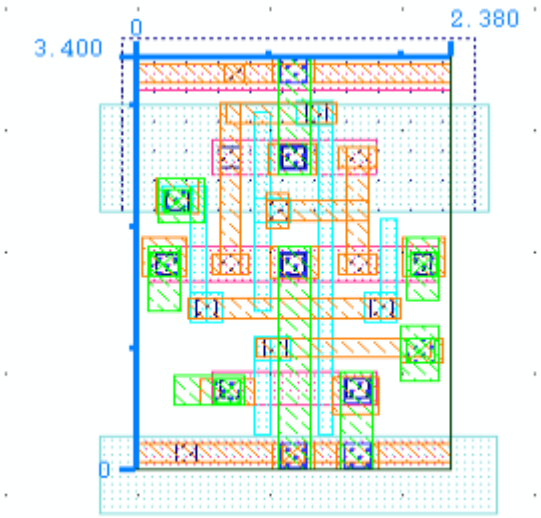


Fig 2.Layout of a single memory cell

Height of a single memory cell=3.400um and width= 2.380um
Aspect ratio=Height/Width= 1.428

1.5 Schematic of memory array

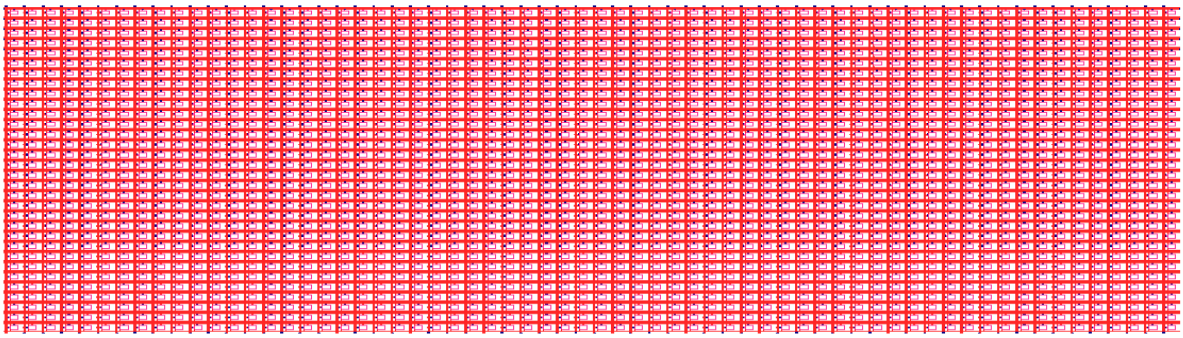


Fig 3. Schematic of memory array

1.6 Layout of memory array

The height and width of the memory array is found to be 100.440 um and 152.320um respectively and the area is 15299.02 squm

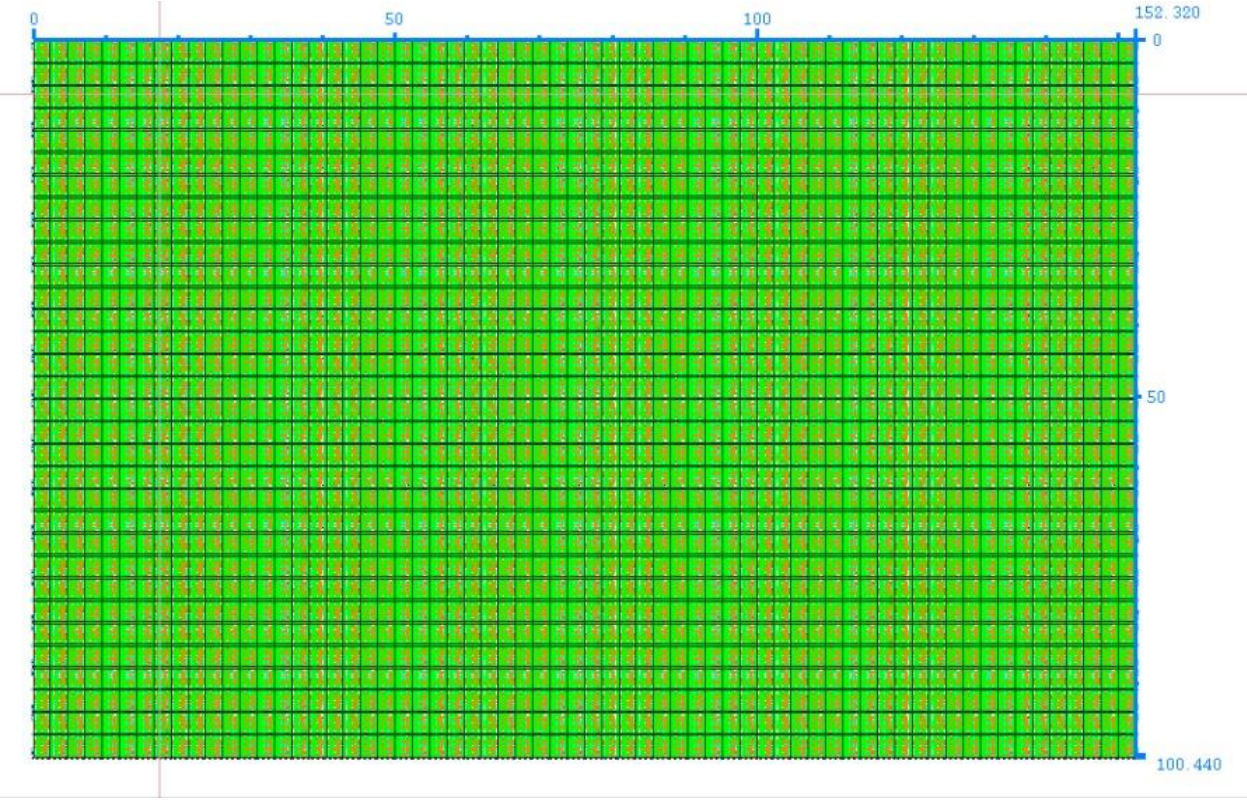


Fig 4. Layout of memory array

2. ROW DECODERS

The row decoder activates one of the rows by asserting one of the wordlines in the memory cell. For a nxm memory cells in a memory array a row decoder decodes n-bits for which row to select. In this project, we have used predecoding style which improves the area.

2.1 Pre-decoded style row decoder and sizing of transistors in row decoder

In row decoder design, we have 5 inputs and address enable given to two NAND3 gates, two NAND2 gates each followed by an inverter in a pre-decoded style. The sizes of transistors, load and number of stages are determined using the logical effort as follows.

Cpoly= 2fF/um x 2 x 0.28 x 64
Cwire= 0.2fF/um x 64 x 2.38
Cload=Cpoly+Cwire=102.144fF= 51.072uF

G= 3.7 (for two NAND3 gates, two NAND2 gates and 4 inverters)
B= 32
H=51.072
F=GBH= 6052.977
No. of stages, N_{opt}=6.79~ 7
f^= 3.469

2.2 Sizing of transistors

Inverter1 (upper and lower rightmost)= 14.722um
NAND2= 5.658um
Inverter2 (single path)= 3.262um
NAND3= 1.5672um
Inverter3= 1.807um
NAND3= 0.8682um

Input drivers of the row decoder

Cload=1.5672um
G=1
B=8
F=GBH= 12.5376
No. of stages, N=$\log_{3.6}(12.5376)$= 1.97~2
f^= 3.54
Inverter1 (upper rightmost)= 1.7708um
Inverter2 (lower rightmost)= 3.331um
Inverter3 (lower)= 1.79um
Inverter4= 1.0004um

The sizes of inverters used in the initial buffer stage to get the negative polarity address bits are 1.011um, 1.8645um and 1um.

The inputs to the row decoder are a0, a1, a2, a3, a4, a0b, a1b, a2b, a3b, a4b, enable and enable bar.

The schematic and layout of the row decoder are below

2.3)Layout of Single row decoder

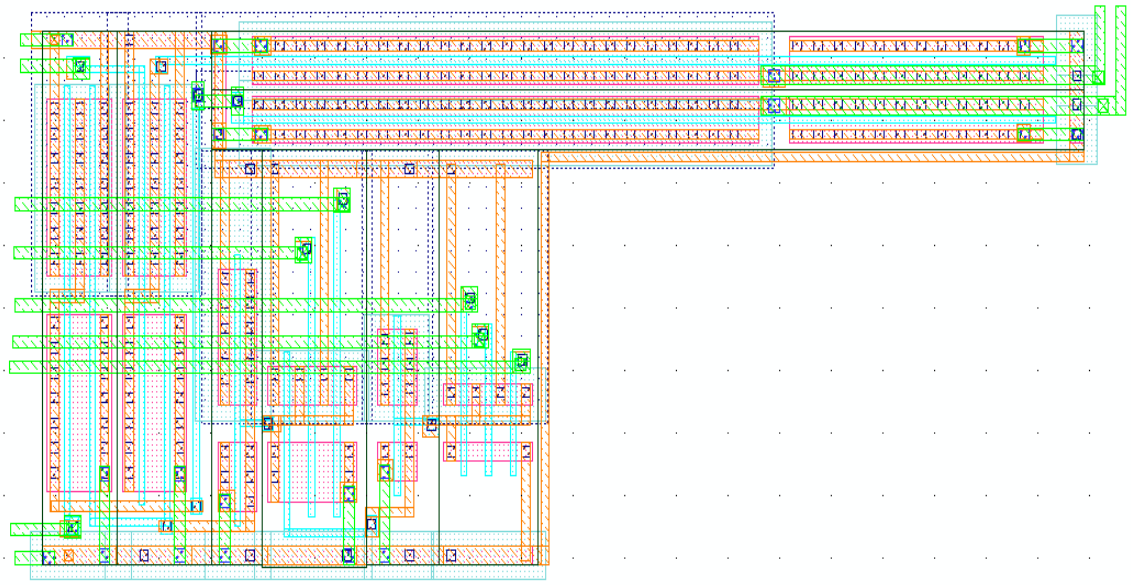


Fig 5. Layout of single row decoder

2.4) Schematic of Row decoder:

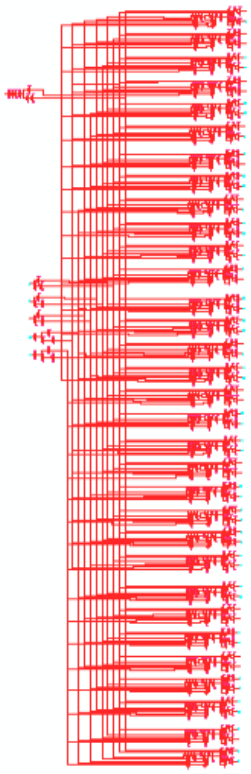


Fig 6. Schematic of row decoder

2.5) Layout of Row decoder:

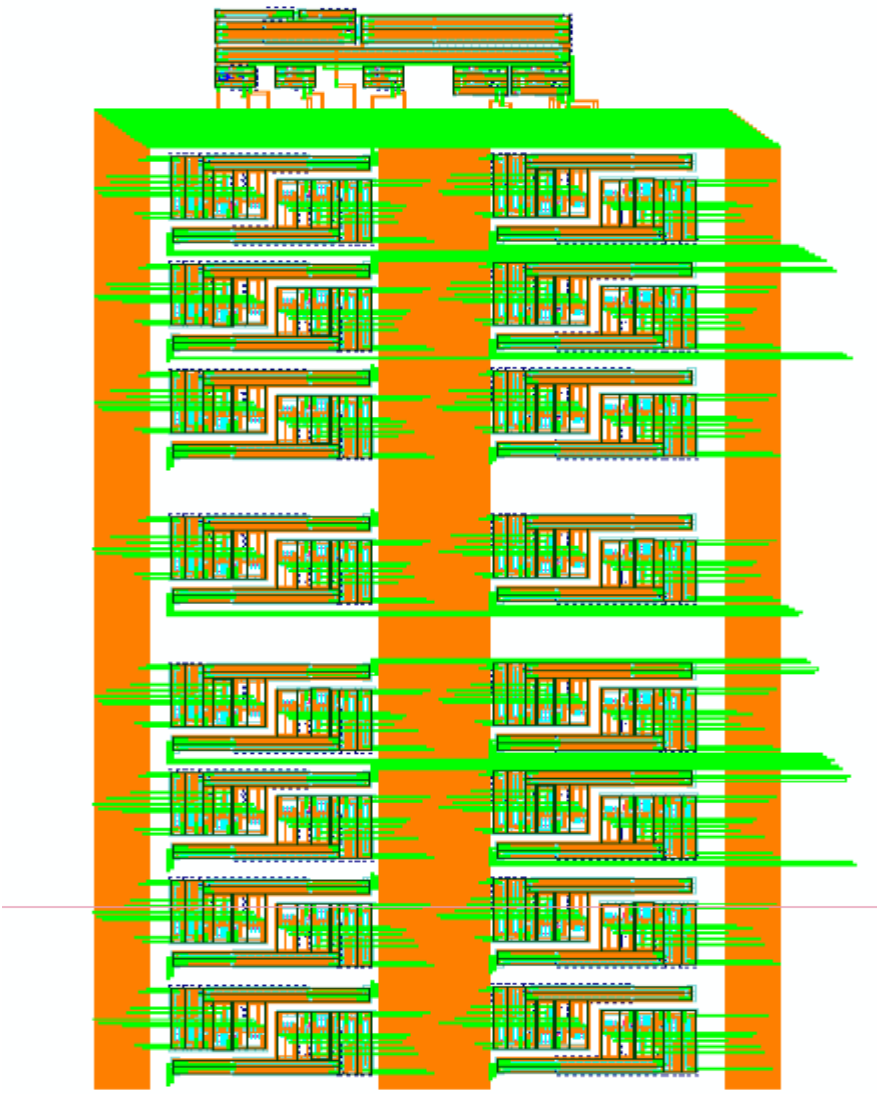


Fig 7. Layout of row decoder

3. COLUMN DECODER

A column decoder decodes ‘m’ bits for which column to be selected in the memory cell. Column decoder used in our SRAM design is given below.

3.1 Sizing of transistors in Column decoder calculation

Cpoly= 0.56(width of T-gate)x 2 = 1.12fF
Cwire= (0.2fFx0.94x64)/8= 1.504fF
Cload= Cpoly+Cwire= 2.624fF= 1.312uF
G=2
B=192

H=1.312
F=GBH= 503.808
N=$\log_{3.6}$(503.808)= 4.85~5
f^=3.47

Sizing,
Inverter1(upper rightmost)= 9.074um
Inverter2(lower rightmost)= 16.90um
Inverter4= 5.230um
Inverter5= 1.507um
Inverter6= 0.868um
Inverter7(polarity stage)= 1.863um

The output the column decoder is given to T-gates.
Schematic and layout of column decoder is given below

3.2 Schematic of column decoder

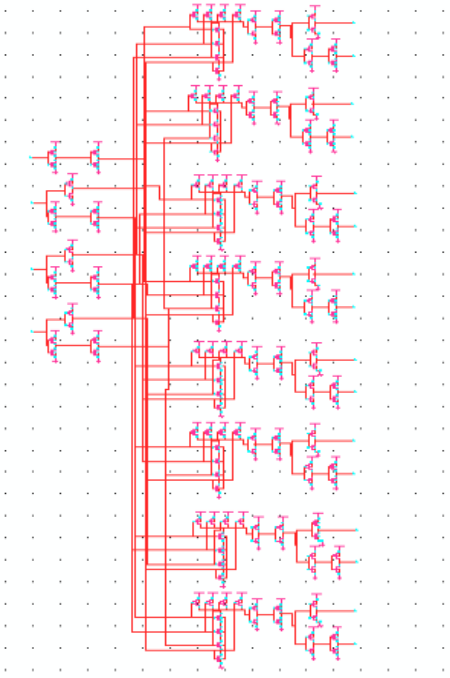


Fig 8. Schematic of column decoder

3.3 Layout of Column Decoder

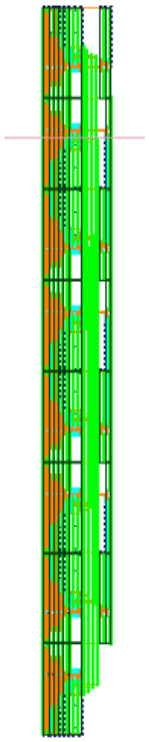


Fig 9. Layout of Column decoder

4. PRE-CHARGER

Pre-charge is done to minimize power dissipation during test. It is used for bit line conditioning. Generally before any read or write operation, the bit lines rea charged to Vdd, For reads, the bit lines are initially pre-charged high and is pulled down by SRAM cell through the access transistor. For writes, the bit line or its compliment is actively driven low and this low value overpowers the cell to write the new value.

In our design we have used 3 prechargers cell with pmos of size 2um given to a single memory cell.

4.1 Schematic of Pre-charger

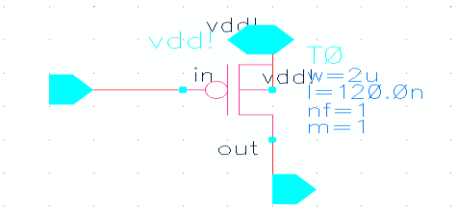


Fig 10. Schematic of Single Pre-charger

4.3 Layout of Pre-charger

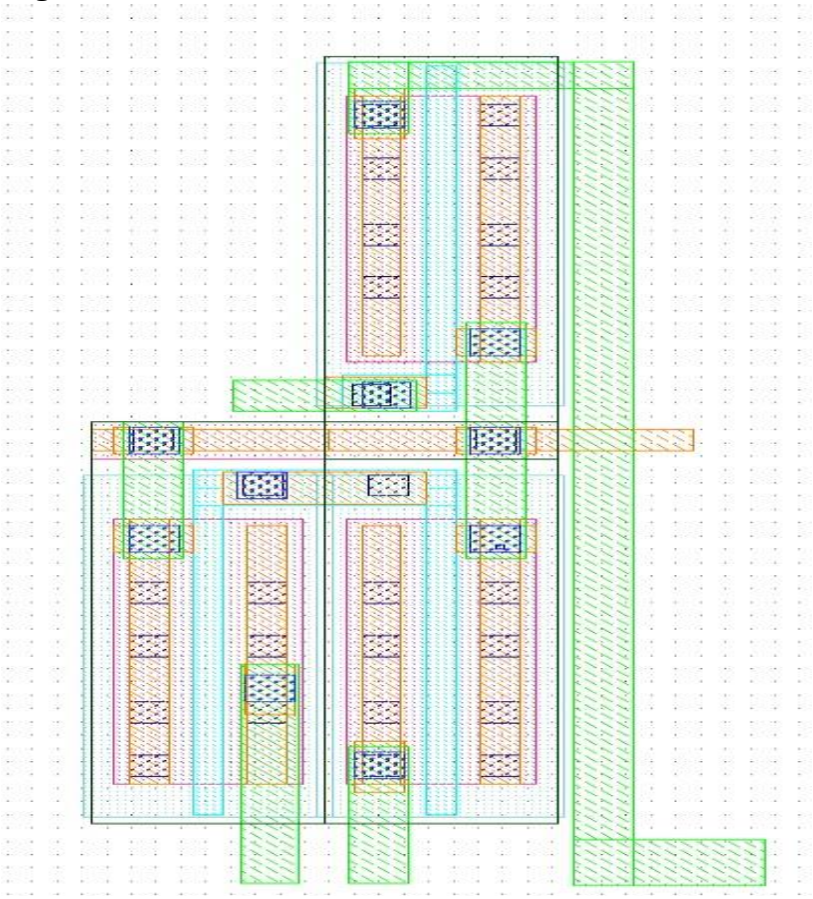


Fig 11. Layout of 3 Pre-chargers

5. WRITE DRIVER

The function of the SRAM write driver is to quickly discharge one of the bit lines from the precharge level to below the write margin of the SRAM cell to write the cell. Normally the write driver is enabled by write enable signal and drives the bit line using full-swing discharge from precharge level to ground.

5.1 Sizing of transistors for Write Driver

Cload=(0.2x100.440) + (2x0.56) + 2= 21.808fF= 10.904uF
G=1
B=16
H=10.904
F=GBH= 174.464
N=$\log_{3.6}$(174.464)= 4.029~4
f^=3.634
Sizing,

Inverter1 (upper rightmost)= 24.0024um

Inverter2 (lower rightmost)= 45.7578um
Inverter3 = 24.0024um
Inverter4=13.2088um
Inverter5= 3.6345um
Inverter6= 1

The schematic and layout of write driver is given below

5.2 Schematic of Write driver

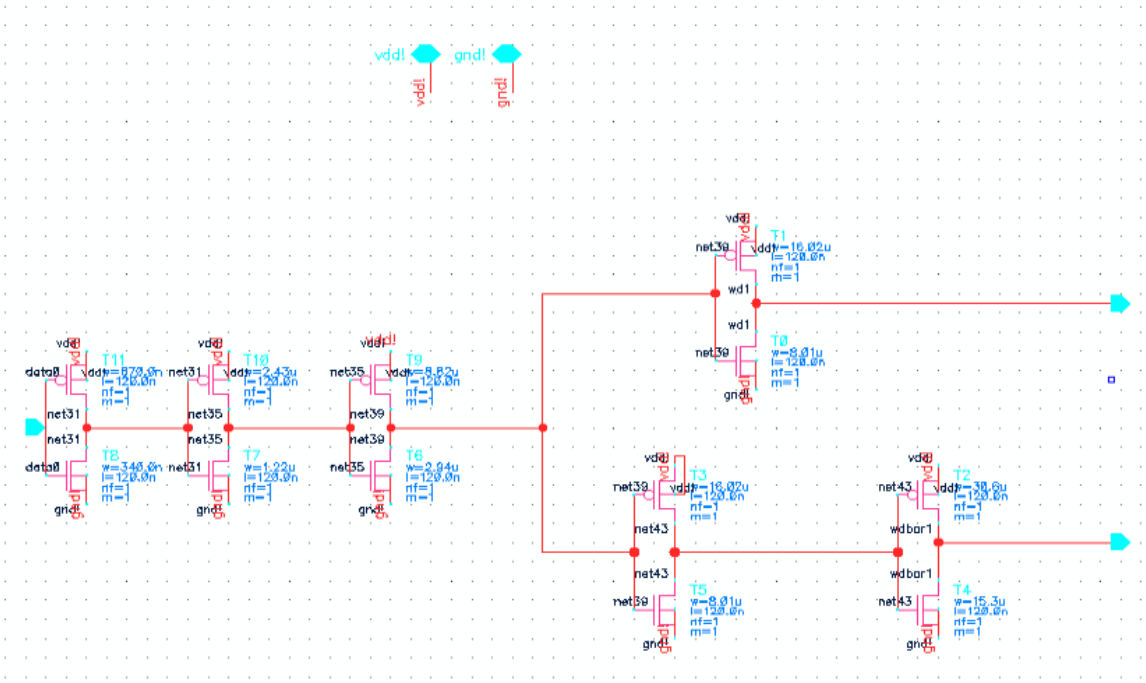


Fig 12. Schematic of Single Write driver

5.3 Layout of Write driver

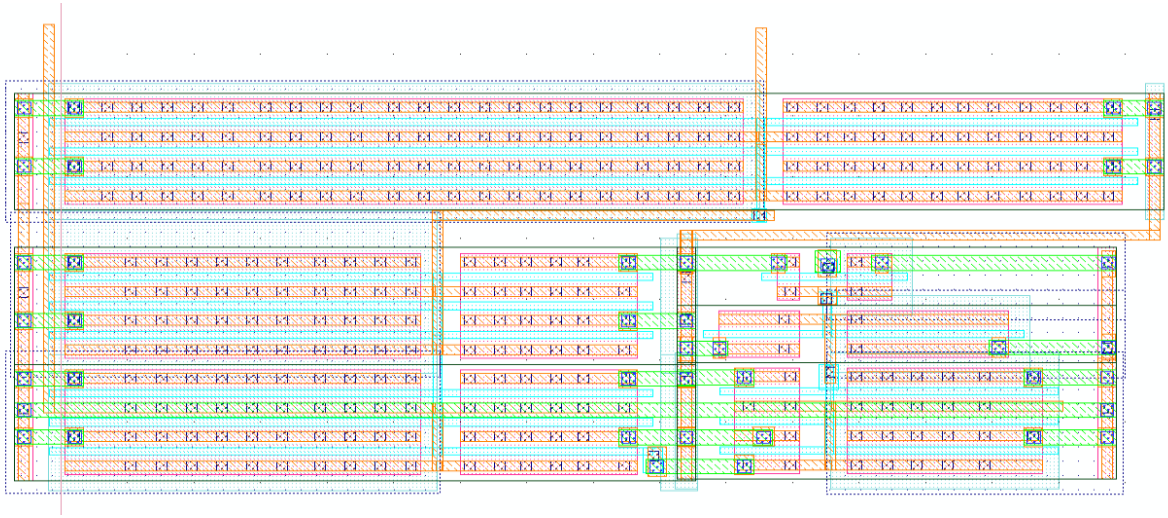


Fig 13. Layout of Single Write driver

6. SENSE AMPLIFIER

The primary function of a sense amplifier is to amplify the small voltage differential voltage developed on the bit lines by a read-accessed cell to the full swing digital output signal thus greatly reducing the time required for a read operation. In our project, we have used Current mode sense amplifier which has a speed improvement compared to other sense amplifiers. The reference voltage is used for comparison.

Transistors of size pmos= 3um and nmos=0.56um are used here.

The layout and schematic for a sense amplifier is given below.

6.1 Schematic of Sense Amplifier

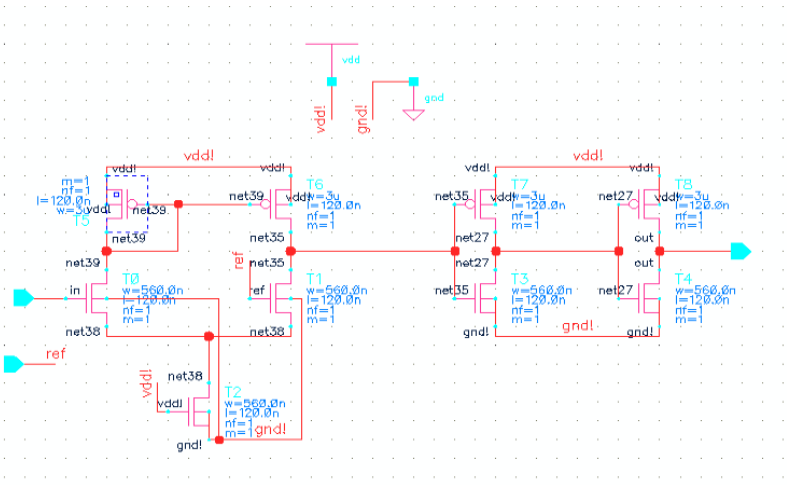


Fig 14. Schematic of Sense Amplifier

6.2 Layout of Sense Amplifier

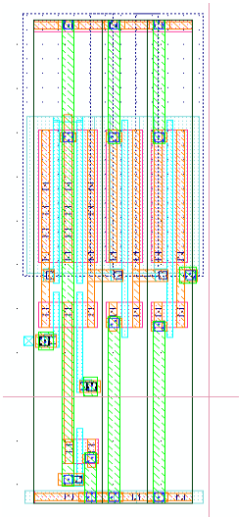


Fig 15. Layout of Sense Amplifier

7. Clock buffer

Clock buffer is critical in designing the timing throughout the SRAM. A function of clock buffer is to capture the rising edge of clock and then create the key internal clock that will be self timed and independent on the falling edge of the clock.

7.1 Sizing of transistors in clock buffer

Cpoly=64x3x2x2= 768fF
Cwire= 0.2x152.320=30.464fF
Cload= Cpoly + Cwire= 798.464fF=399.232uF
G=1
B=1
H=399.232um
F=GBH=399.232um
N=$\log_{3.6}$(399.232)= 4.67~5
f^= 4.464

Sizing,
Inverter1(rightmost)= 89.33um
Inverter2= 19.989um
Inverter3= 4.4728um
Inverter4= 1.008um

7.2 Schematic of clock buffer

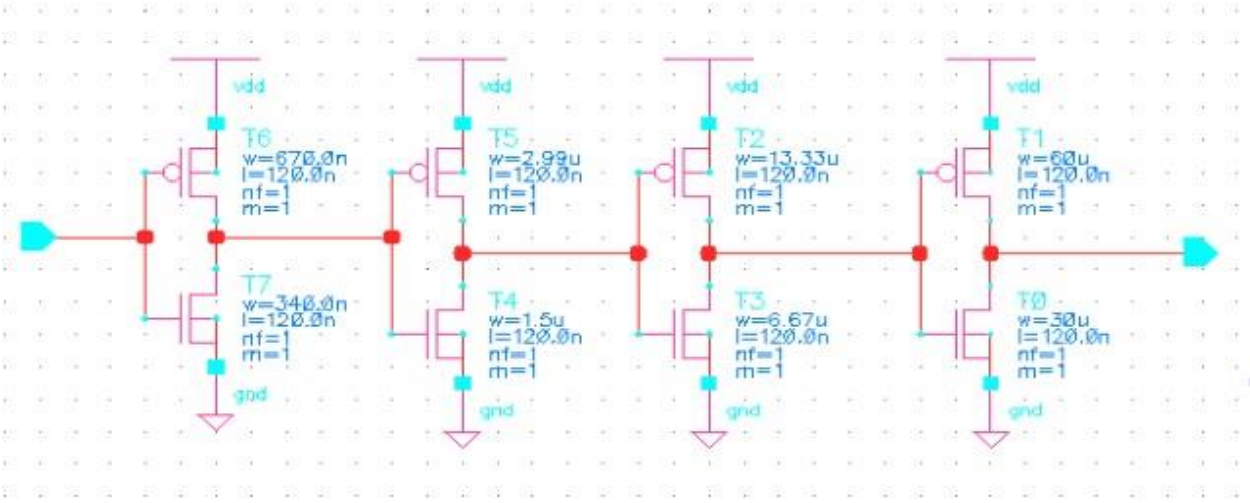


Fig 16. Schematic of clock buffer

7.3 Layout of clock buffer

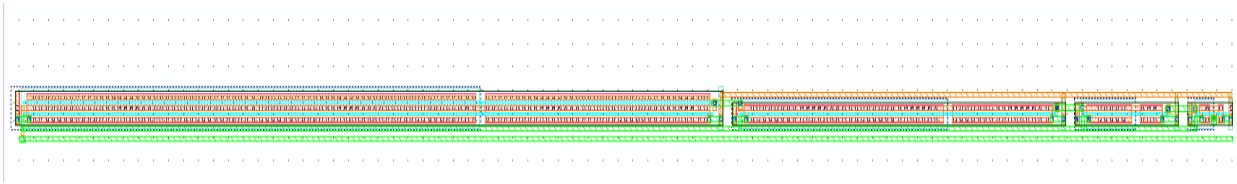


Fig 17. Layout of Clock buffer

8. T-gate

The schematic and layout of T-gate used in our design are given below

8.1 Schematic of T-gate

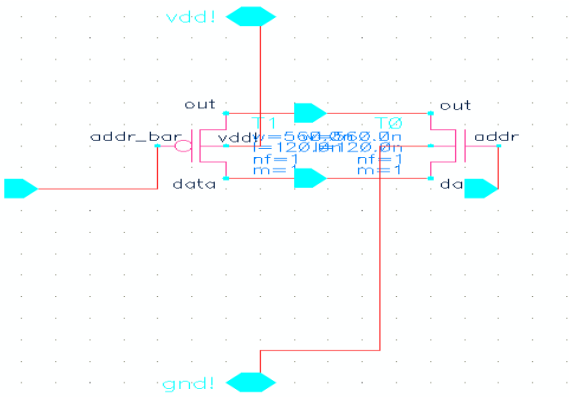


Fig 18. Schematic of T-gate

8.2 Layout of T-gate

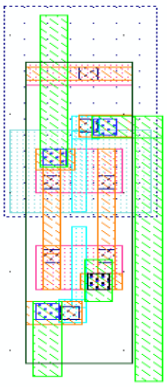


Fig 19. Layout of T-gate

9. DRC and LVS of 8T SRAM design

9.1 Schematic of final 8T SRAM memory array

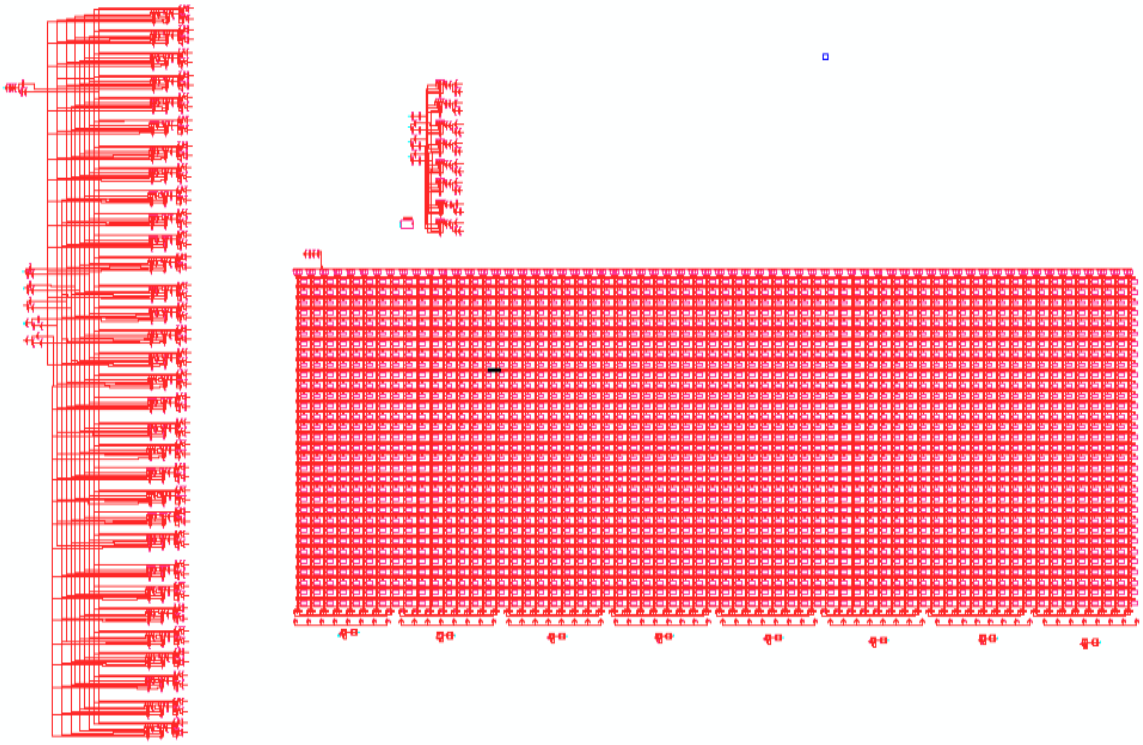


Fig 20. Schematic of 8T-SRAM Design

9.2 Layout of final 8T SRAM memory array

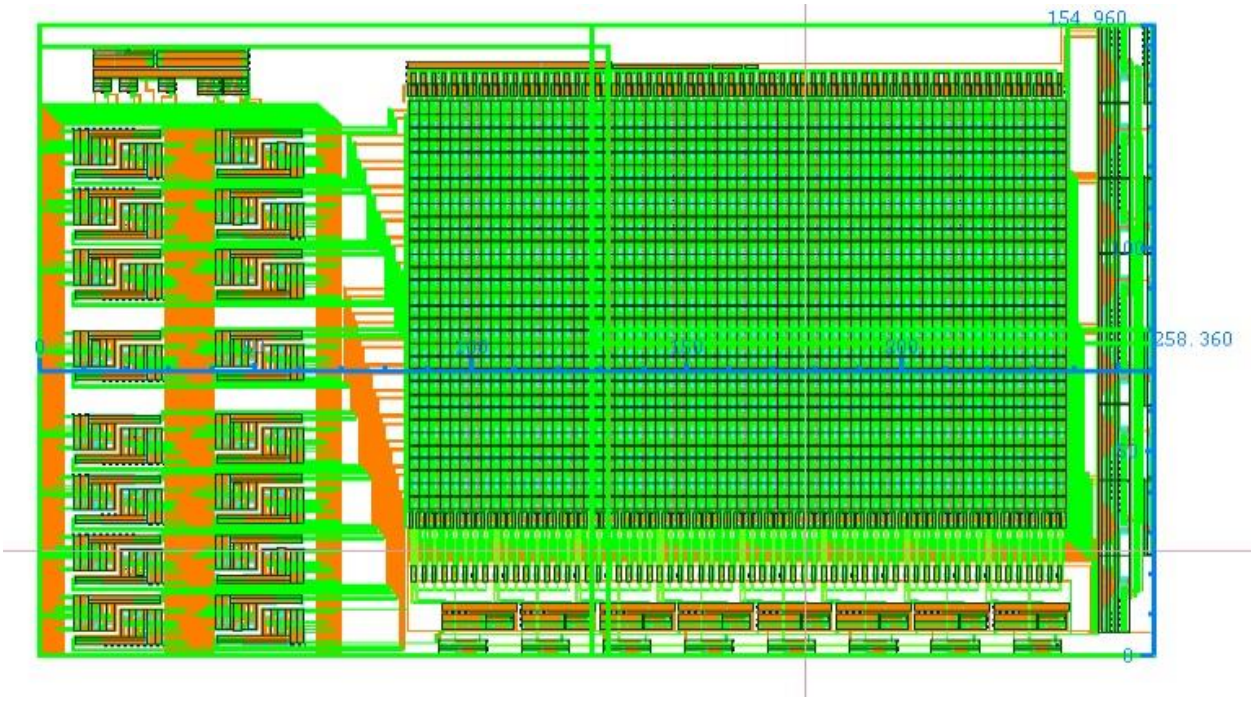


Fig 21. Layout of 8T-SRAM

The height of the final SRAM design 154.800um and width=270.870um

Aspect Ratio =Height/Width= 0.57149um

Total area= 270.870um x 154.800um=41930.676um

9.3 DRC report of 8T-SRAM design

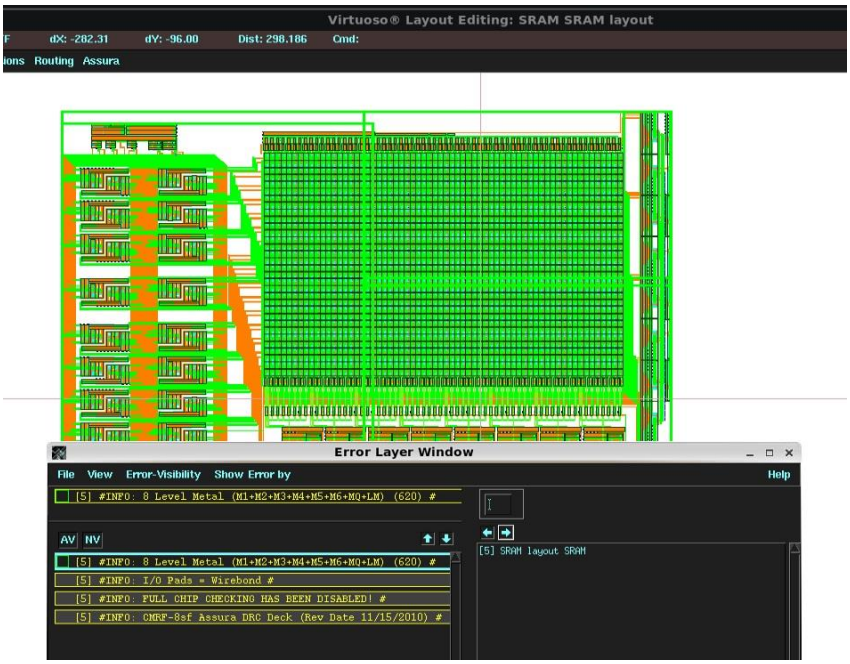


Fig 22. DRC report

9.4 LVS report of 8T-SRAM

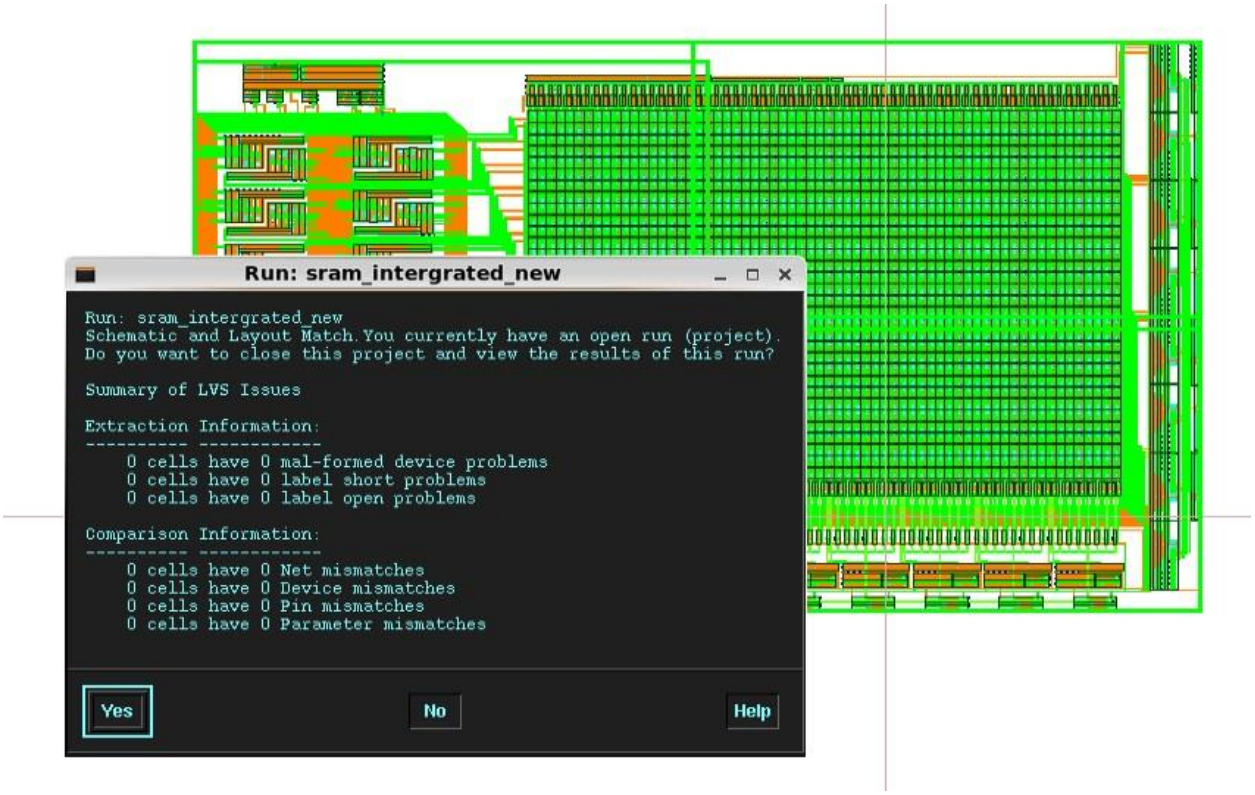


Fig 23. LVS report

10. Timing Analysis

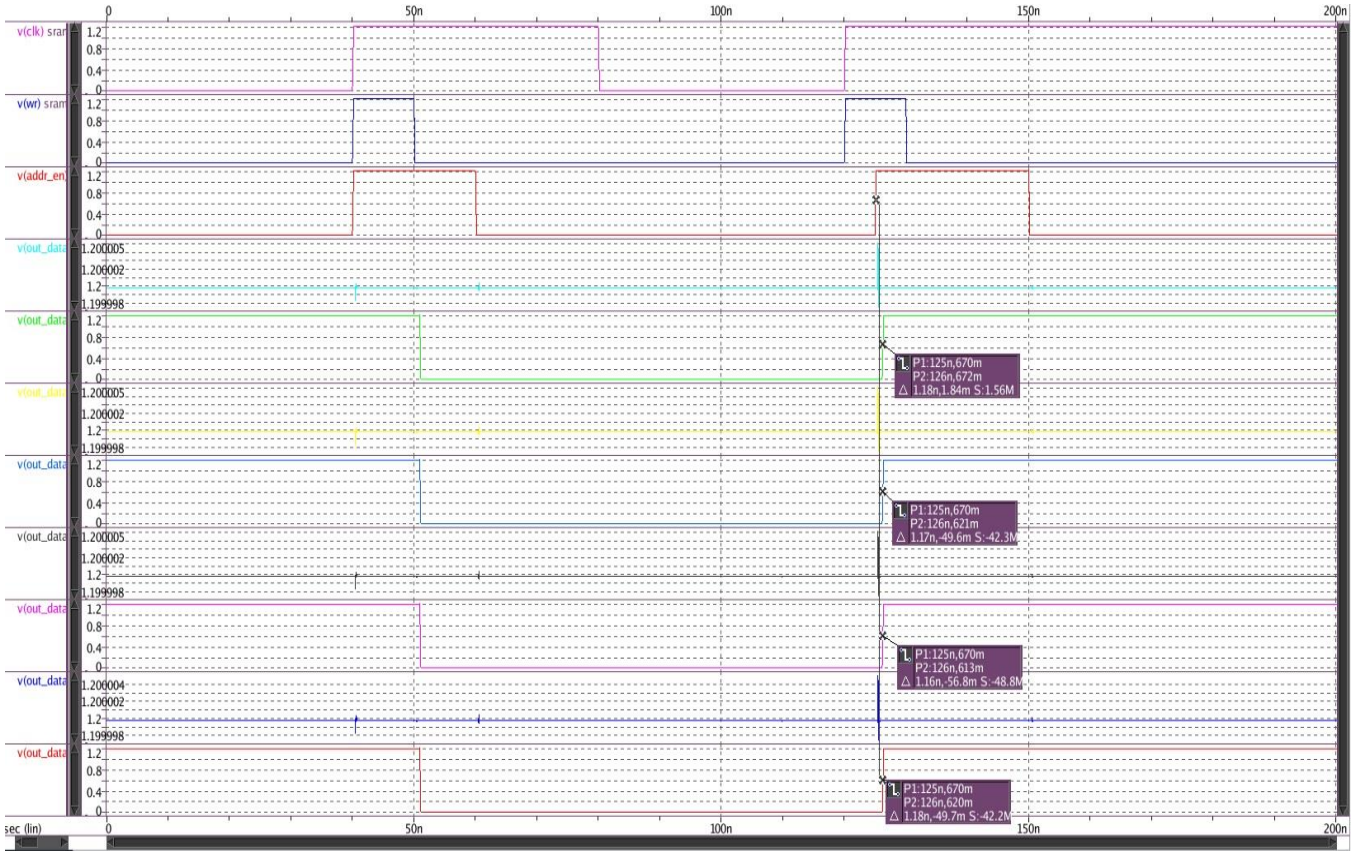
11.1 Hspice code

```
$
$
$transistor model

.include "/home/cad/kits/IBM_CMRF8SF-LM013/IBM_PDK/cmrf8sf/V1.2.0.0LM/HSPICE/models/model013.lib_inc"

.include "sram_intergrated_new.sp"

.option post runlvl=5

xi addr0 addr1 addr2 addr3 addr4 addr5 addr6 addr7 addr_en clk
+ in_data0 in_data1 in_data2 in_data3 in_data4 in_data5 in_data6 in_data7 ref wr
+ out_data0 out_data1 out_data2 out_data3 out_data4 out_data5 out_data6
+ out_data7 SRAM

vdd vdd! vss 1.2V
vss vss 0 0V
Vref ref vss 0.6V
Cout_1 out_data0 0 25fF
Cout_2 out_data1  0 25fF
```

```
Cout_3 out_data2 0 25fF
Cout_4 out_data3 0 25fF
Cout_5 out_data4 0 25fF
Cout_6 out_data5 0 25fF
Cout_7 out_data6 0 25fF
Cout_8 out_data7 0 25fF

**Address lines for row and column decoders

Va0 addr0 vss PWL 0ns 1.2V
Va1 addr1 vss PWL 0ns 1.2V
Va2 addr2 vss PWL 0ns 1.2V
Va3 addr3 vss PWL 0ns 1.2V
Va4 addr4 vss PWL 0ns 1.2V
Va5 addr5 vss PWL 0ns 1.2V
Va6 addr6 vss PWL 0ns 1.2V
Va7 addr7 vss PWL 0ns 1.2V

**Data values to be written
Vd1 in_data0 vss PWL 0ns 1.2V
Vd2 in_data1 vss PWL (0ns 0V 100ns 0V 120.2ns 1.2V)
Vd3 in_data2 vss PWL 0ns 1.2V
Vd4 in_data3 vss PWL (0ns 0V 100ns 0V 120.2ns 1.2V)
Vd5 in_data4 vss PWL 0ns 1.2V
Vd6 in_data5 vss PWL (0ns 0V 100ns 0V 120.2ns 1.2V)
Vd7 in_data6 vss PWL 0ns 1.2V
Vd8 in_data7 vss PWL (0ns 0V 100ns 0V 120.2ns 1.2V)

**Values for Read enable, Write enable and CLK

V1 wr vss PWL(0ns 0V 40ns 0V 40.2ns 1.2V 50ns 1.2V 50.2ns 0V 120ns 0V 120.2ns 1.2V 130ns 1.2V 130.2ns 0V)
V2 addr_en vss PWL(0ns 0V 40ns 0V 40.2ns 1.2V 60ns 1.2V 60.2ns 0V 125ns 0V 125.2ns 1.2V 150ns 1.2V 150.2ns 0V)
V3 clk vss PWL(0ns 0V 40ns 0V 40.2ns 1.2V 80ns 1.2V 80.2ns 0V 120ns 0V 120.2ns 1.2V)
.tr 0.01ns 200ns
.end
```

11. Simulation results

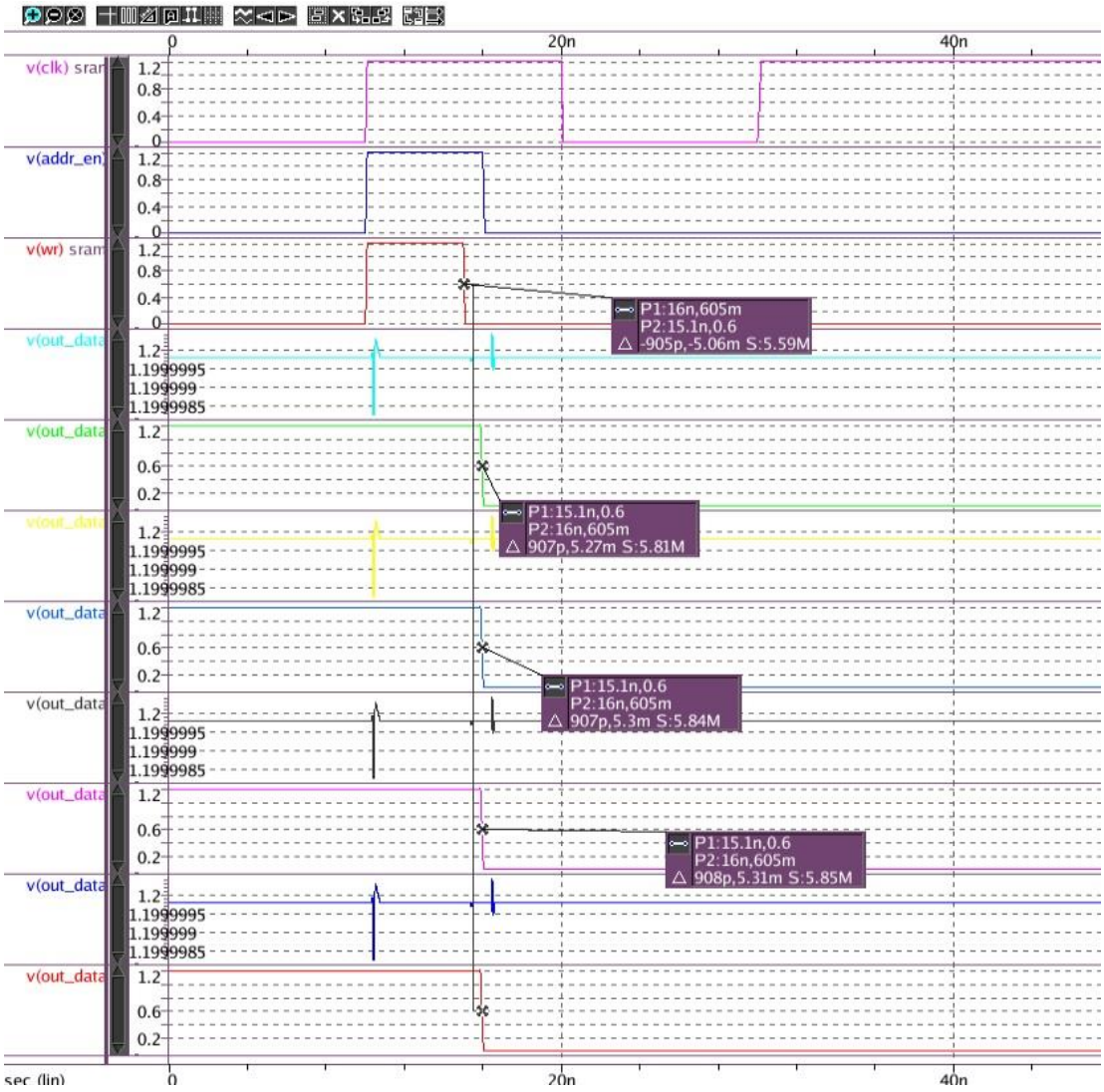
11.1 Worst case delay for reading ‘1’= 1.18ns



The measurement is done using out_data signals and wr or addr_en signal.

The input given initially is given as 10101010 and then made 11111111 to know the worst case time for reading a ‘1’.

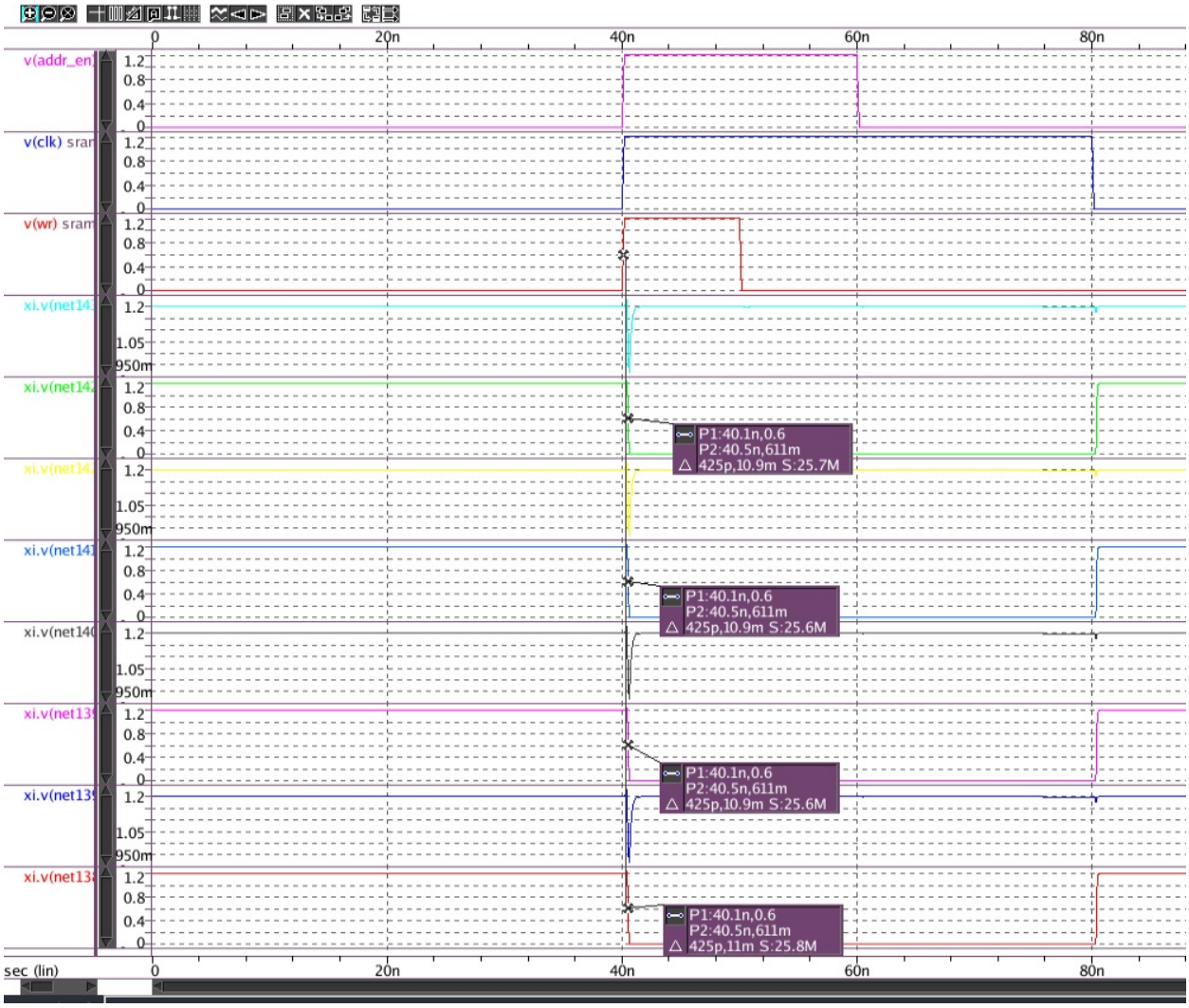
11.3 Worst case delay for reading a ‘0’= 908ps



The measurement is done using out_data signals and wr or addr_en signal.

The input given initially is given as 10101010 to know the worst case time for reading a ‘0’.

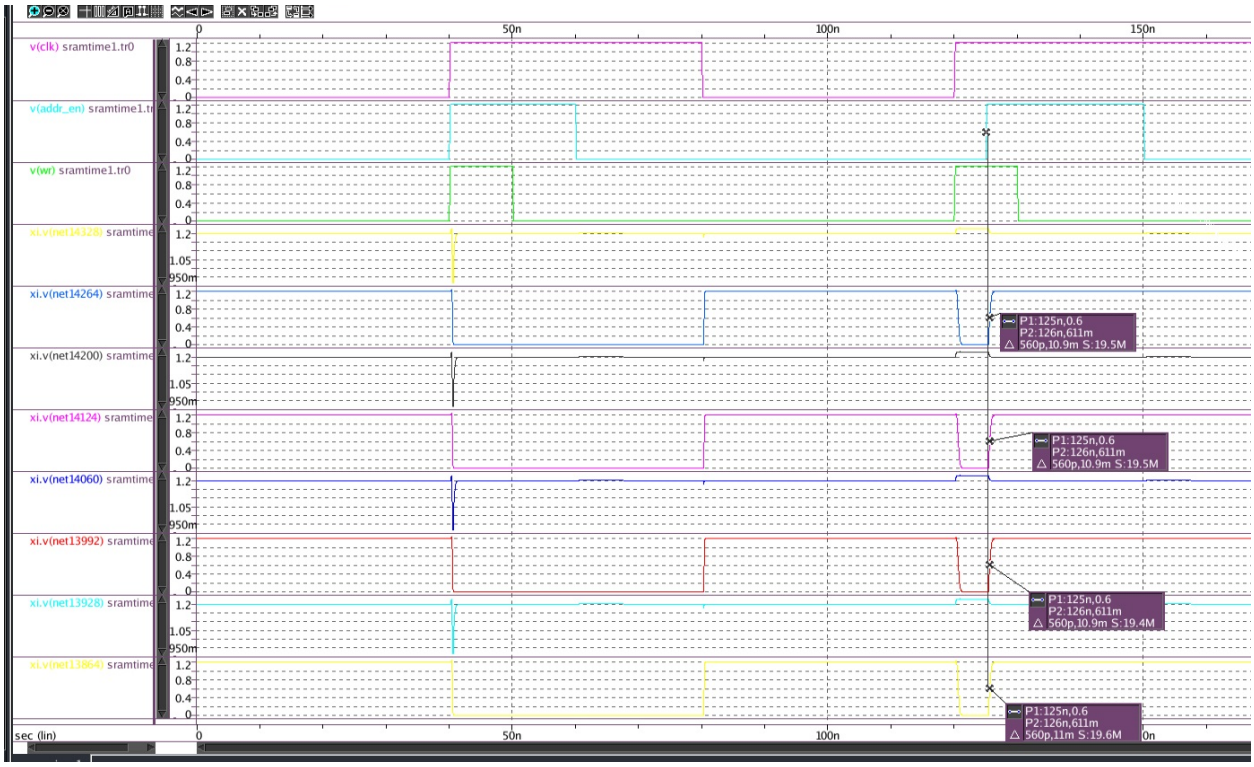
11.3 Worst case delay for writing a ‘0’= 425ps



The measurement is done using net signals at the wbl positions compared to addr_en or wr.

The input given initially is given as 10101010 to know the worst case time for writing a ‘0’.

11.4 Worst case delay for writing a ‘1’= 560ps



The measurement is done using net signals at the wbl positions compared to addr_en or wr.

The input given initially is given as 10101010 and then made 11111111 to know the worst case time for writing a ‘1’.

12. Operating frequency:

The SRAM memory was found functioning correctly even at a period of 10ns.
The ON time of the clock is equal to the worst case read time i.e., 1.18ns.

13. Results and Conclusion:

The SRAM cell of 256 words size is designed with a total area of 40035.3656squm.
The worst case read time is 1.18ns and write time is 560ps.
The SRAM functions coorectly by writing when ‘wr’ signal is high and read otherwise.