

LEVEL SHIFTER

VLSI DESIGN TECHNIQUES

EEM-613

DHA

Session: 2024-2025

Submitted by

Suraj - 220169

Submitted to

Dr. Gufran Ahmad



Dayalbagh Educational Institute, Agra

(Deemed to be University)

Department of Electrical Engineering

Positive Level Shifter for High-Speed Symmetric Switching in Flash Memories

1. TYPE I LEVEL SHIFTER

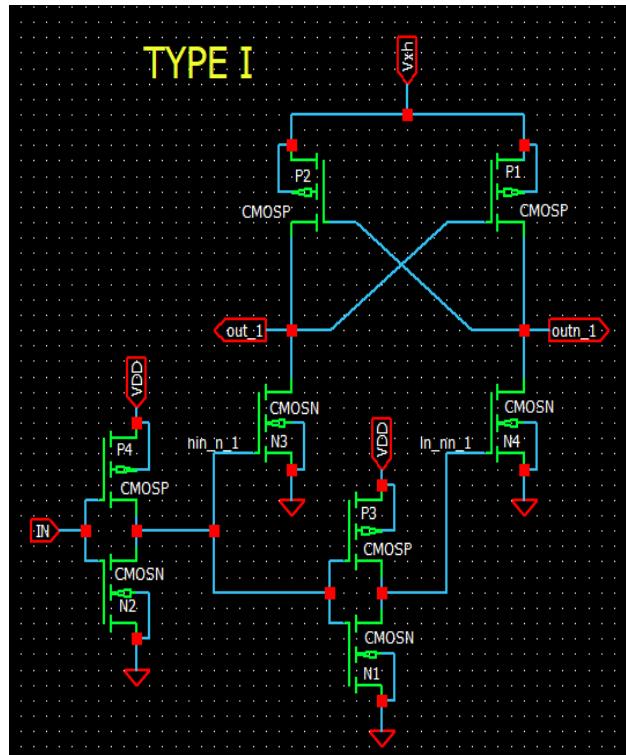


Figure 1: Schematic diagram of type I Level Shifter

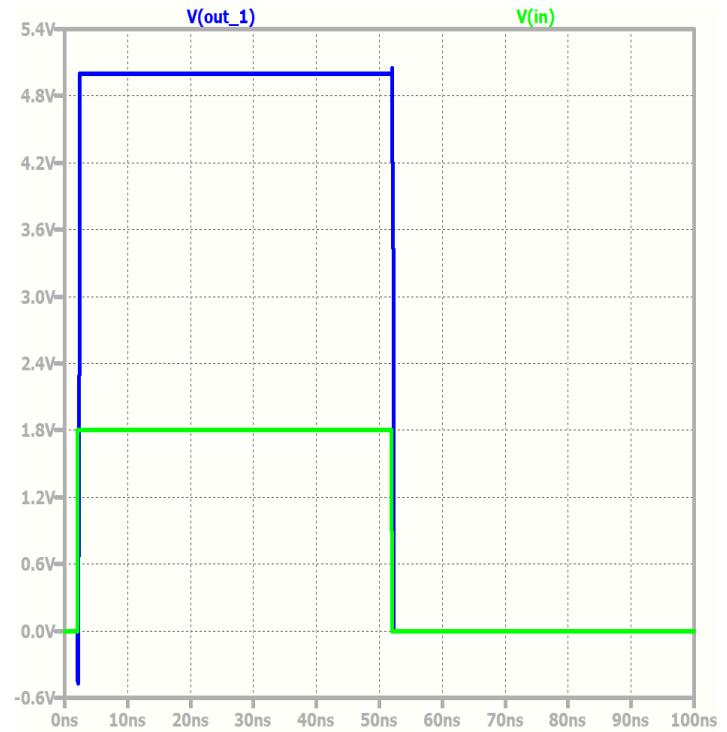


Figure 3: Output of type I Level shifter

2. TYPE II LEVEL SHIFTER

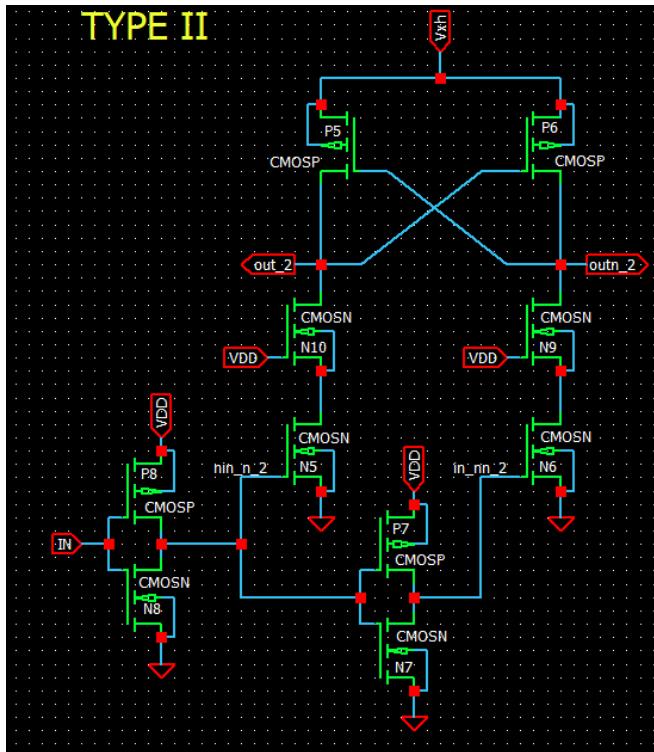


Figure 2: Schematic Diagram of type II Level Shifter



Figure 4: Output of Type II Level shifter

3. TYPE II LEVEL SHIFTER

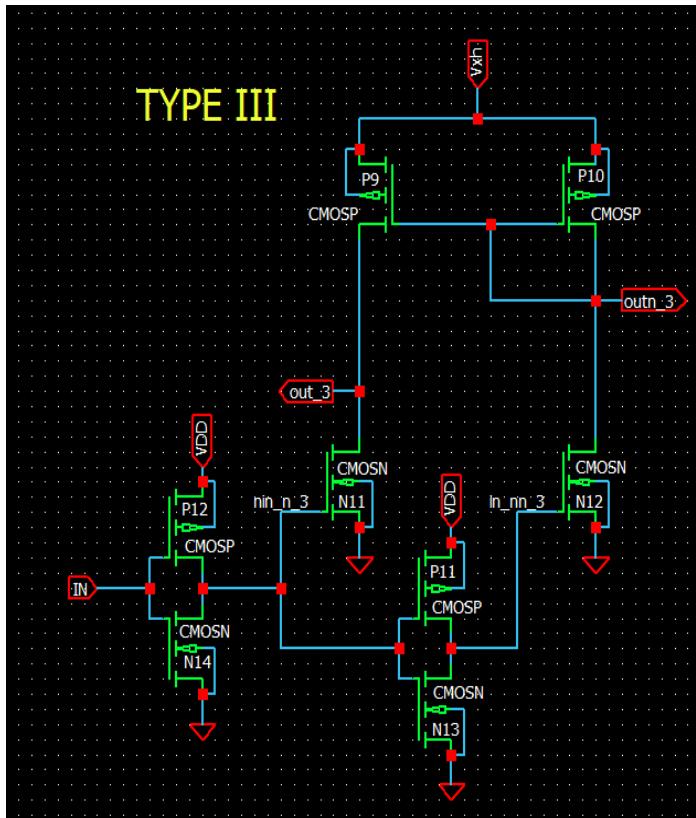


Figure 5: Schematic Diagram of Type III Level Shifter



Figure 7: Output of type III Level Shifter

4. TYPE IV LEVEL SHIFTER

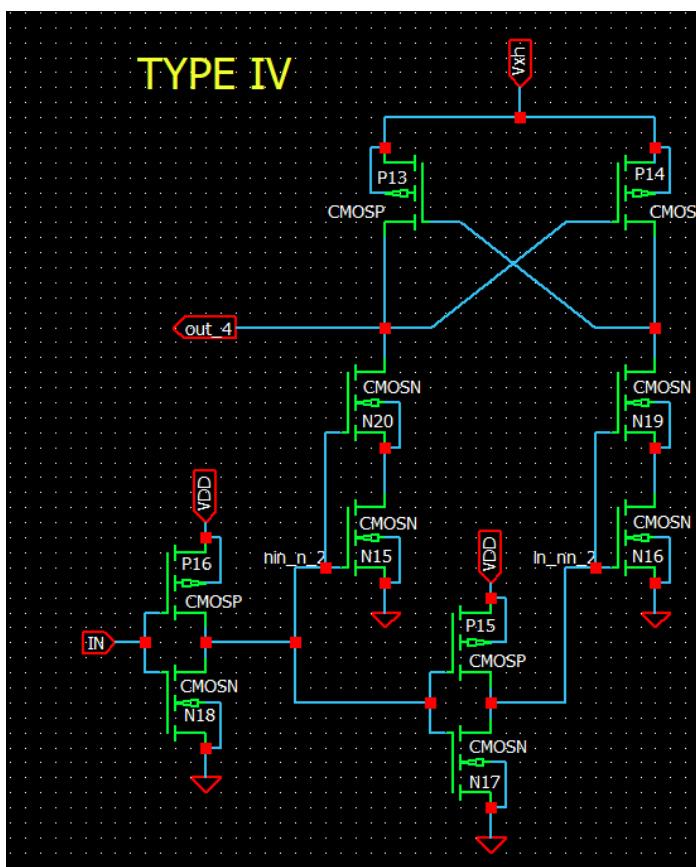


Figure 6: Schematic Diagram of type IV level shifter

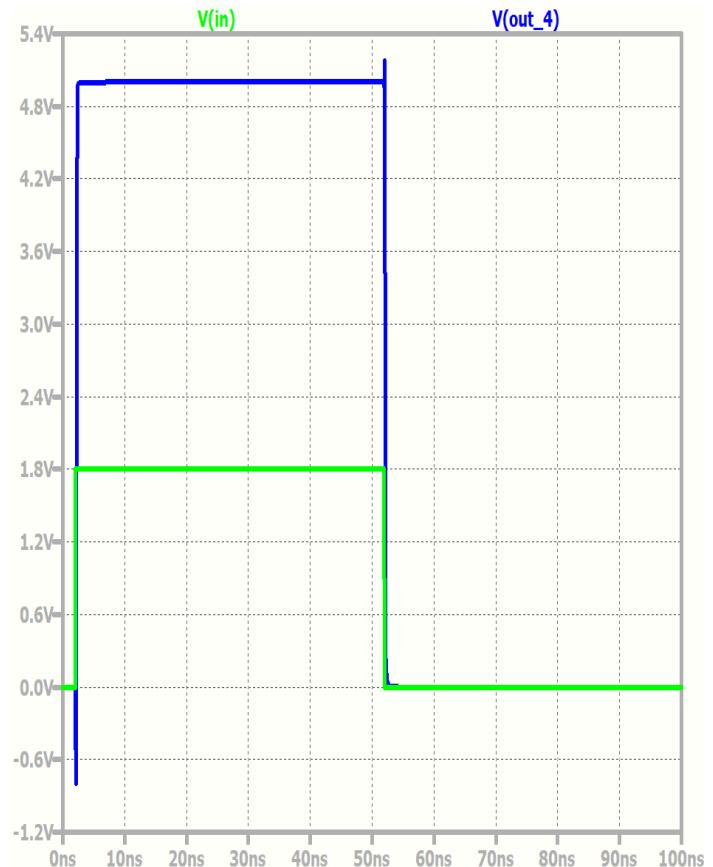


Figure 8: Output of type IV Level Shifter

5. PROPOSED LEVEL SHIFTER

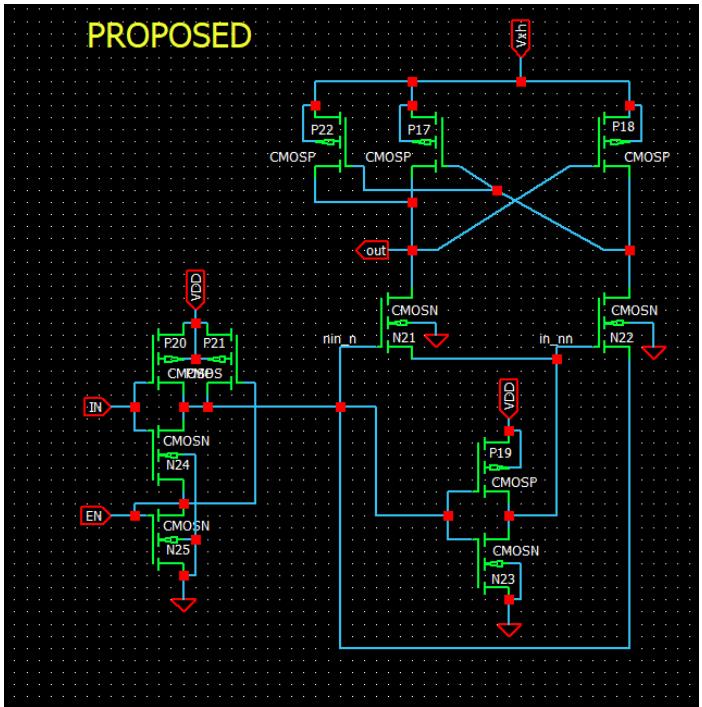


Figure 9: Schematic Diagram of proposed level Shifter

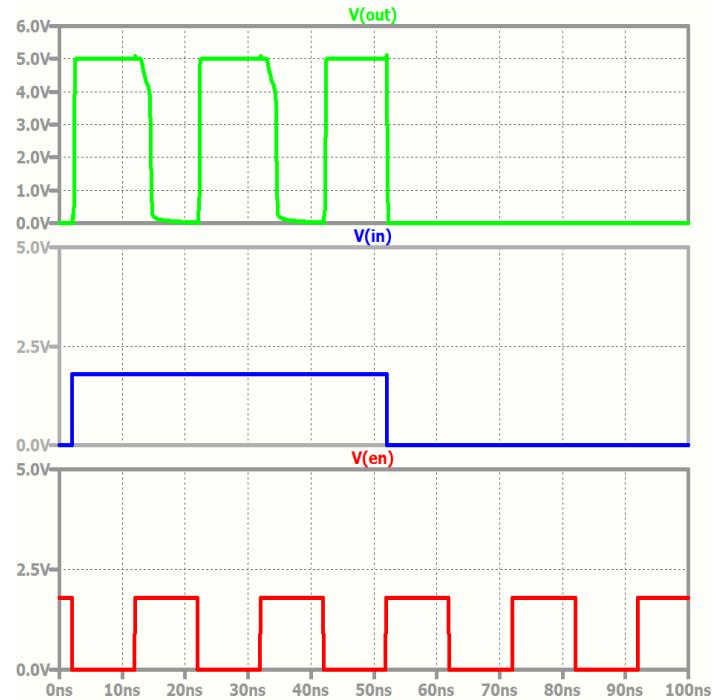


Figure 10: Output of Proposed Level Shifter



CORNER ANALYSIS

1. SLOW SLOW (WORST CASE ANALYSIS)



AVERAGE SWITCHING POWER DISSIPATION WORST CASE

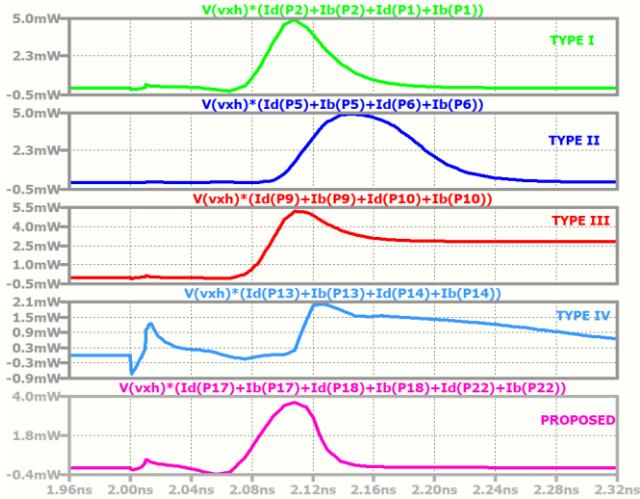


Table 1: Average Switching Delay for worst case

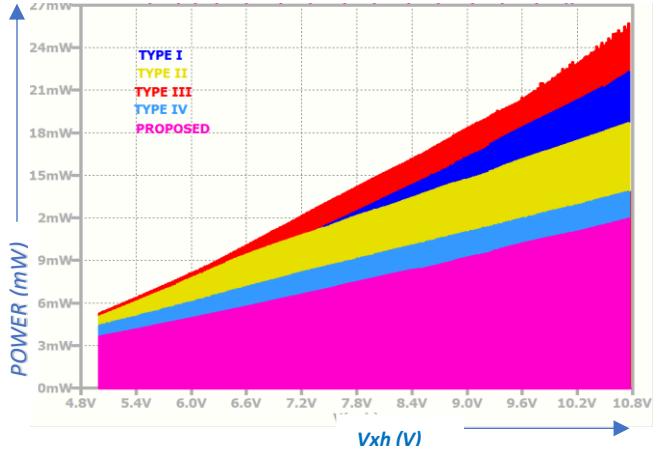
TYPE	CHARGING TIME	DISCHARGING TIME	AVERAGE DELAY
I	1.22943e-10	6.98303e-11	9.63867e-11
II	1.8332e-10	9.31432e-11	1.38232e-10
III	1.13077e-10	6.73133e-11	9.01952e-11
IV	2.54232e-10	1.47135e-10	2.00684e-10
PROPOSED	1.1022e-10	7.27341e-10	4.1878e-10

Table 2: Power Dissipation in Worst Case

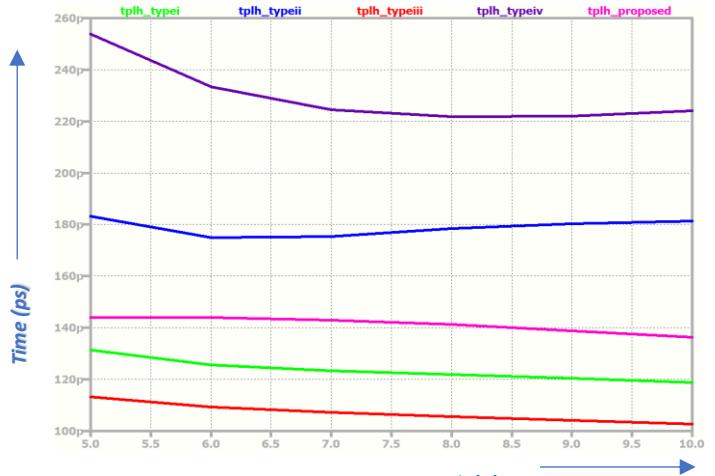
TYPE	STATIC POWER	DYNAMIC POWER	TOTAL POWER
I	3.0718nW	5.0796μW	5.0796μW
II	3.2321nW	8.3577μW	8.3577μW
III	16.176nW	1.4175mw	1.4175mw
IV	23.707pW	16.557μW	16.557μW
PROPOSED	3.1478nW	12.215μW	12.215μW

VOLTAGE VARIATIONS

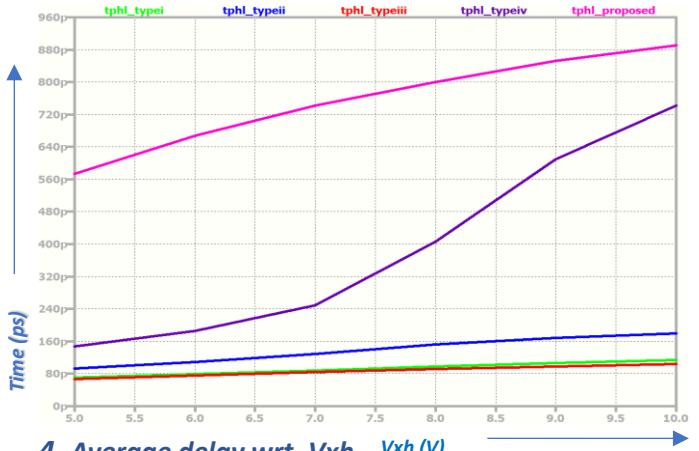
1. Dynamic Power dissipation wrt V_{xh}



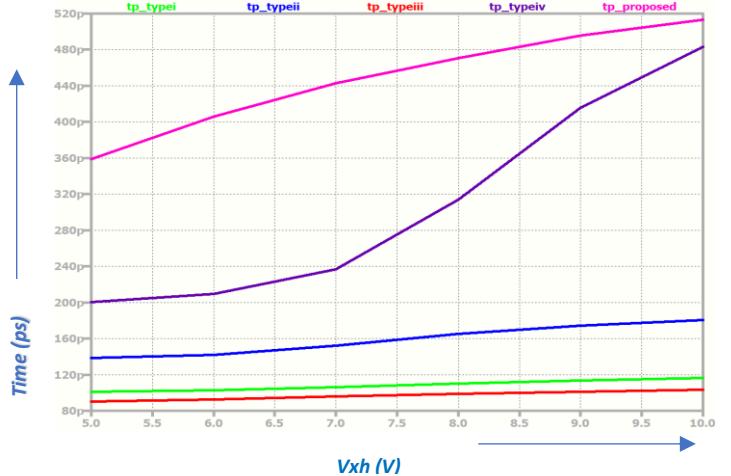
2. Charging time wrt V_{xh}



3. Discharging time wrt V_{xh}



4. Average delay wrt. V_{xh}



2. BEST CASE ANALYSIS (Fast Fast)



DYNAMIC POWER DISSIPATION

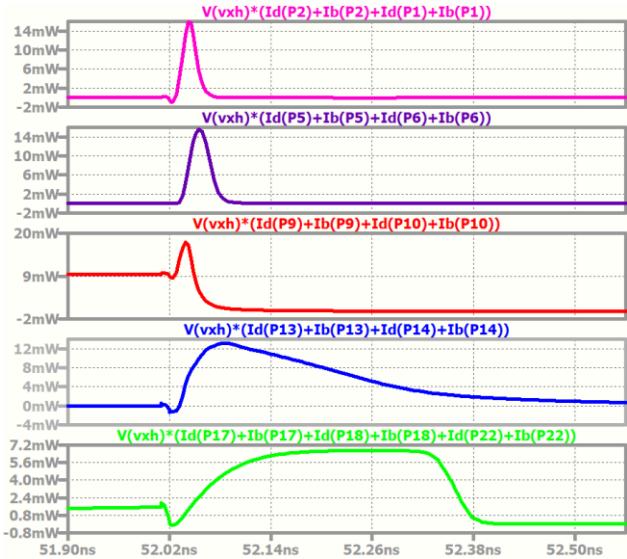


Table 3: Average Switching Delay for Best case

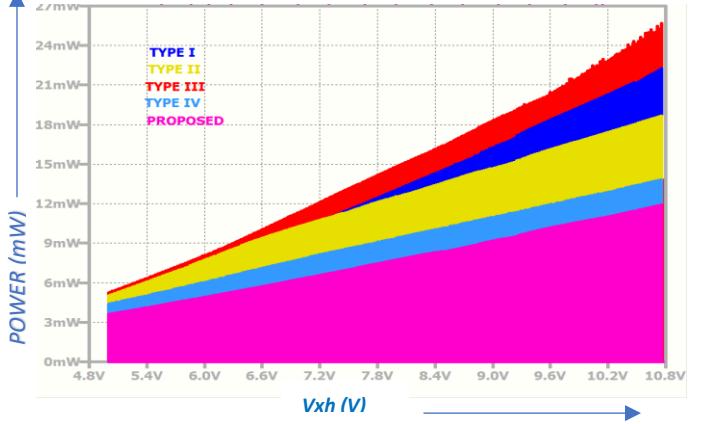
TYPE	CHARGING TIME	DISCHARGING TIME	AVERAGE DELAY
I	4.2474e-11	2.26034e-11	3.25387e-11
II	6.18439e-11	3.1072e-11	4.6458e-11
III	3.92468e-11	2.17248e-11	3.04858e-11
IV	7.94685e-11	5.04124e-11	6.49404e-11
PROPOSED	4.59794e-11	1.46955e-10	9.64673e-11

Table 4: Power Dissipation in Best Case

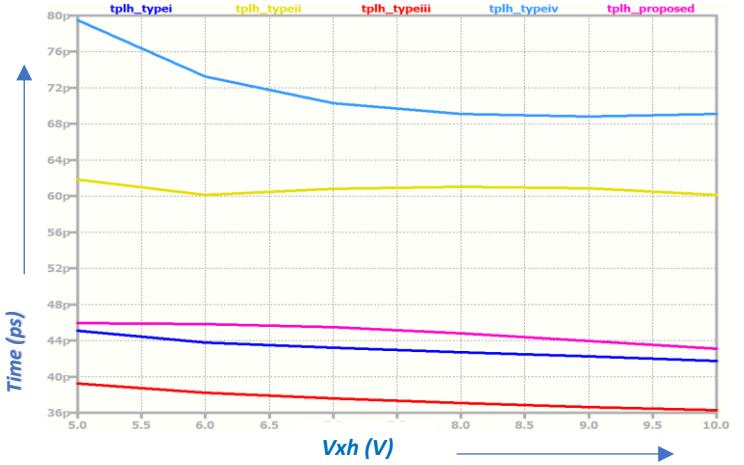
TYPE	STATIC POWER	DYNAMIC POWER	TOTAL POWER
I	6.6925nW	5.0796μW	5.0796μW
II	1.3097nW	8.3577μW	8.3577μW
III	506.04nW	1.4175mw	1.4175mw
IV	923.04pW	16.557μW	16.557μW
PROPOSED	730.41pW	12.215μW	12.215μW

VOLTAGE VARIATIONS

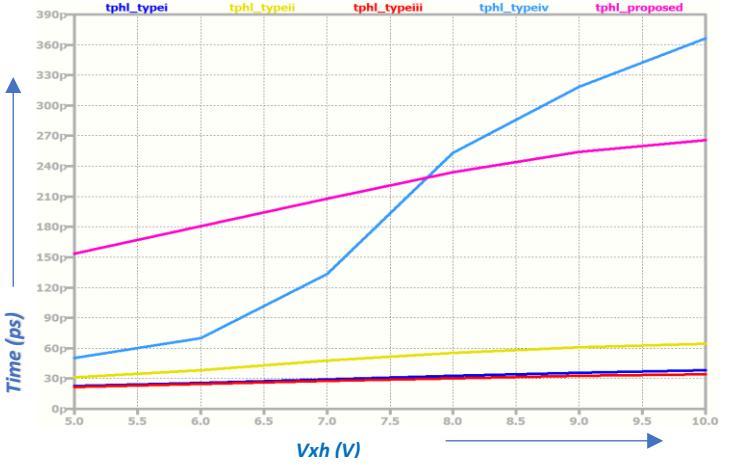
1. Dynamic Power wrt V_{xh}



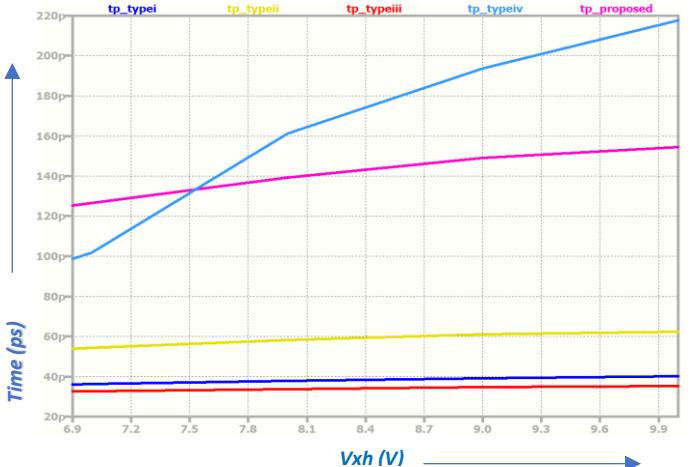
2. Charging time wrt V_{xh}



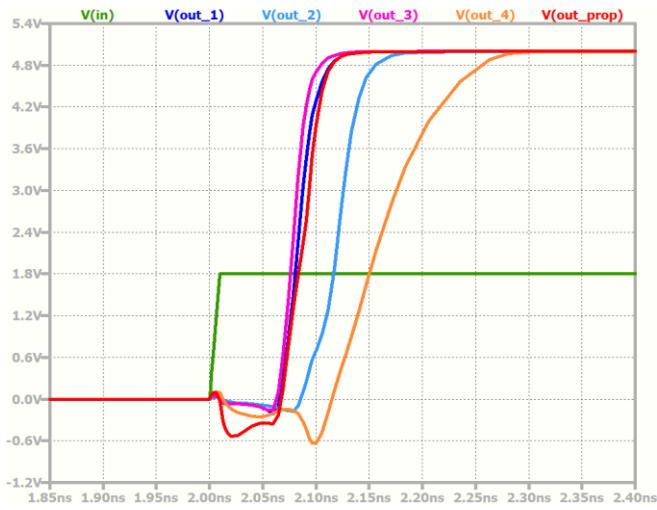
3. Discharging time wrt V_{xh}



4. Average Delay



4. SLOW FAST



DYNAMIC POWER DISSIPATION

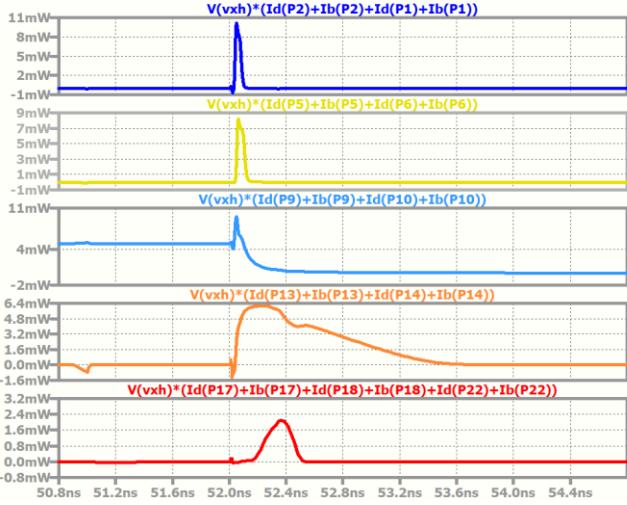


Table 5: Average Switching Delay for SF Corner

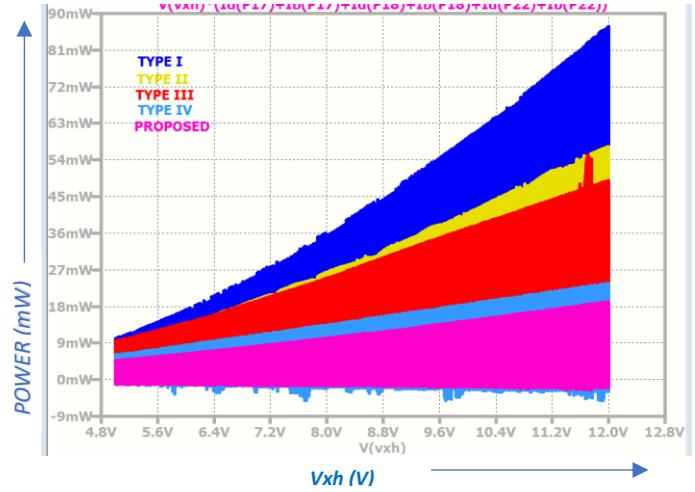
TYPE	CHARGING TIME	DISCHARGING TIME	AVERAGE DELAY
I	7.98237e-11	3.57101e-11	5.77669e-11
II	1.1686e-10	5.6047e-11	8.64536e-11
III	7.47015e-11	3.39316e-11	5.43166e-11
IV	1.59248e-10	1.13429e-10	1.36338e-10
PROPOSED	8.51776e-11	4.05918e-10	2.45548e-10

Table 6: Power Dissipation at SF Corner

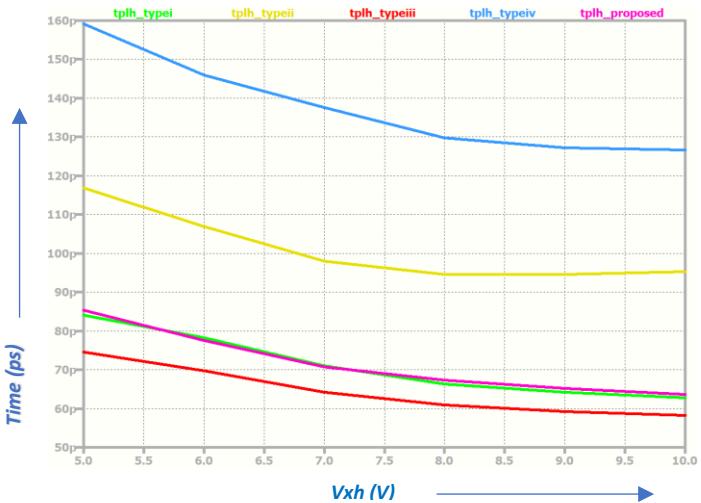
TYPE	STATIC POWER	DYNAMIC POWER	TOTAL POWER
I	5.2129nW	6.4778μW	6.4778μW
II	5.0038nW	8.3617μW	8.3617μW
III	514.17nW	2.5171mW	2.5171mW
IV	5.0038nW	47.787μW	47.787μW
PROPOSED	4.3114nW	5.2717μW	5.2717μW

VOLTAGE

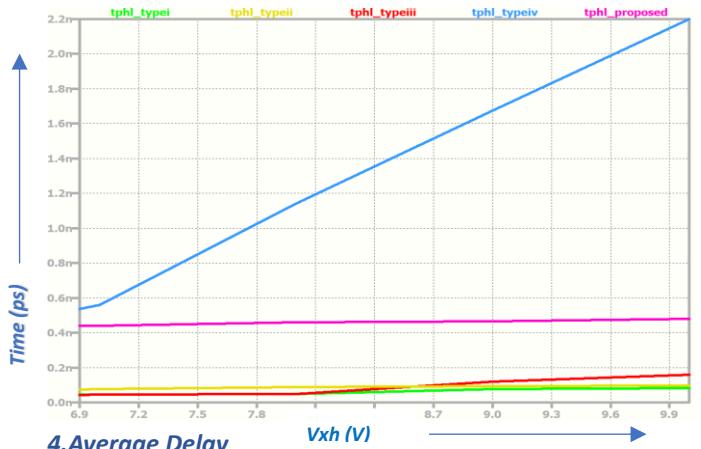
1. Dynamic Power wrt Vxh



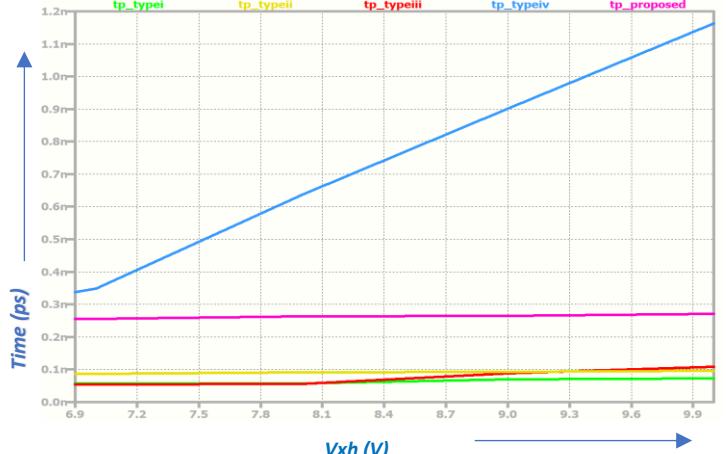
2. Charging time wrt Vxh



1. Discharging time wrt Vxh



4. Average Delay



3. FAST SLOW



DYNAMIC POWER DISSIPATION

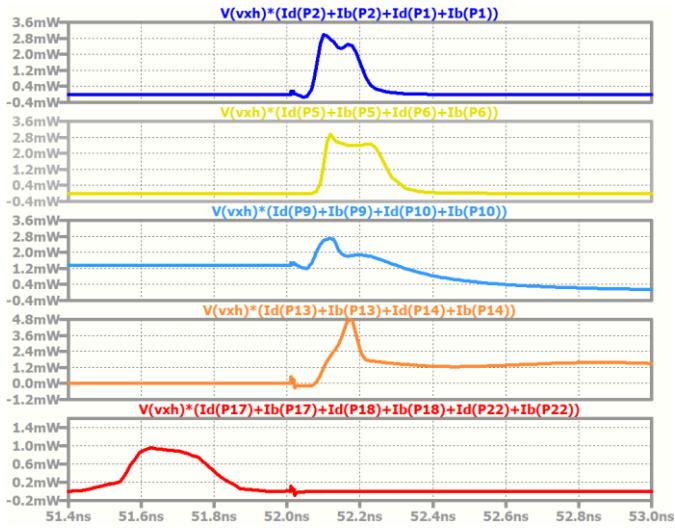


Table 7: Average Switching Delay for FS Corner

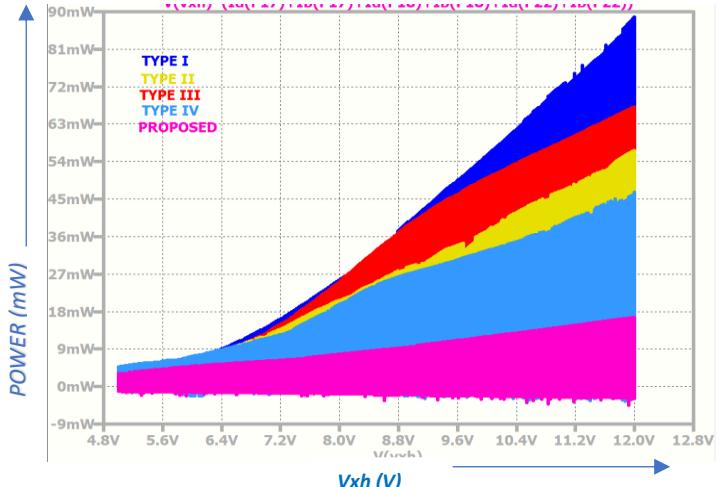
TYPE	CHARGING TIME	DISCHARGING TIME	AVERAGE DELAY
I	$1.15233e-10$	$8.05628e-11$	$9.7898e-11$
II	$1.97961e-10$	$9.8253e-11$	$1.48107e-10$
III	$9.93106e-11$	$7.80521e-11$	$8.86814e-11$
IV	$3.06579e-10$	$1.41839e-10$	$2.24209e-10$
PROPOSED	$1.3643e-10$	$-3.56174e-10$	$1.09872e-10$

Table 8: Power Dissipation in FS Corner

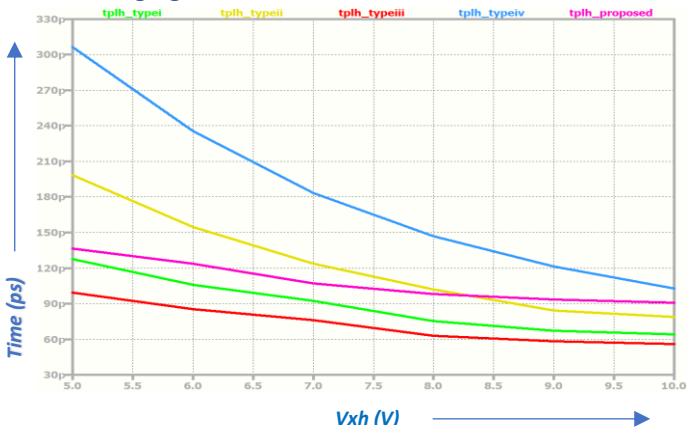
TYPE	STATIC POWER	DYNAMIC POWER	TOTAL POWER
I	$4.1936nW$	$6.0325\mu W$	$6.0325\mu W$
II	$-1.1892nW$	$9.1231\mu W$	$9.1231\mu W$
III	$17.084\mu W$	$683.56\mu W$	$683.56\mu W$
IV	$286.83pW$	$32.009\mu W$	$32.009\mu W$
PROPOSED	$801.45pW$	$3.3996\mu W$	$3.3996\mu W$

VOLTAGE VARIATIONS

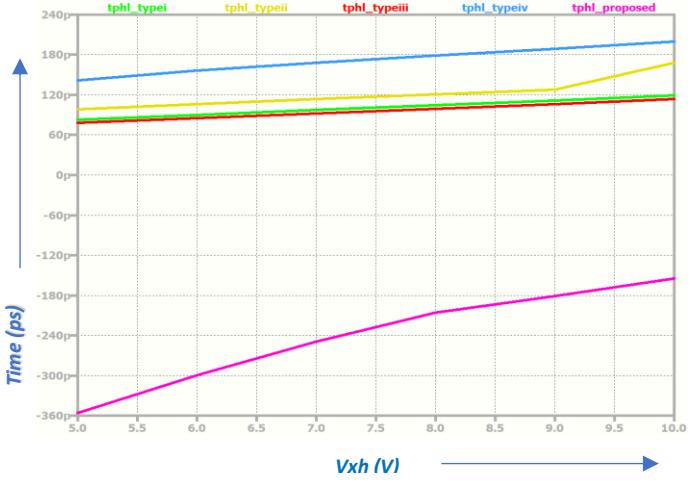
1. Dynamic Power wrt Vxh



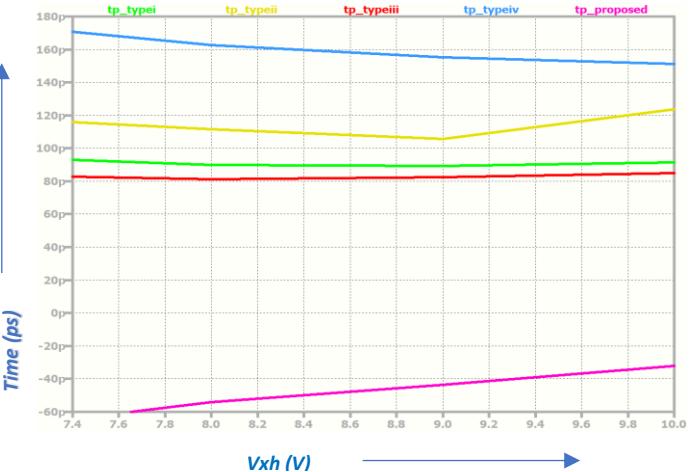
2. Charging time wrt Vxh



3. Discharging=g time wrt Vxh



4. Average Delay wrt Vxh



5. TYPICAL TYPICAL



DYNAMIC POWER DISSIPATION

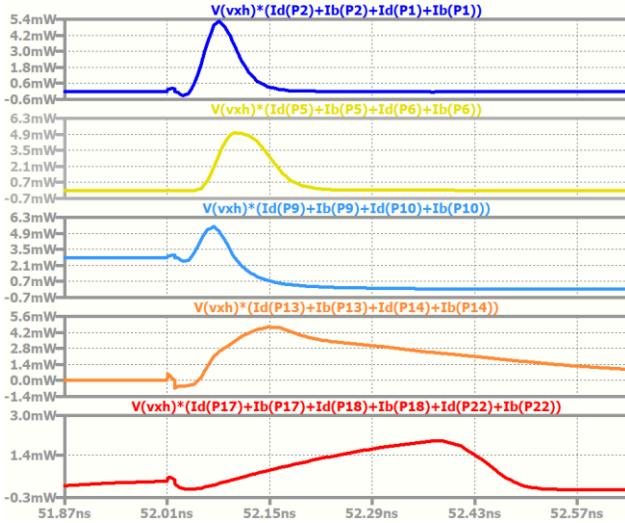


Table 9: Average Switching Delay for Normal Case

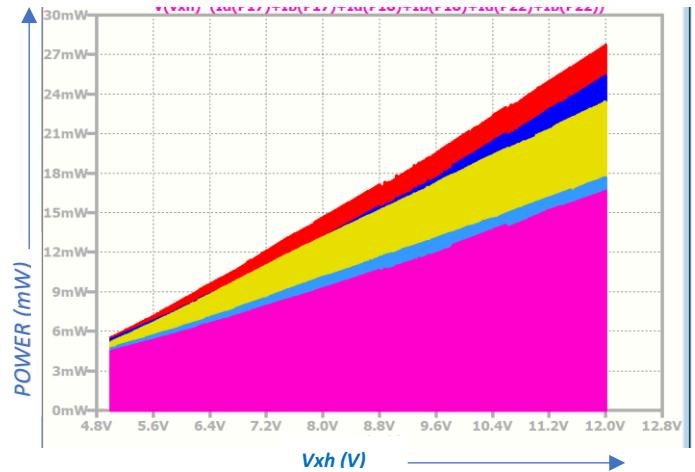
TYPE	CHARGING TIME	DISCHARGING TIME	AVERAGE DELAY
I	4.2474e-11	2.26034e-11	3.25387e-11
II	6.18439e-11	3.1072e-11	4.6458e-11
III	3.92468e-11	2.17248e-11	3.04858e-11
IV	7.94685e-11	5.04124e-11	6.49404e-11
PROPOSED	4.59794e-11	1.46955e-10	9.64673e-11

Table 10: Power Dissipation in Normal Case

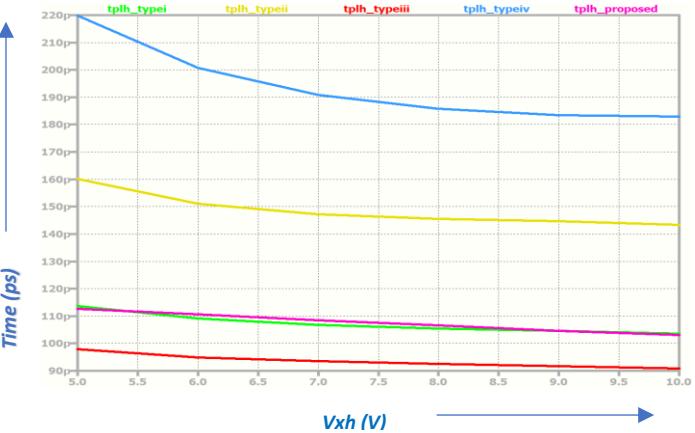
TYPE	STATIC POWER	DYNAMIC POWER	TOTAL POWER
I	1.9426nW	5.05μW	5.05μW
II	642.4pW	8.2071μW	8.2071μW
III	244.75nW	1.393mW	1.393mW
IV	539.98pW	21.375μW	21.375μW
PROPOSED	631.56pW	6.95μW	6.95μW

VOLTAGE VARIATION

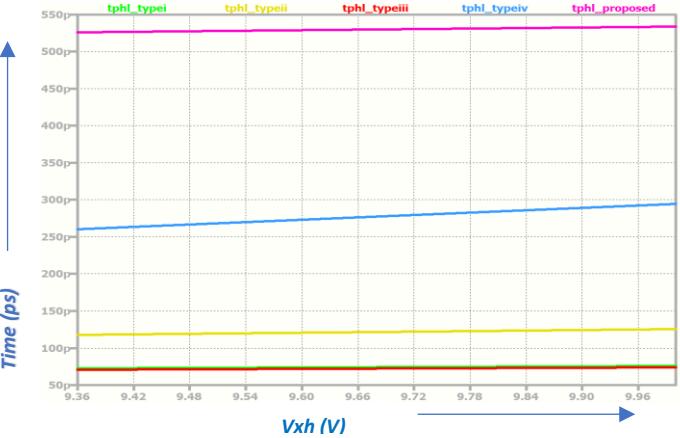
1. Average Power wrt Vxh



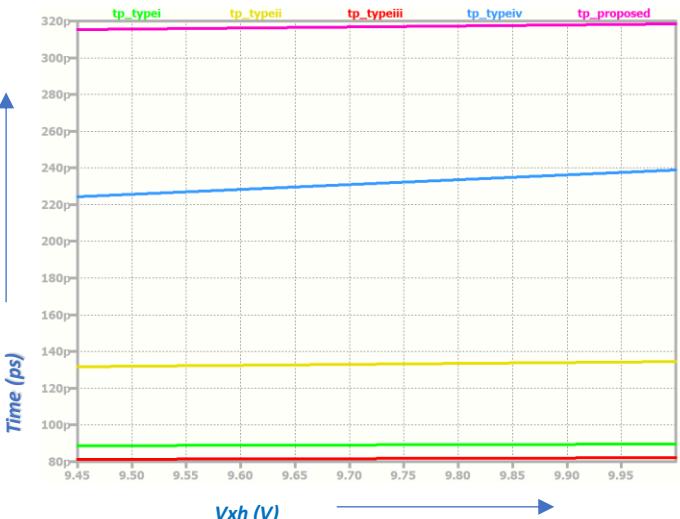
2. Charging time wrt Vxh



3. Discharging=g time wrt Vxh



4. Average Delay wrt Vxh



2. VOLATGE VARIATION

TYPE 4

TYPE 1

<i>Vxh</i>	<i>Charging time (tplh)</i>	<i>Discharging Time (tphl)</i>	<i>Average delay (tpd)</i>
1	1.06864e-10	4.97813e-11	7.83229e-11
2	1.02963e-10	5.58026e-11	7.93828e-11
3	1.01246e-10	6.15575e-11	8.14016e-11
4	1.00334e-10	6.73628e-11	8.38481e-11
5	9.93924e-11	7.31901e-11	8.62913e-11

<i>Vxh</i>	<i>Charging time (tplh)</i>	<i>Discharging Time (tph)</i>	<i>Average delay (tpd)</i>
1	2.19951e-10	1.09505e-10	1.64728e-10
2	2.00483e-10	1.33801e-10	1.67142e-10
3	1.90609e-10	1.62221e-10	1.76415e-10
4	1.85625e-10	1.96899e-10	1.91262e-10
5	1.83448e-10	2.41628e-10	2.12538e-10

TYPE 2

<i>Vxh</i>	<i>Charging time (tplh)</i>	<i>Discharging Time (tphl)</i>	<i>Average delay (tpd)</i>
1	1.60326e-10	6.9078e-11	1.14702e-10
2	1.51274e-10	7.86397e-11	1.14957e-10
3	1.47049e-10	8.93513e-11	1.182e-10
4	1.45633e-10	1.01028e-10	1.23331e-10
5	1.44471e-10	1.13595e-10	1.29033e-10

TYPE 5

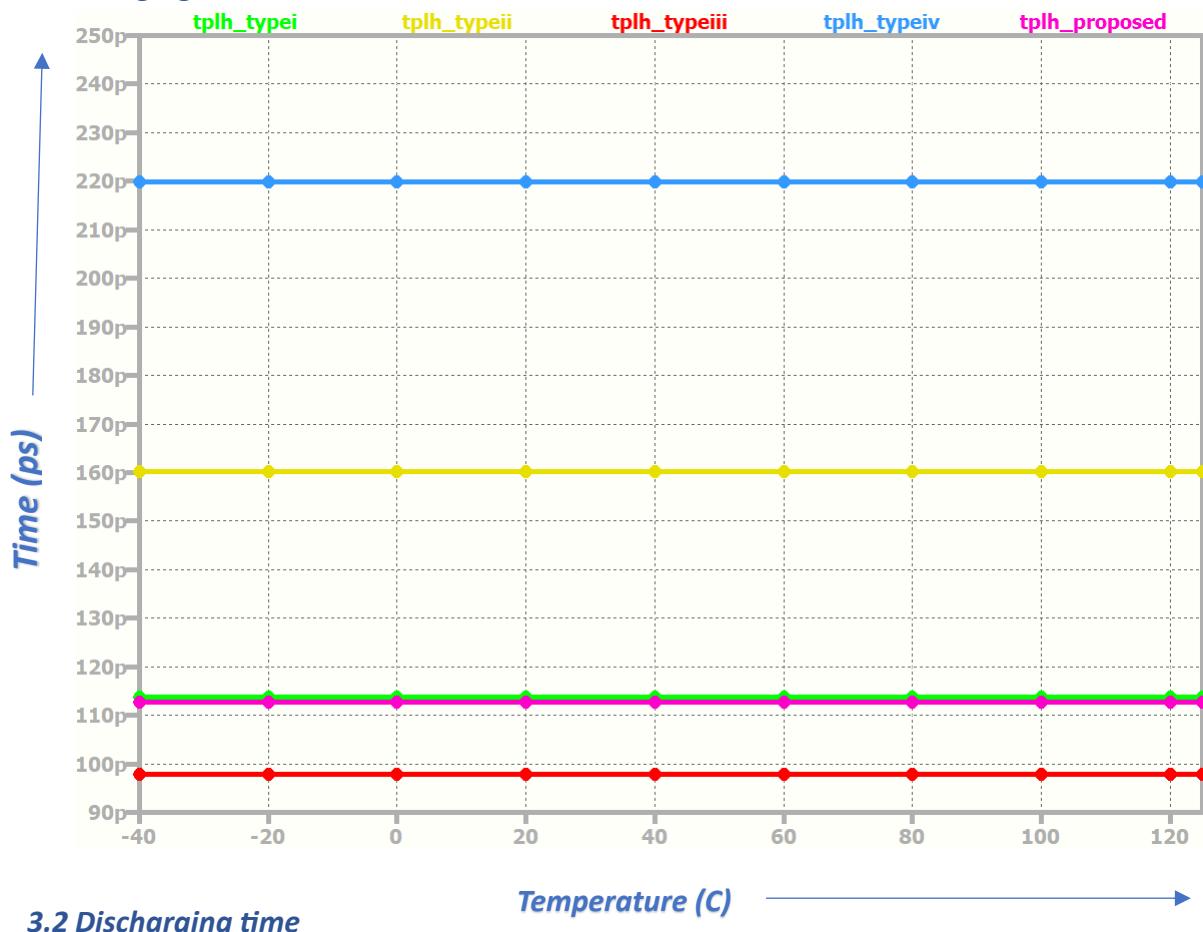
<i>Vxh</i>	<i>Charging time (tplh)</i>	<i>Discharging Time (tph)</i>	<i>Average delay (tpd)</i>
1	1.12525e-10	3.97201e-10	2.54863e-10
2	1.10502e-10	4.45835e-10	2.78169e-10
3	1.08481e-10	4.76093e-10	2.92287e-10
4	1.0649e-10	5.00106e-10	3.03298e-10
5	1.04703e-10	5.18227e-10	3.11465e-10

TYPE 3

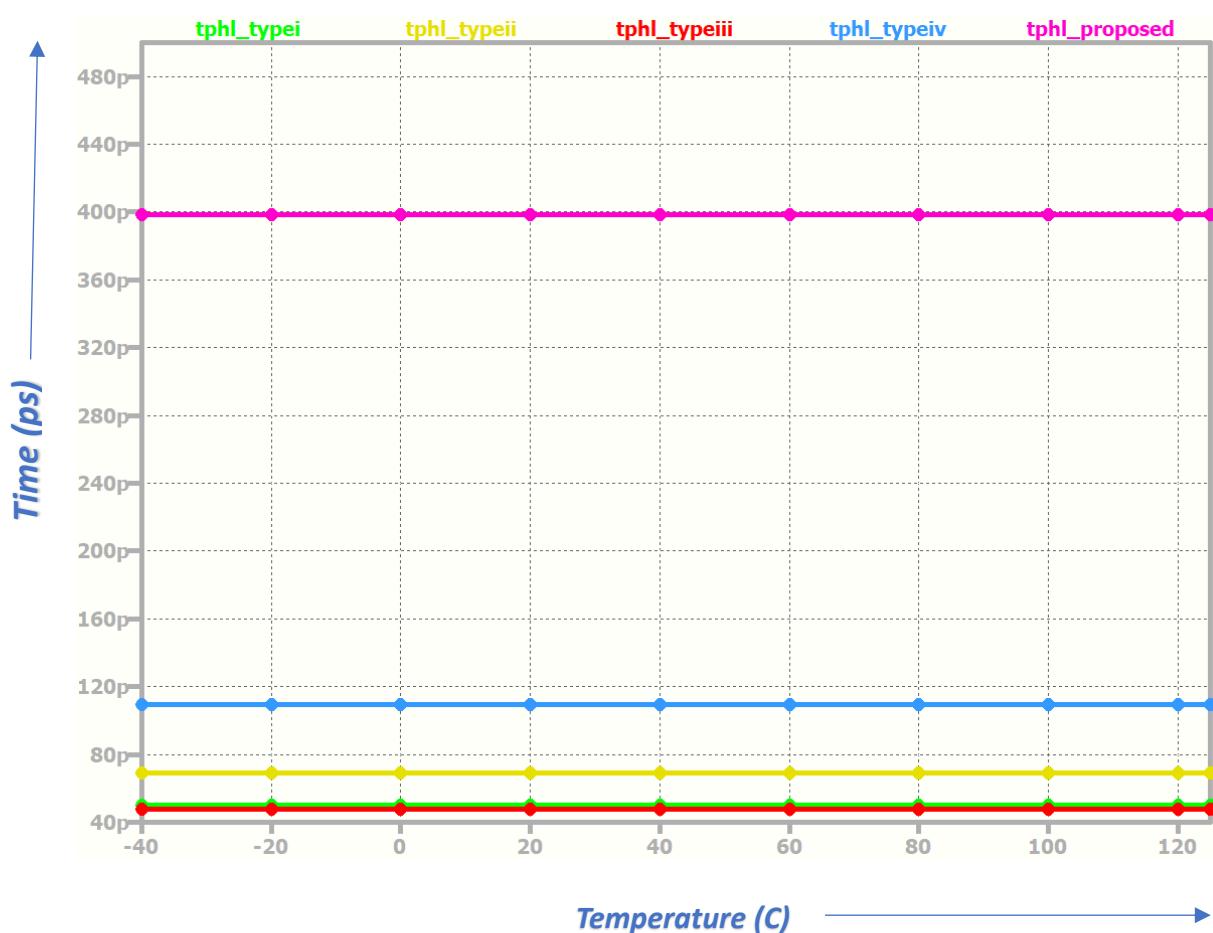
<i>Vxh</i>	<i>Charging time (tplh)</i>	<i>Discharging Time (tphl)</i>	<i>Average delay (tpd)</i>
1	9.77608e-11	4.76249e-11	7.26928e-11
2	9.48304e-11	5.32926e-11	7.40615e-11
3	9.33998e-11	5.85403e-11	7.59701e-11
4	9.25461e-11	6.36698e-11	7.8108e-11
5	9.16509e-11	6.87426e-11	8.01968e-11

3. TEMPERATURE VARIATIONS

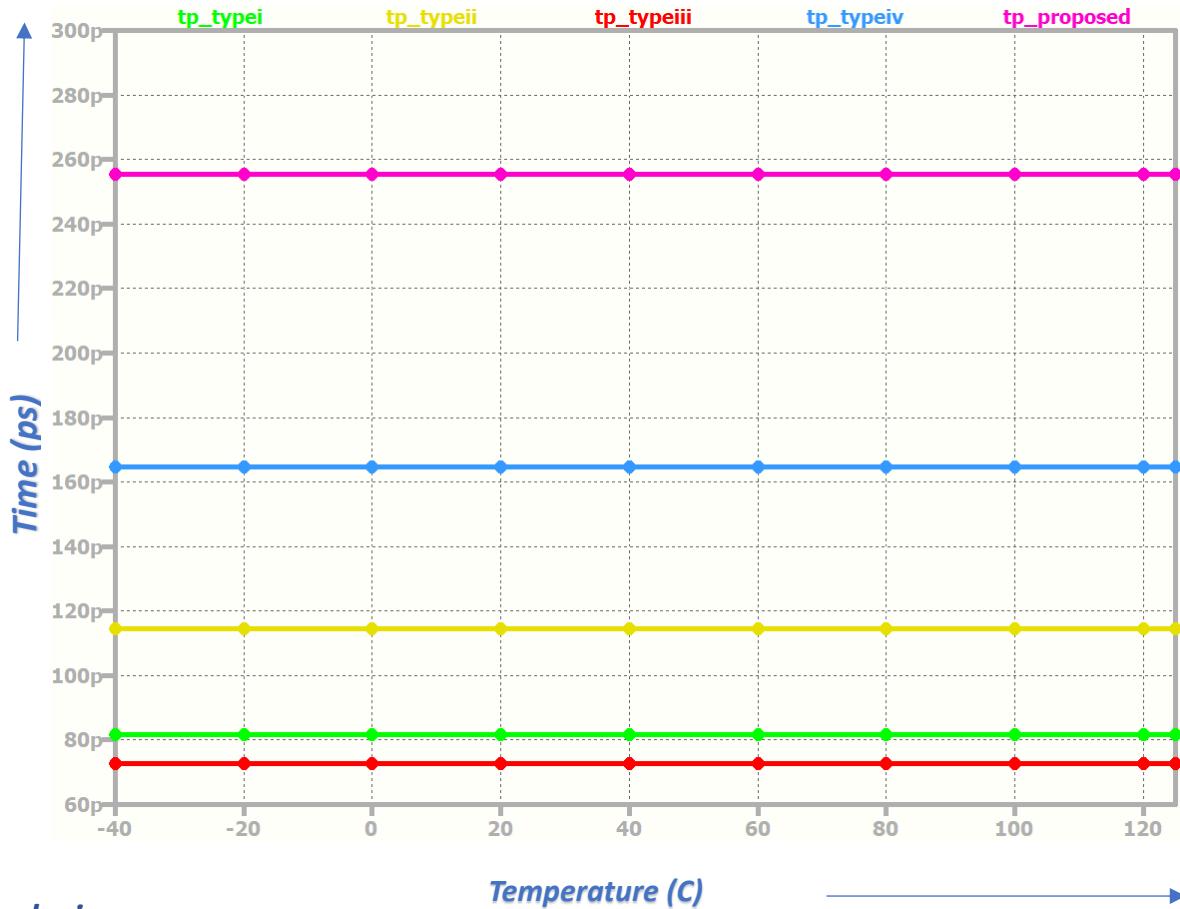
3.1 Charging time



3.2 Discharging time



3.3 Average Delay



Conclusion

1. Voltage Variations:

- 1.1 Traditional level shifters exhibit significant voltage fluctuations, leading to unreliable switching behavior.
- 1.2 The proposed design stabilizes voltage transitions, ensuring consistent operation even under supply variations.

2. Temperature Analysis:

- 2.1 Higher temperatures typically increase leakage currents and impact delay performance in standard level shifters.
- 2.2 The proposed level shifter demonstrates improved thermal stability, maintaining consistent performance across different temperature conditions.

3. Performance Comparison

3.1 For low-speed, simple designs:

Type I and Type II may suffice, but they are less efficient for power-sensitive applications.

3.2 For high-speed applications:

Type III and Type IV provide better performance but at the cost of higher power consumption.

3.3 For energy-efficient and high-speed circuits:

The proposed level shifter with enable control provides the best balance between speed, power efficiency, and robustness against voltage and temperature variations

4. Advantages of the Proposed Level Shifter

The proposed design incorporates an enable signal, offering several key improvements:

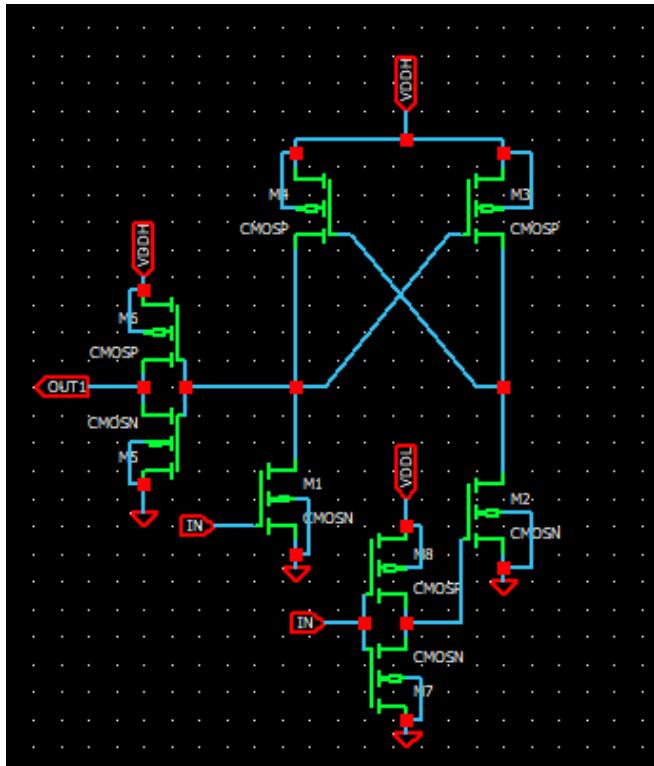
4.1 Dynamic Power Saving: The enable function allows the circuit to be active only when needed, minimizing static power dissipation.

4.2 Improved Voltage Shifting: Ensures better voltage regulation across different logic levels, minimizing fluctuations.

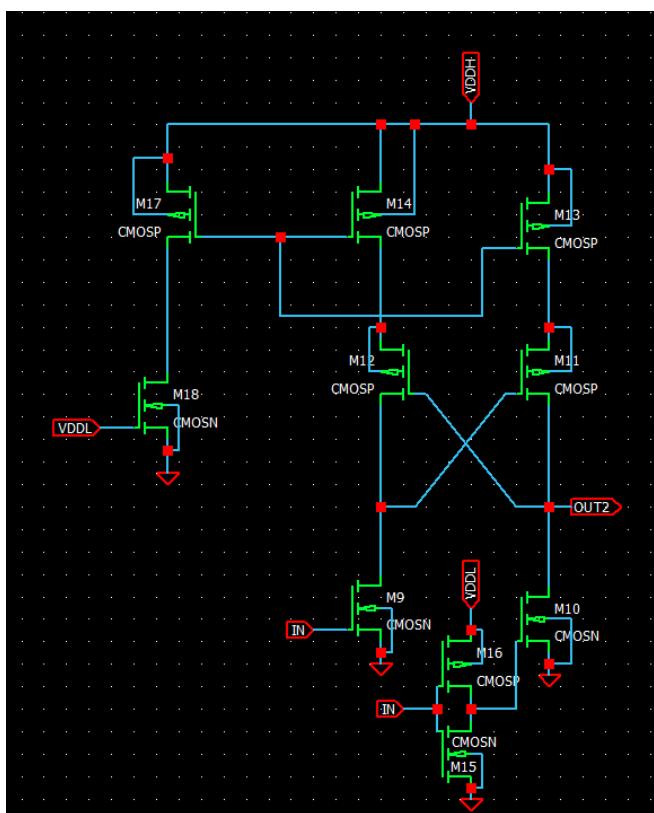
4.3 Reduced Propagation Delay: Enhances timing performance by enabling faster transitions between logic states.

An Energy-Efficient Level Shifter for Low-Power Applications

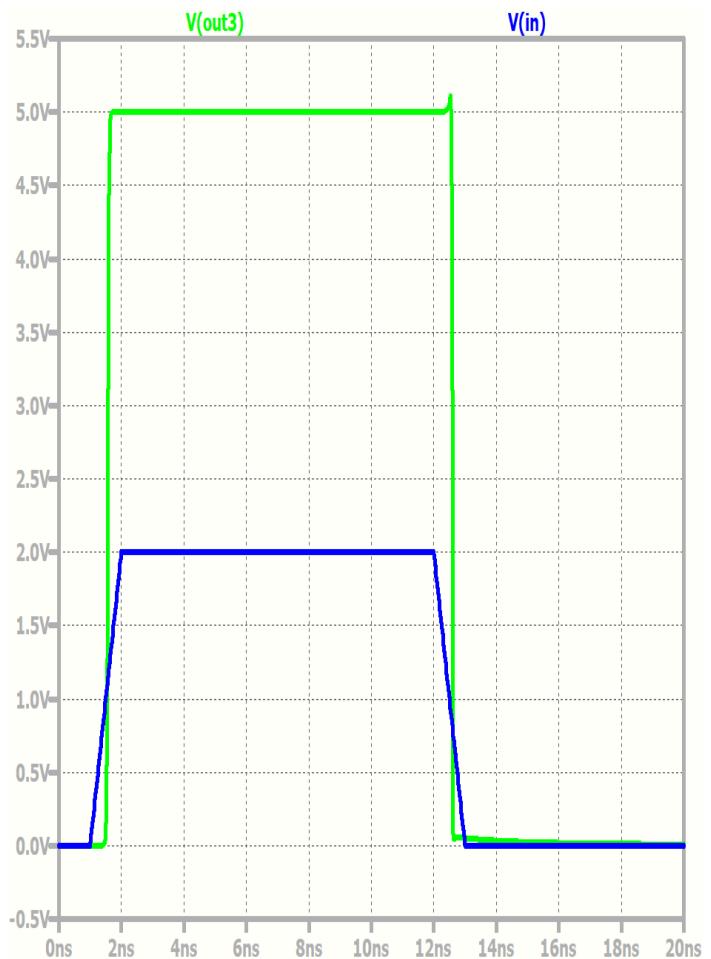
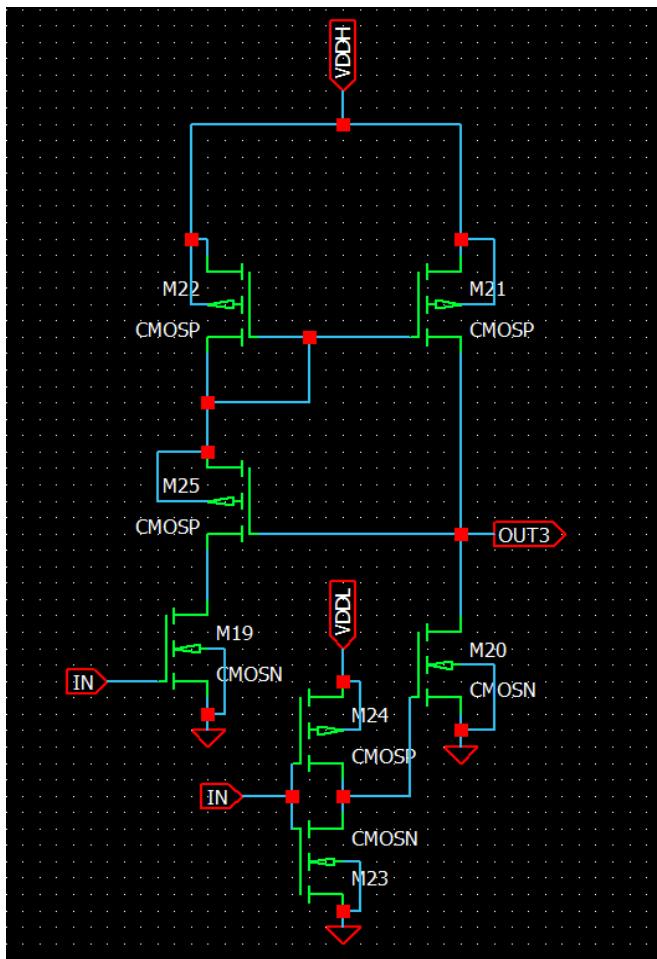
1. TYPE I



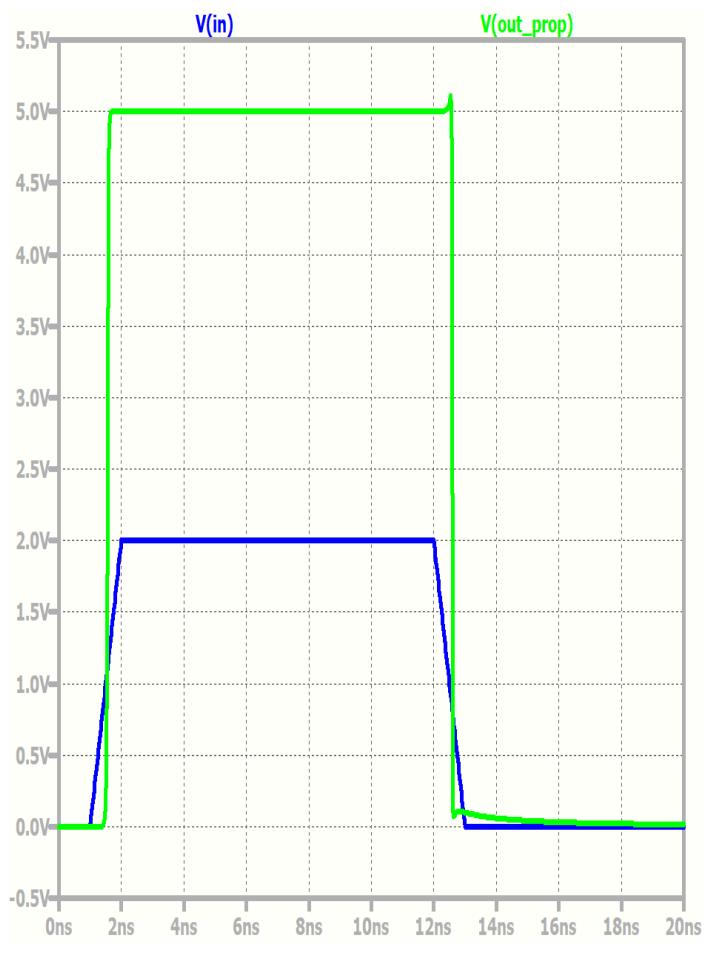
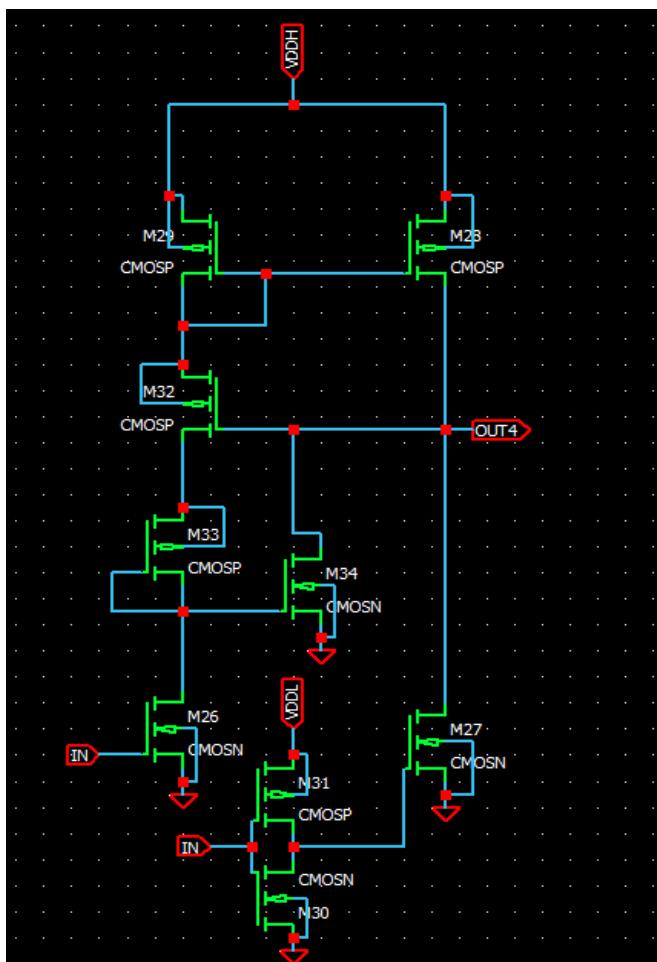
2. TYPE II



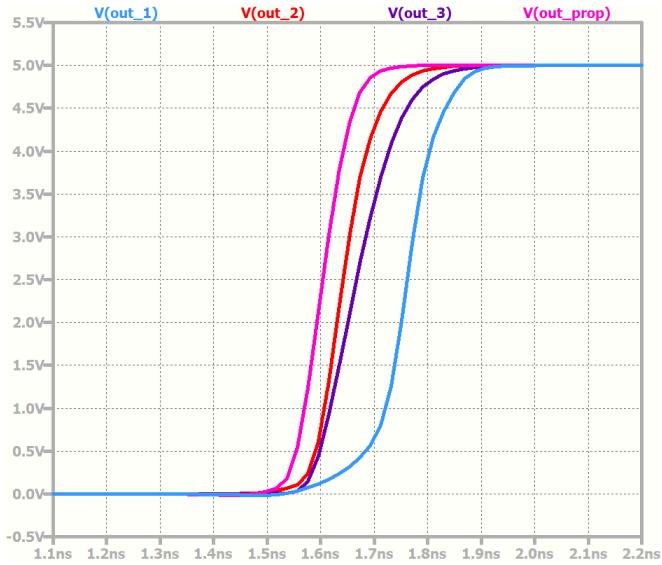
3. TYPE III



4. PROPOSED



1a. SLOW SLOW



DYNAMIC POWER DISSIPATION

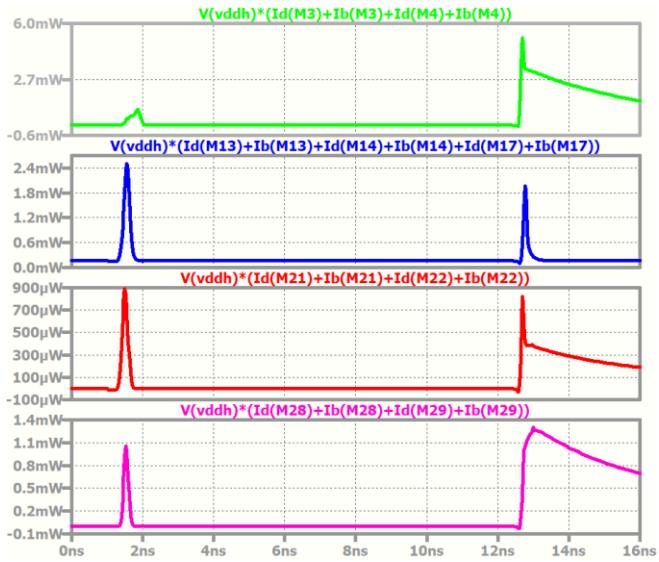


Table 2: Average Switching Delay for worst case

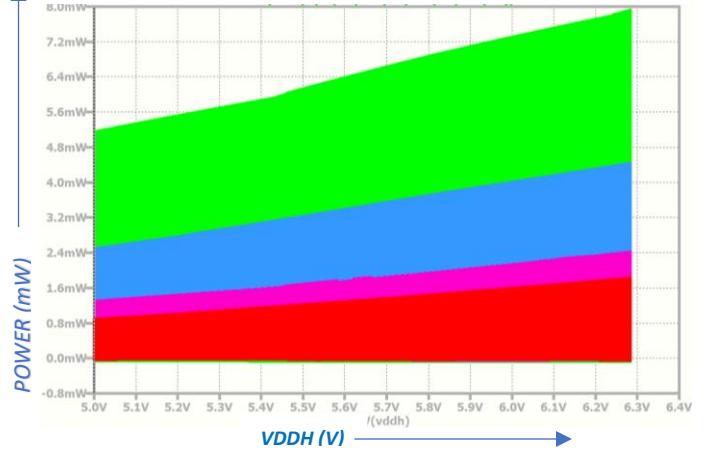
TYPE	CHARGING TIME	DISCHARGING TIME	AVERAGE DELAY
I	3.12031e-10	4.76398e-09	2.53801e-09
II	1.91455e-10	2.01507e-10	1.96481e-10
III	1.59168e-10	1.04663e-10	1.31916e-10
PROPOSED	1.53522e-10	1.43803e-10	1.48662e-10

Table 3: Power Dissipation in Worst case

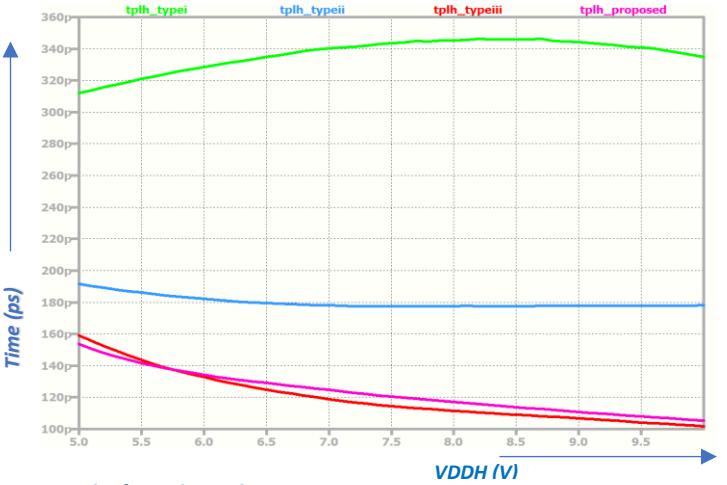
TYPE	STATIC POWER	DYNAMIC POWER	TOTAL POWER
I	1.9426nW	583.84μW	583.84μW
II	642.4pW	203.79μW	203.79μW
III	244.75nW	80.827μW	80.827μW
PROPOSED	631.56pW	254.13μW	254.13μW

VOLTAGE VARIATION

1. Average Power wrt VDDH



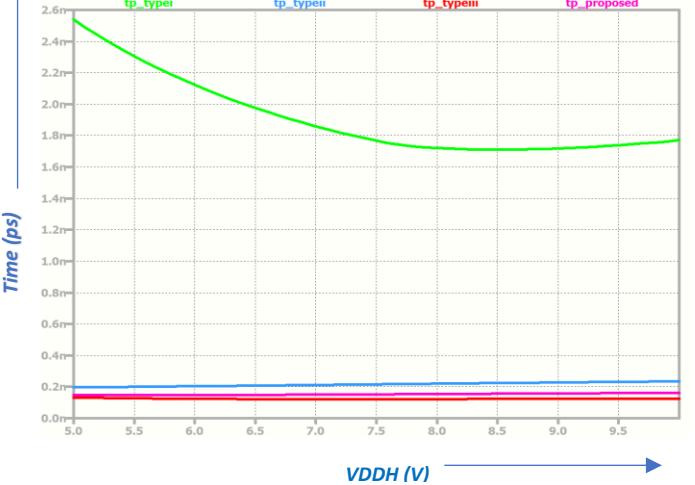
2. Charging type wrt. VDDH



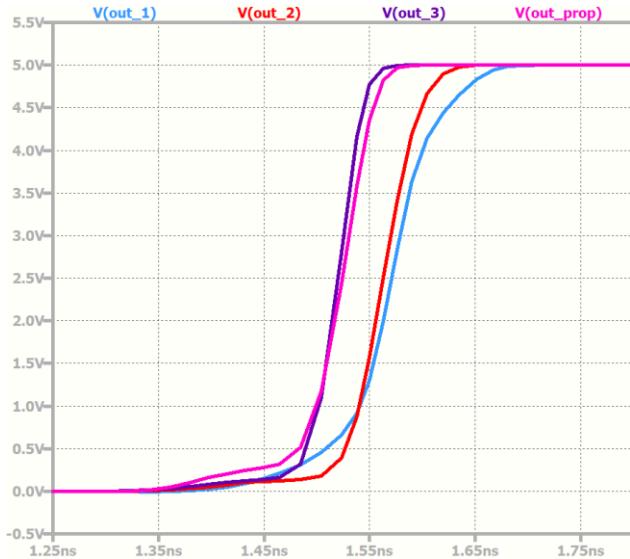
3. Discharging Time wrt. VDDH



4. Average Delay wrt. VDDH



1b. Fast fast



DYNAMIC POWER DISSIPATION

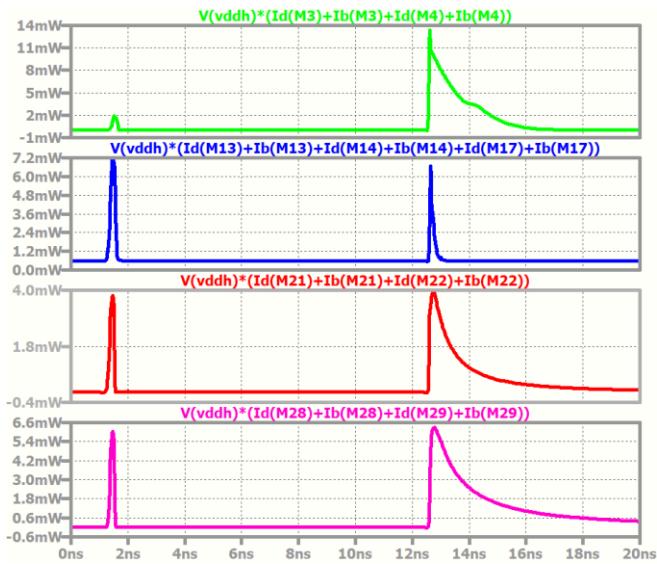


Table 4: Average Switching Delay for Best Case

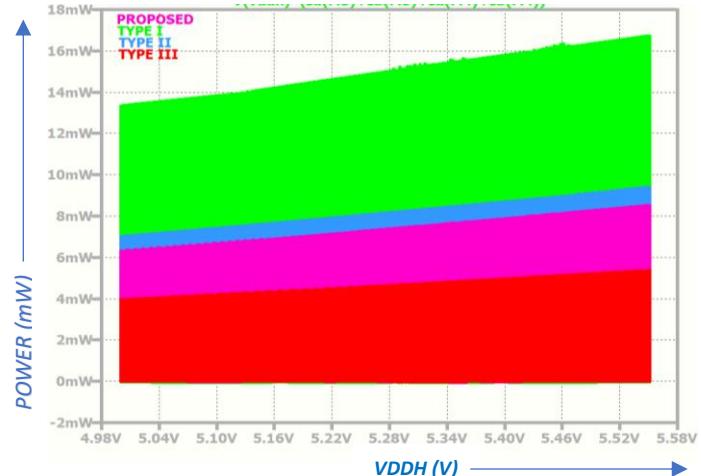
TYPE	CHARGING TIME	DISCHARGING TIME	AVERAGE DELAY
I	$1.20498e-10$	$1.49709e-09$	$8.08794e-10$
II	$1.12462e-10$	$7.84347e-11$	$9.54482e-11$
III	$7.00406e-11$	$2.74143e-11$	$4.87274e-11$
PROPOSED	$7.42926e-11$	$4.77541e-11$	$6.10233e-11$

Table 5: Power Dissipation in Best Case

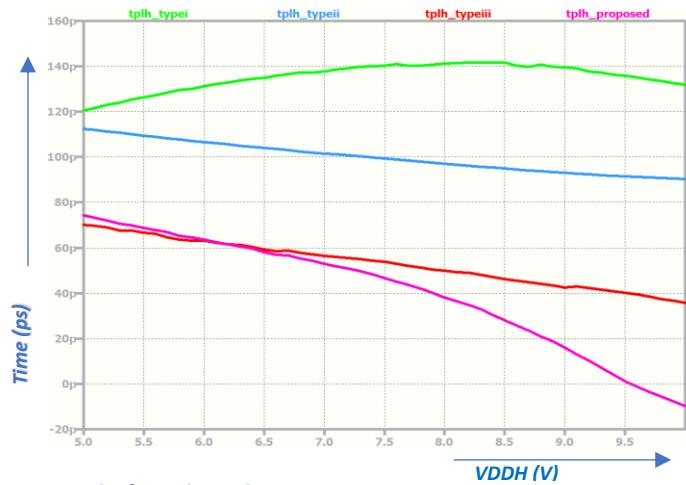
TYPE	STATIC POWER	DYNAMIC POWER	TOTAL POWER
I	$1.2798nW$	$732.79\mu W$	$732.79\mu W$
II	$850.38\mu W$	$627.8\mu W$	$627.8\mu W$
III	$333.98nW$	$267.12\mu W$	$267.12\mu W$
PROPOSED	$49.115nW$	$644.65\mu W$	$644.65\mu W$

VOLTAGE VARIATION

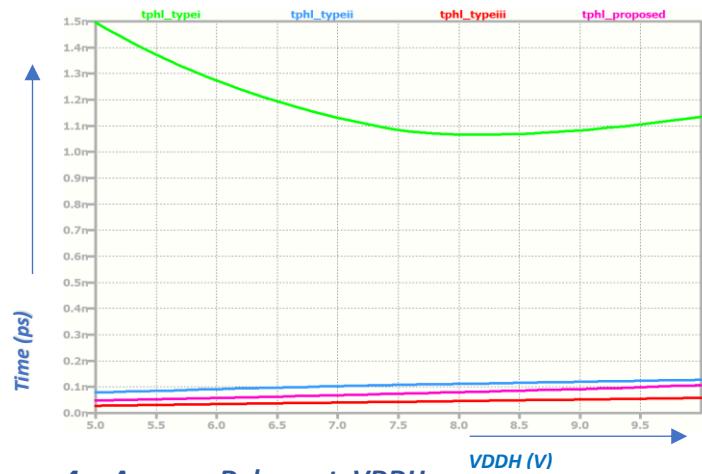
5. Average Power wrt VDDH



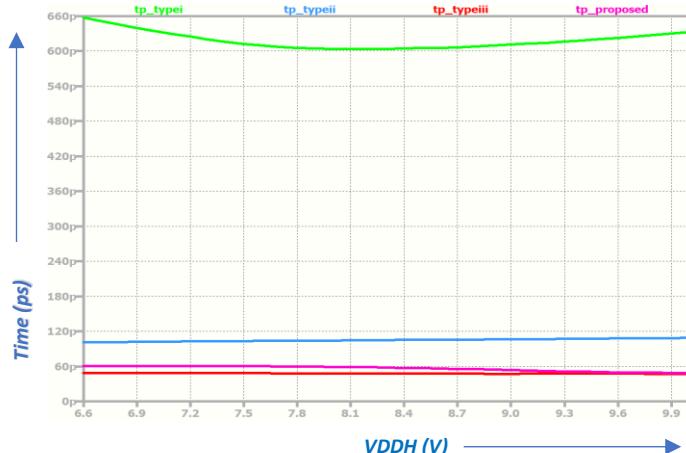
2. Charging Time wrt. VDDH



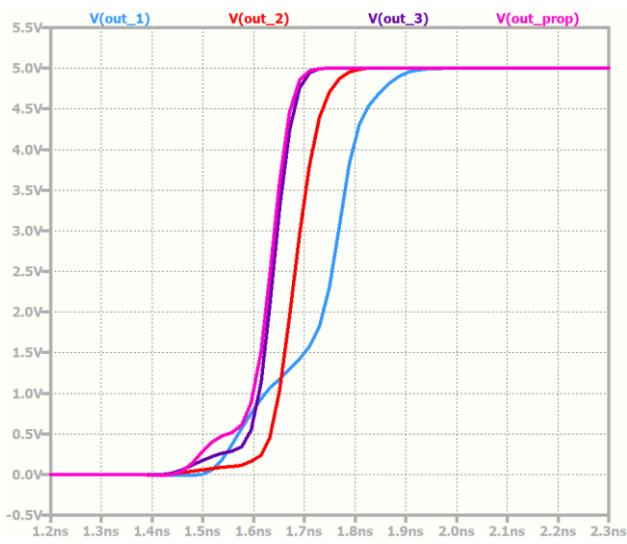
3. Discharging Time wrt. VDDH



4. Average Delay wrt. VDDH



1c. Slow fast



DYNAMIC POWER DISSIPATION

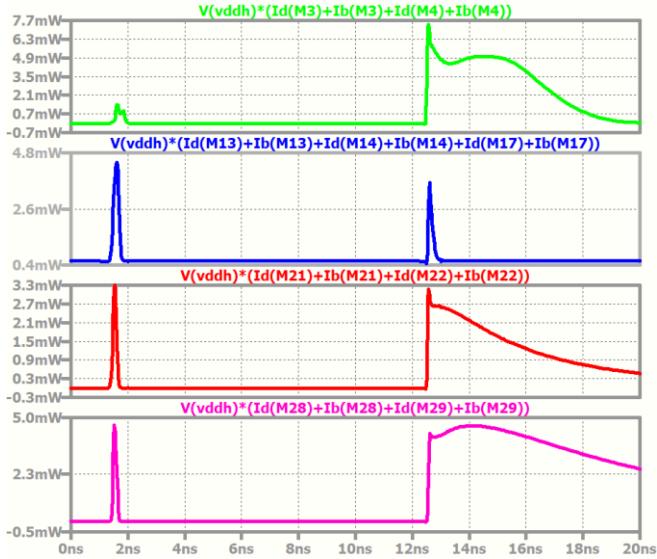


Table 6: Average Switching Delay for SF Corner

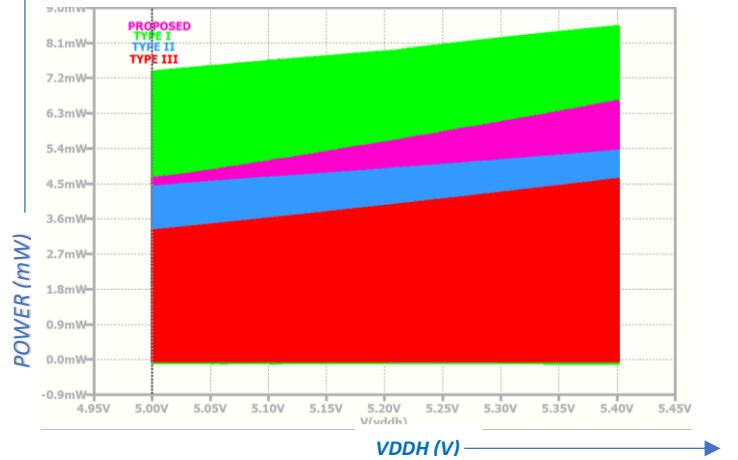
TYPE	CHARGING TIME	DISCHARGING TIME	AVERAGE DELAY
I	$3.04111e-10$	$2.39865e-09$	$1.35138e-09$
II	$2.31606e-10$	$4.33293e-11$	$1.37468e-10$
III	$1.88903e-10$	$2.74599e-11$	$8.07214e-11$
PROPOSED	$1.82848e-10$	$4.46177e-12$	$9.36551e-11$

Table 7: Power Dissipation in case SF Corner

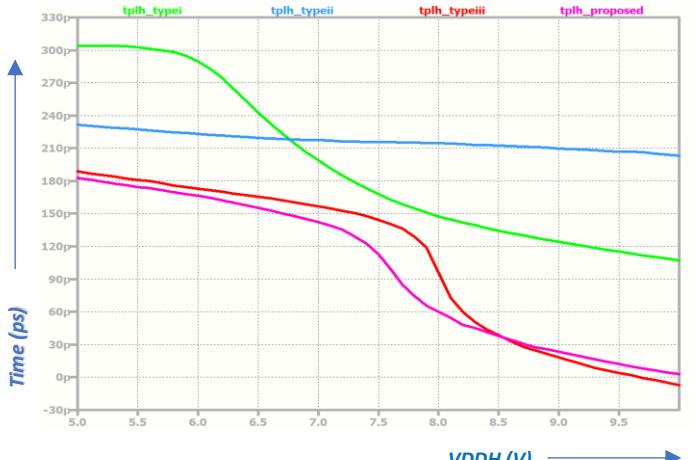
TYPE	STATIC POWER	DYNAMIC POWER	TOTAL POWER
I	$222.76pW$	$1.1168mW$	$1.1168mW$
II	$624.72\mu W$	$616.59\mu W$	$616.59\mu W$
III	$10.005nW$	$1.4388mW$	$1.4388mW$
PROPOSED	$2.1458nW$	$535.14\mu W$	$535.14\mu W$

VOLTAGE VARIATION

1. Average Power wrt VDDH



2. Charging Time wrt. VDDH



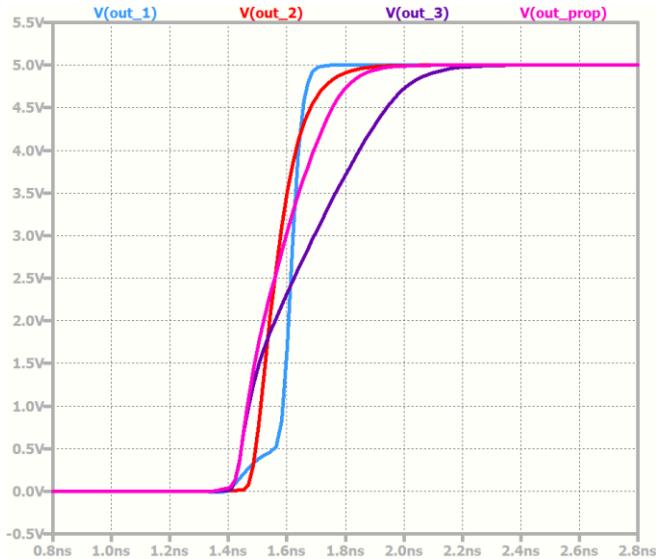
3. Discharging time wrt. VDDH



4. Average Delay wrt. VDDH



1d Fast slow



VOTAGE VARIATION



DYNAMIC POWER DISSIPATION

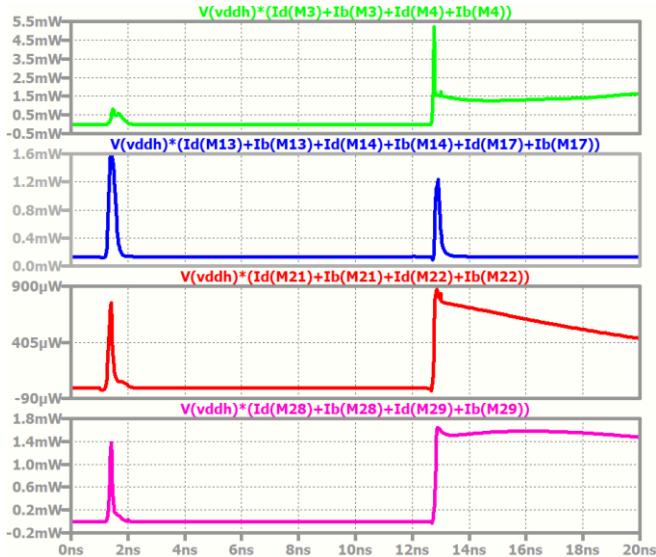


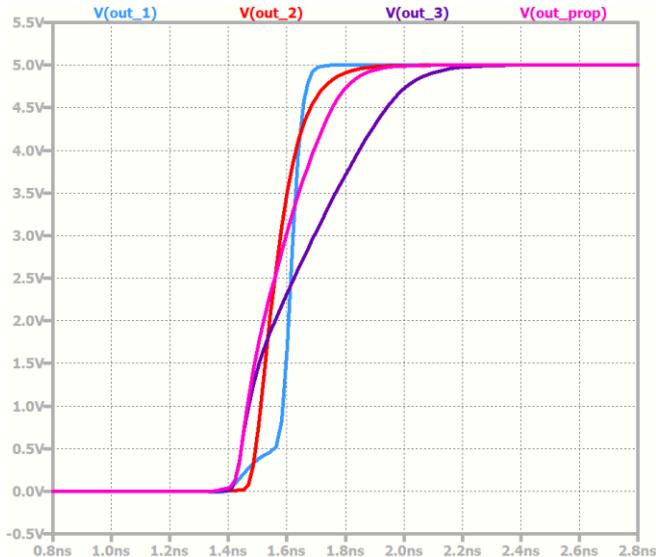
Table 8: Average Switching Delay for FS corner

TYPE	CHARGING TIME	DISCHARGING TIME	AVERAGE DELAY
I	1.6387e-10	4.45984e-09	2.31186e-09
II	1.0879e-10	2.98017e-10	1.75308e-10
III	1.75308e-10	2.02414e-10	1.88861e-10
PROPOSED	1.08045e-10	2.41156e-10	1.74601e-10

Table 9:Power Dissipation in FS Corner

TYPE	STATIC POWER	DYNAMIC POWER	TOTAL POWER
I	1.0145nW	530.66μW	530.66μW
II	157μW	163.98μW	163.98μW
III	538.71nW	565.82μW	565.82μW
PROPOSED	84.309nW	223.76μW	223.76μW

1e. TYPICAL TYPICAL



DYNAMIC POWER DISSIPATION

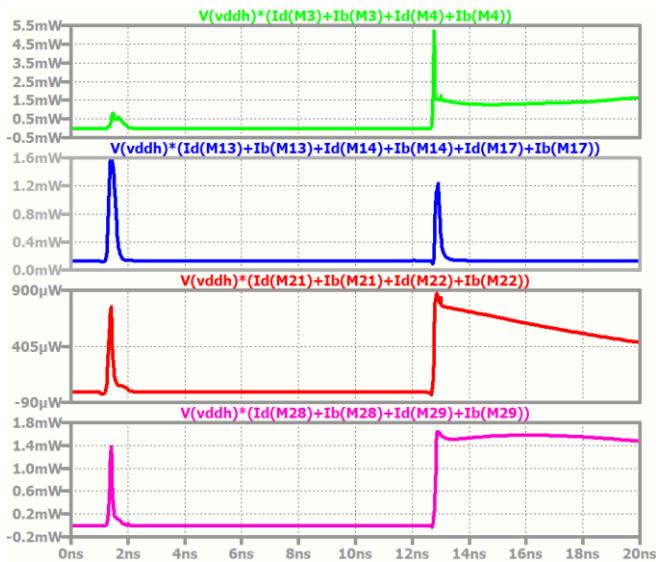


Table 19: Average Switching Delay for Normal Case

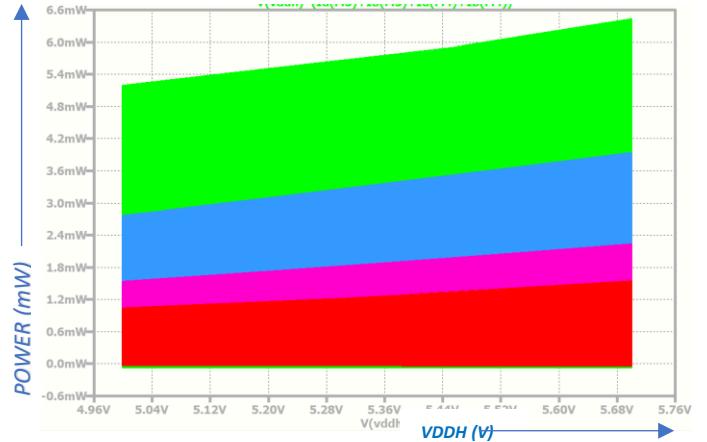
TYPE	CHARGING TIME	DISCHARGING TIME	AVERAGE DELAY
I	1.6387e-10	4.45984e-09	2.31186e-09
II	1.0879e-10	2.98017e-10	1.75308e-10
III	1.75308e-10	2.02414e-10	1.88861e-10
PROPOSED	1.08045e-10	2.41156e-10	1.74601e-10

Table 20: Power Dissipation in Normal Case

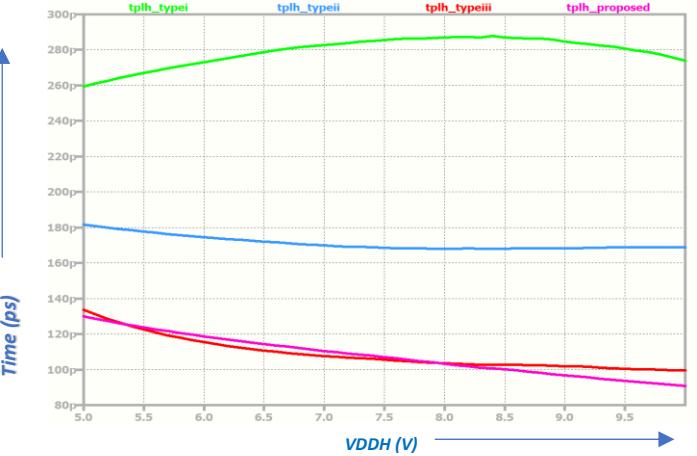
TYPE	STATIC POWER	DYNAMIC POWER	TOTAL POWER
I	1.0145nW	530.66μW	530.66μW
II	157μW	163.98μW	163.98μW
III	538.71nW	565.82μW	565.82μW
PROPOSED	84.309nW	223.76μW	223.76μW

VOLTAGE VARIATION

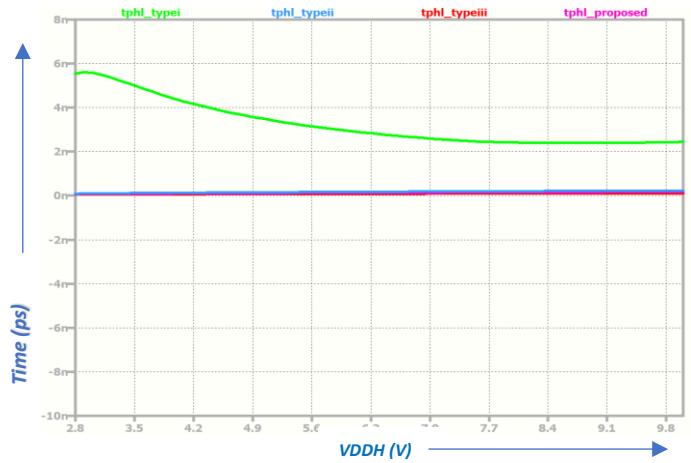
1. Average Power wrt VDDH



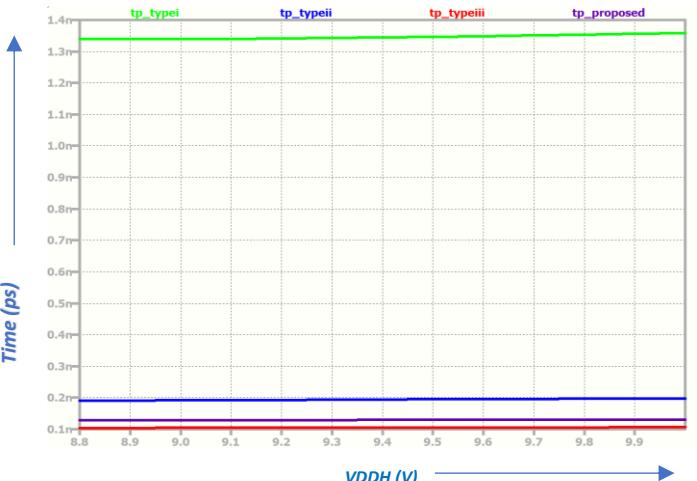
2. Charging time wrt VDDH



3. Discharging time wrt. VDDH

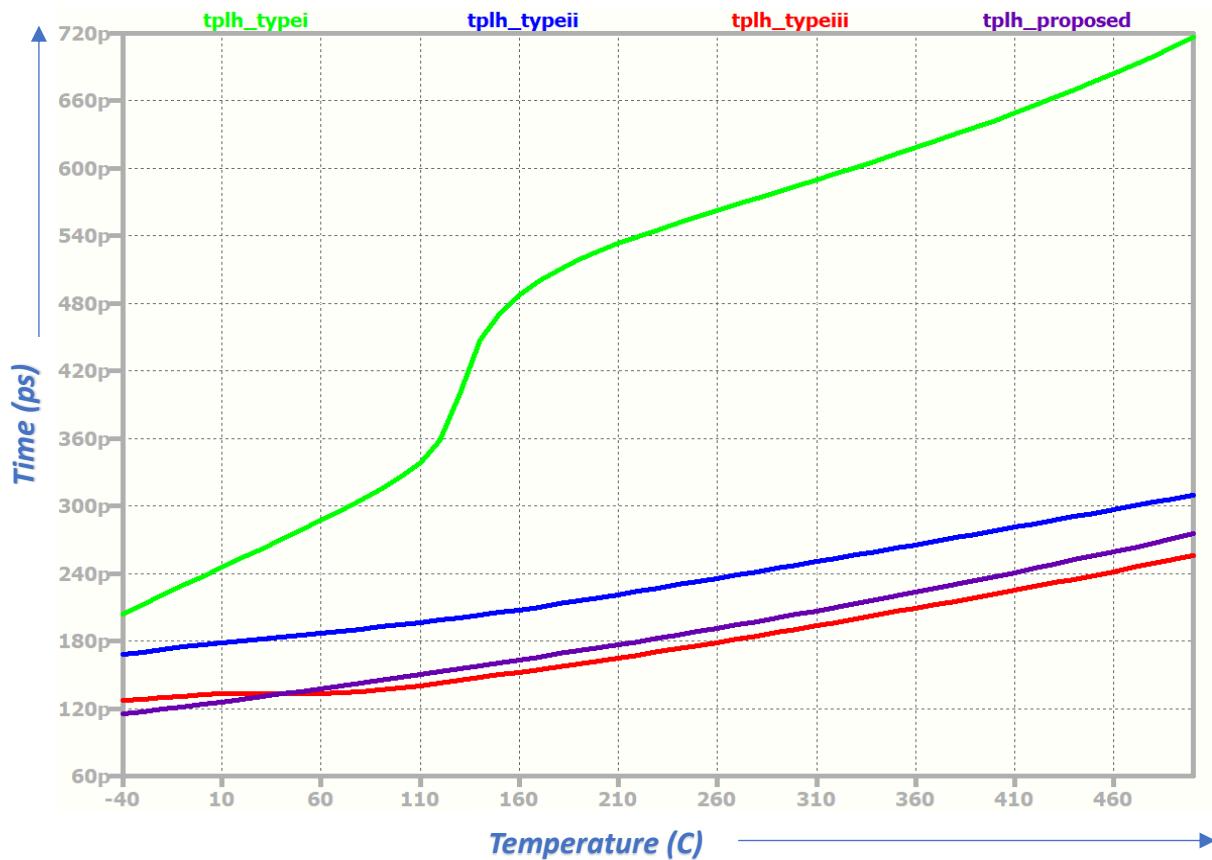


4. Average Delay wrt. VDDH

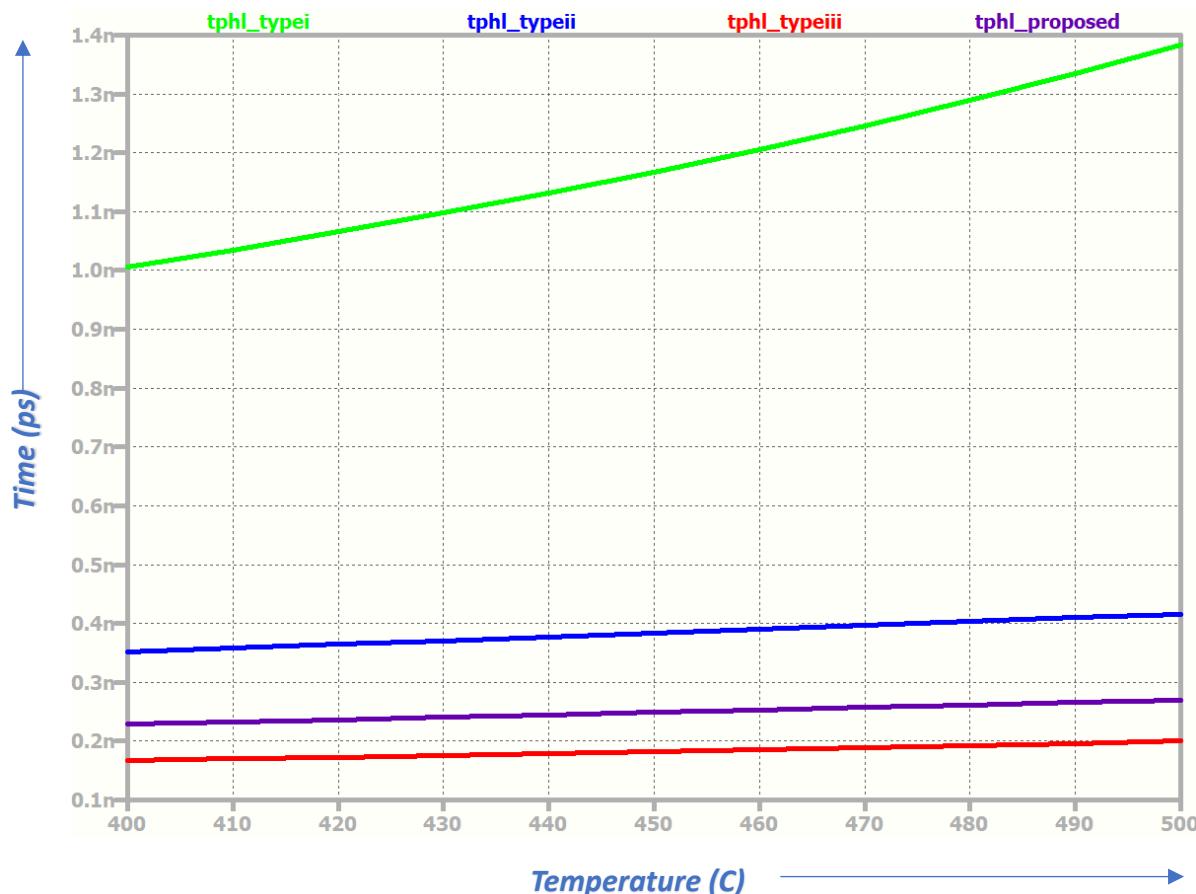


2. TEMPRATURE VARIATIONS

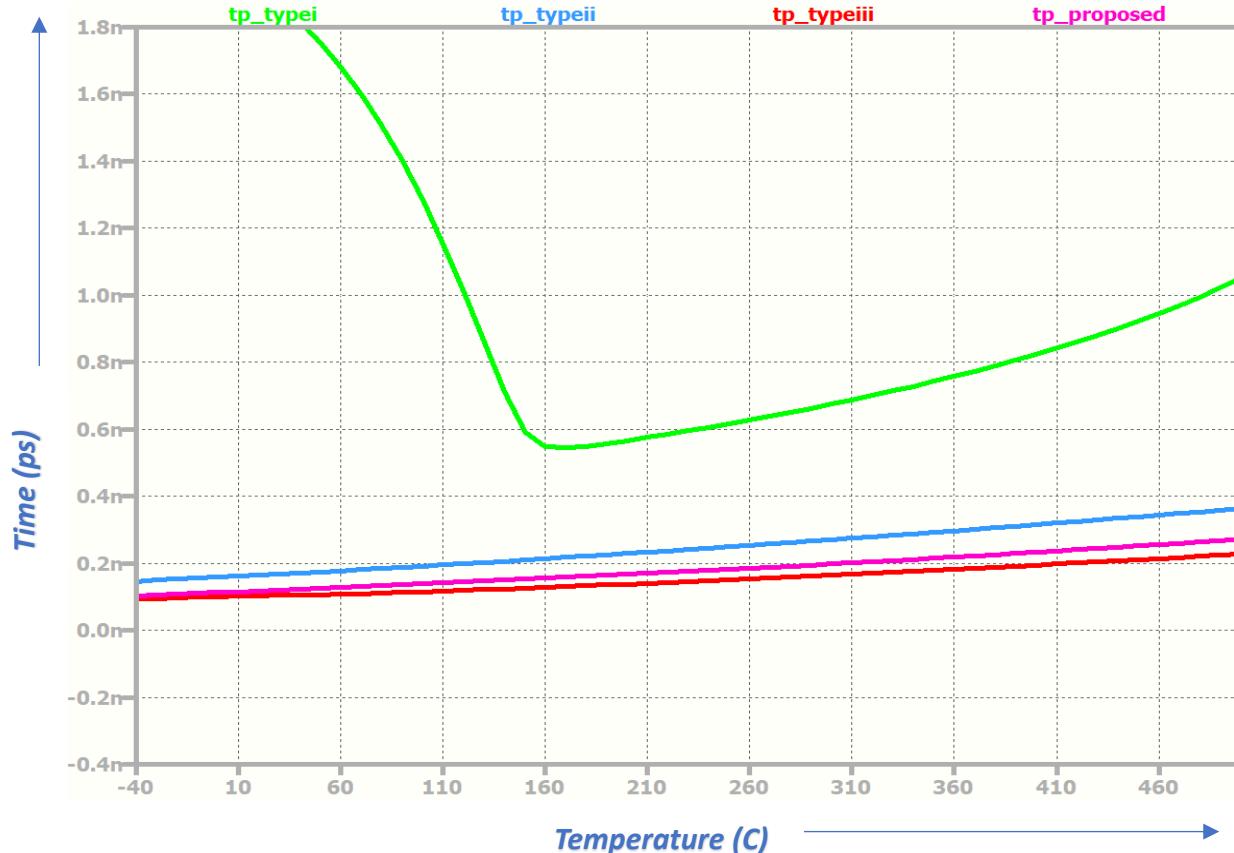
2.1 Charging time wrt temperature



2.2 Discharging time wrt. temperature



2.3 Average Delay wrt. temperature



Conclusion

1. Voltage Variations:

- 1.1 Conventional level shifters experience **significant variations in output voltage**, leading to potential switching errors.
- 1.2 The proposed design **minimizes voltage fluctuations**, ensuring reliable operation across different supply voltages.

2. Temperature Effects:

- 2.1 High temperatures **increase leakage current and delay**, negatively affecting standard level shifters.
- 2.2 The proposed level shifter **maintains stable performance**, making it ideal for high-temperature applications like automotive and industrial systems.

3. Performance Comparison

- 3.1 For low-speed, simple applications: Type I and Type II can be used, but they lack efficiency for modern low-power designs.
- 3.2 For high-speed applications: Type III and Type IV are preferable, but they consume more power.
- 3.3 For power-efficient, high-speed circuits: The proposed level shifter with enable control offers the best combination of speed, power efficiency, and robustness against voltage and temperature variations

4. Advantages of the Proposed Level

- 4.1 **Dynamic Power Management**: The enable signal activates the circuit only when needed, reducing static power consumption.
- 4.2 **Improved Voltage Transition**: Provides a stable and reliable voltage shift, minimizing glitches and ensuring better logic level conversion.
- 4.3 **Reduced Propagation Delay**: Enables faster signal transitions, improving overall circuit timing.