

EXPERIMENT -01

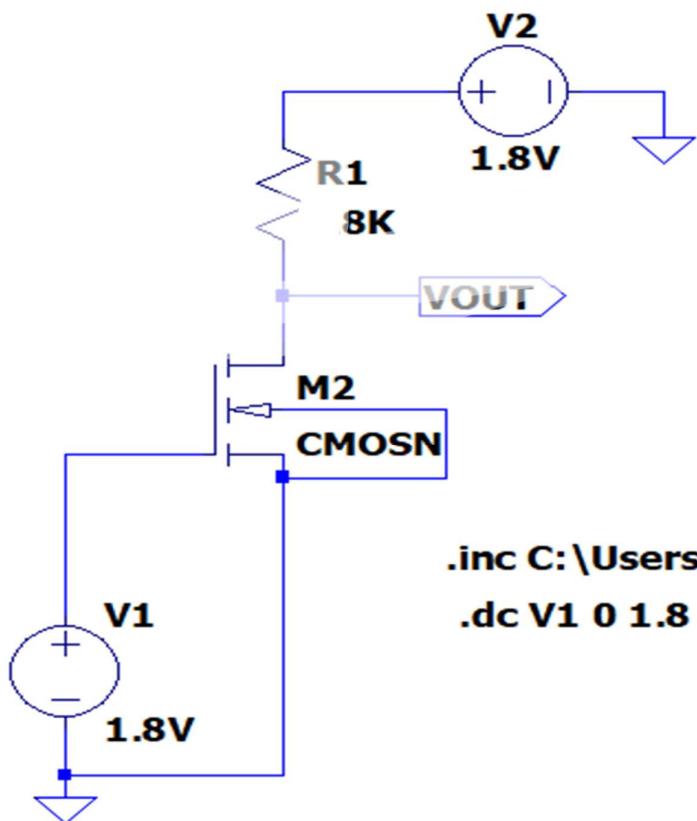
VLSI DESIGN - LAB (EEM 614)



NAME – SURAJ

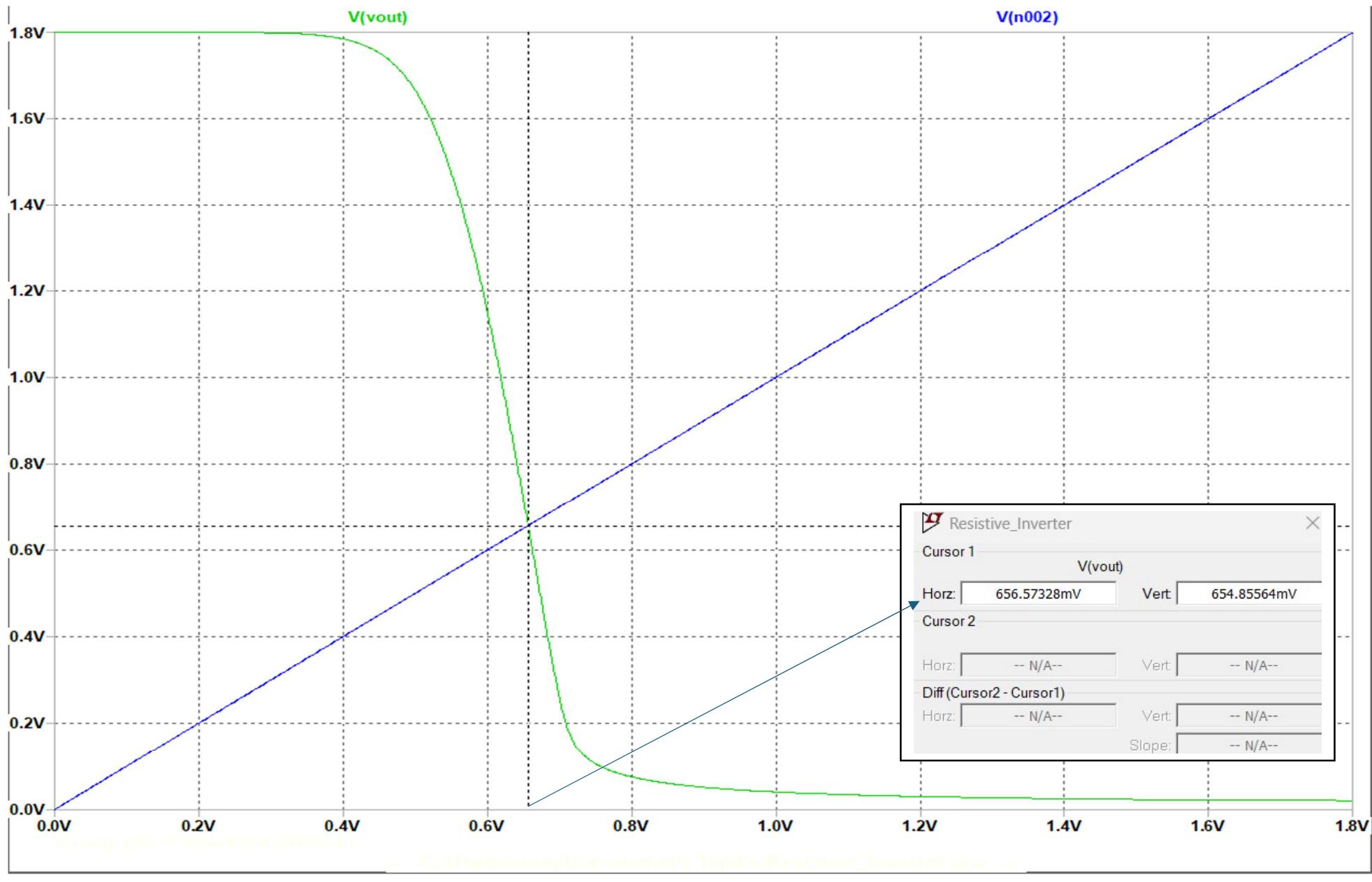
ROLL NO. -2201769

RESISTIVE LOAD INVERTER (tsmc180nm)

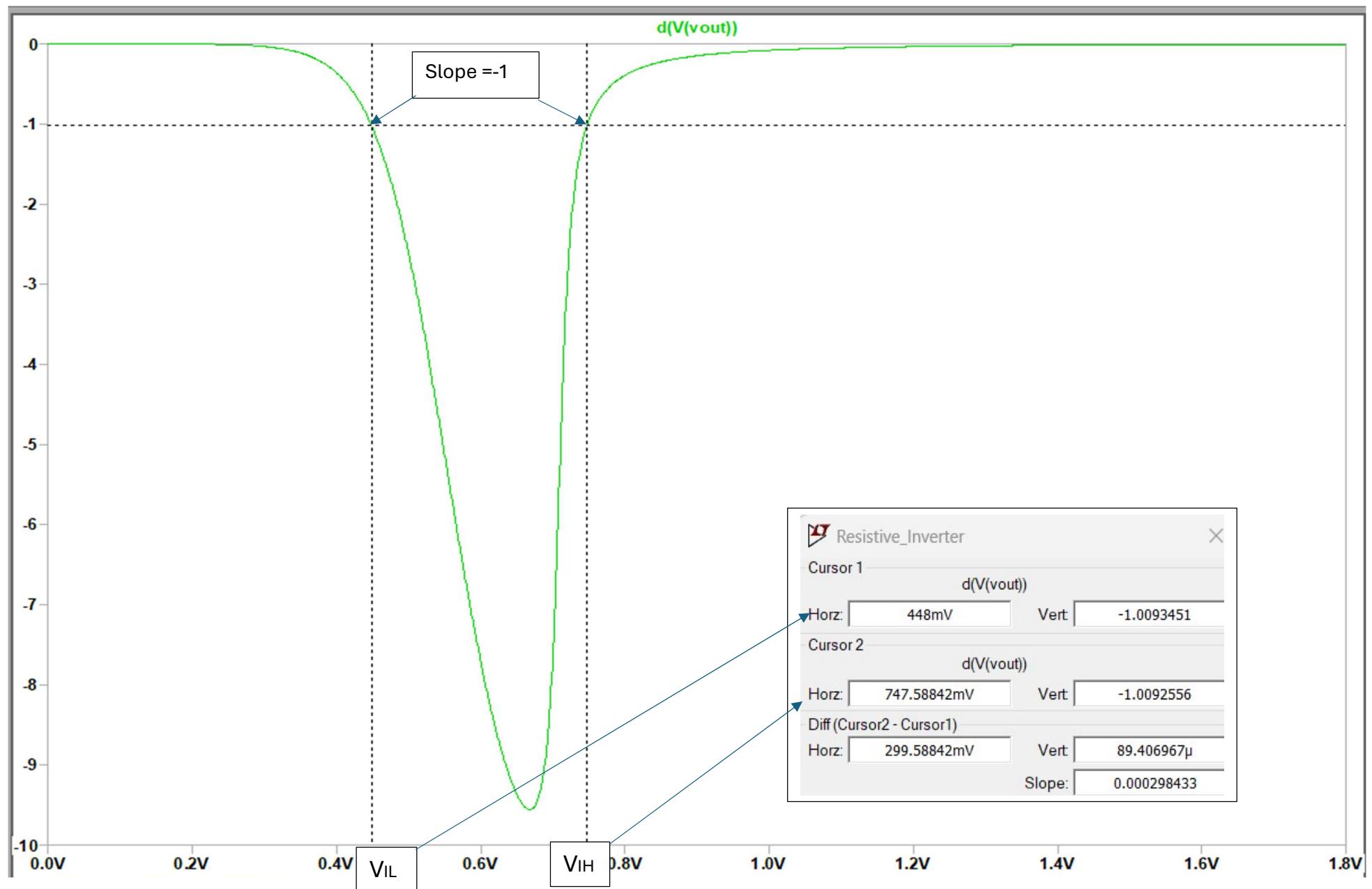


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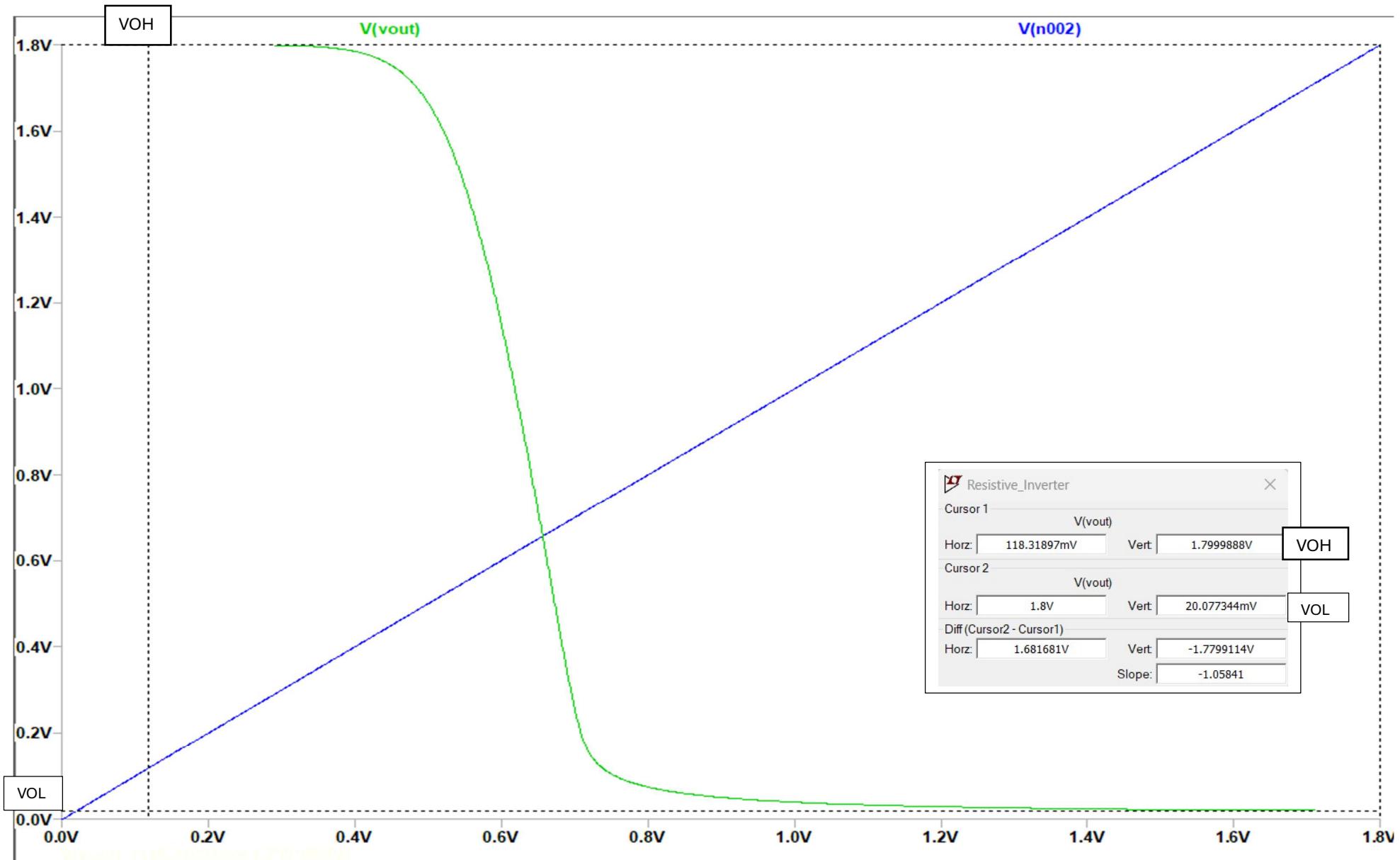
1a.VTC CHARACTERISTICS OF RESISTIVE INVERTER (tsmc180nm)



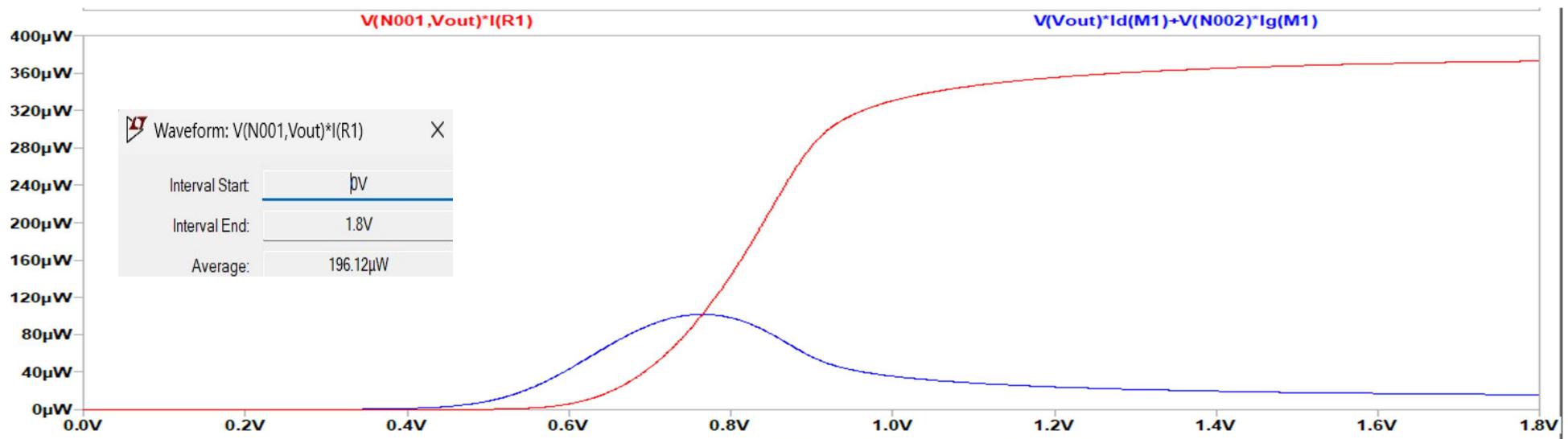
1b. Finding V_{IL} and V_{IH} from differentiation of VTC curve (tsmc180nm) :



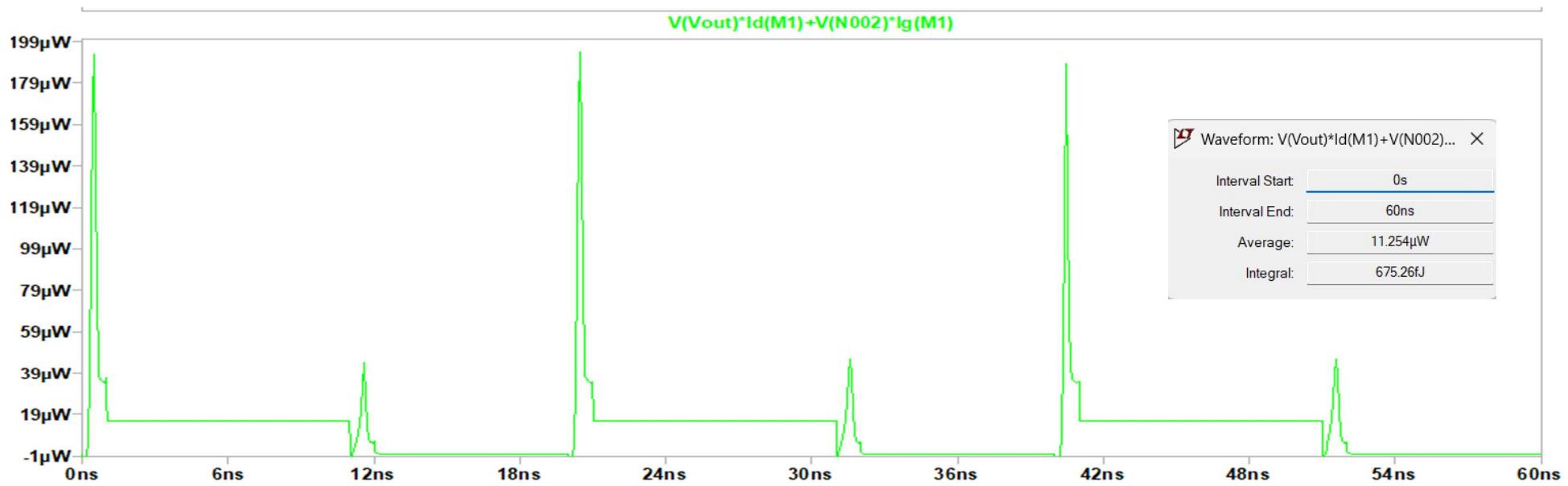
1c Finding V_{OL} and V_{OH} from VTC curve (tsmc180nm):



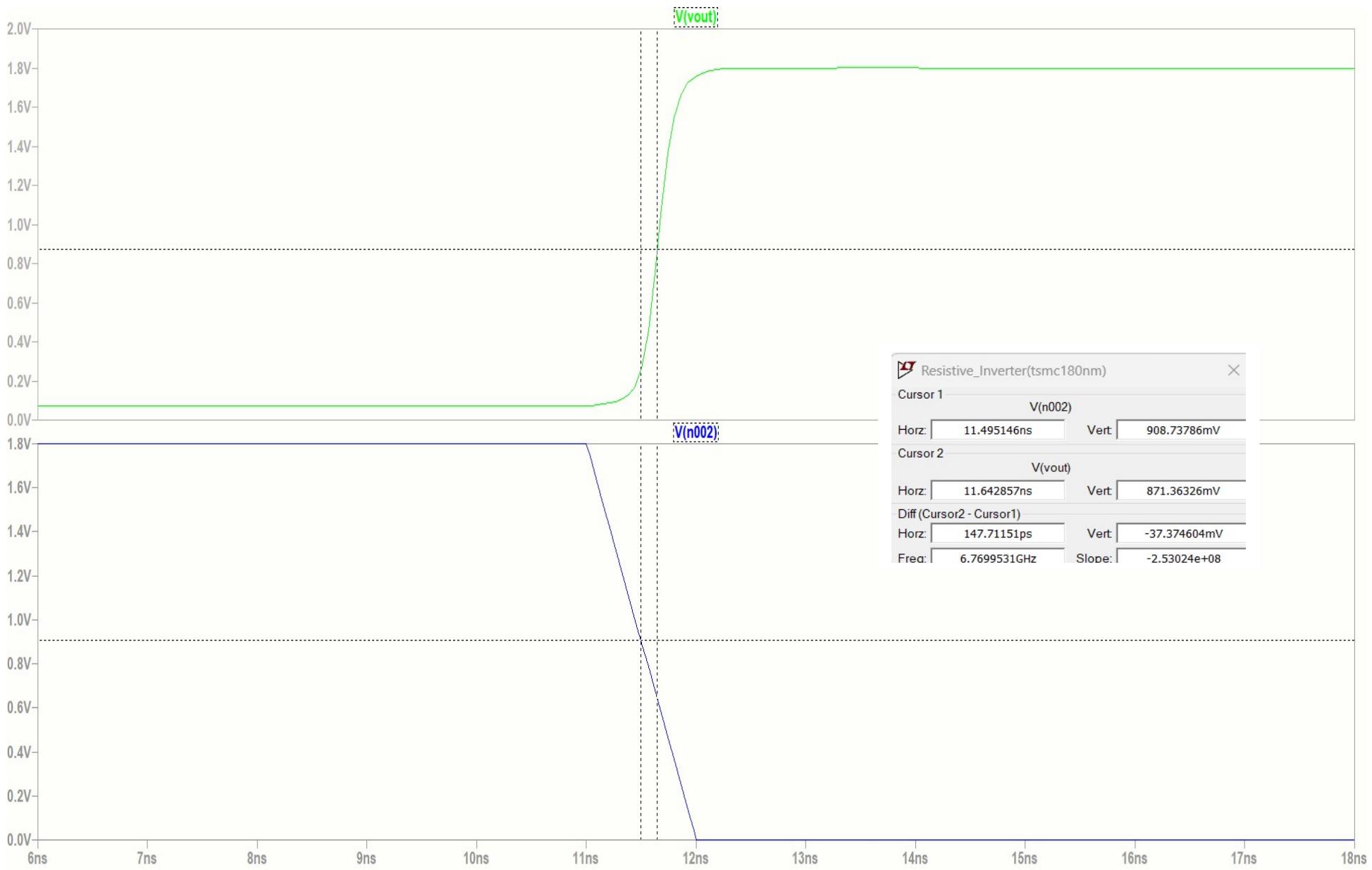
1d. Static Power in Resistive Load Inverter (tsmc180nm)



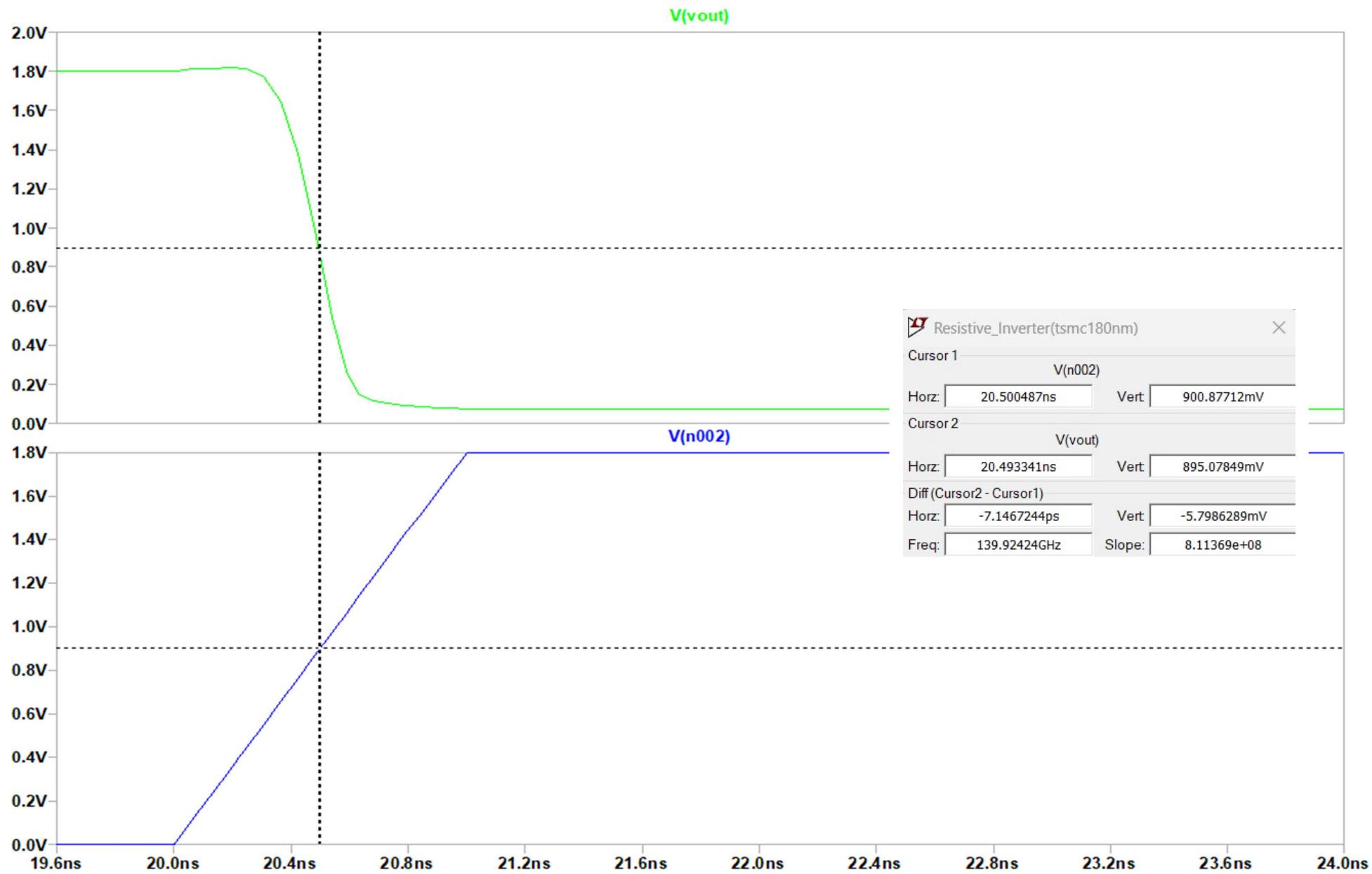
1e. Dynamic Power in Resistive load Inverter (tsmc180nm):



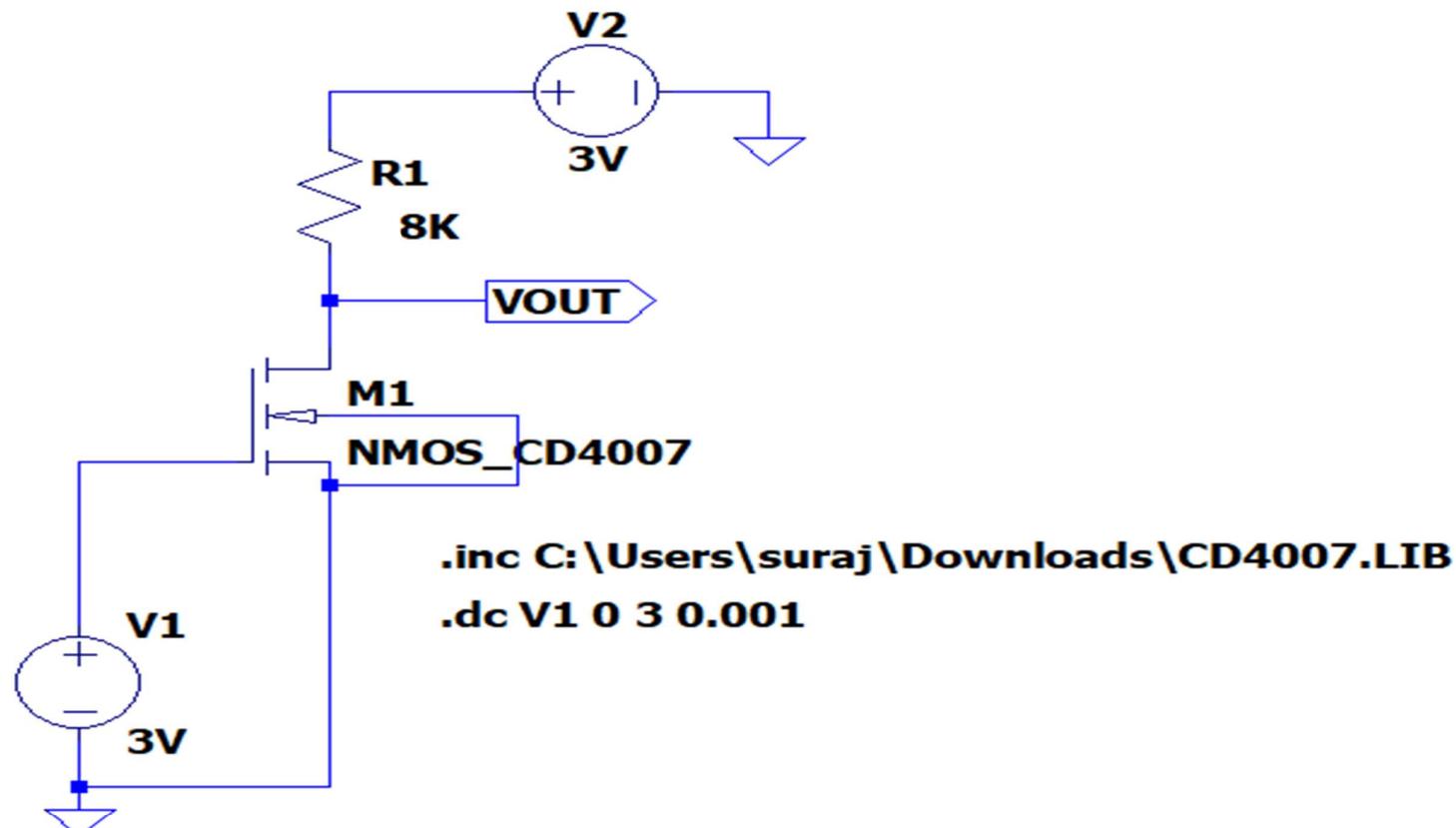
1e. Low to High Delay in Resistive load Inverter (tsmc180nm):



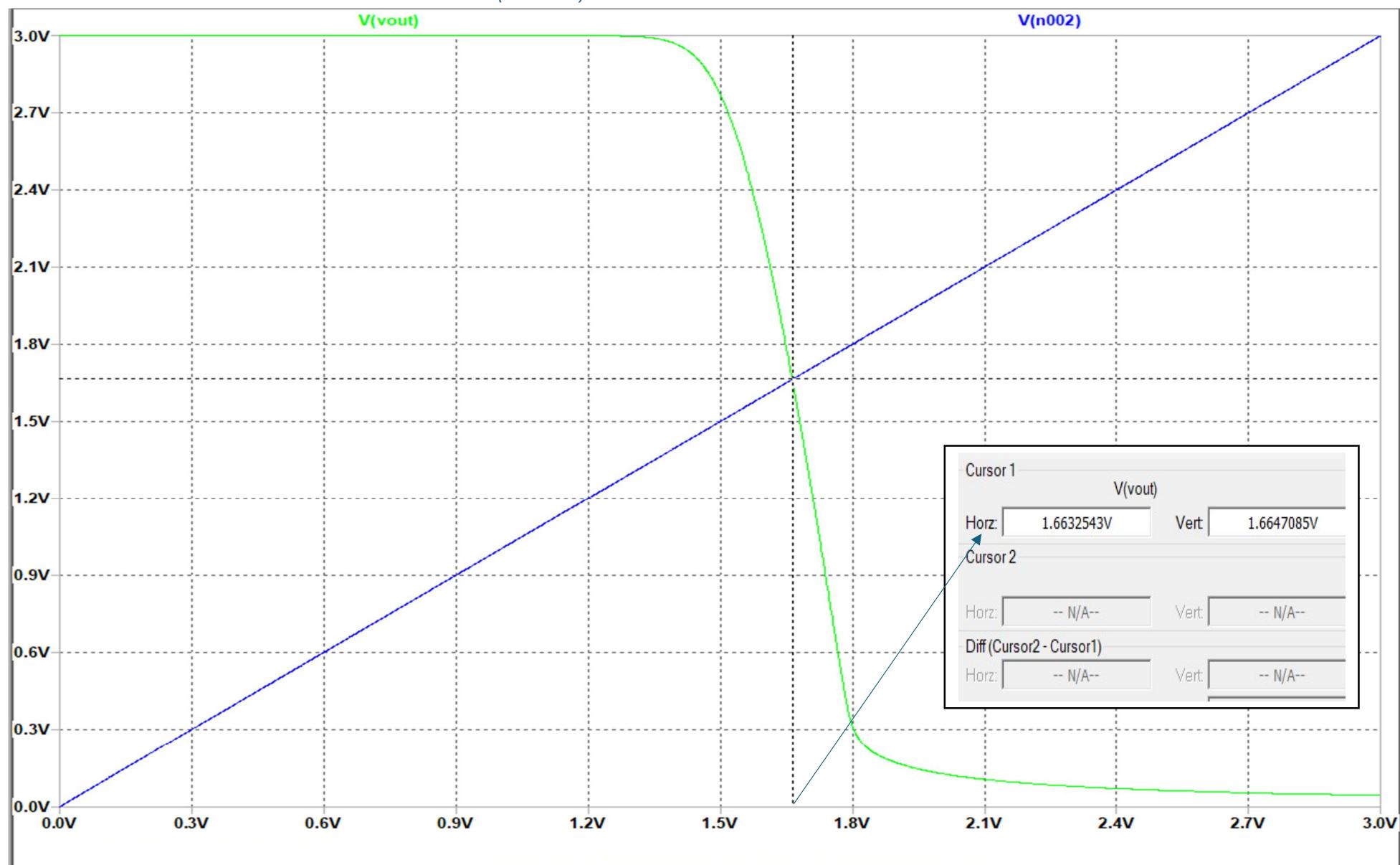
1f. High to Low Delay in Resistive load Inverter (tsmc180nm):



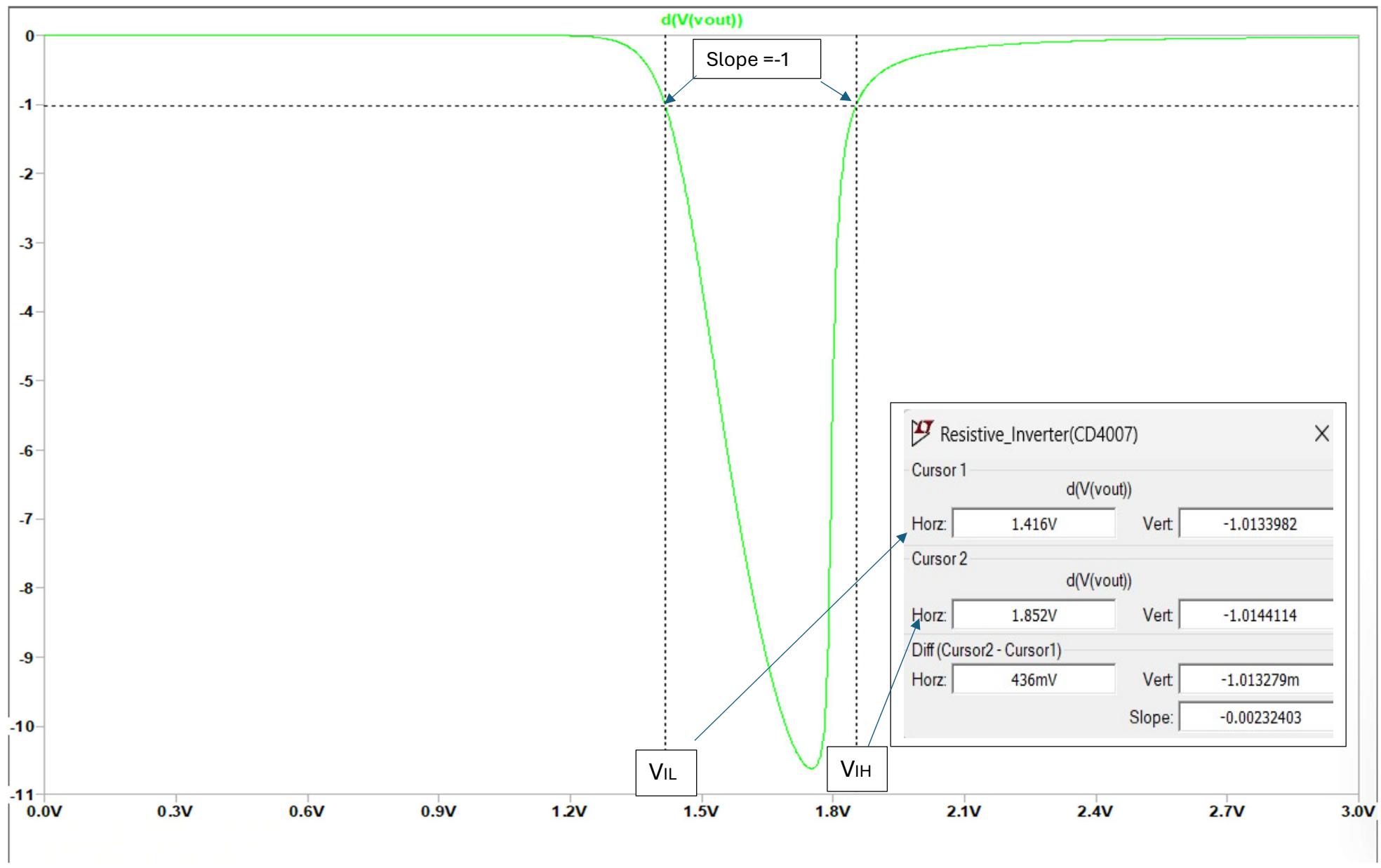
2. RESISTIVE LOAD INVERTER (CD4007)



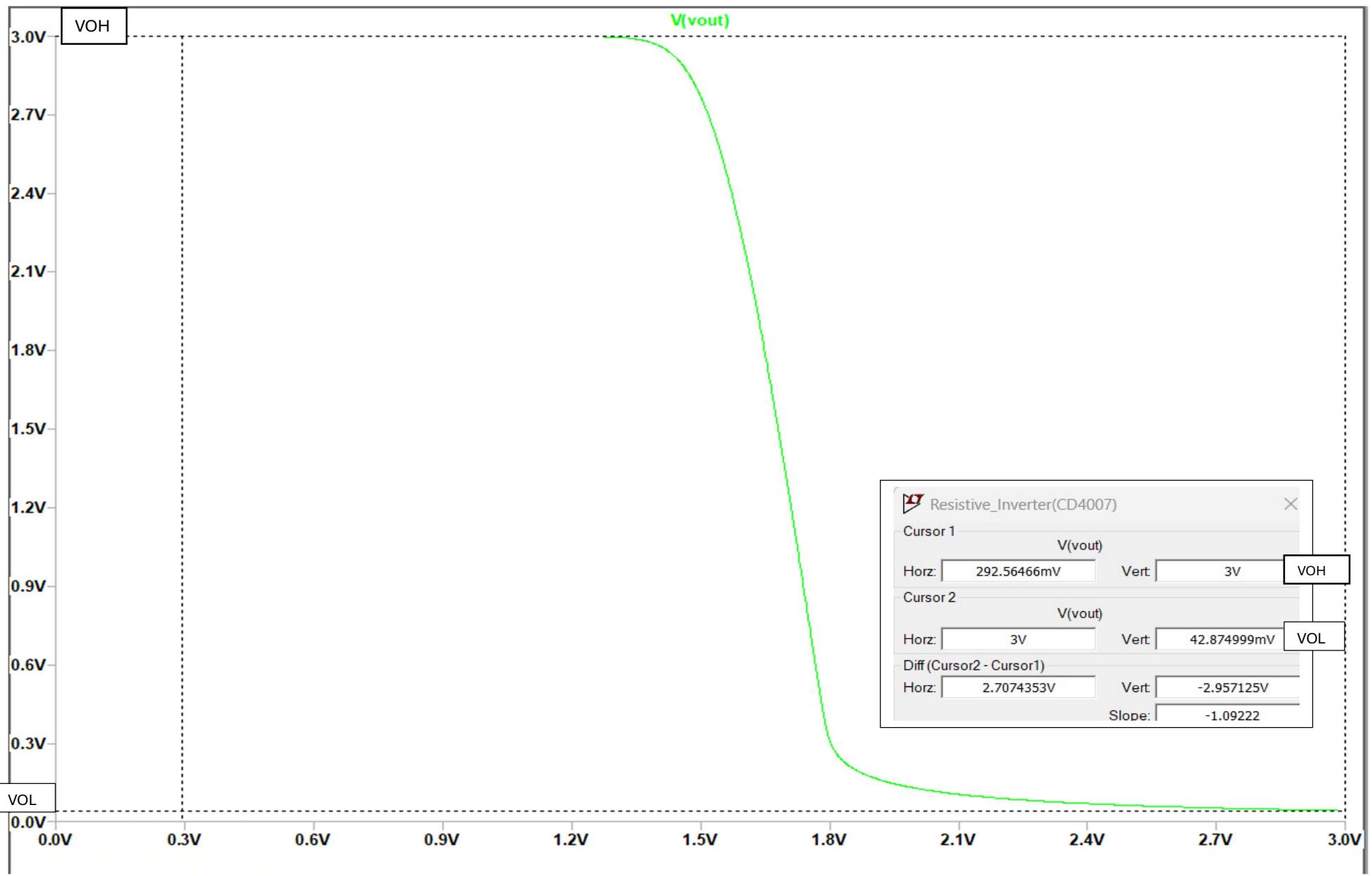
2a. VTC CHARACTERISTICS OF RESISTIVE INVERTER (CD4007)



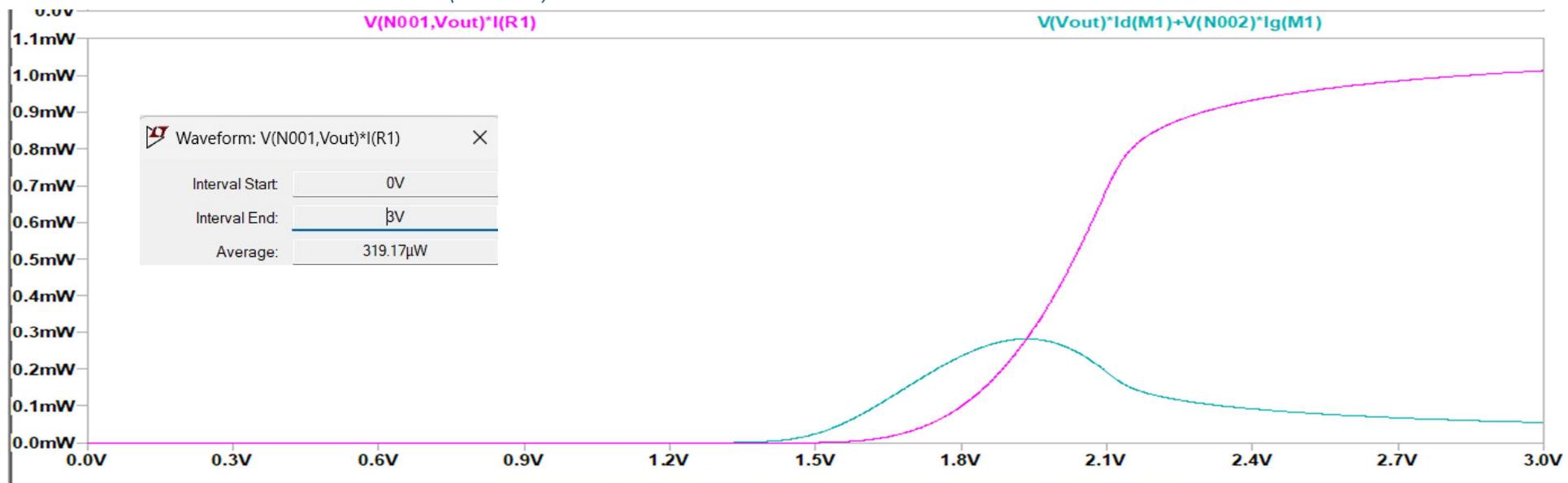
2b. Finding V_{IL} and V_{IH} from differentiation of VTC curve (CD4007)



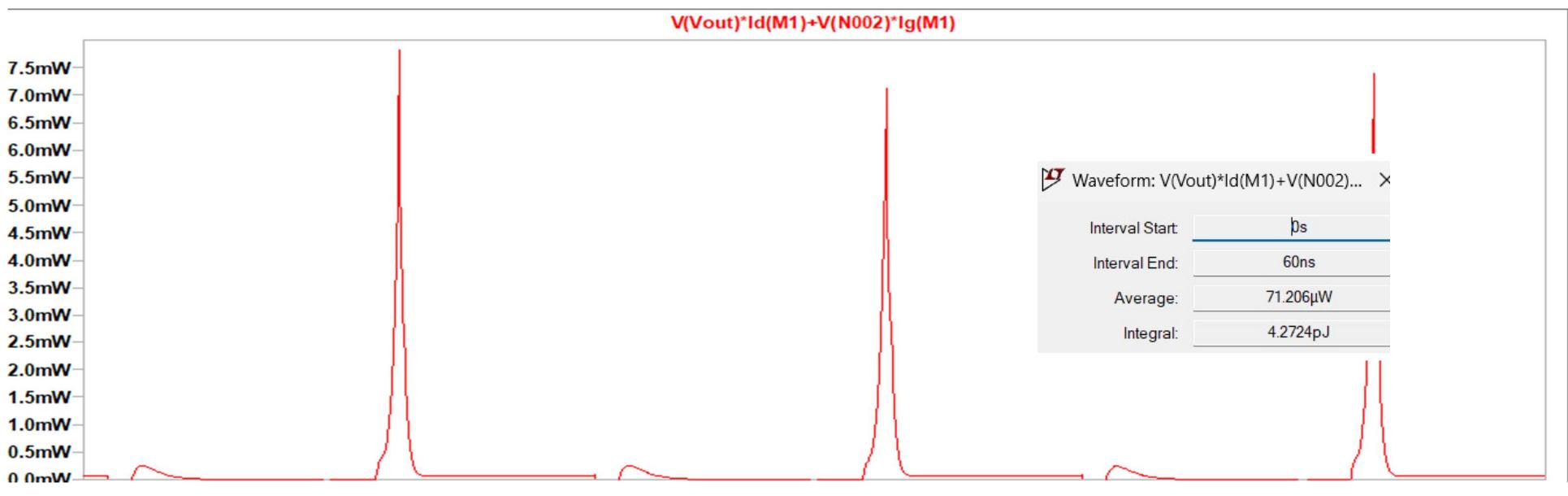
2c. Finding V_{OL} and V_{OH} from VTC curve (CD4007):



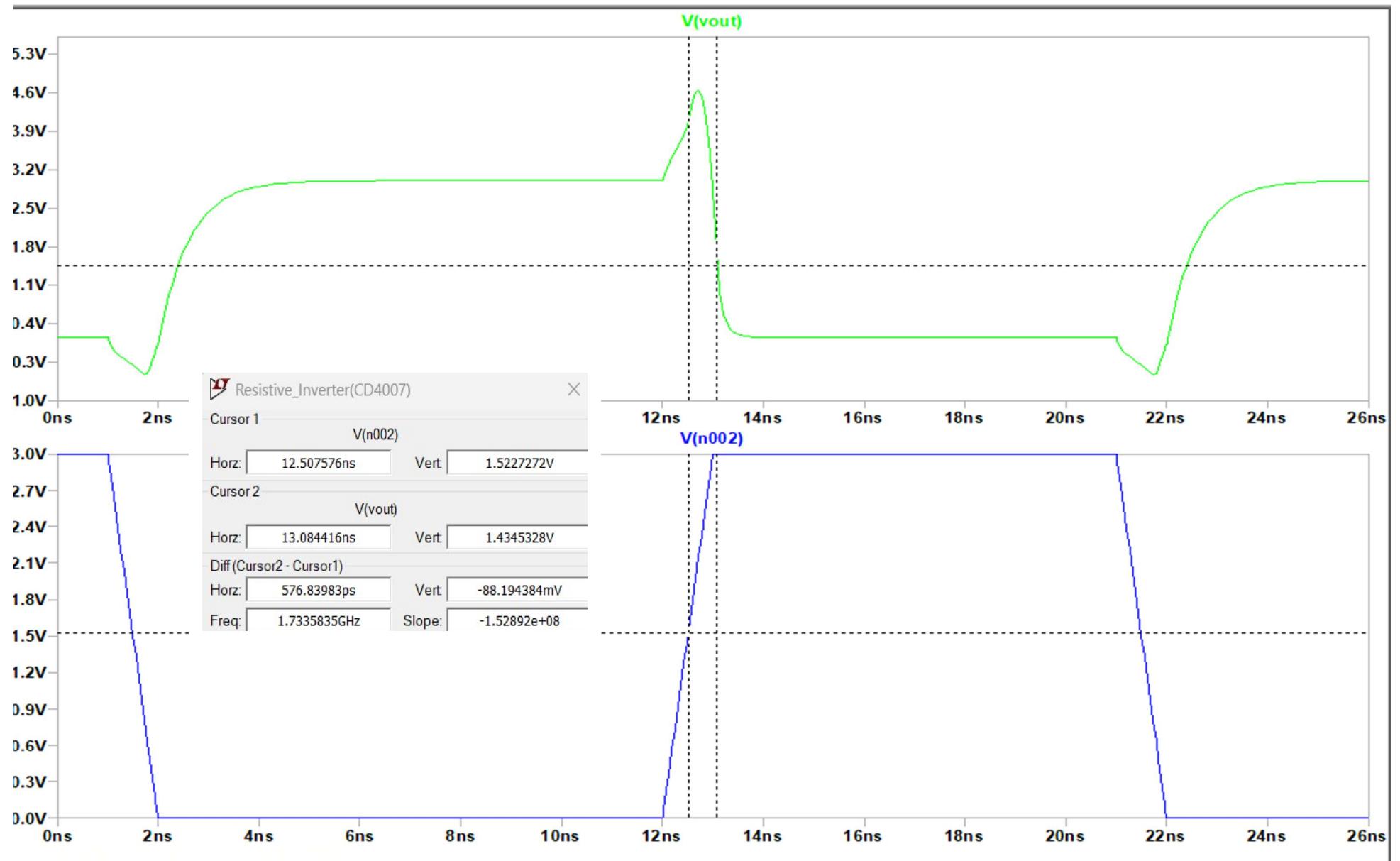
1d. Static Power in Resistive Load Inverter (CD4007):



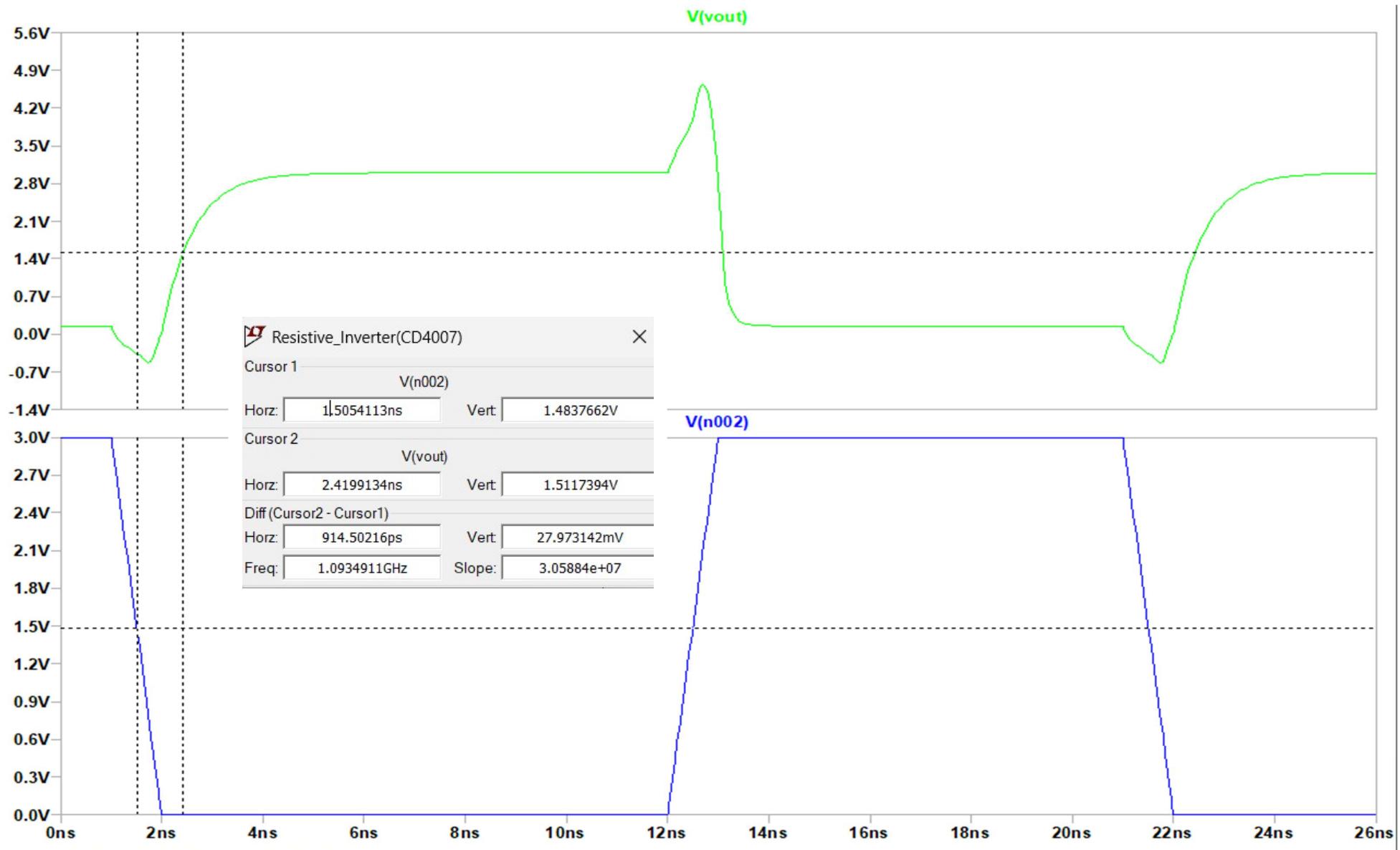
1e. Dynamic Power in Resistive Load Inverter (CD4007):



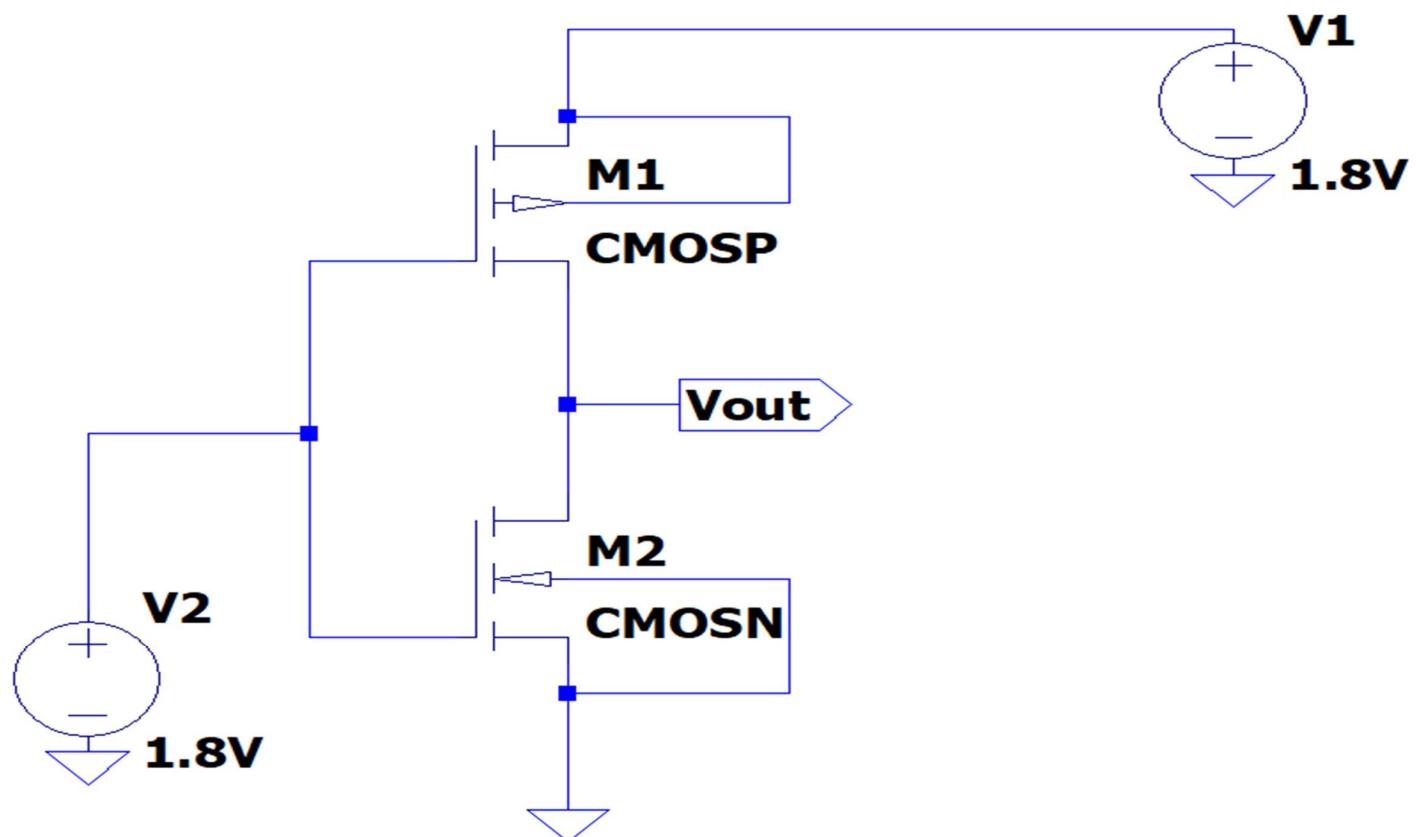
1f. High to Low Delay in Resistive Load Inverter (CD4007):



2g. Low to High Delay in Resistive Load Inverter (CD4007)

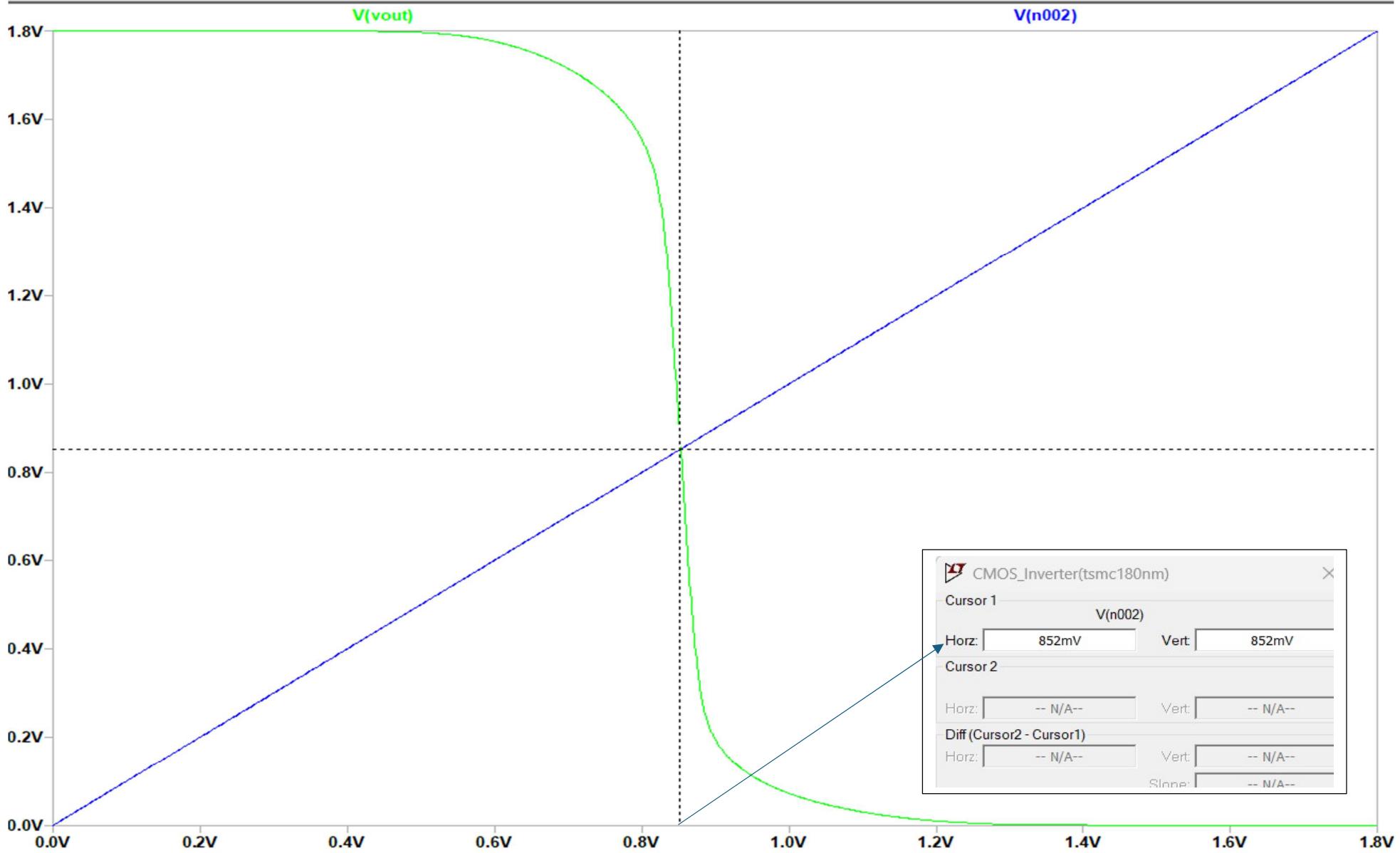


3.CMOS INVERTER

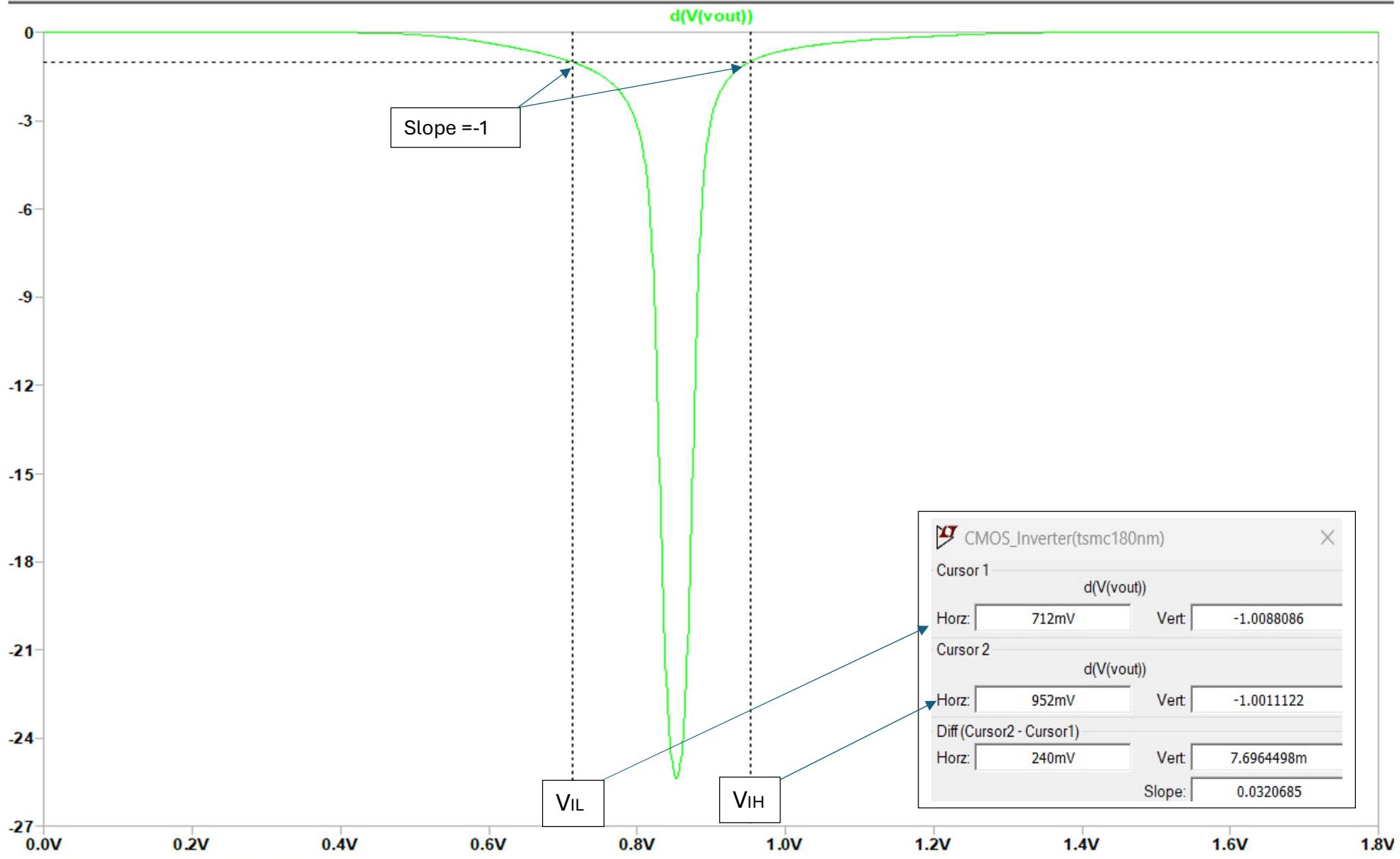


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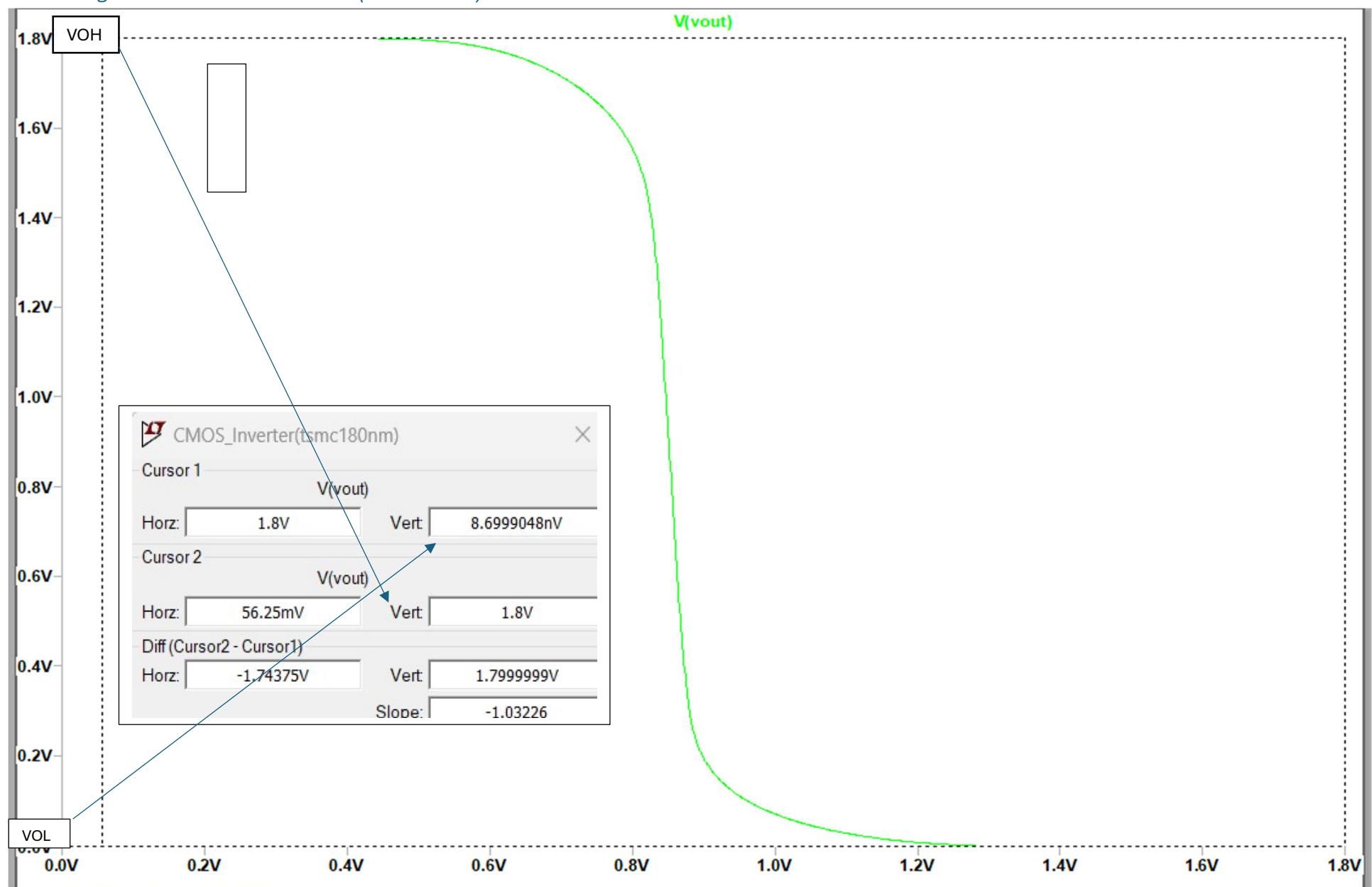
2a. VTC CHARACTERISTICS OF CMOS INVERTER (tsmc180nm)



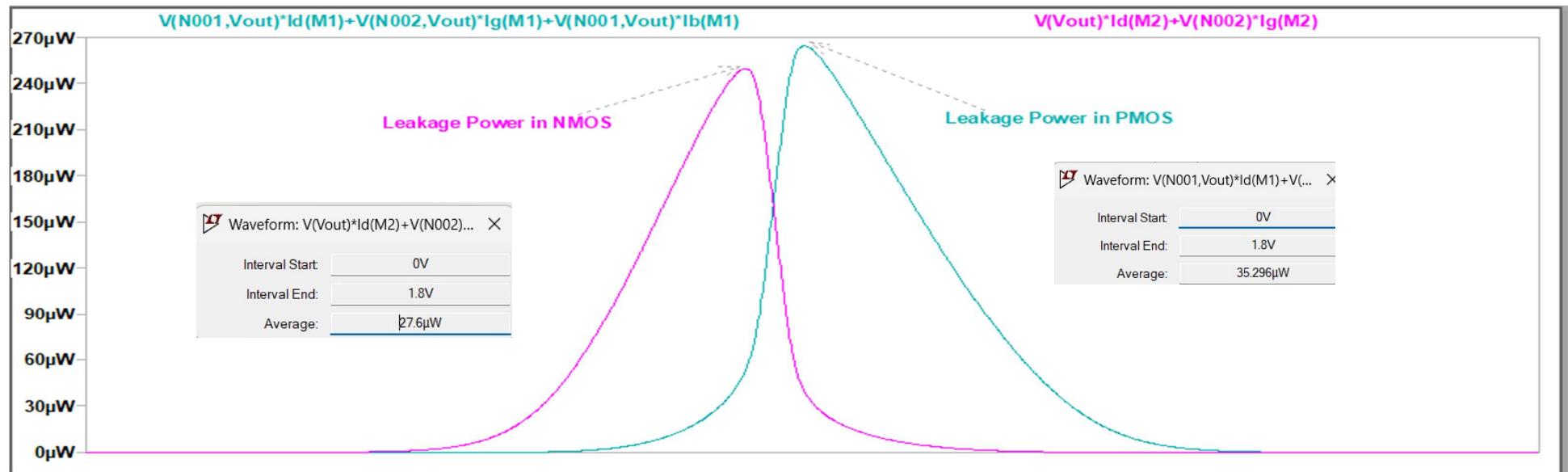
3b. Finding V_{IL} and V_{IH} from differentiation of VTC curve (tsmc180nm)



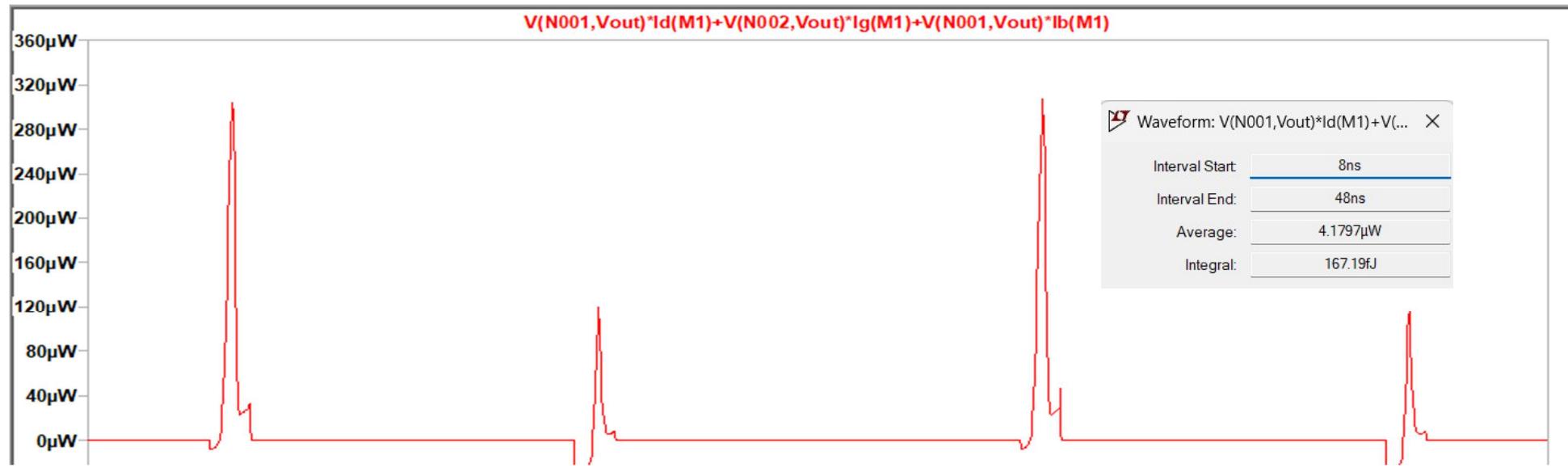
1c. Finding V_{OL} and V_{OH} from VTC curve (tsmc180nm):



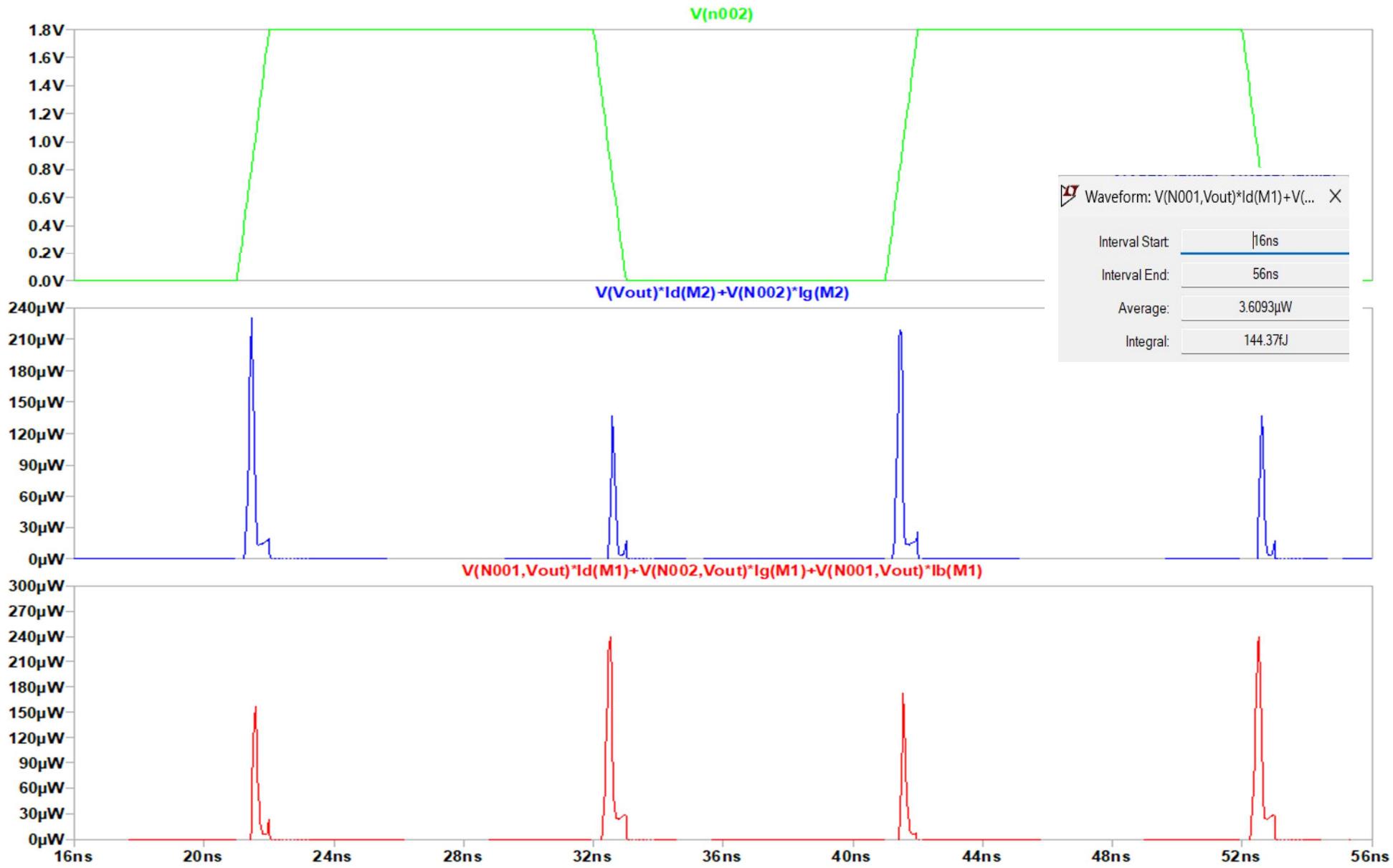
3d. Static Power In CMOS (tsmc180nm):



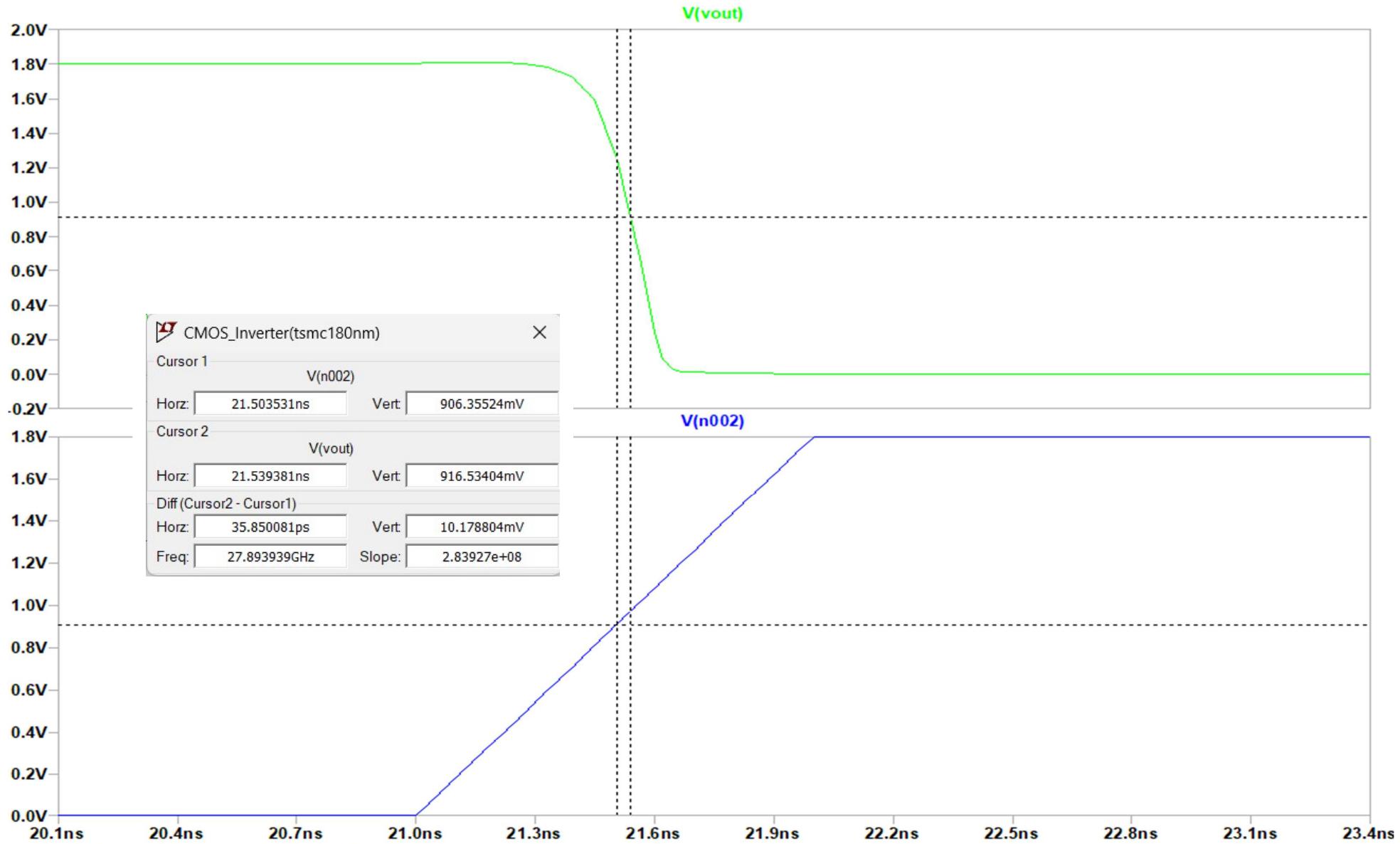
3e. Switching Power in CMOS Inverter (tsmc180nm):



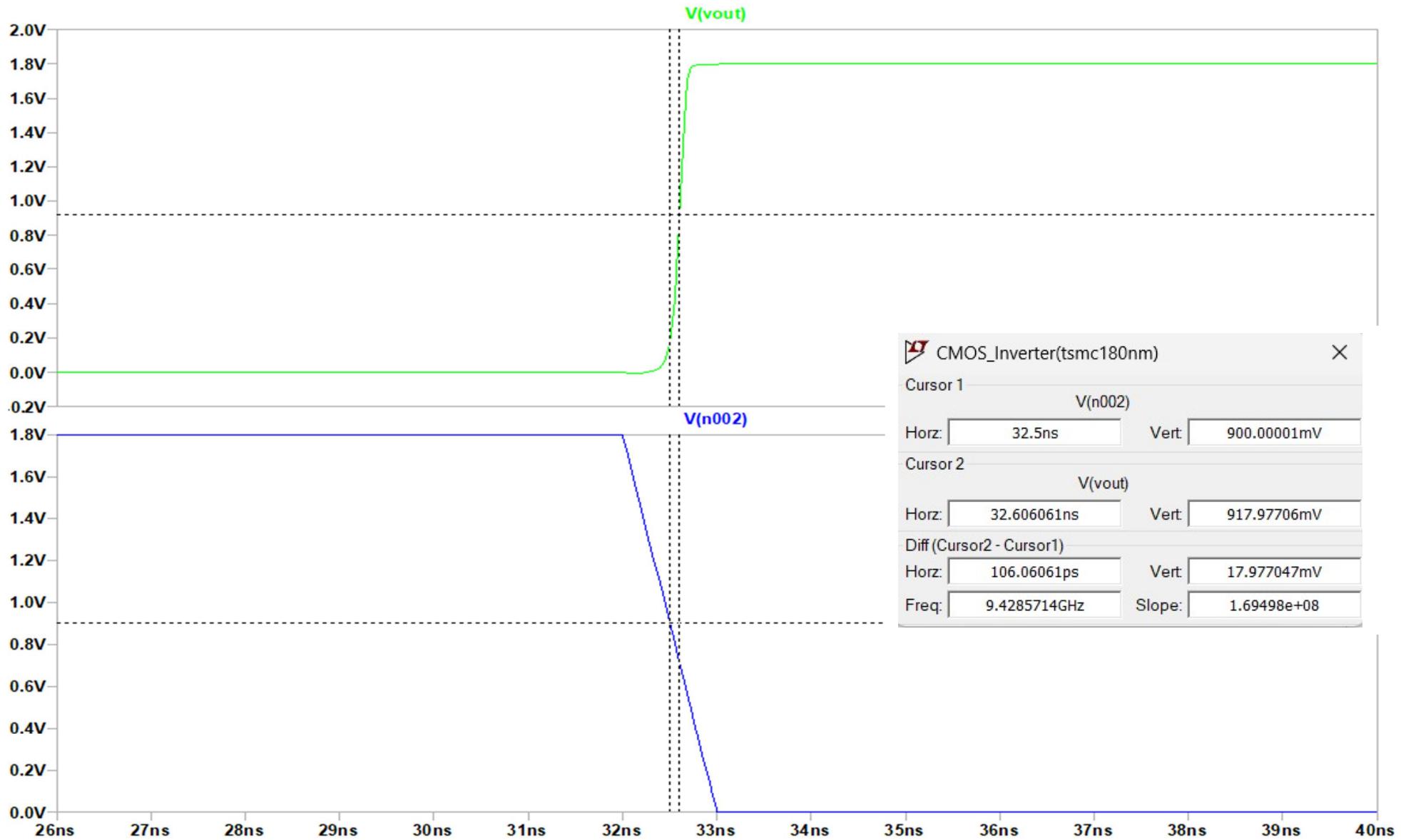
3f. Short Circuit Power in CMOS inverter (tsmc180nm):



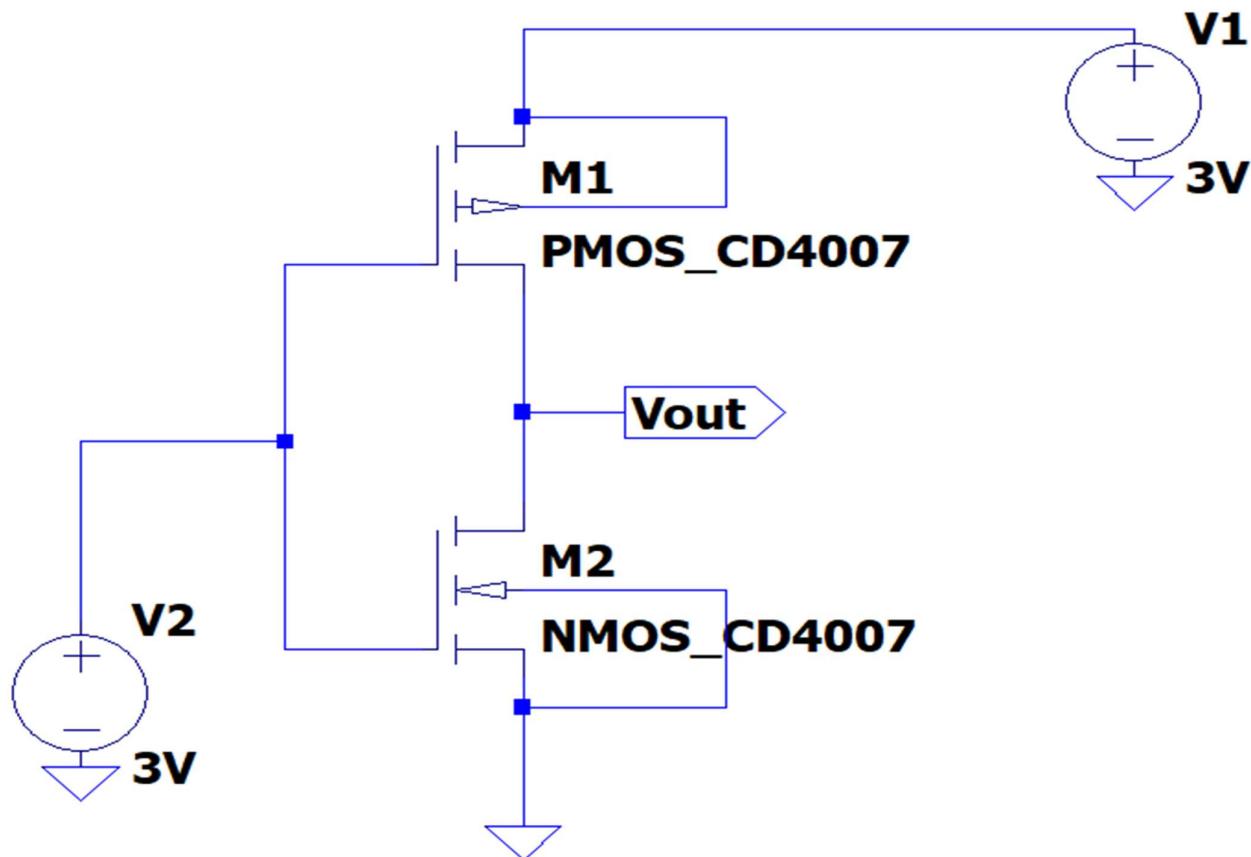
2g. High to Low Delay (t_{PHL}) in CMOS Inverter (tsmc180nm):



2h. Low to High Delay (t_{PLH}) in CMOS inverter (tsmc180nm):



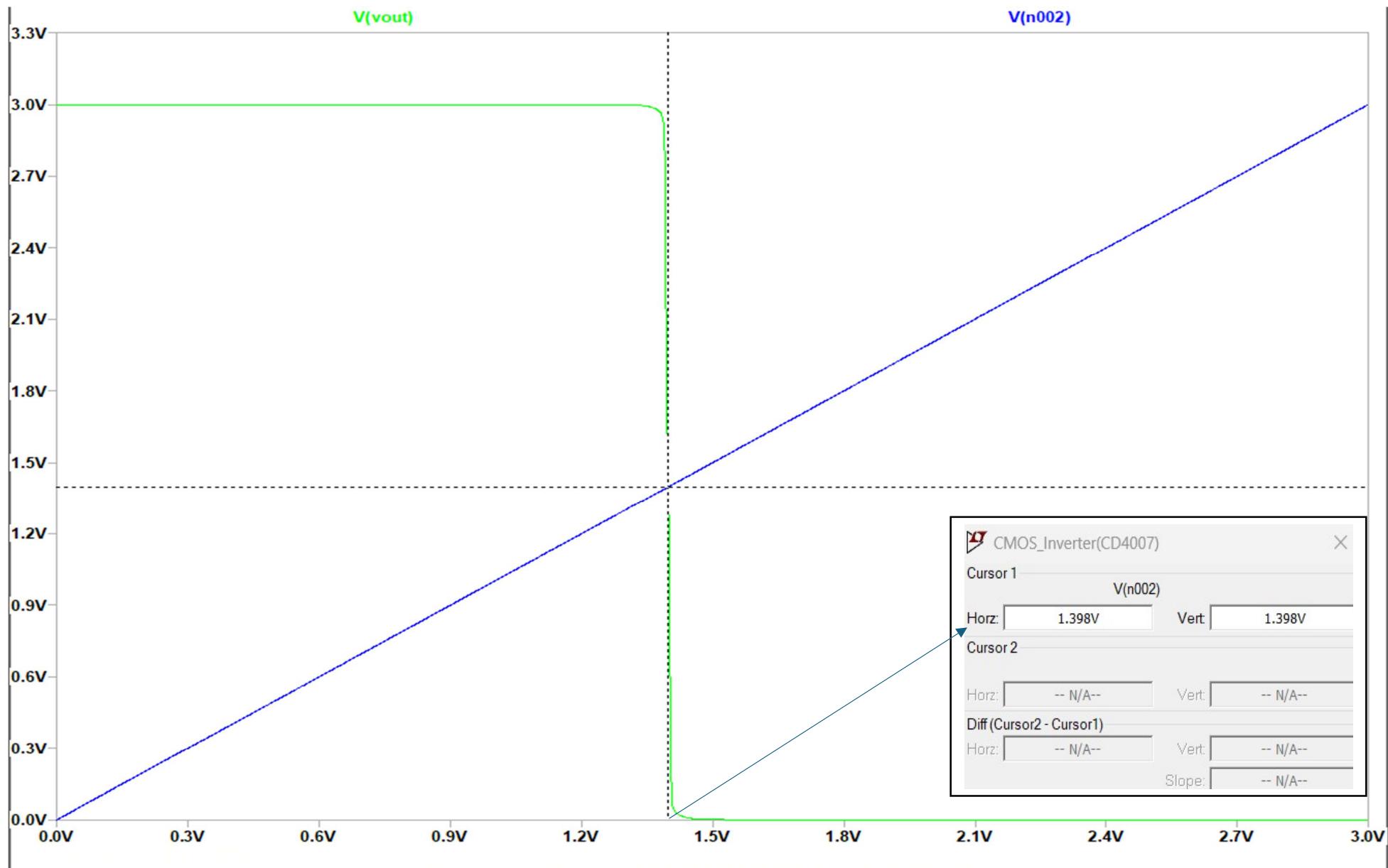
4.CMOS INVERTER (CD4007)



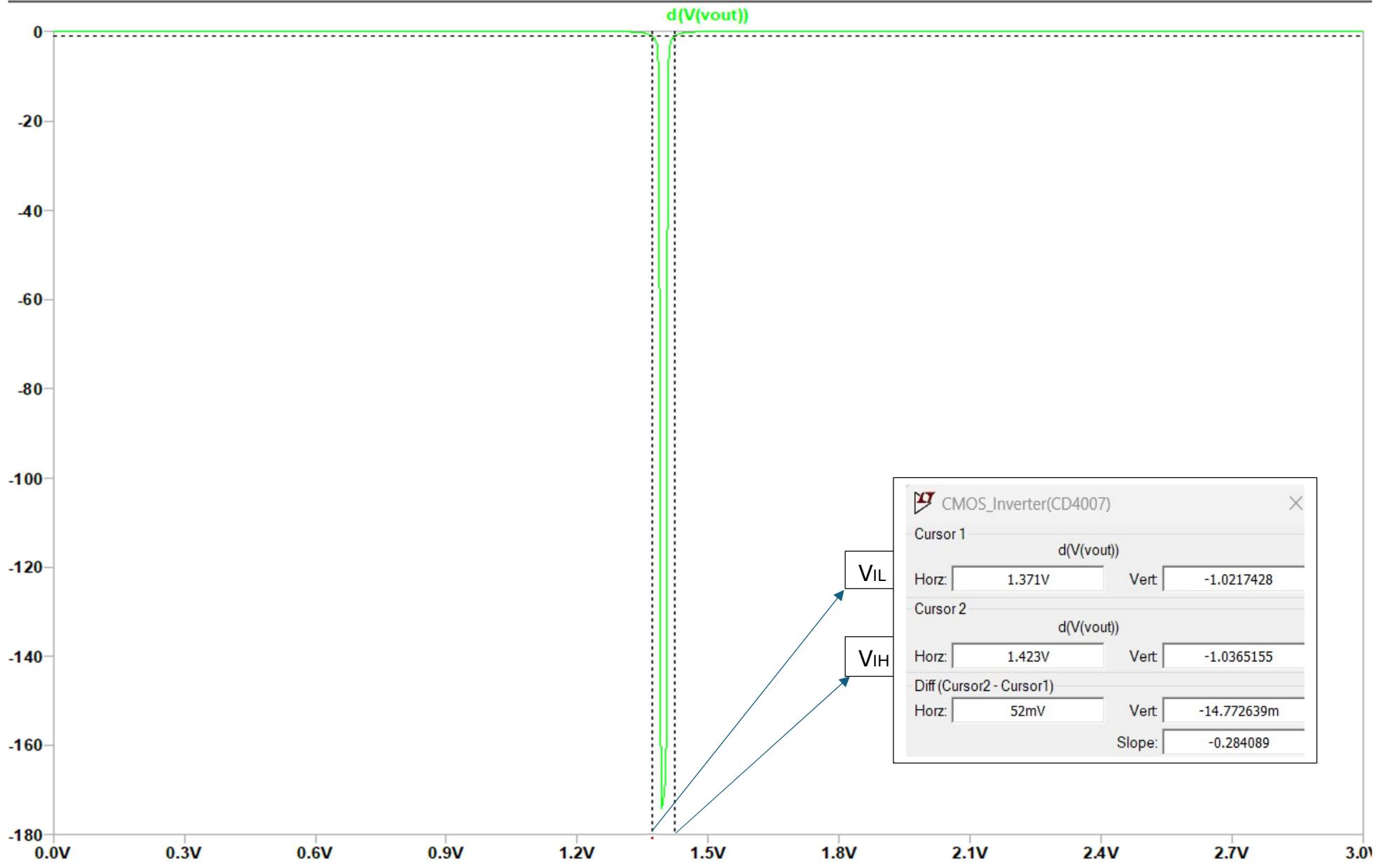
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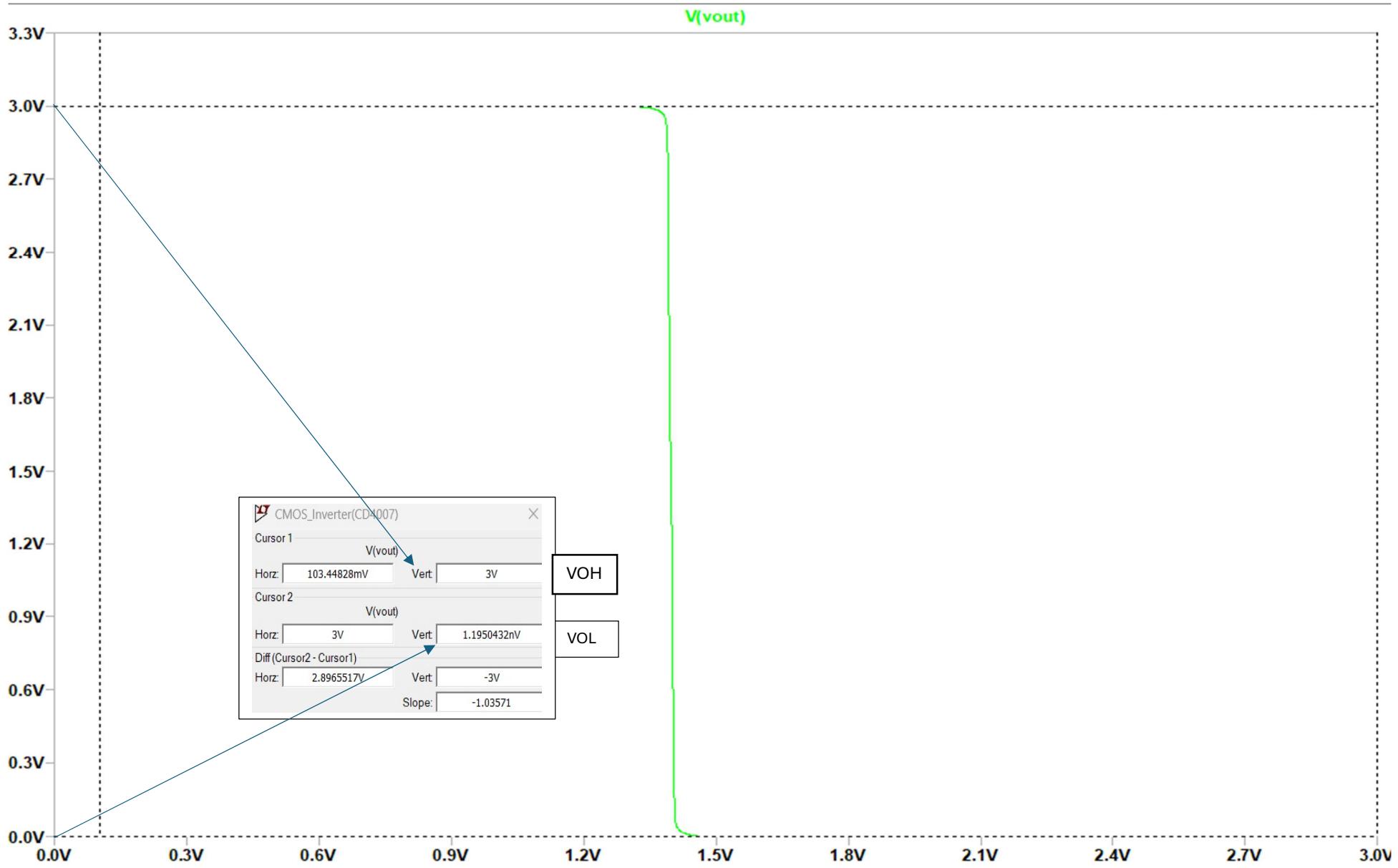
4a. VTC CHARACTERISTICS OF CMOS INVERTER (CD4007)



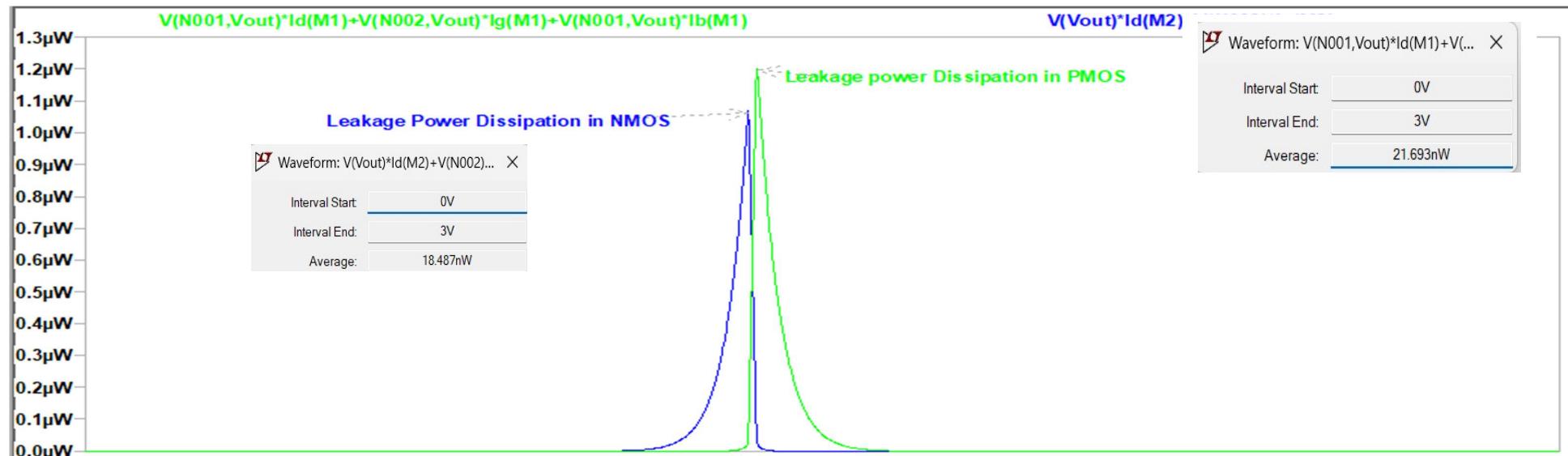
4b. Finding V_{IL} and V_{IH} from differentiation of VTC curve (CD4007)



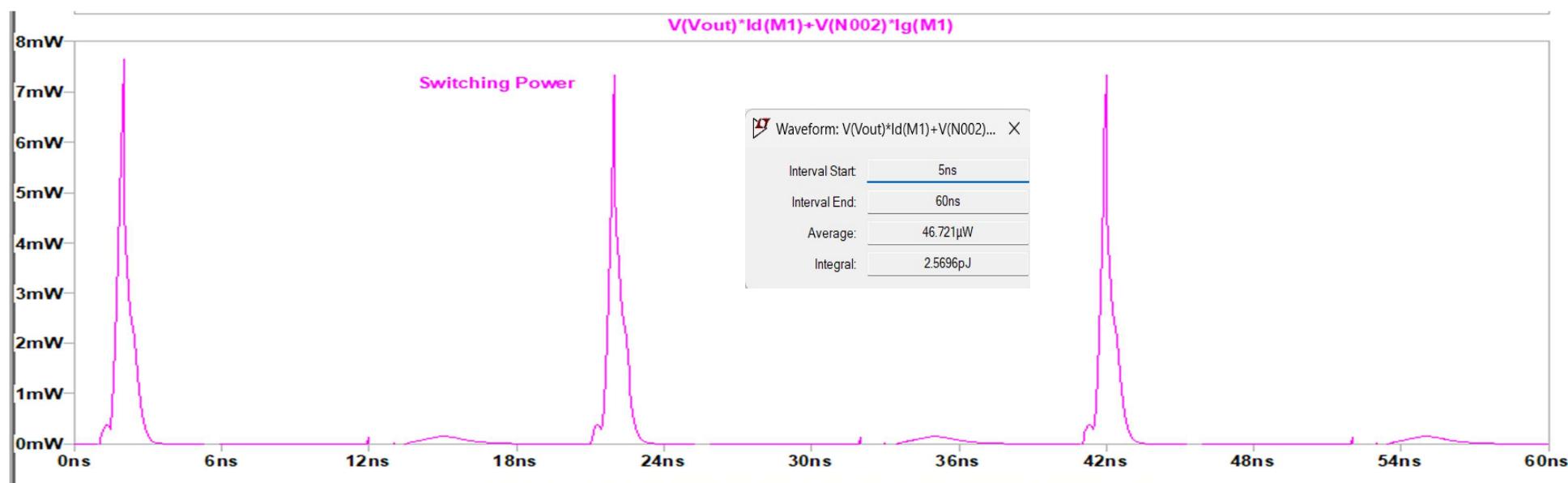
4c. Finding V_{OL} and V_{OH} from VTC curve (CD4007):



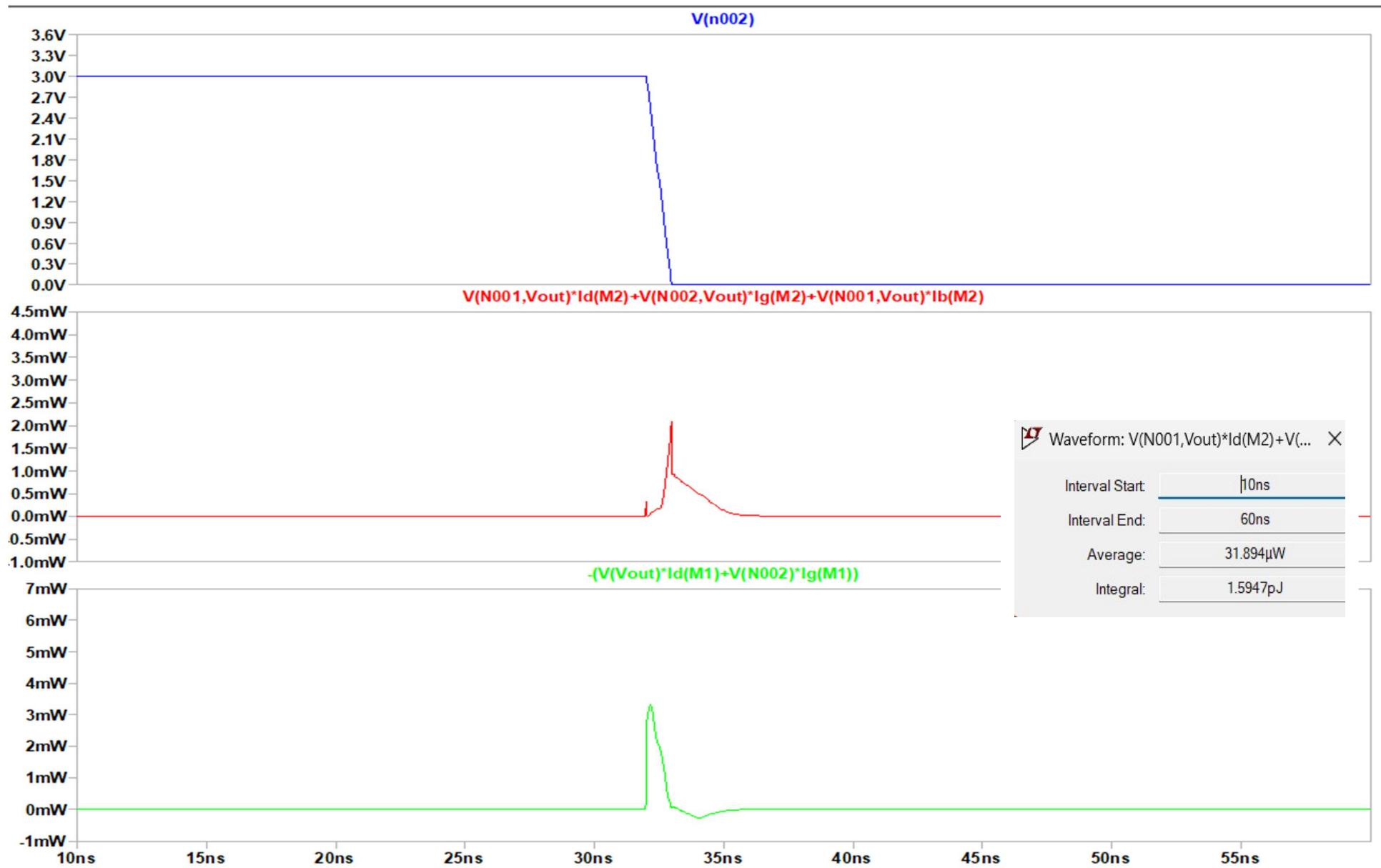
4d. Static Power in CMOS Inverter (CD4007);



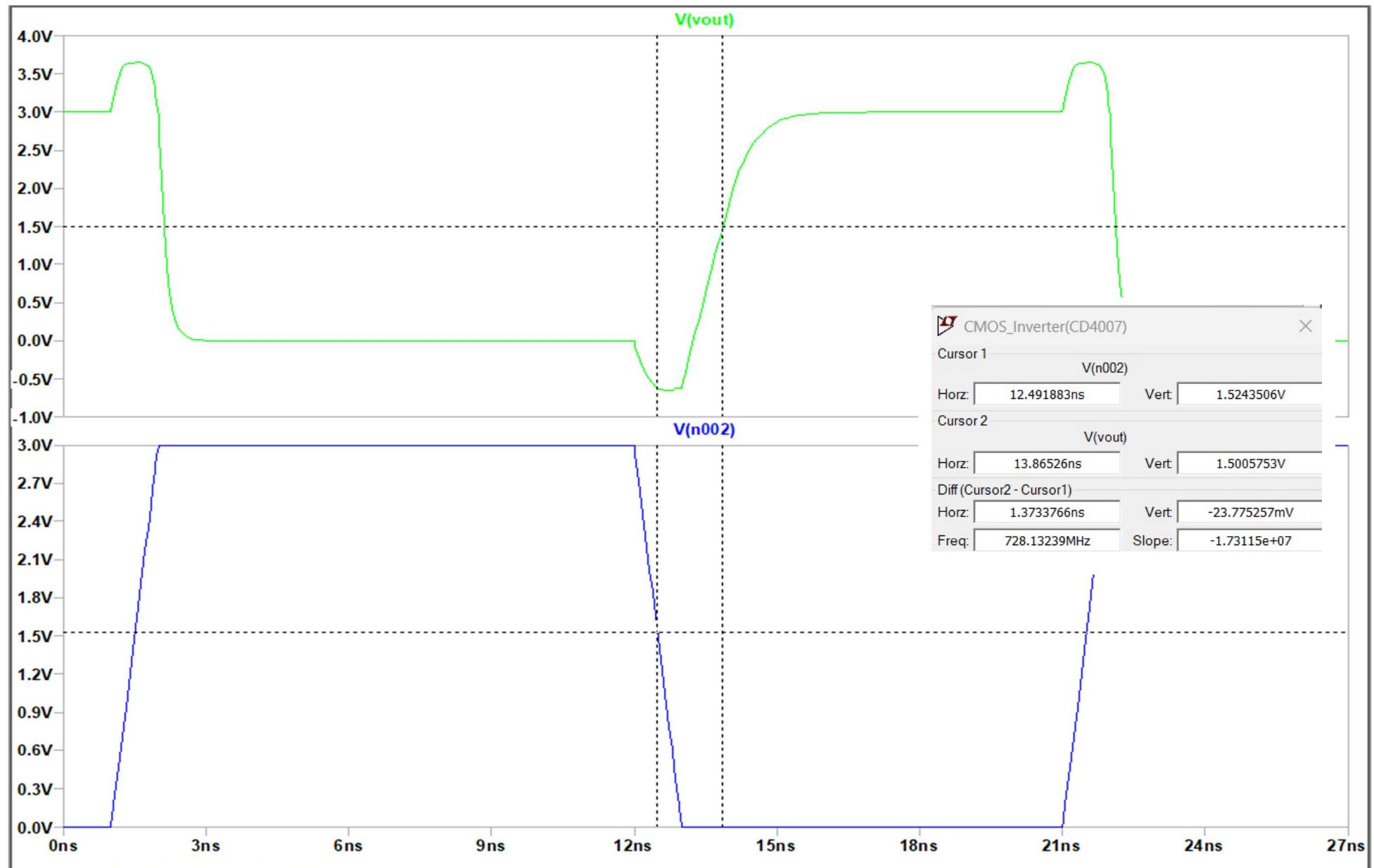
4e. Switching Power in CMOS Inverter (CD4007):



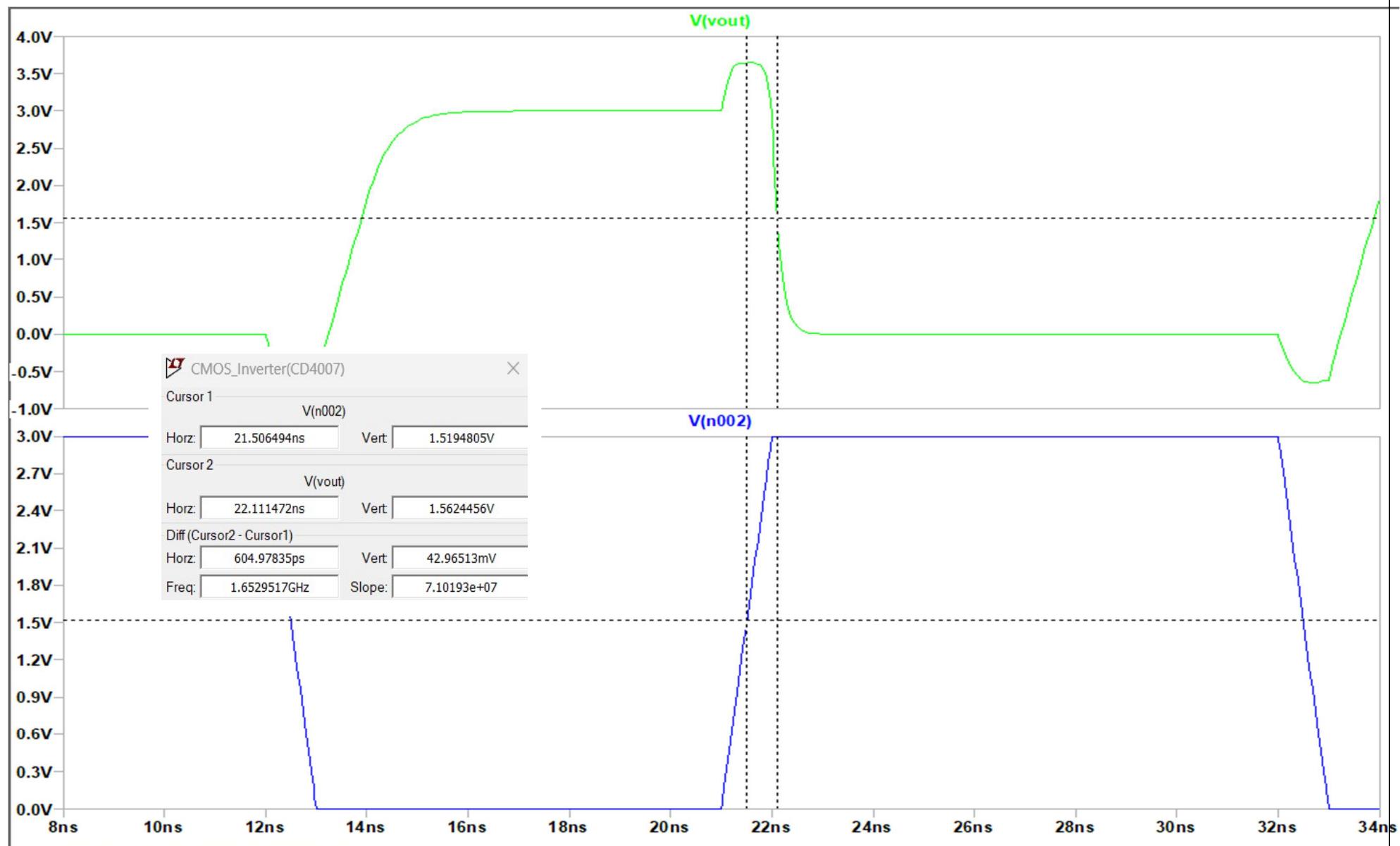
4f. Short Circuit Power in CMOS Inverter (CD4007):



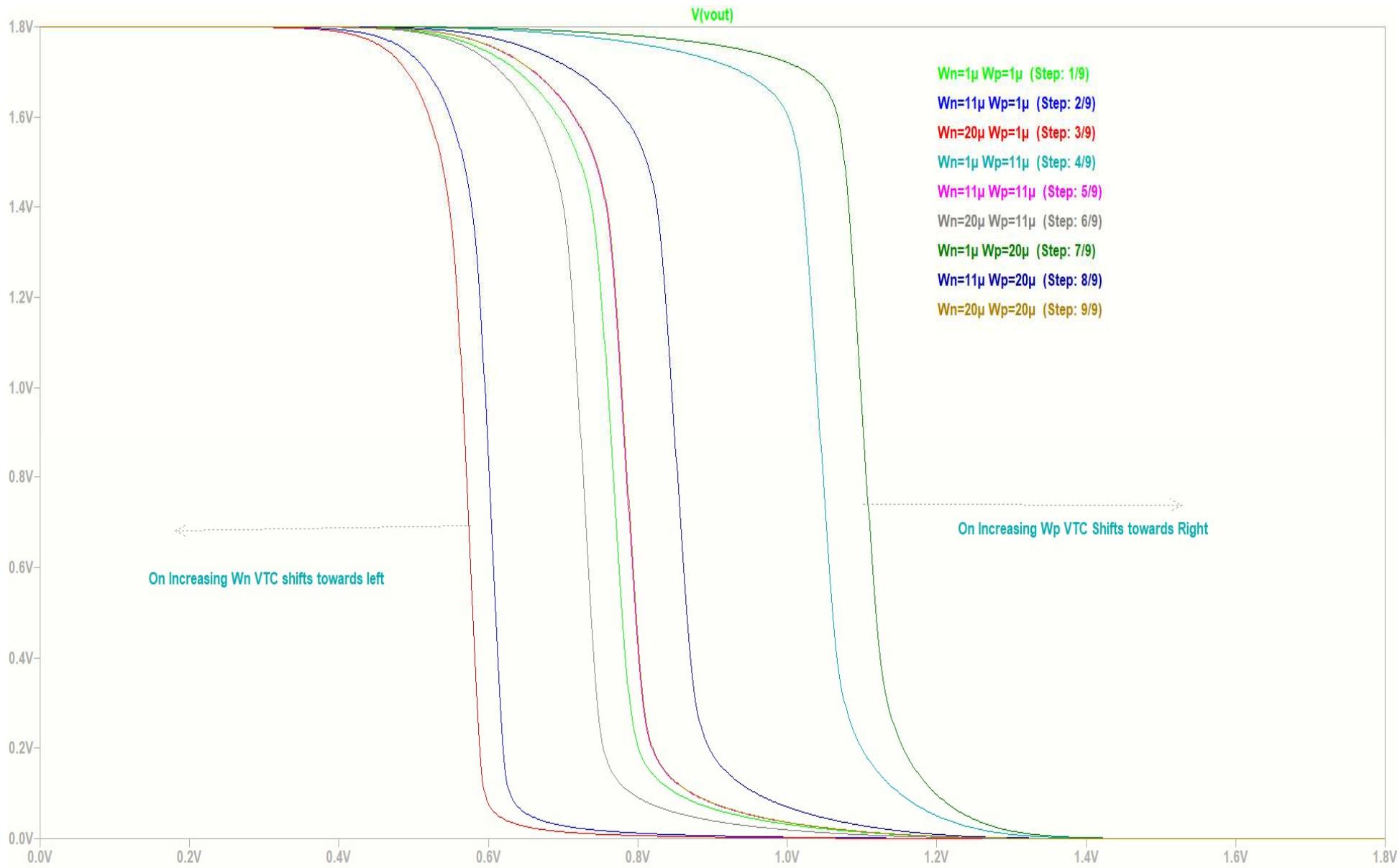
4e. Low to High Delay (t_{PLH}) in CMOS Inverter (CD4007)



4f. High to Low Time Delay (t_{PHL}) in CMOS Inverter (CD4007):



VTC OF CMOS INVERTER FOR DIFFERENT VALUES OF W_p AND W_n



RESULT

Sr. No-	PARAMETER	RESISTIVE LOAD INVERTER		CMOS INVERTER	
1.	MODEL FILE	TSMC180nm	CD4007	TSMC180nm	CD4007
2.	SUPPLY VOLTAGE (VDD)	1.8 V	3 V	1.8 V	3 V
3.	INVERTER THRESHOLD VOLTAGE (V_{tin})	0.656 V	1.66 V	0.852 V	1.398 V
4.	$NMH = V_{OH} - V_{IH}$	1.053 V	1.148 V	0.848 V	1.577 V
5.	$NML = V_{IL} - V_{OL}$	0.428 V	1.374 V	0.712 V	1.371 V
6.	STATIC POWER	196 μW	319 μW	32 μW	20 μW
7.	DYNAMIC POWER DISSIPATION	SWITCHING POWER	11.25 μW	71.2 μW	4.2 μW
		SHORT CIRCUIT POWER	N/A	N/A	3.6 μW
8.	TOTAL POWER DISSIPATION	207 μW	390 μW	39.8 μW	108 μW
9.	HIGH TO LOW DELAY (t_{PHL})	65 ps	577 ps	35 ps	604 ps
10.	LOW TO HIGH DELAY (t_{PLH})	147.7 ps	915 ps	106 ps	1373 ps
SA11.	TOTAL DELAY	106 ps	746 ps	70 ps	988 ps

CONCLUSION

Power Dissipation:

- **CMOS Inverter** (TSMC180nm) exhibits much lower power dissipation (207 μ W at 1.8V and 39.8 μ W at 3V) compared to the **Resistive Load Inverter** (CD4007), which consumes significantly higher power (390 μ W at 1.8V and 108 μ W at 3V).
- This indicates that the **CMOS Inverter** is more power-efficient, making it preferable for low-power applications.

Area Consumption:

- **CMOS Inverter** (TSMC180nm) is more area-efficient (low area), while the **Resistive Load Inverter** (CD4007) requires a larger area due to its resistive load and transistor characteristics.
- Therefore, **CMOS Inverter** is more suitable for applications where area efficiency is crucial.

Delay:

- The **CMOS Inverter** (TSMC180nm) offers **faster switching** with significantly lower delay (106 ps total delay at 1.8V and 70 ps at 3V) compared to the **Resistive Load Inverter** (CD4007), which has much higher delays (746 ps total delay at 1.8V and 988 ps at 3V).
- This makes **CMOS Inverter** better for high-speed applications, while **Resistive Load Inverter** is slower due to its larger parasitics and different technology.

Why there is Overshot and Undershoot in output Waveform of CD4007 technology Inverter

The overshoot and undershoot in the CD4007 inverter output waveform are primarily due to the combination of slower transistor switching times, higher parasitic capacitance, and resistance effects in the older technology. Additionally, the resistive load and potential power supply issues can exacerbate these voltage spikes. Improvements in transistor switching speed, capacitance, and load handling in modern technologies can reduce or eliminate such behaviors.