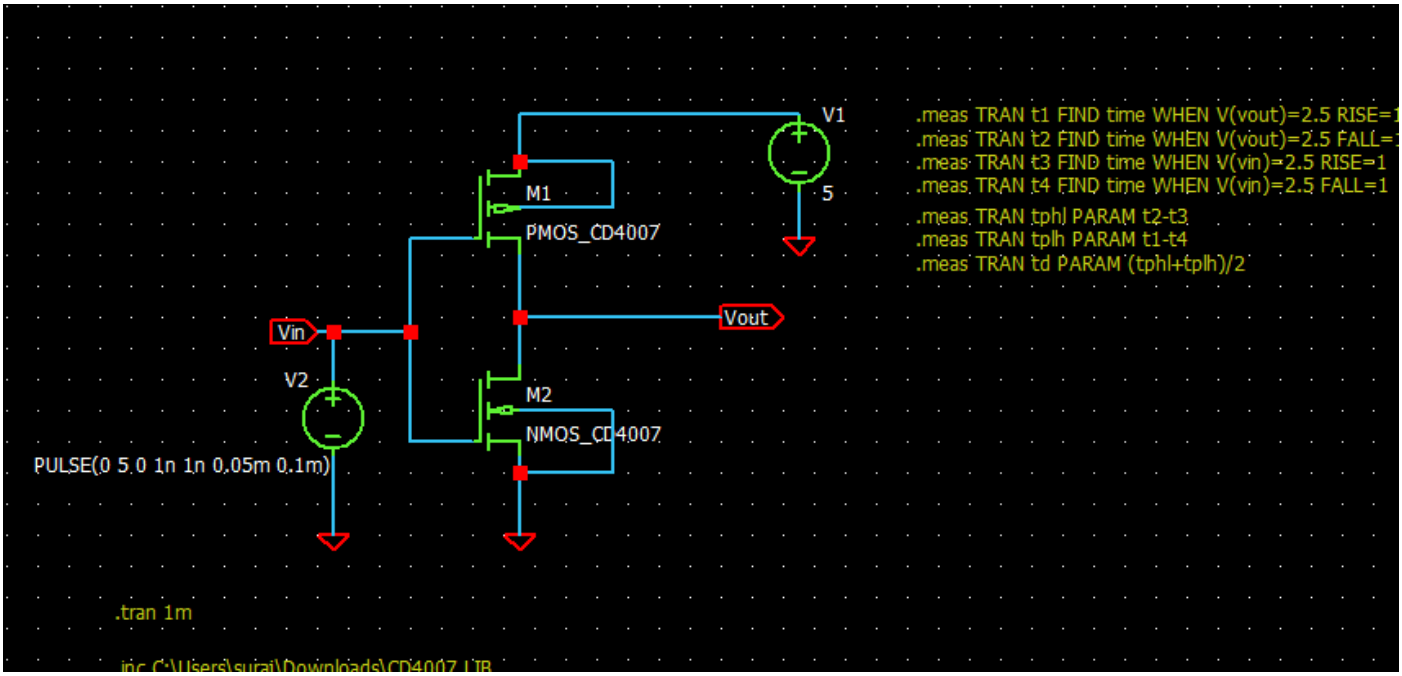
EXPERIMENT – 06

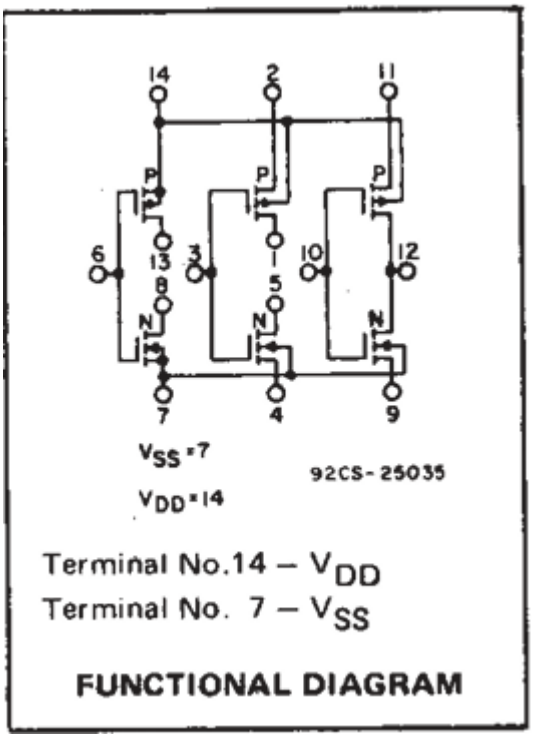
NAME – SURAJ **EEM614 (VLSI Lab)**

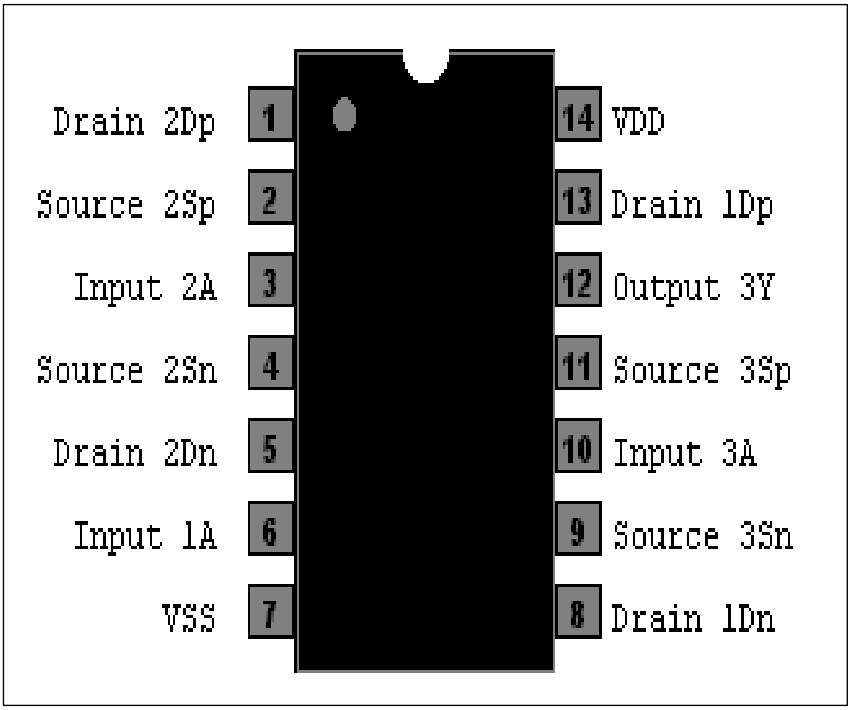
ROLL NO. -2201769

(a) To realize CMOS inverter using CD4007 IC and perform the transient analysis with and without load at different input frequencies.

(b) To realize 3-stage CMOS ring oscillator using CD4007 IC and calculate the oscillation frequency.

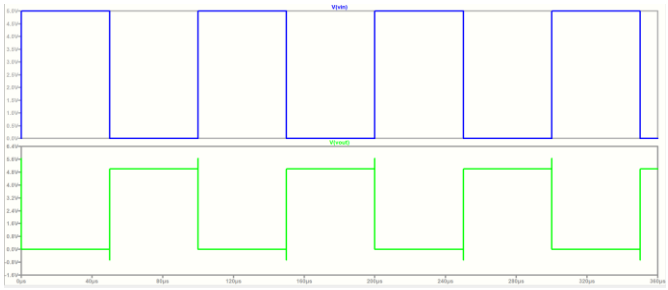




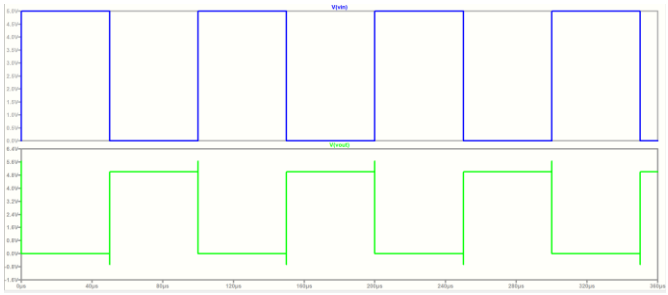


1. WITHOUT LOAD

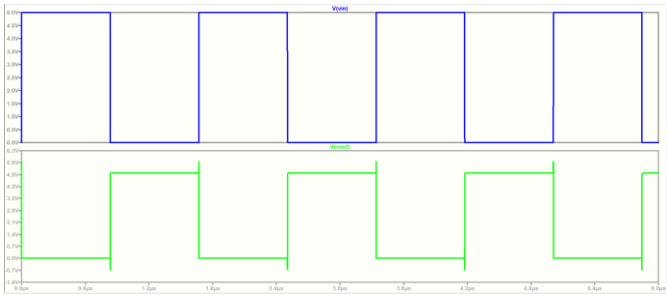
At 10 KHz



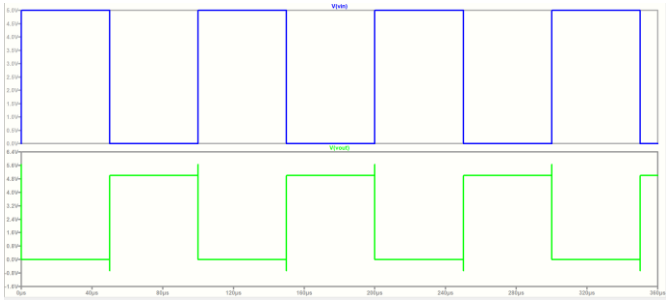
At 100 KHz



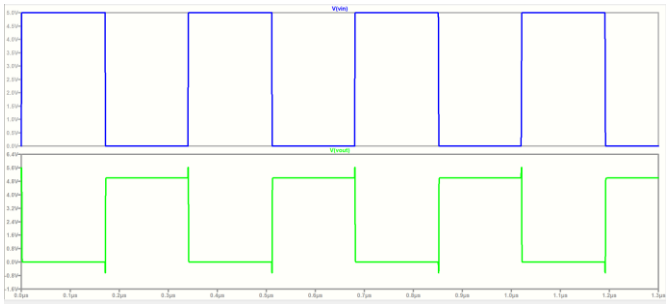
At 600 KHz



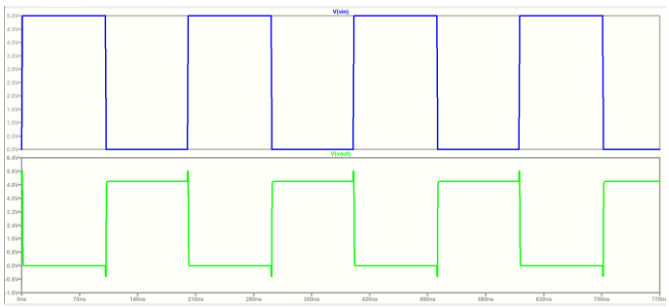
At 1000 KHz



At 3000 KHz

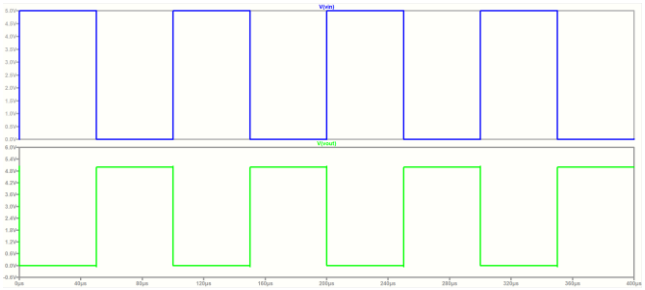


At 5000 KHz

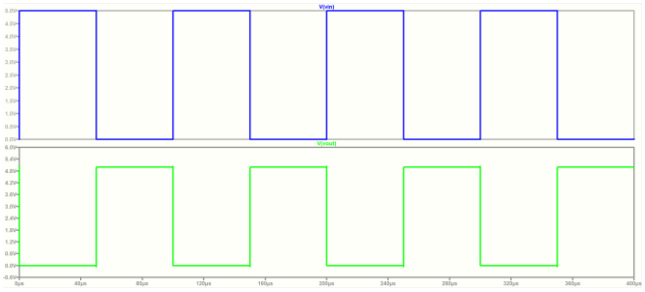


2. WITH LOAD 30PF

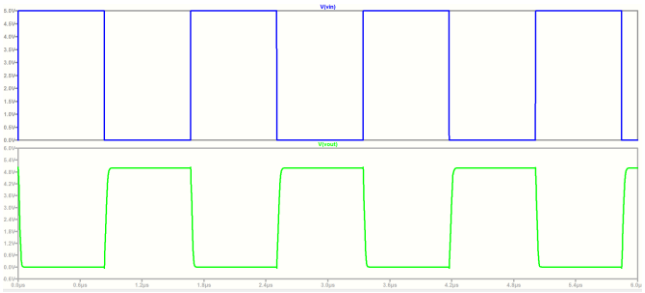
At 10 KHz



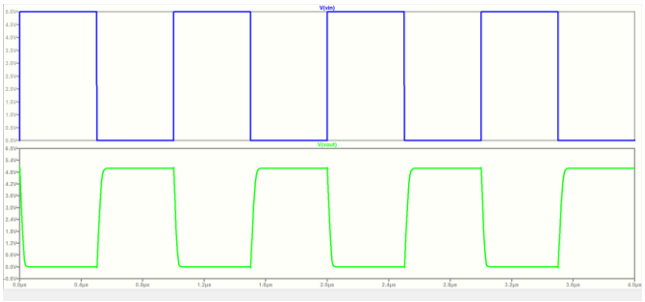
At 100 KHz



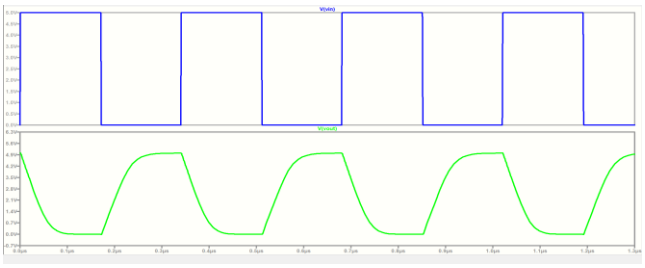
At 600 KHz



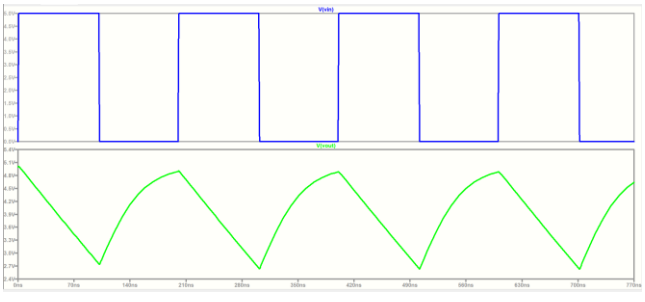
At 1000 KHz



At 3000 KHz



At 5000 KHz



Simulation Results:

1.WITHOUT LOAD

WITHOUT LOAD				
Sr.no.	**Frequency(kHz)**	**Rise Time**	**Fall time**	**Delay**
1.	5	5.78284e-10	5.21393e-10	5.49838e-10
3.	50	5.75303e-10	5.21393e-10	5.48348e-10
4.	100	5.75022e-10	5.21393e-10	5.48207e-10
5.	200	5.75303e-10	5.2025e-10	5.47776e-10
6.	400	5.75303e-10	5.2025e-10	5.47776e-10
7.	600	5.75303e-10	5.2025e-10	5.47776e-10
8.	800	5.75303e-10	5.2025e-10	5.47776e-10
9.	1000	5.75303e-10	5.2025e-10	5.47776e-10
10.	1200	5.76496e-10	5.2025e-10	5.48373e-10
11.	1600	5.75303e-10	5.2025e-10	5.47776e-10
12.	2000	5.76496e-10	5.2025e-10	5.48373e-10
13.	3000	5.75303e-10	5.2025e-10	5.47776e-10
14.	4000	5.76271e-10	5.2025e-10	5.48261e-10
15.	5000	5.75615e-10	5.75615e-10	5.47932e-10

2. WITH LOAD 30pF

WITH LOAD 30pF				
Sr.no.	**Frequency(kHz)**	**Rise Time**	**Fall time**	**Delay**
1.	5	2.49051e-08	2.14262e-08	2.31656e-08
2.	50	2.49051e-08	2.14262e-08	2.31656e-08
4.	100	2.49051e-08	2.14262e-08	2.31656e-08
5.	200	2.49051e-08	2.14262e-08	2.31656e-08
6.	400	2.49051e-08	2.14262e-08	2.31656e-08
7.	600	2.49051e-08	2.14262e-08	2.31656e-08
8.	800	2.49051e-08	2.14262e-08	2.31656e-08
9.	1000	2.49051e-08	2.14262e-08	2.31656e-08
10.	1200	2.49051e-08	2.14262e-08	2.31656e-08
11.	1600	2.49051e-08	2.14262e-08	2.31656e-08
12.	2000	2.49051e-08	2.14262e-08	2.31656e-08
13.	3000	2.42934e-08	2.08256e-08	2.25595e-08
14.	4000	2.42926e-08	2.08256e-08	2.25591e-08
15.	5000	2.42804e-08	2.08256e-08	2.2553e-08

Experimental Results

1.

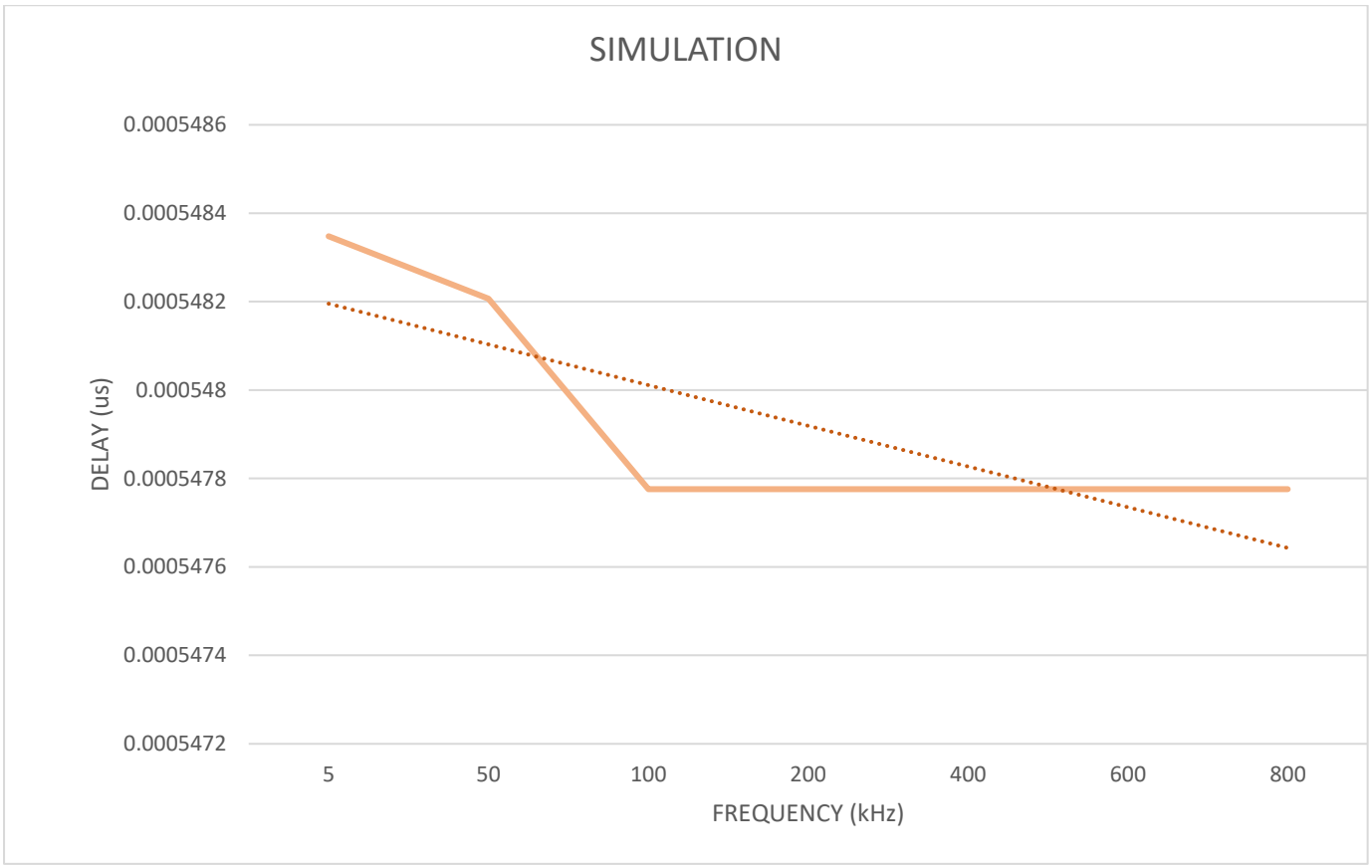
WITHOUT LOAD				
Sr.no.	**Frequency KHz**	**Rise Time(us)**	**Fall time(us)**	**Delay(us)**
1.	5	0.0985	0.0227	0.0606
2.	10	0.0985	0.0227	0.0606
3.	30	0.0985	0.0227	0.0606
4.	50	0.0985	0.0227	0.0606
5.	80	0.0985	0.0227	0.0606
6.	100	0.0985	0.0228	0.06065
7.	150	0.0985	0.0227	0.0606
8.	200	0.0985	0.0227	0.0606
9.	300	0.0973	0.0227	0.0606
10.	400	0.0972	0.0227	0.05995
11.	500	0.0972	0.0227	0.05995
12.	800	0.09655	0.0227	0.059625
13.	1000	0.09655	0.0224	0.059475
14.	1500	0.09655	0.0224	0.059475
15.	2000	0.09655	0.0225	0.059525
16.	4000	0.09544	0.022	0.05872
17.	5000	0.09544	0.022	0.05872

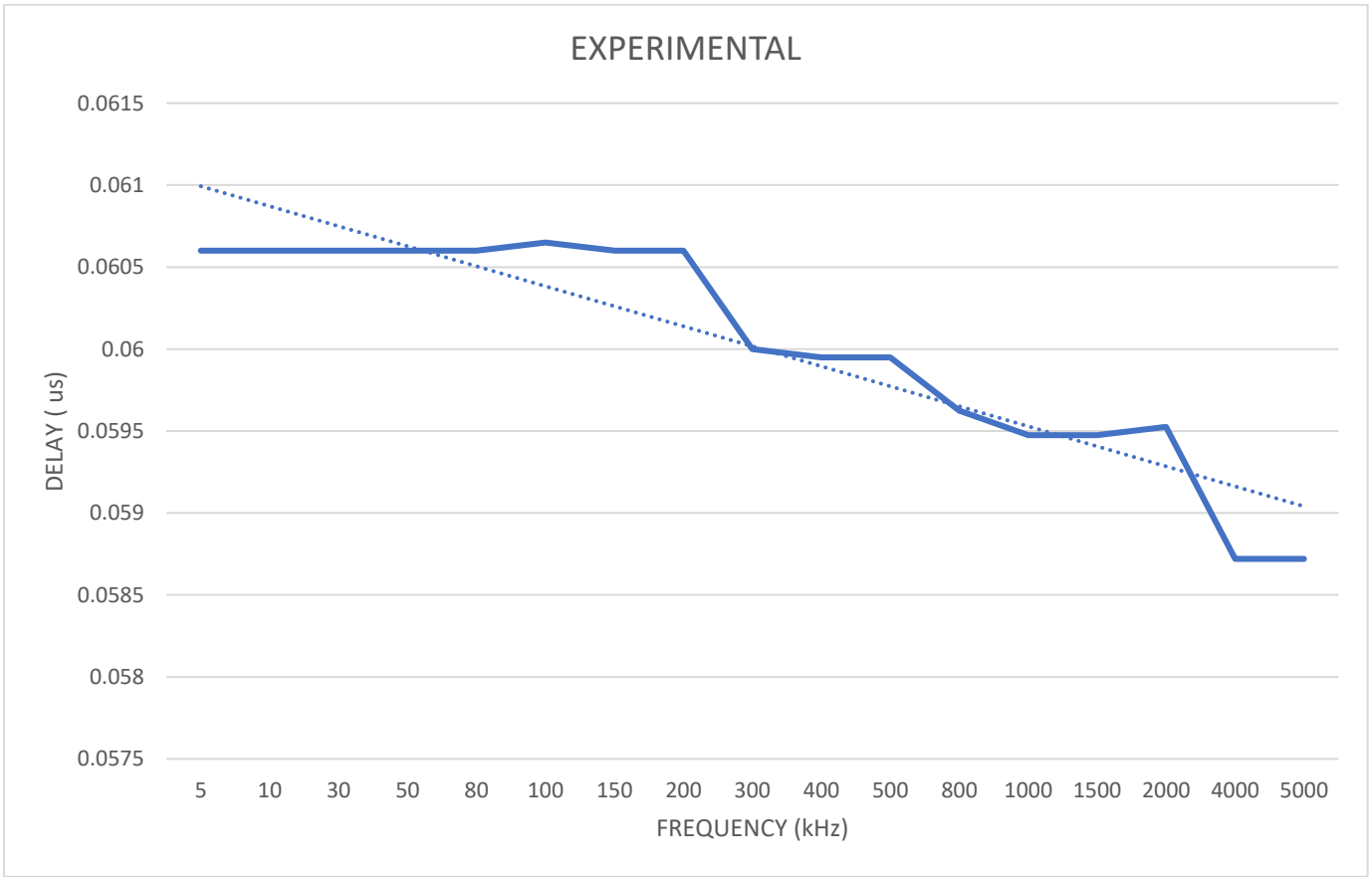
2.

WITH LOAD 30pF				
Sr.no	**Frequency Khz**	**Rise Time(us)**	**Fall time(us)**	**Delay(us)**
1.	5	0.132	0.0311	0.08155
2.	50	0.132	0.0311	0.08155
3.	80	0.132	0.0311	0.08155
5.	100	0.132	0.0311	0.08155
6.	200	0.131	0.0311	0.08105
7.	300	0.13	0.0311	0.08055
8.	400	0.13	0.0311	0.08055
9.	500	0.13	0.0311	0.08055
11.	1000	0.13	0.0311	0.08055
12.	1500	0.13	0.0311	0.08055
13.	2000	0.13	0.0311	0.08055
14.	4000	0.13	0.0311	0.08055
15.	5000	0.13	0.0311	0.08055

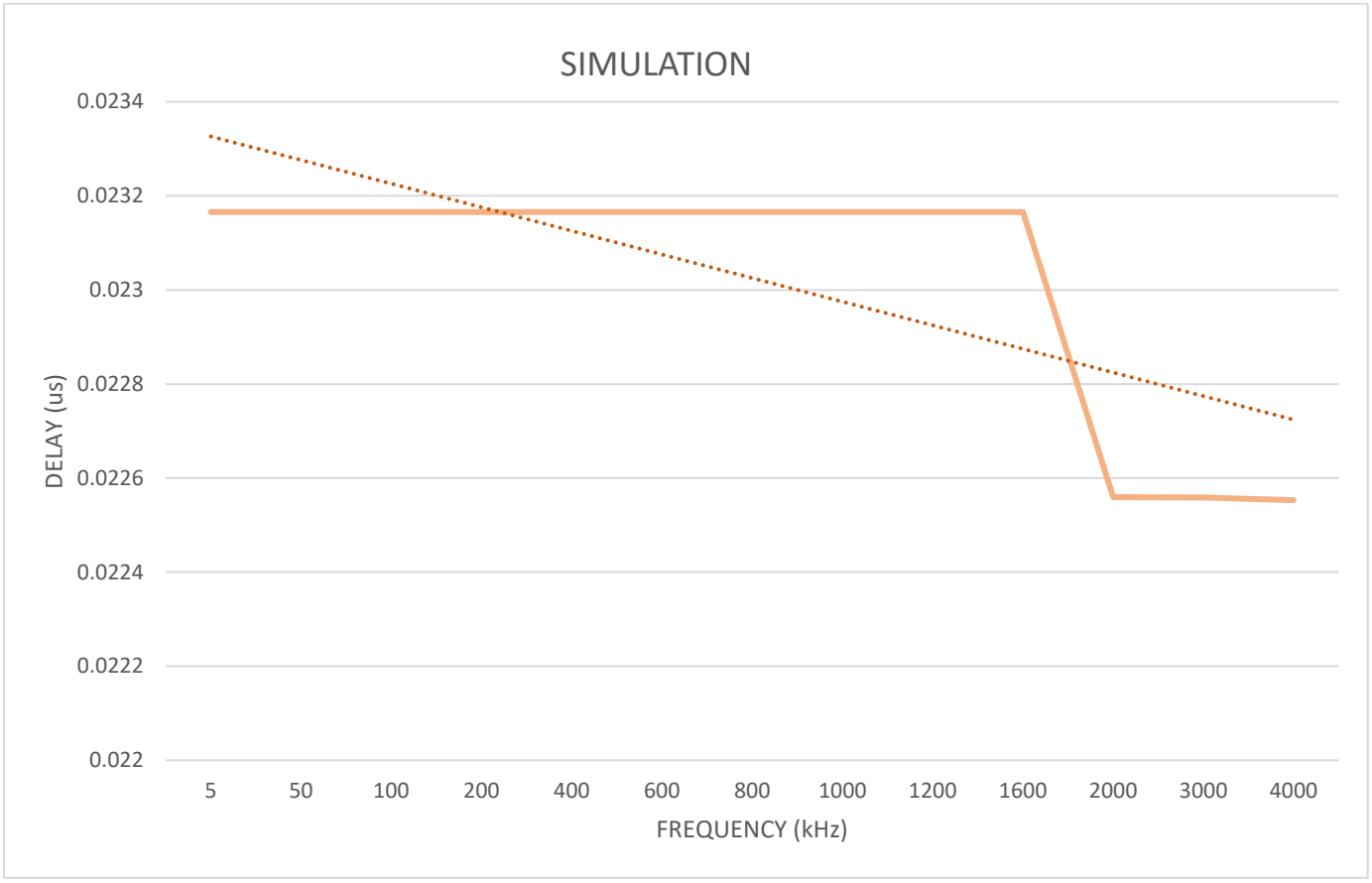
SIMULATION VS EXPERIMENTAL

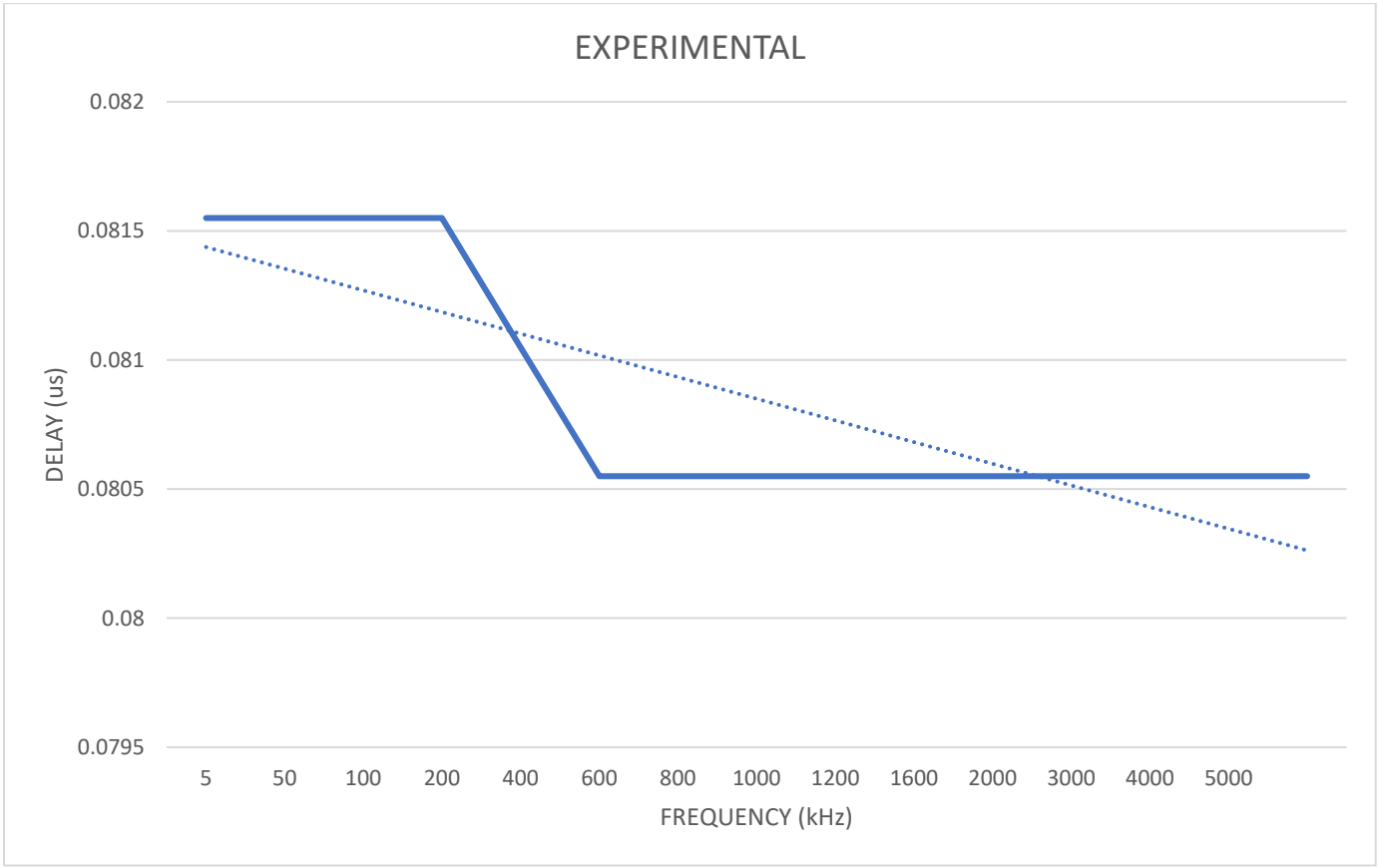
1.WITHOUT LOAD





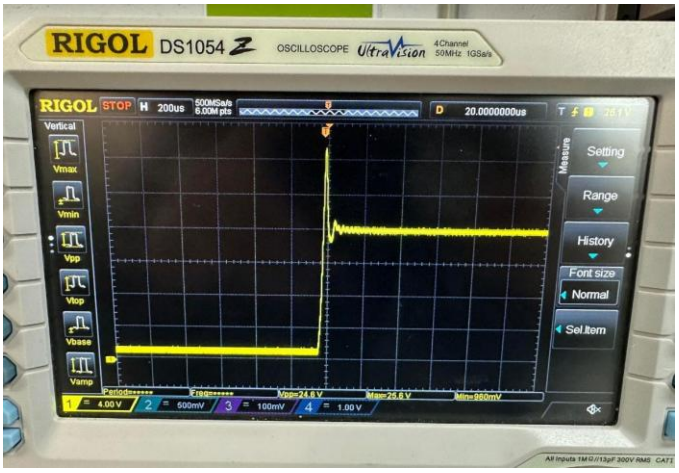
2.WITH LOAD

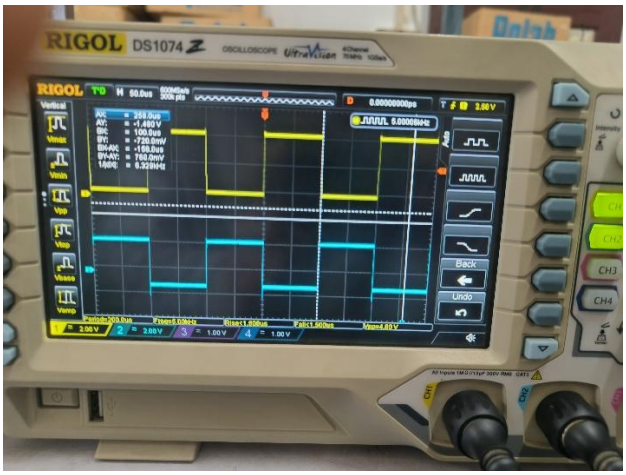

SIMULATION
0.0234
0.0232
0.023
0.0228
0.0226
0.0224
0.0222
0.022
DELAY (us)
5
50
100
200
400
600
800
1000
1200
1600
2000
3000
4000
FREQUENCY (kHz)

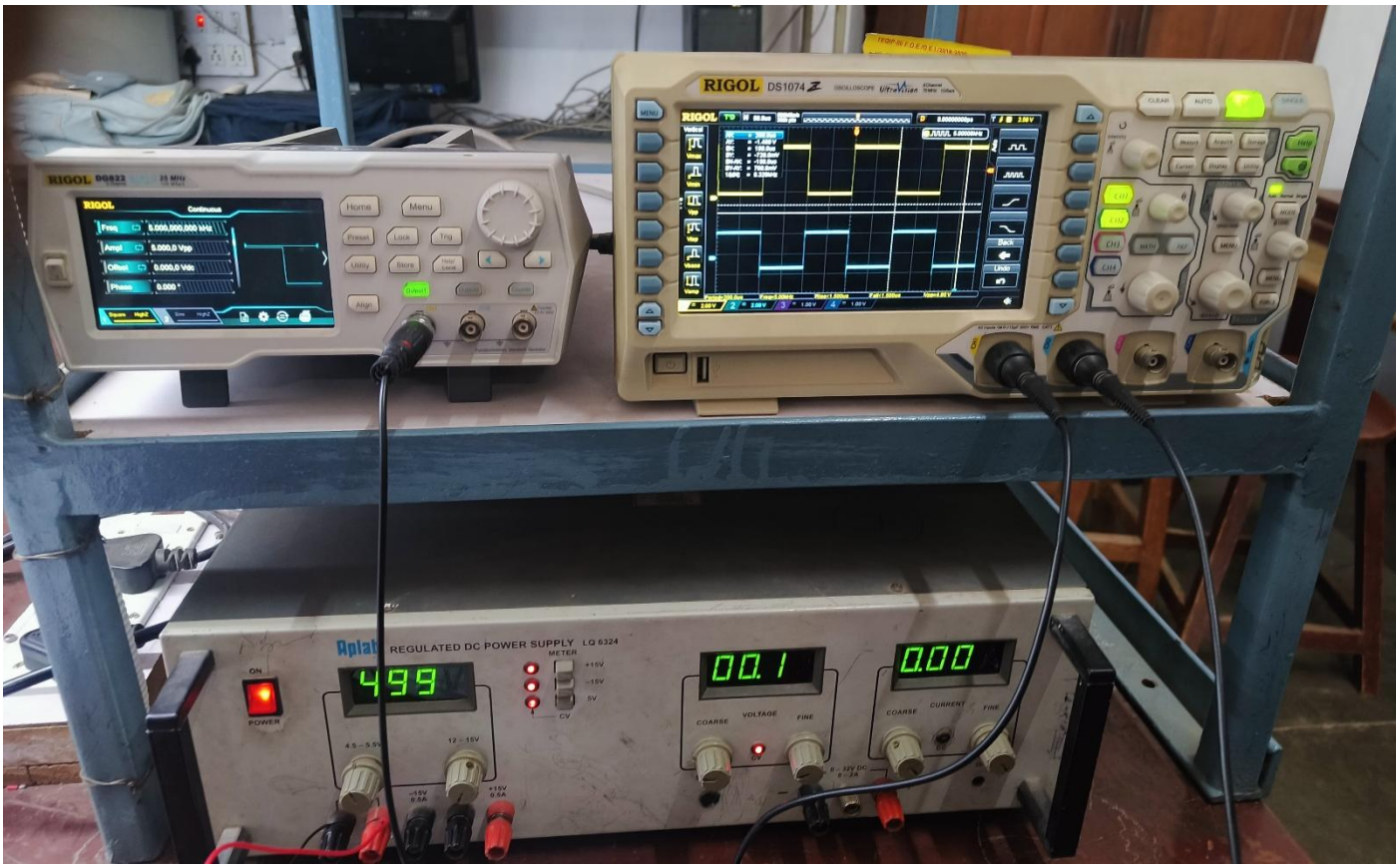

EXPERIMENTAL
0.082
0.0815
0.081
0.0805
0.08
0.0795
DELAY (us)
5
50
100
200
400
600
800
1000
1200
1600
2000
3000
4000
5000
FREQUENCY (kHz)

CONCLUSION:

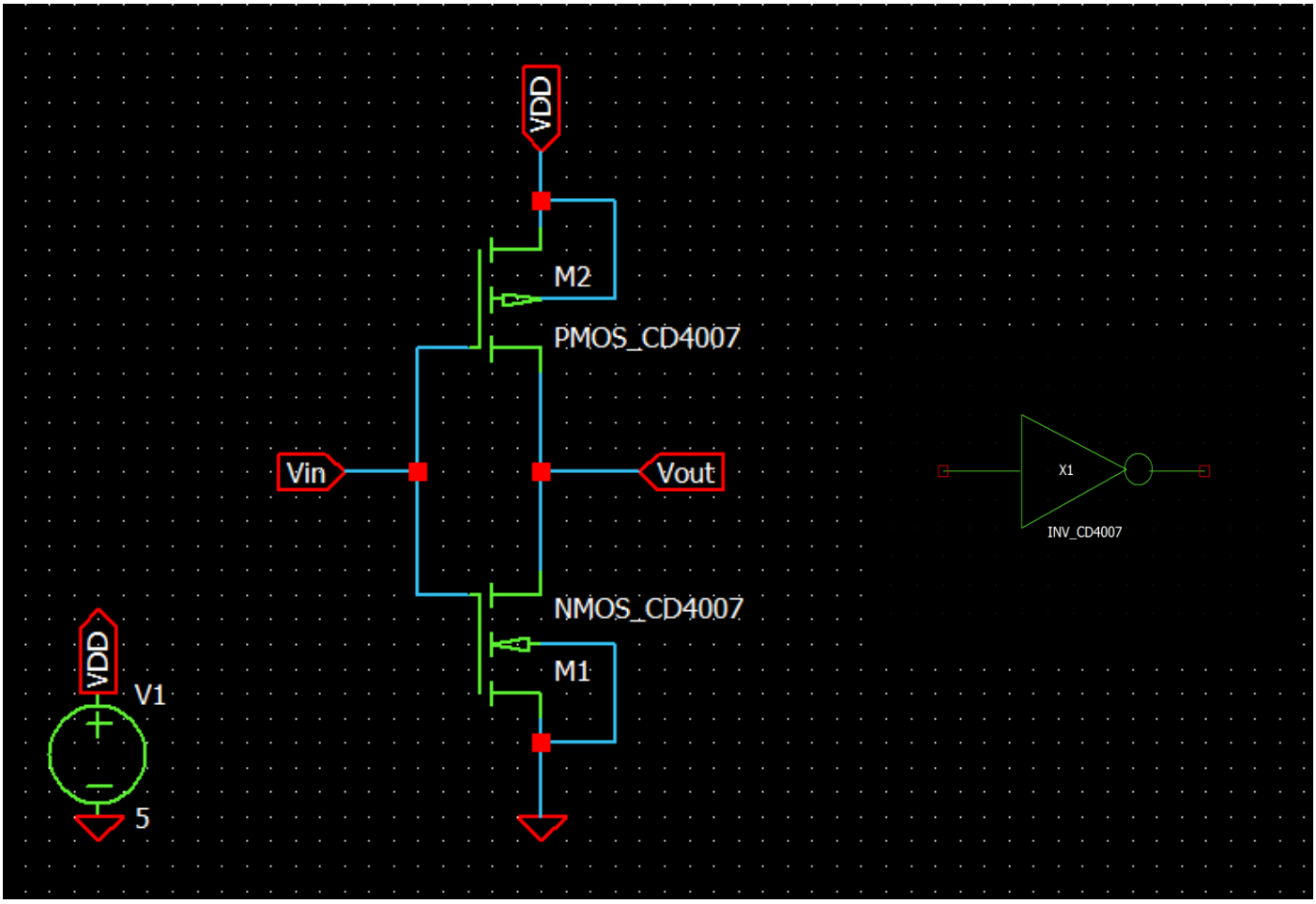
1. **Impact of Load on Output:** After connecting a load, the inverter output becomes distorted even at low frequencies, indicating that the CD4007 IC struggles with higher loads.
2. **Current-Driving Limitations:** The distortion is caused by the limited current-driving capability of the CD4007 IC, making it unsuitable for high-load applications**.**
3. **Capacitive Load Effects**: A capacitive load exceeding 50pF results in increased propagation delay and degraded signal integrity, further impacting the inverter's performance**.**
4. **Recommended Usage:** The CD4007 IC is best suited for low-load, low-frequency applications due to its limitations when driving higher loads**.**

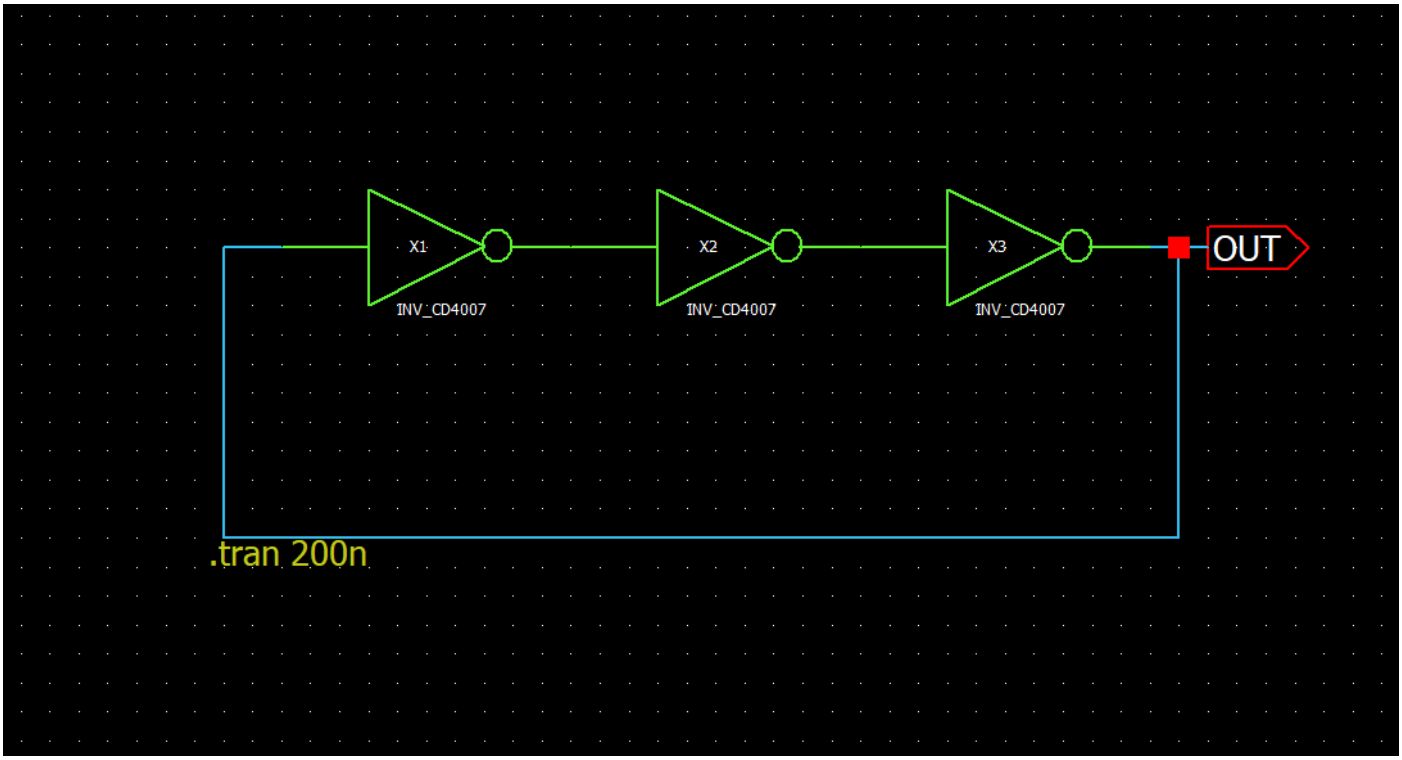


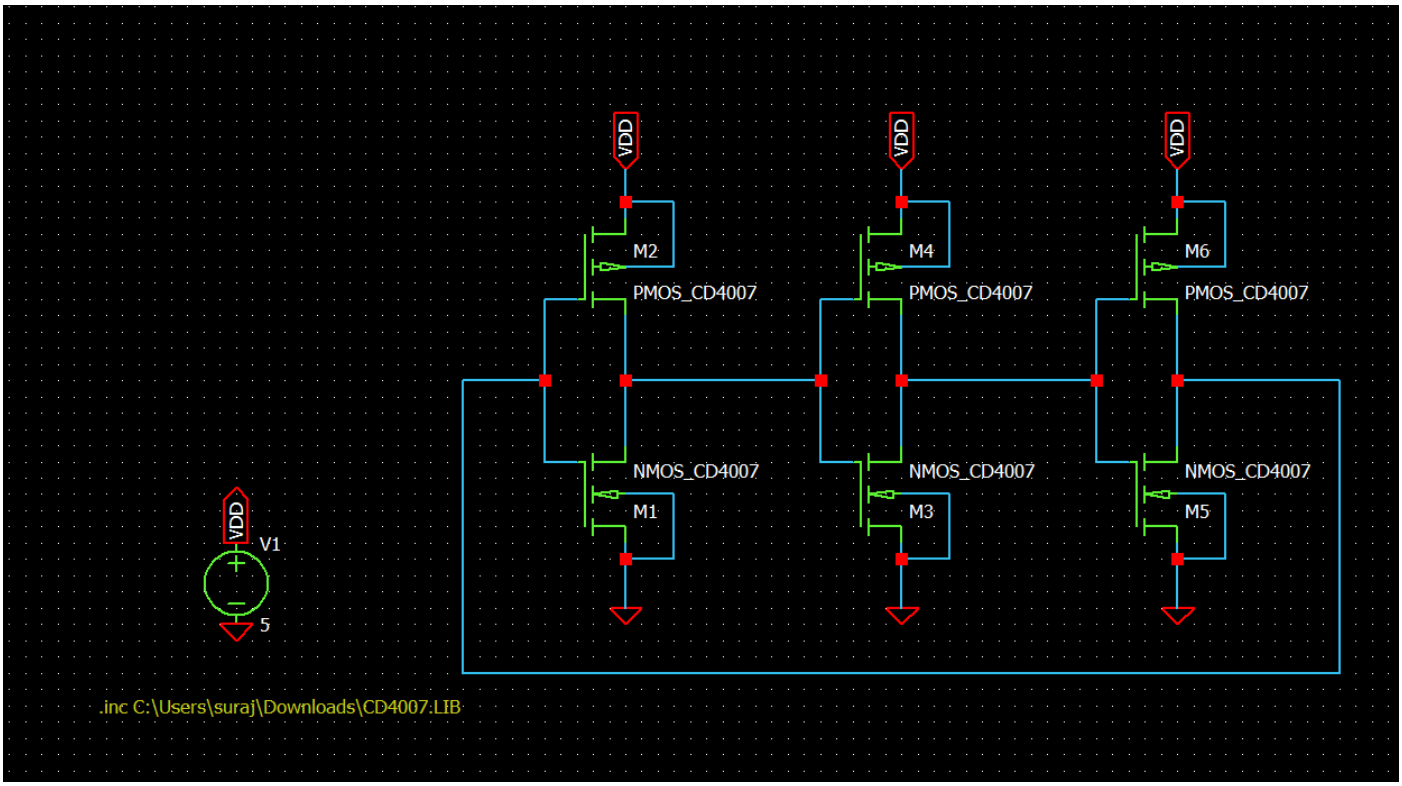


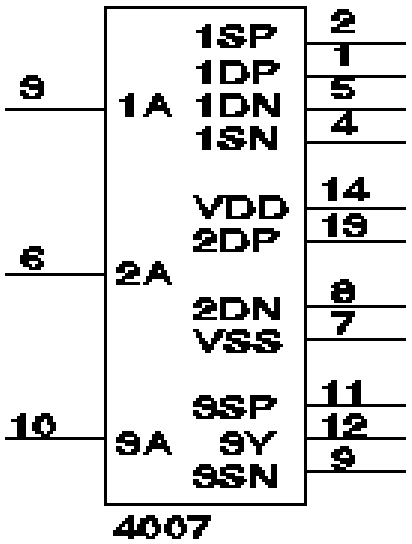


6(b) 3 STAGE RING OSCILLATOR

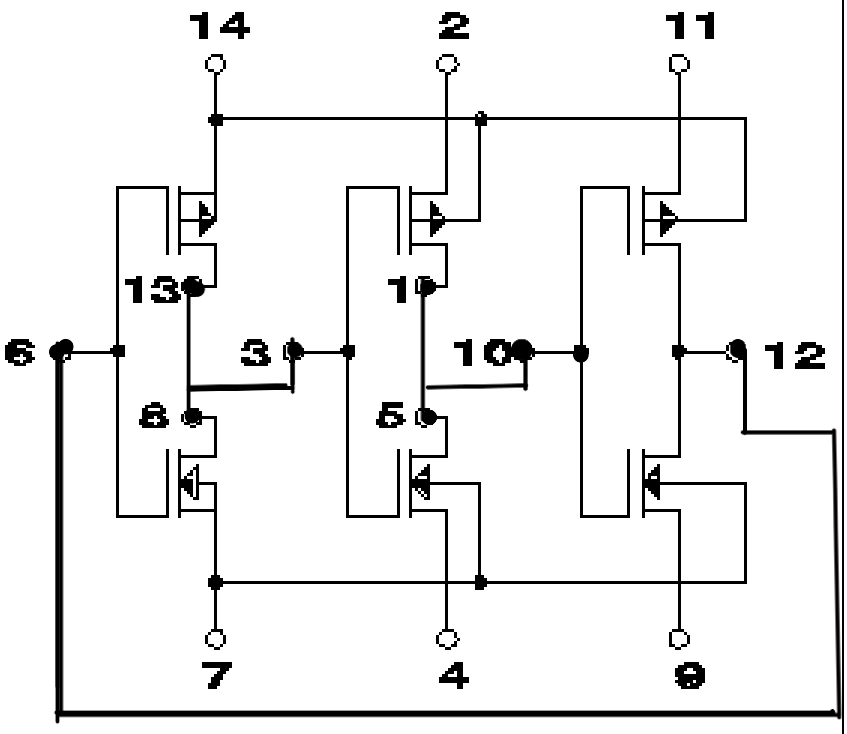




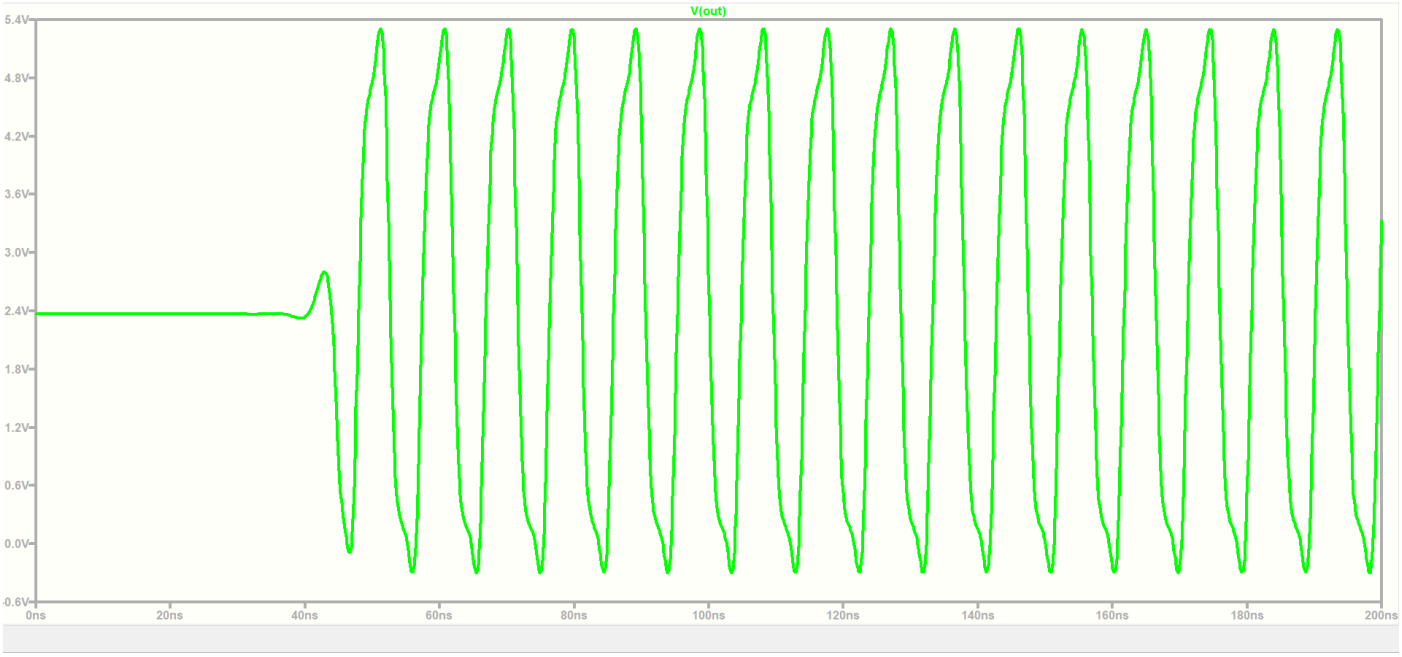




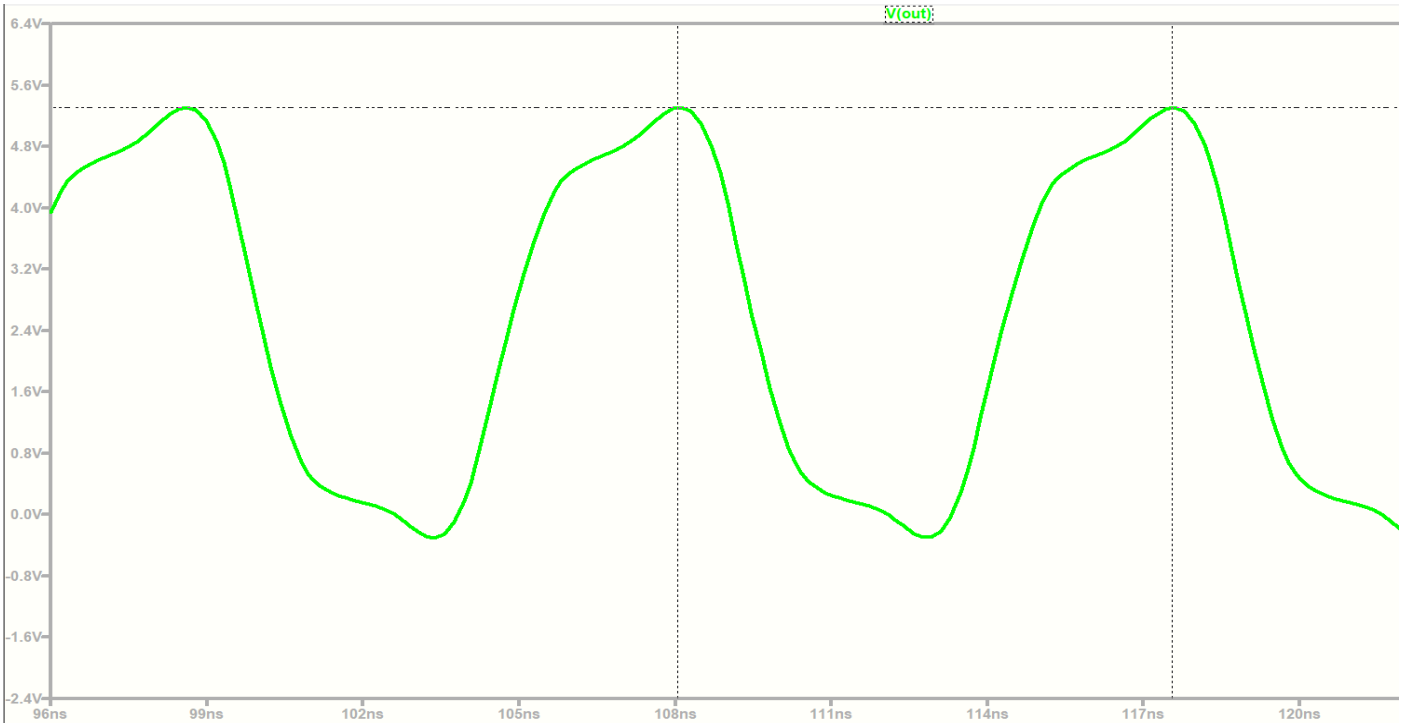
(a) The Connection Diagram

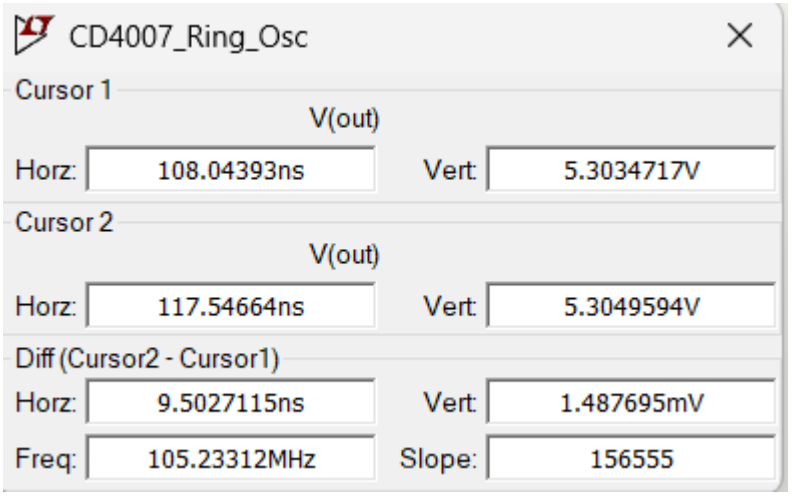


(b) The Schematic Diagram



Frequency of Oscillation





f_{osc} = 105MHz

Conclusions from the Ring Oscillator Experiment:

1. **Oscillation Frequency Discrepancy:**
    - This large difference highlights the impact of non-idealities in real hardware, such as parasitic capacitances, resistances, and device mismatches.
2. **Influence of Parasitic Elements:**
    - Parasitic capacitances from the breadboard, wiring, and measurement instruments increased the overall delay per stage, significantly reducing the oscillation frequency in the experiment compared to the simulation**.**
3. **Measurement Load Effect:**
    - The oscilloscope probe introduced additional capacitance, further loading the circuit and reducing the observed frequency during the experiment.
4. **Experimental Results can be Improved by following ways:**
    - Use a PCB instead of a breadboard to reduce parasitic elements.
    - Employ proper decoupling capacitors and a stable power supply.
    - Include parasitic elements in the simulation for more realistic results.
    - Use low-capacitance measurement probes to minimize loading effects**.**