EXPERIMENT -08

VLSI DESIGN - LAB (EEM 614)

NAME – SURAJ

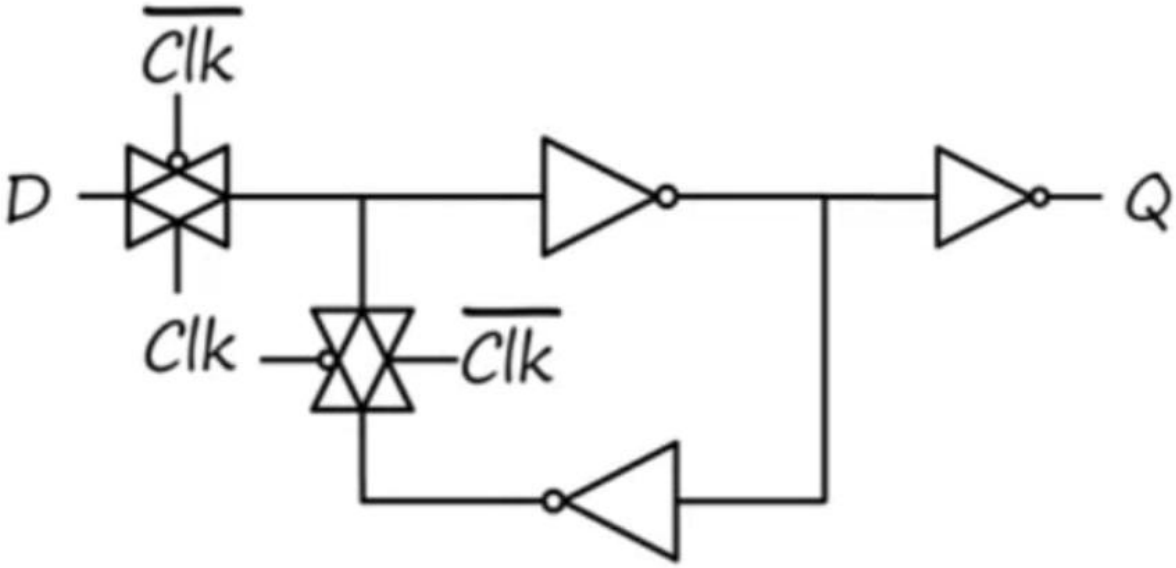
ROLL NO. -2201769

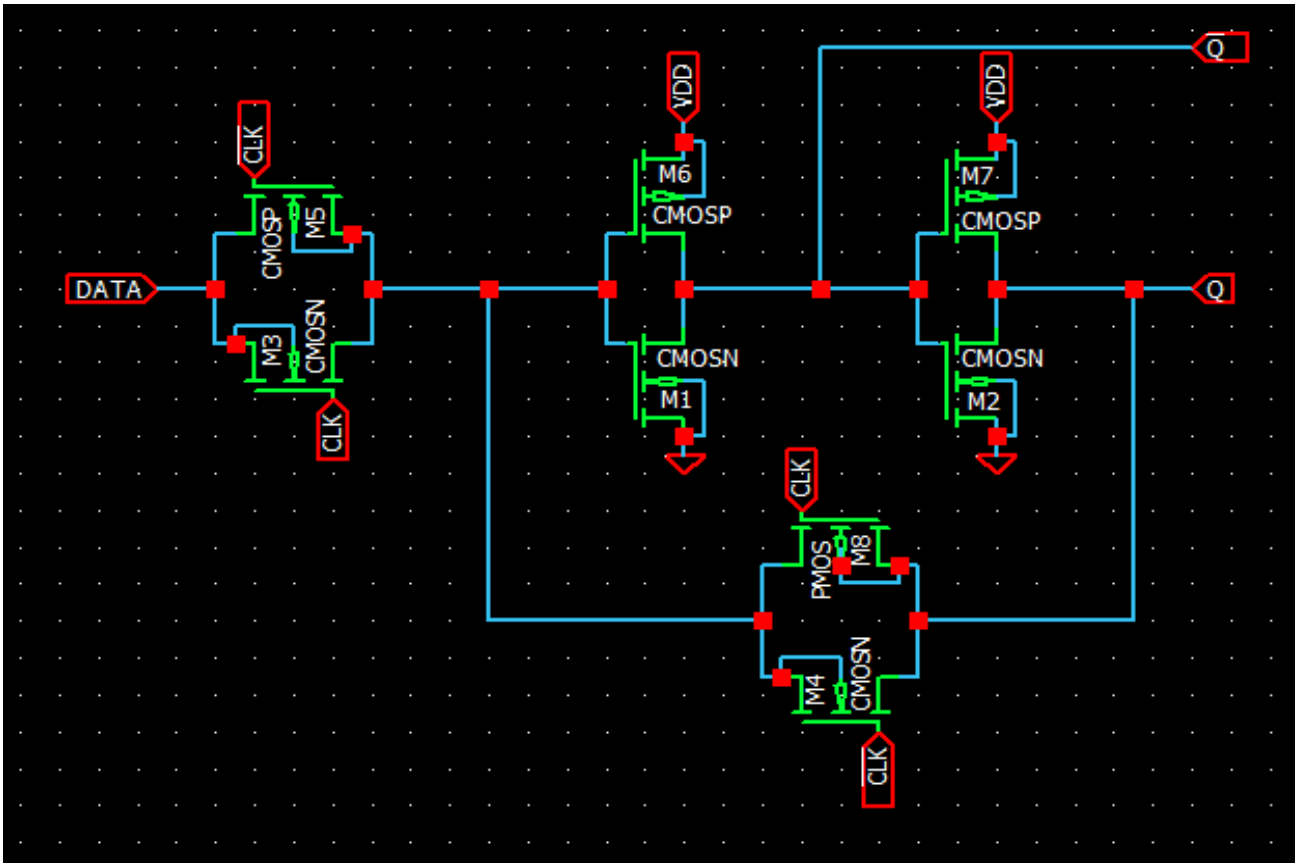
AIM: *Design a one-bit D-latch and positive edge triggered D-FF with CD4007 and 180nm technology node.*

I have Considered the following points while performing simulation for proper generation of output

- *The input signal should not change during this period*
- *The data must remain stable after the clock transition to avoid incorrect latching.*

1. ***D-LATCH***

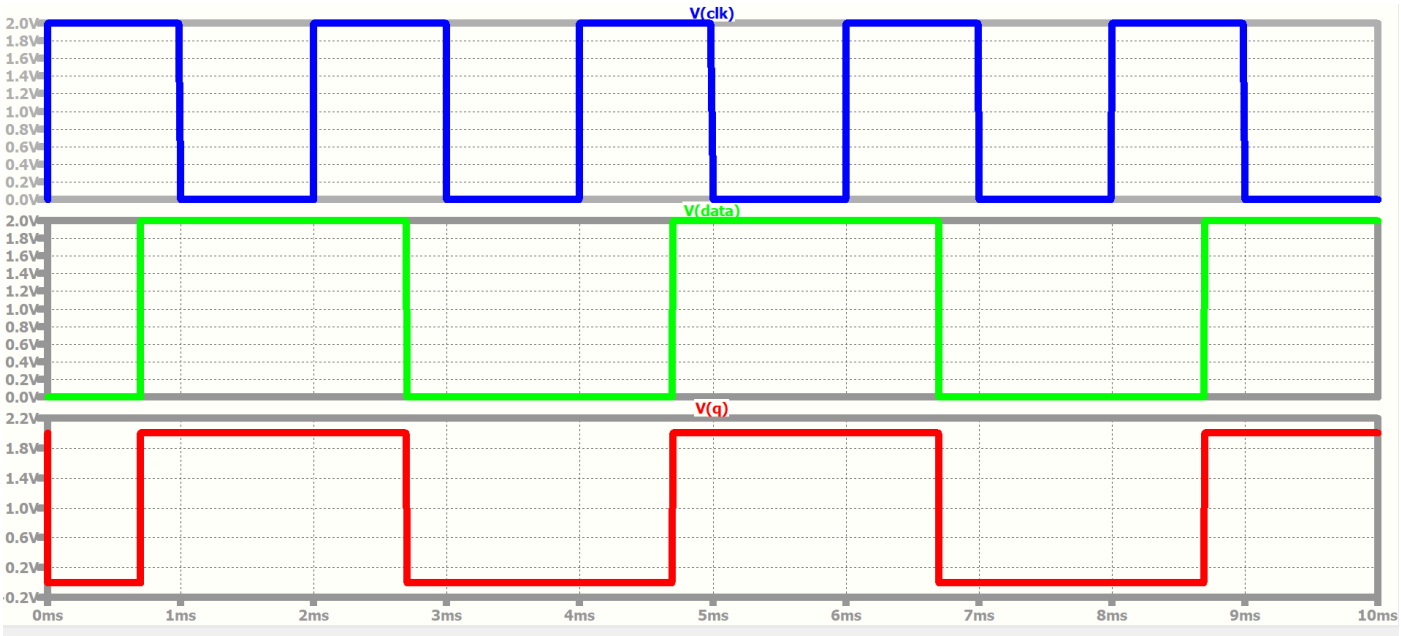




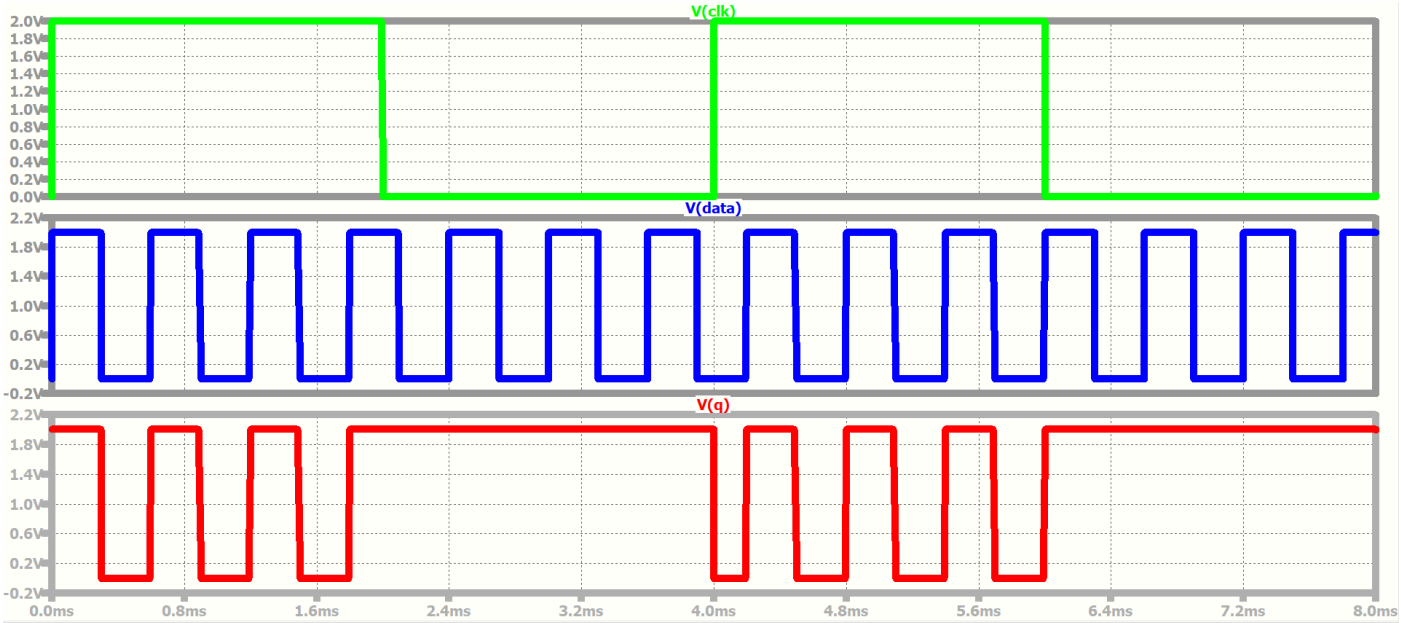
D-LATCH TRUTH TABLE

D	CLK	Q_n	Q_{n+1}	State
X	0	0	0	Hold
X	0	1	1	Hold
0	1	X	0	Reset
1	1	X	1	Set

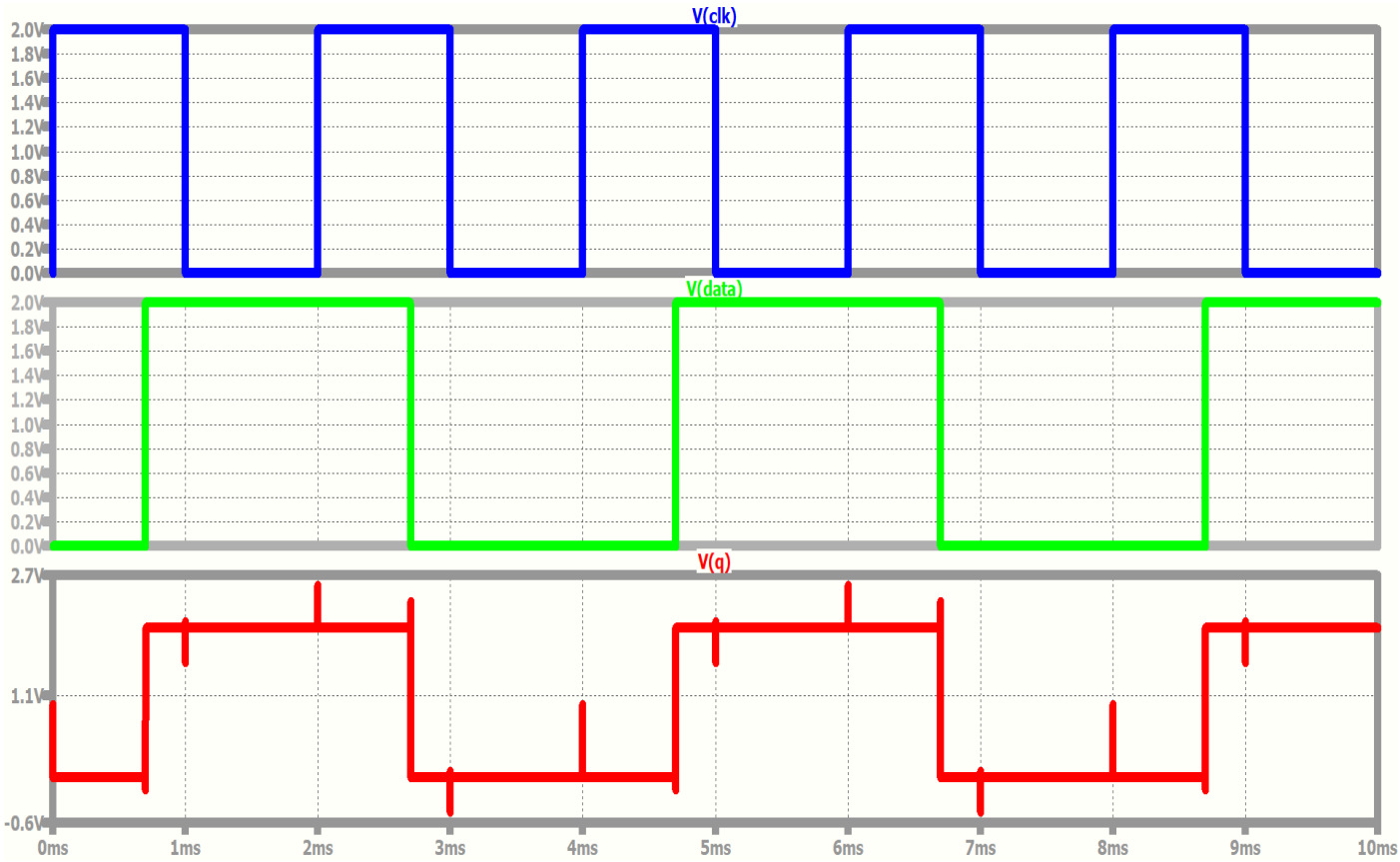
OUTPUT FORM FOR 180nm Technology:



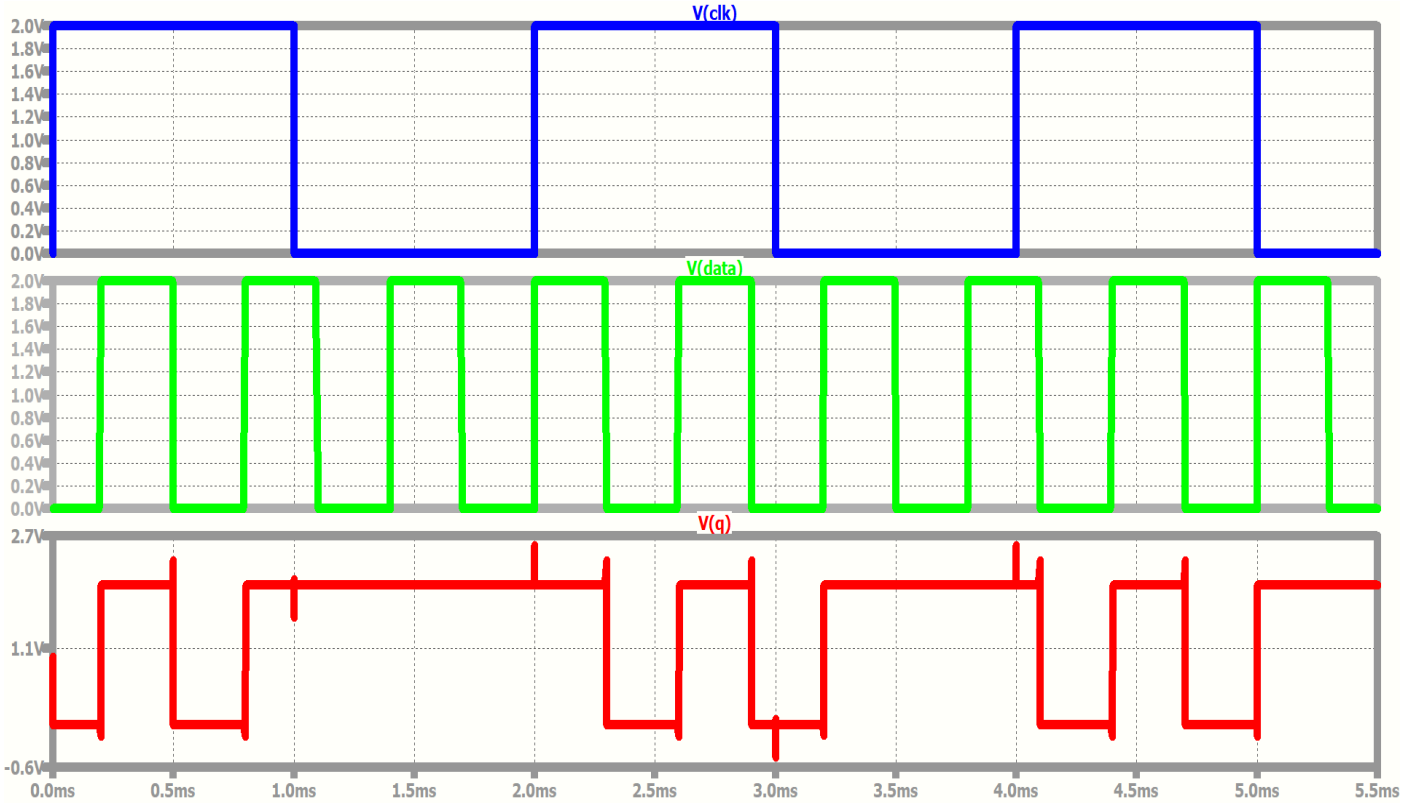
For latched condition



OUTPUT FORM FOR CD4007 Technology:

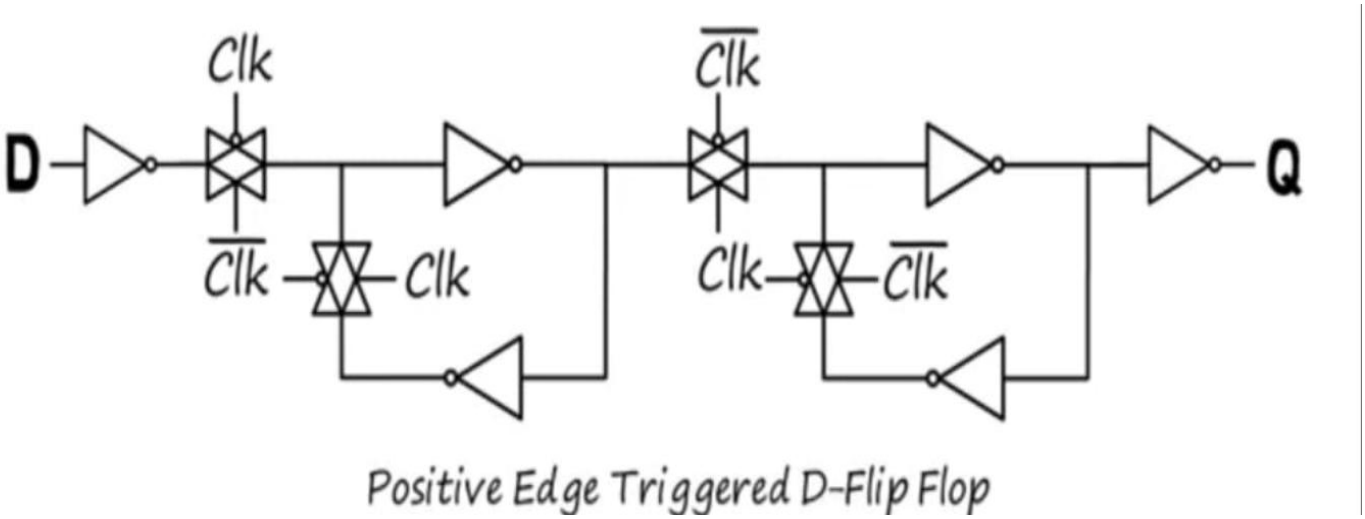


For latched condition



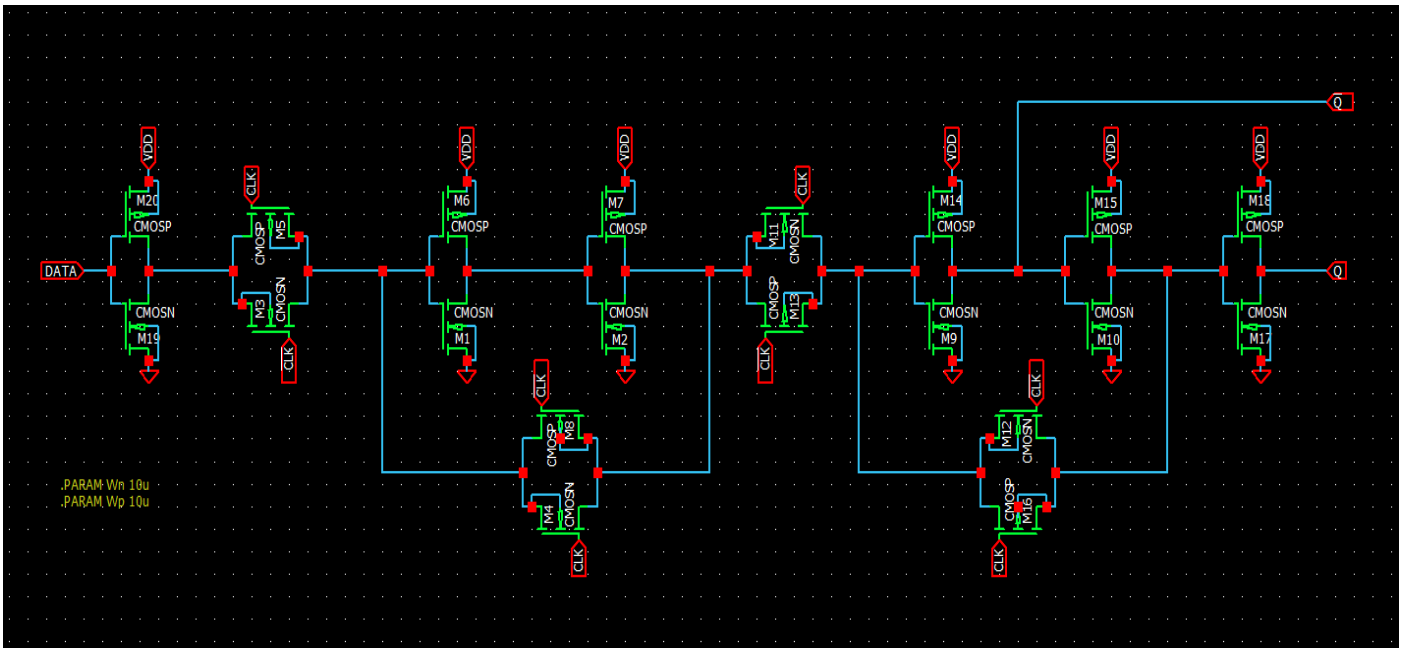
2.D-FLIP FLOP

CIRCUIT DIGRAM



Positive Edge Triggered D-Flip Flop

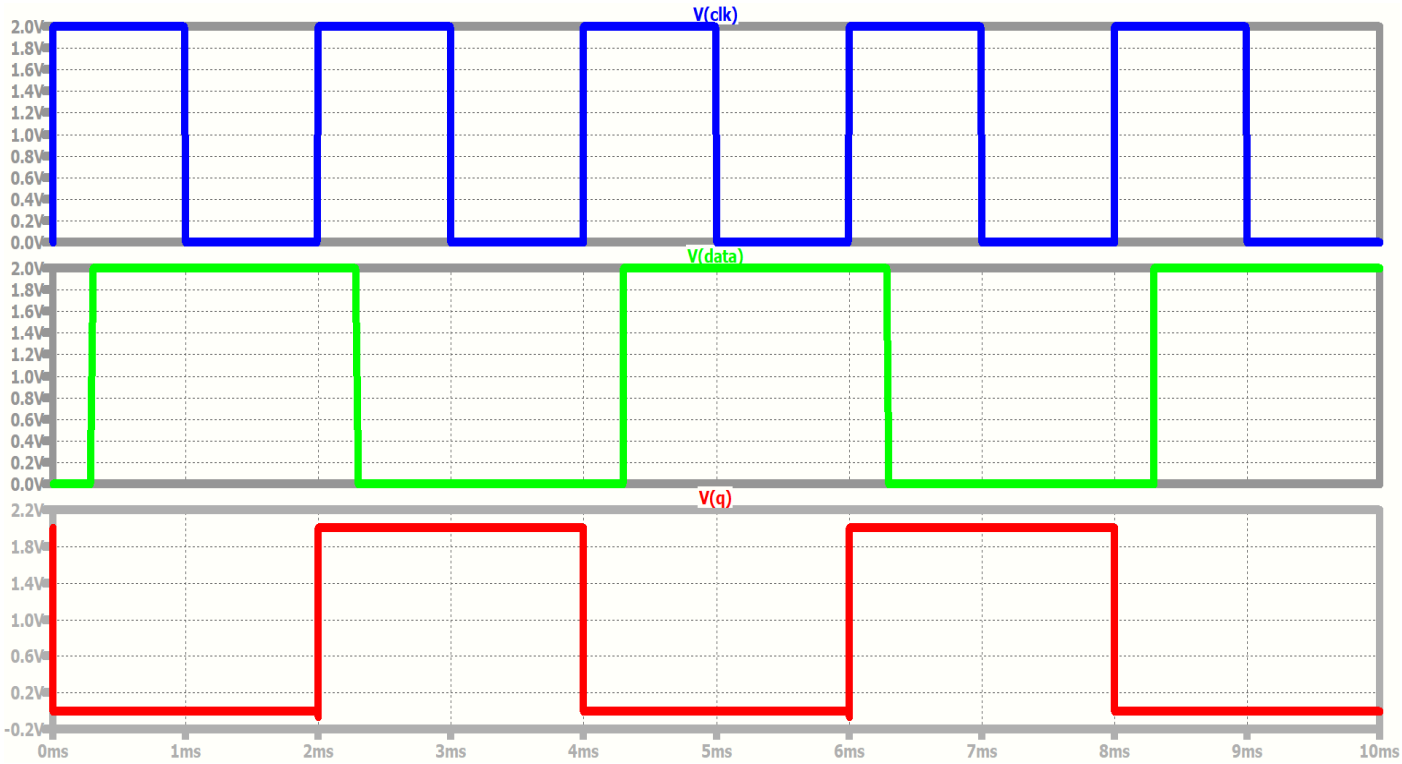
SCHEMATIC DIAGRAM



D-LATCH TRUTH TABLE

Clock (CLK)	Data Input (D)	Previous Output (Q^n)	Next Output (Q^{n+1})	State
↑ (Positive Edge)	0	X	0	Reset
↑ (Positive Edge)	1	X	1	Set
0 or ↓ (Negative Edge)	X	Q^n	Q^n	Hold
↑ (Positive Edge)	X	Q^n	Q^n	Hold

OUTPUT FOR 180nm technology node



OUTPUT FOR CD4007 technology node