EXPERIMENT -03

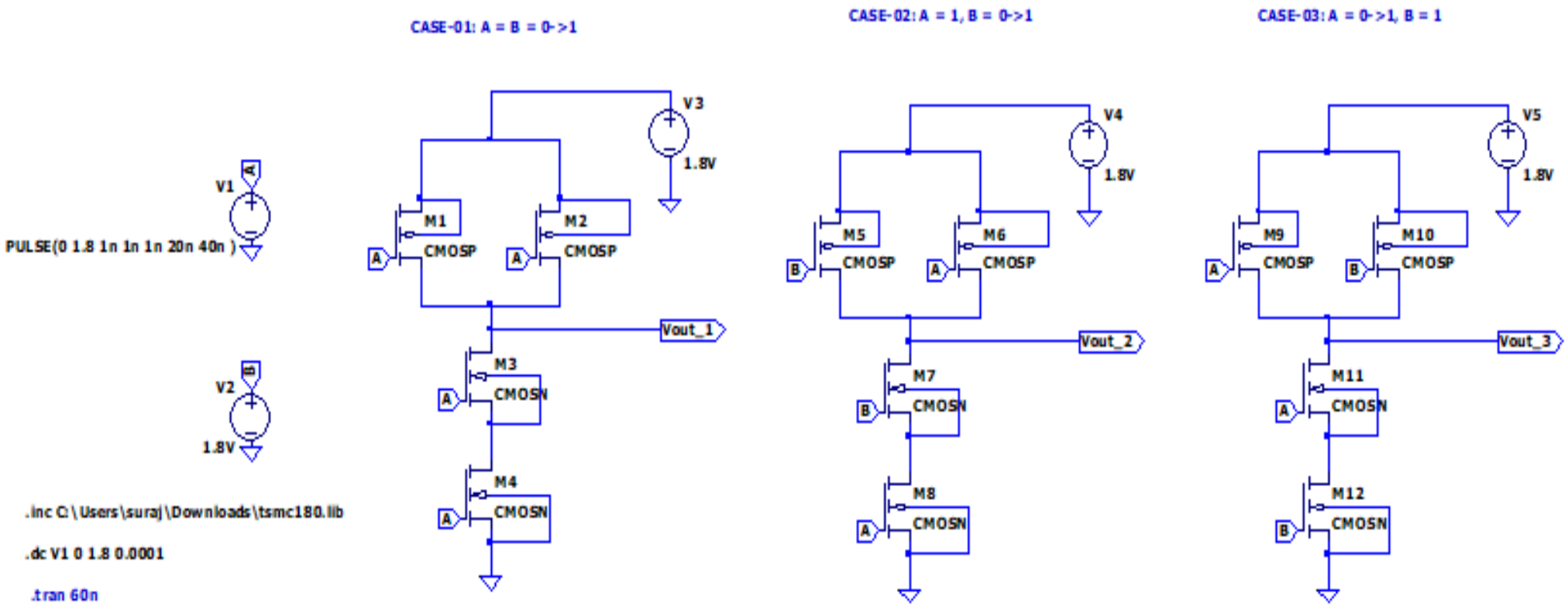
VLSI DESIGN - LAB (EEM 614)

NAME – SURAJ

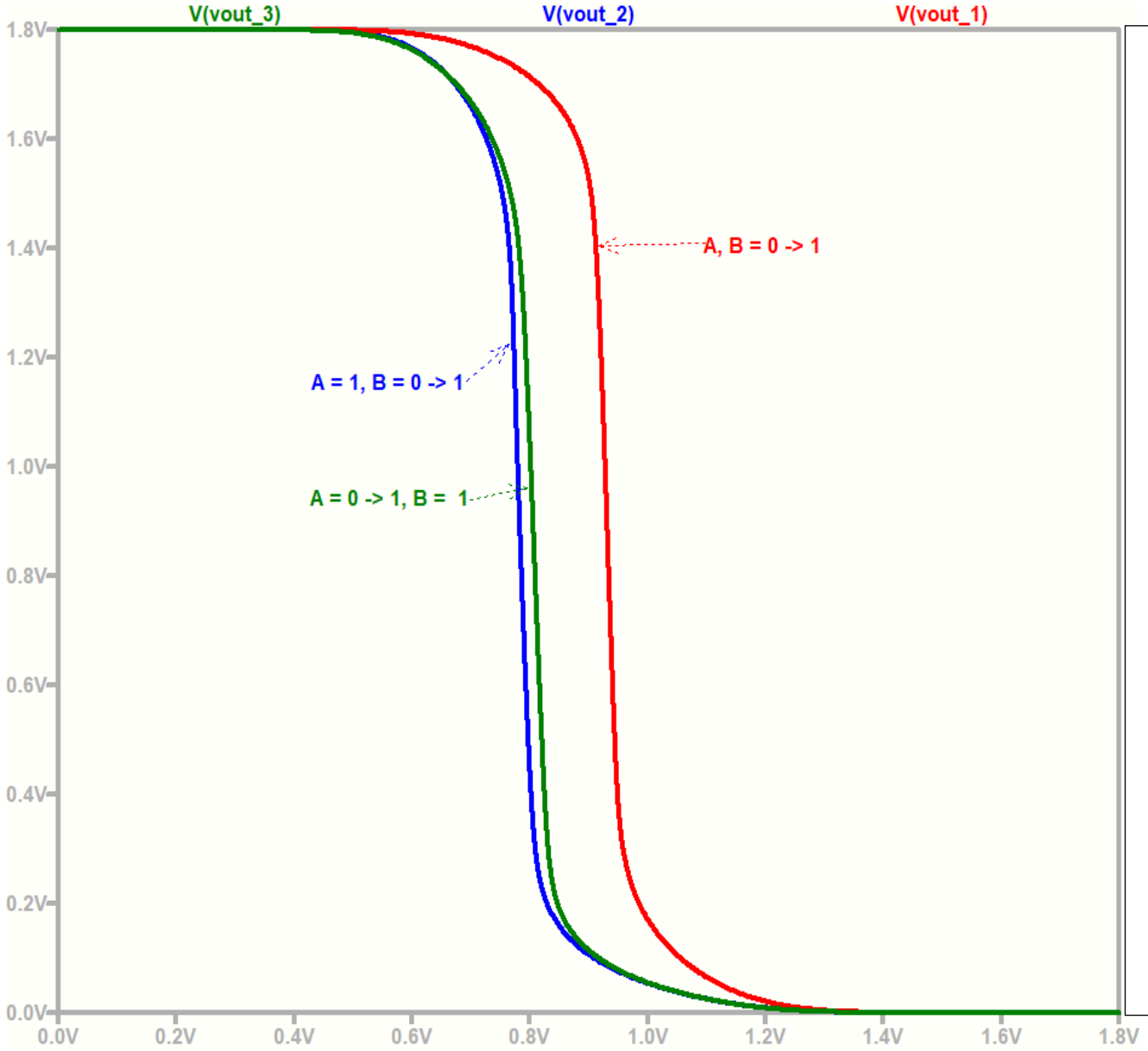
ROLL NO. -2201769

STATIC ANALYSIS OF NAND GATE:

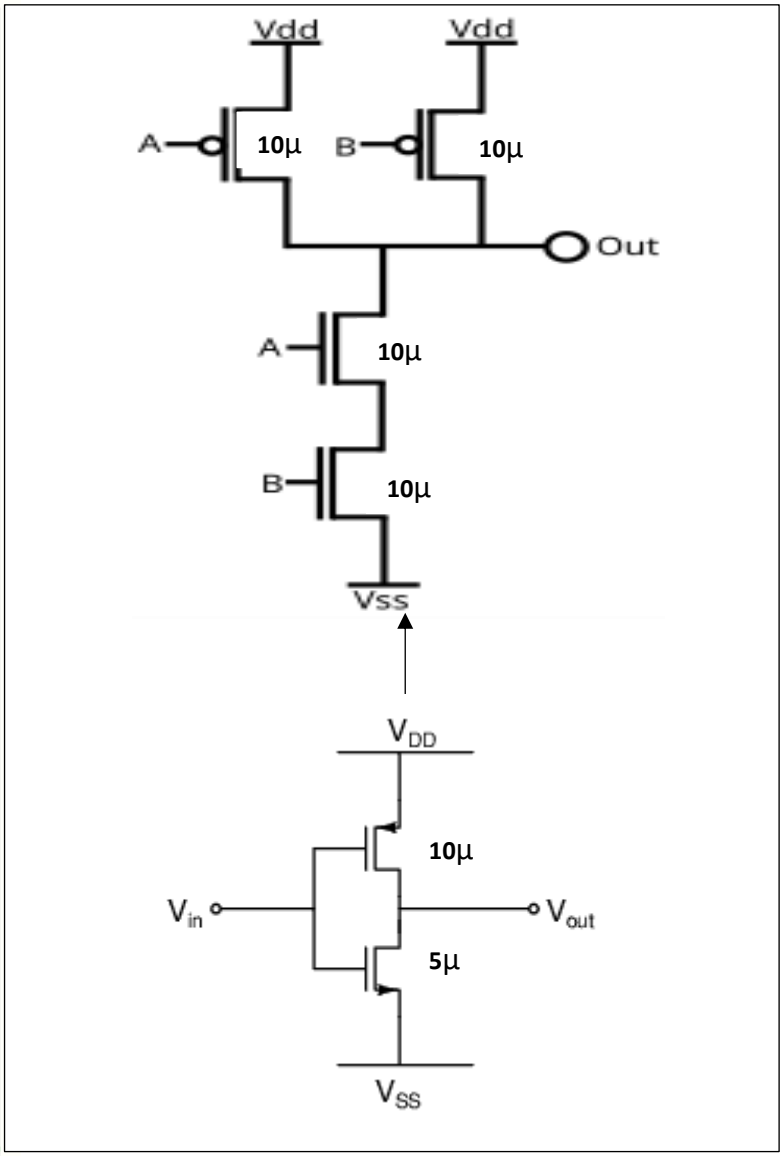
1.CIRCUIT DIAGRAM



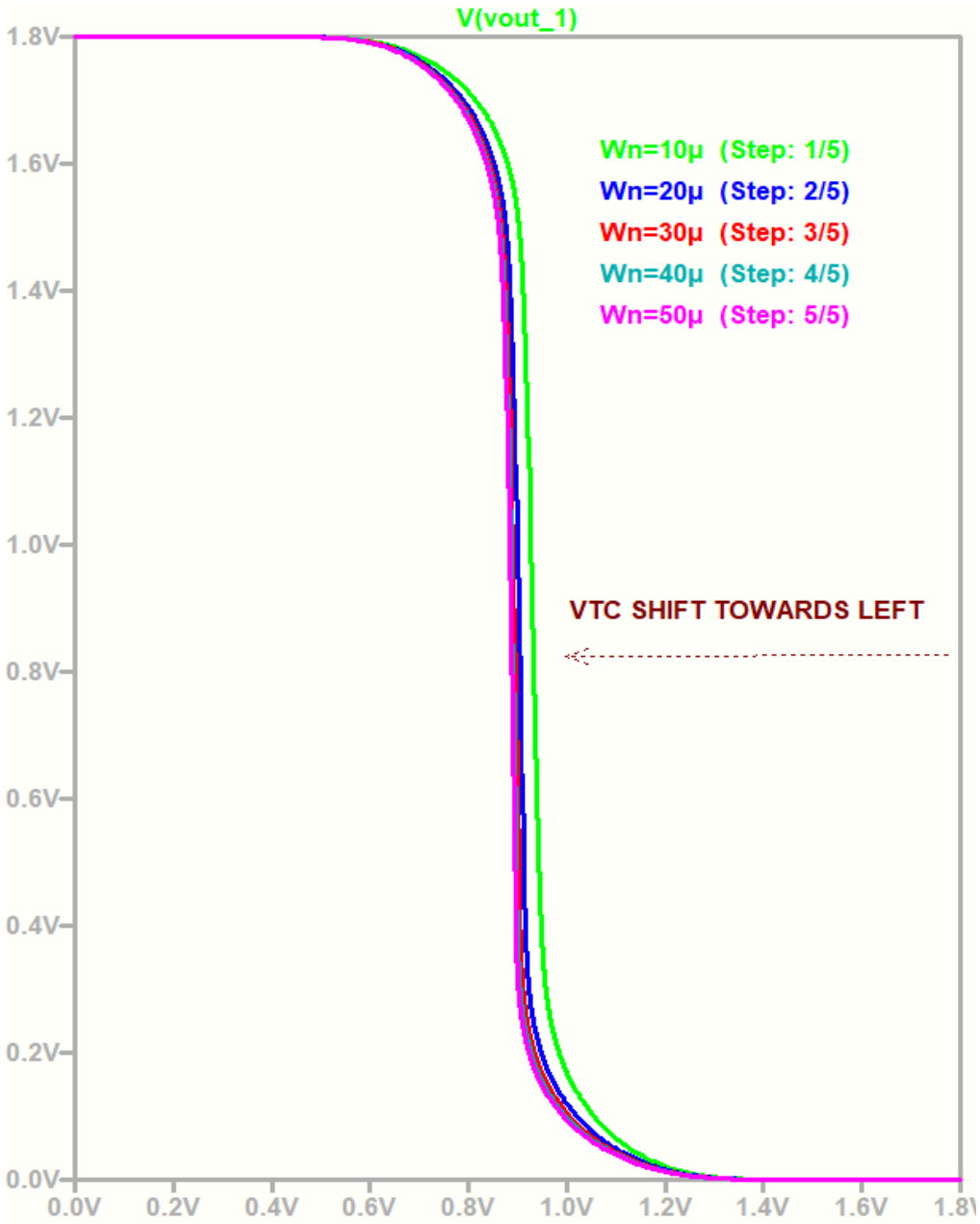
2.STATIC CHARACTERISTICS OF NAND GATE



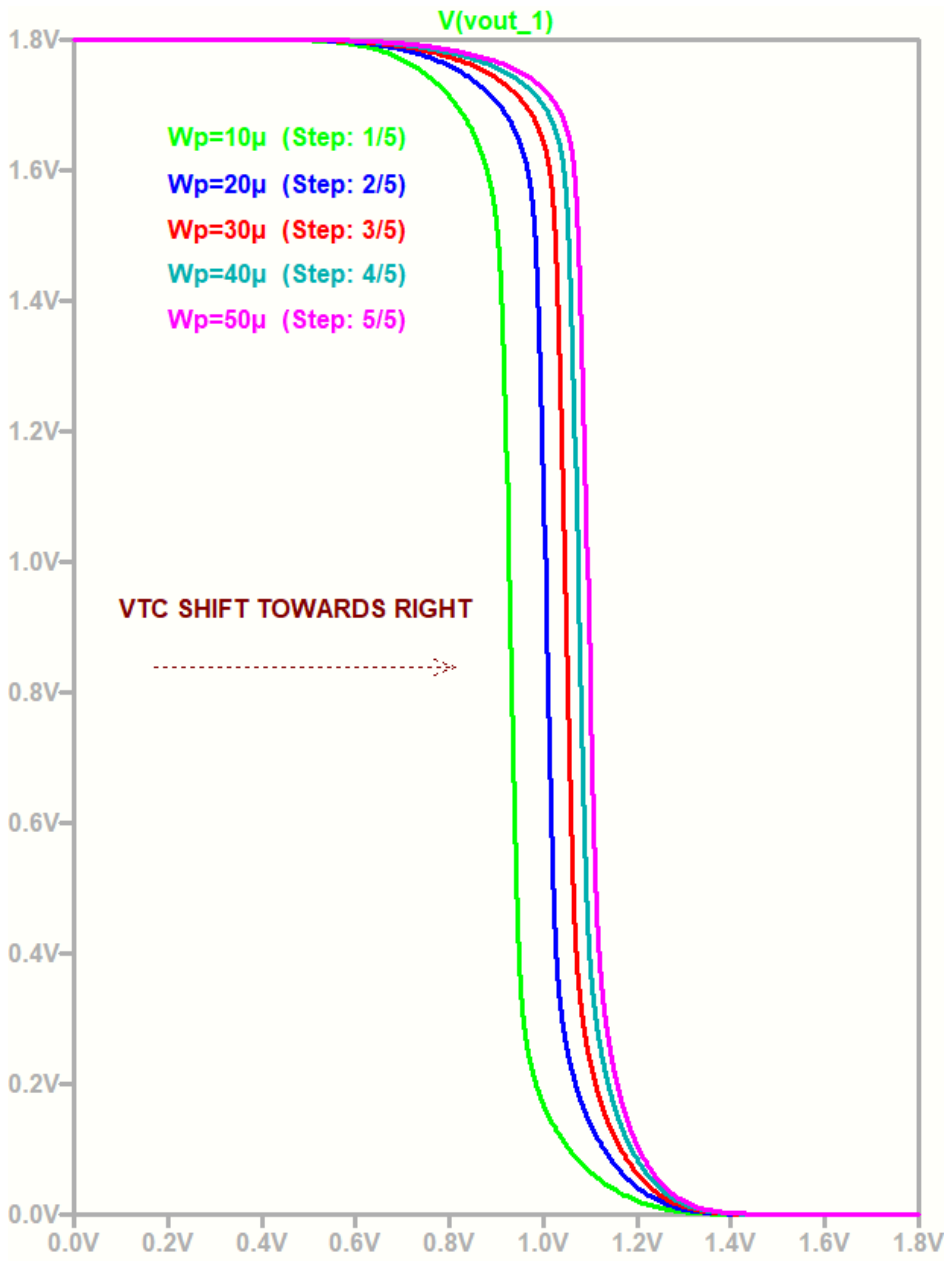
3. TRANSISTOR SIZING



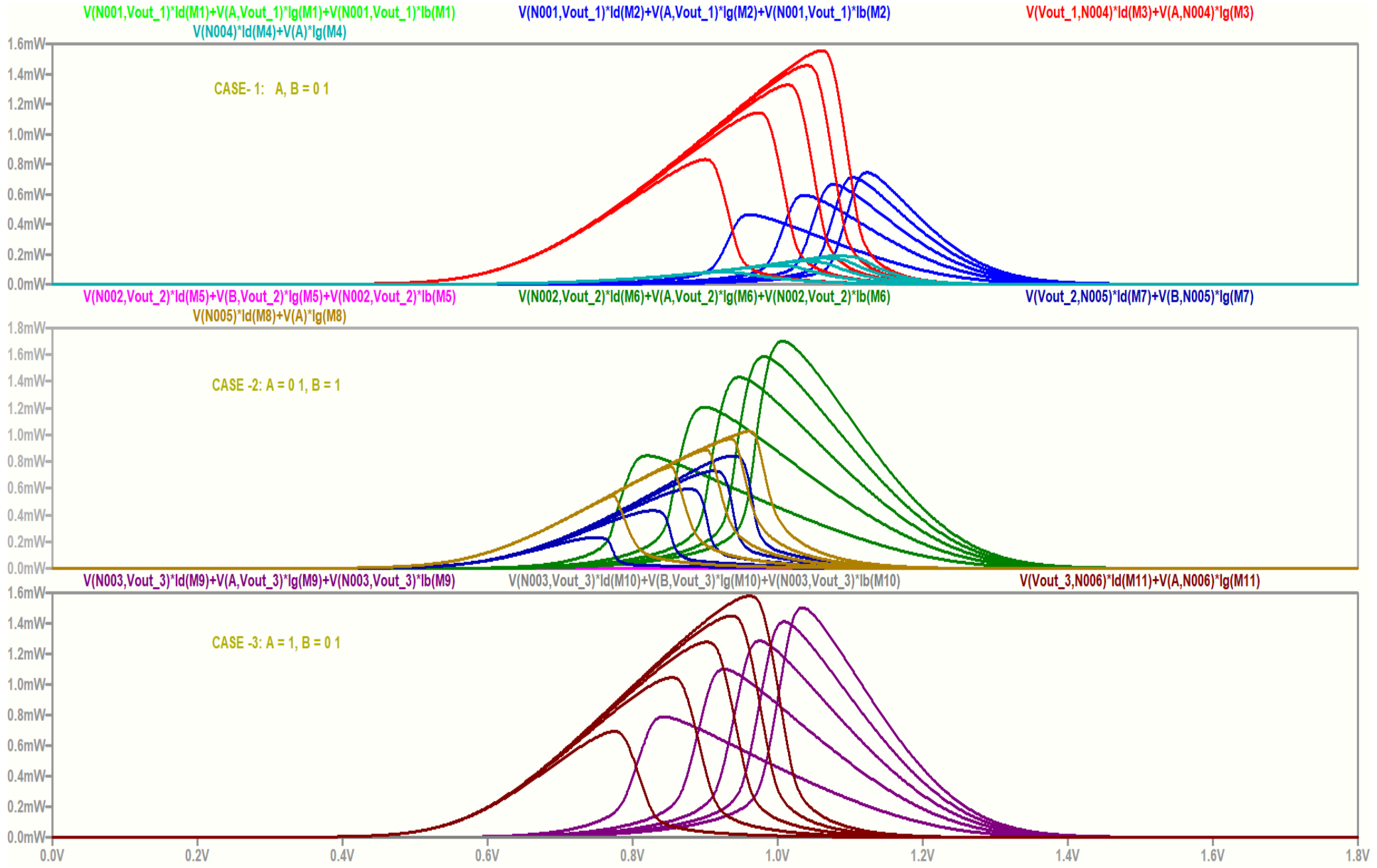
4.EFFECT OF INCREASING W_N



5. EFFECT OF INCREASING W_P



6.STATIC POWER DISSIPATION



CASE- 1: A, B = 0 →1

Sr.No.	Wp (µm)	Vth (V)	V_{IL}	V_{OH}	V_{IH}	V_{OL}	NML	NMH	Power
1.	10	0.930	0.820	1.8	1.049	0.000	0.820	0.751	5.22868e-05
2.	20	1.005	0.915	1.8	1.141	0.000	0.915	0.659	7.02919e-05
3.	30	1.045	0.966	1.8	1.189	0.000	0.966	0.611	8.10883e-05
4.	40	1.072	0.999	1.8	1.200	0.000	0.999	0.600	8.8677e-05
5.	50	1.091	1.022	1.8	1.234	0.000	1.022	0.566	9.44766e-05

CASE -2: A = 0 →1, B = 1

Sr.No.	Wp (µm)	Vth (V)	V_{IL}	V_{OH}	V_{IH}	V_{OL}	NML	NMH	Power
1.	10	0.78689	0.648307	1.8	0.875	0.000	0.648307	0.925	4.6774e-05
2.	20	0.864425	0.738999	1.8	0.987	0.000	0.738999	0.813	7.03846e-05
3.	30	0.91259	0.802007	1.8	1.037	0.000	0.802007	0.763	8.63353e-05
4.	40	0.94676	0.846507	1.8	1.095	0.000	0.846507	0.704	9.82141e-05
5.	50	0.972766	0.879899	1.8	1.124	0.000	0.879899	0.676	0.000107581

CASE -3: A = 1, B = 0 →1

Sr.No.	Wp (µm)	Vth (V)	V_{IL}	V_{OH}	V_{IH}	V_{OL}	NML	NMH	Power
1.	10	0.809076	0.659107	1.8	0.894	0.000	0.659107	0.906	4.57163e-05
2.	20	0.891012	0.763507	1.8	1.000	0.000	0.763507	0.800	6.72599e-05
3.	30	0.940116	0.829207	1.8	1.071	0.000	0.829207	0.729	8.13231e-05
4.	40	0.97412	0.873807	1.8	1.113	0.000	0.873807	0.687	9.15743e-05
5.	50	0.999562	0.906599	1.8	1.145	0.000	0.906599	0.655	10.0100e-05

CASE- 1: A, B = 0 →1

Sr.No.	Wn (µm)	Vth (V)	V_{IL}	V_{OH}	V_{IH}	V_{OL}	NML	NMH	Power
1.	10	0.930388	0.820299	1.8	1.049	0.000	0.820299	0.751	5.22868e-05
2.	20	0.902818	0.788907	1.8	1.006	0.000	0.788907	0.794	5.82543e-05
3.	30	0.893655	0.778907	1.8	0.993	0.000	0.778907	0.807	6.03048e-05
4.	40	0.889267	0.774199	1.8	0.986	0.000	0.774199	0.814	6.13144e-05
5.	50	0.886708	0.771309	1.8	0.975	0.000	0.771309	0.825	6.19173e-05

CASE -2: A = 0 →1, B = 1

Sr.No.	Wn (µm)	Vth (V)	V_{IL}	V_{OH}	V_{IH}	V_{OL}	NML	NMH	Power
1.	10	0.78689	0.648307	1.8	0.874	0.000	0.78689	0.926	4.6774e-05
2.	20	0.721662	0.588099	1.8	0.791	0.000	0.721662	1.009	5.7831e-05
3.	30	0.688972	0.560899	1.8	0.749	0.000	0.688972	1.051	6.40474e-05
4.	40	0.668049	0.543699	1.8	0.724	0.000	0.668049	1.076	6.83245e-05
5.	50	0.652979	0.531209	1.8	0.705	0.000	0.652979	1.095	7.15703e-05

CASE -3: A = 1, B = 0 →1

Sr.No.	Wn (µm)	Vth (V)	V_{IL}	V_{OH}	V_{IH}	V_{OL}	NML	NMH	Power
1.	10	0.809076	0.659107	1.8	0.895	0.000	0.809076	0.905	4.57163e-05
2.	20	0.737749	0.587299	1.8	0.807	0.000	0.737749	0.993	5.74917e-05
3.	30	0.701576	0.556599	1.8	0.762	0.000	0.701576	1.038	6.41297e-05
4.	40	0.67844	0.537909	1.8	0.735	0.000	0.67844	1.065	6.86782e-05
5.	50	0.66184	0.524699	1.8	0.715	0.000	0.66184	1.085	7.21128e-05

CONCLUSION

1.Effect of Increasing Wp:

- *Vth increases with Wp across all cases, indicating higher threshold voltage for PMOS.*
- *NML increases and NMH decreases with Wp, showing an asymmetry in noise margins.*
- *Power consumption increases with Wp due to higher drive strength.*

2.Effect of Increasing Wn:

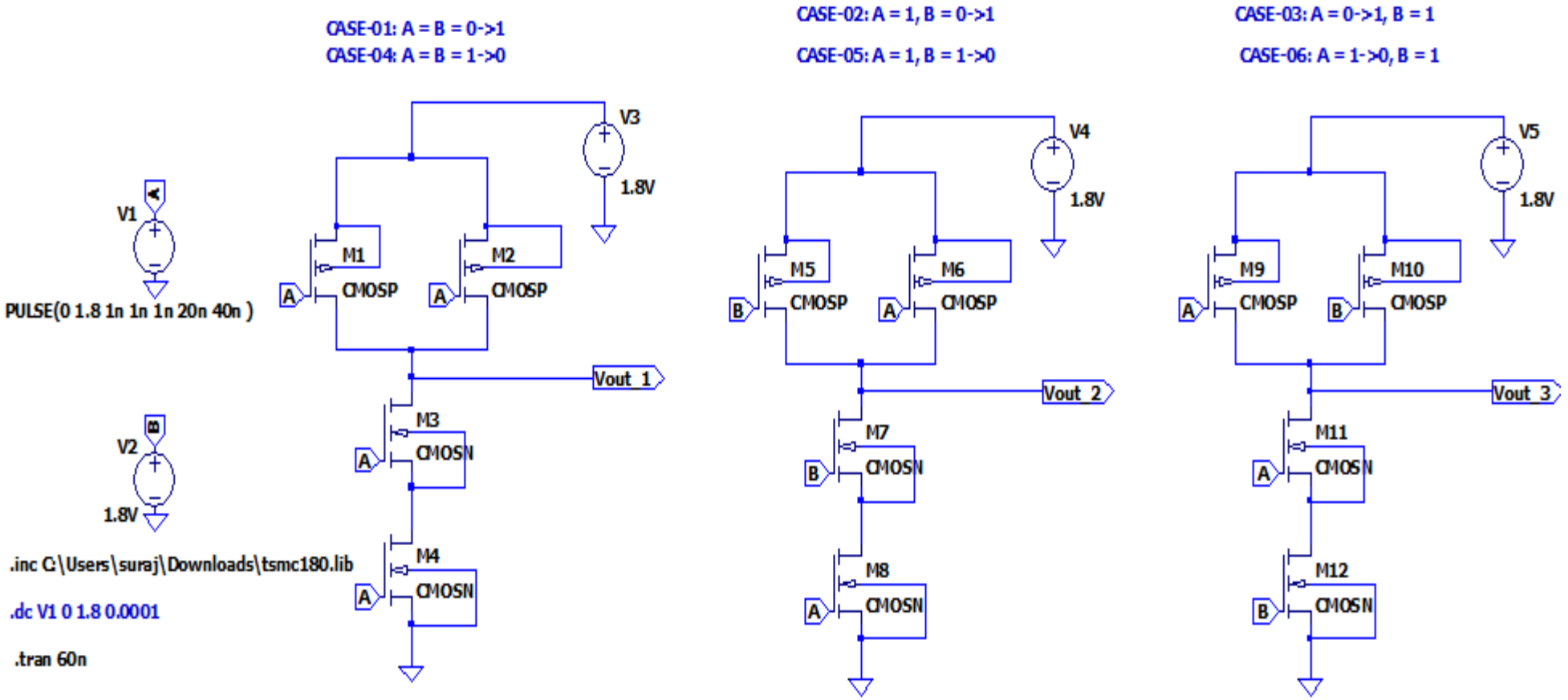
- *Vth decreases with Wn across all cases, indicating a reduced threshold voltage for NMOS.*
- *NML decreases, and NMH increases with Wn, improving high-state noise margins but reducing low-state margins.*
- *Power consumption increases with Wn due to higher current drive capabilities.*

3.General Observations:

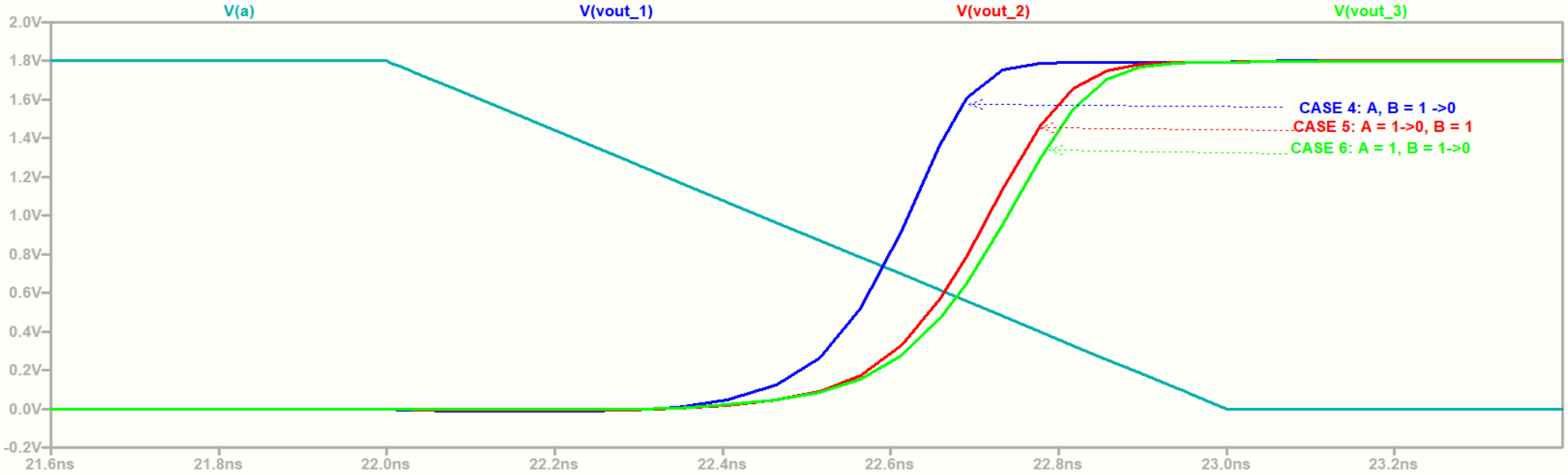
- *Optimal values of Wp and Wn are needed to balance noise margins, power, and switching thresholds.*
- *Larger transistors (Wp or Wn) lead to higher power consumption due to increased leakage and switching currents.*

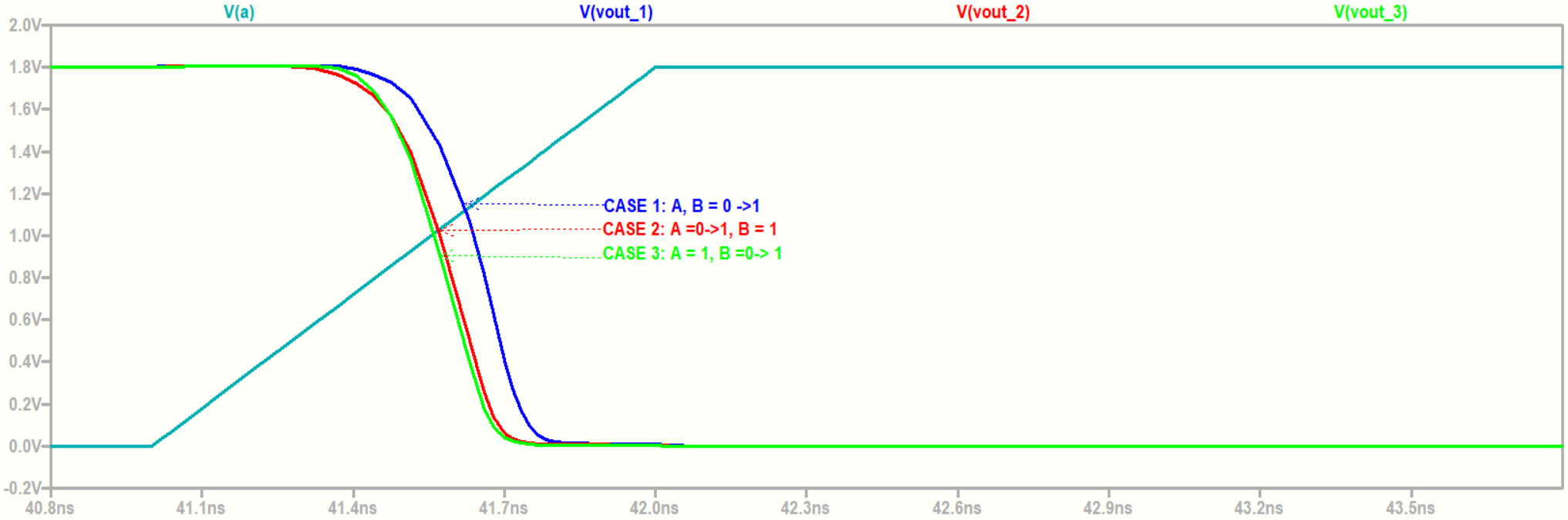
DYNAMIC ANALYSIS OF NAND GATE:

1.CIRCUIT DIAGRAM

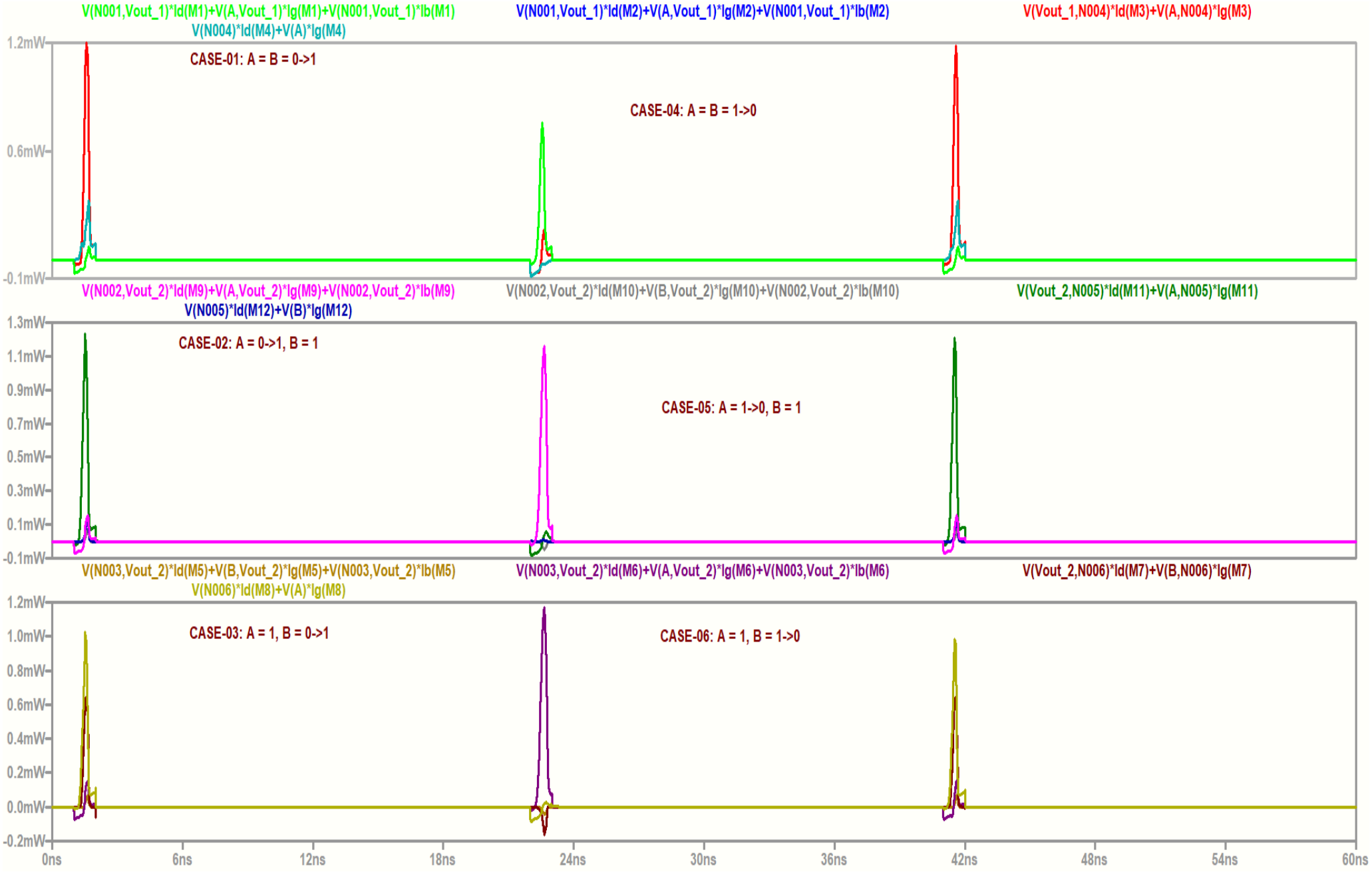


2.TRANSIENT CHARACTERISTICS OF NAND GATE





3.DYNAMIC POWER DISSIPATION



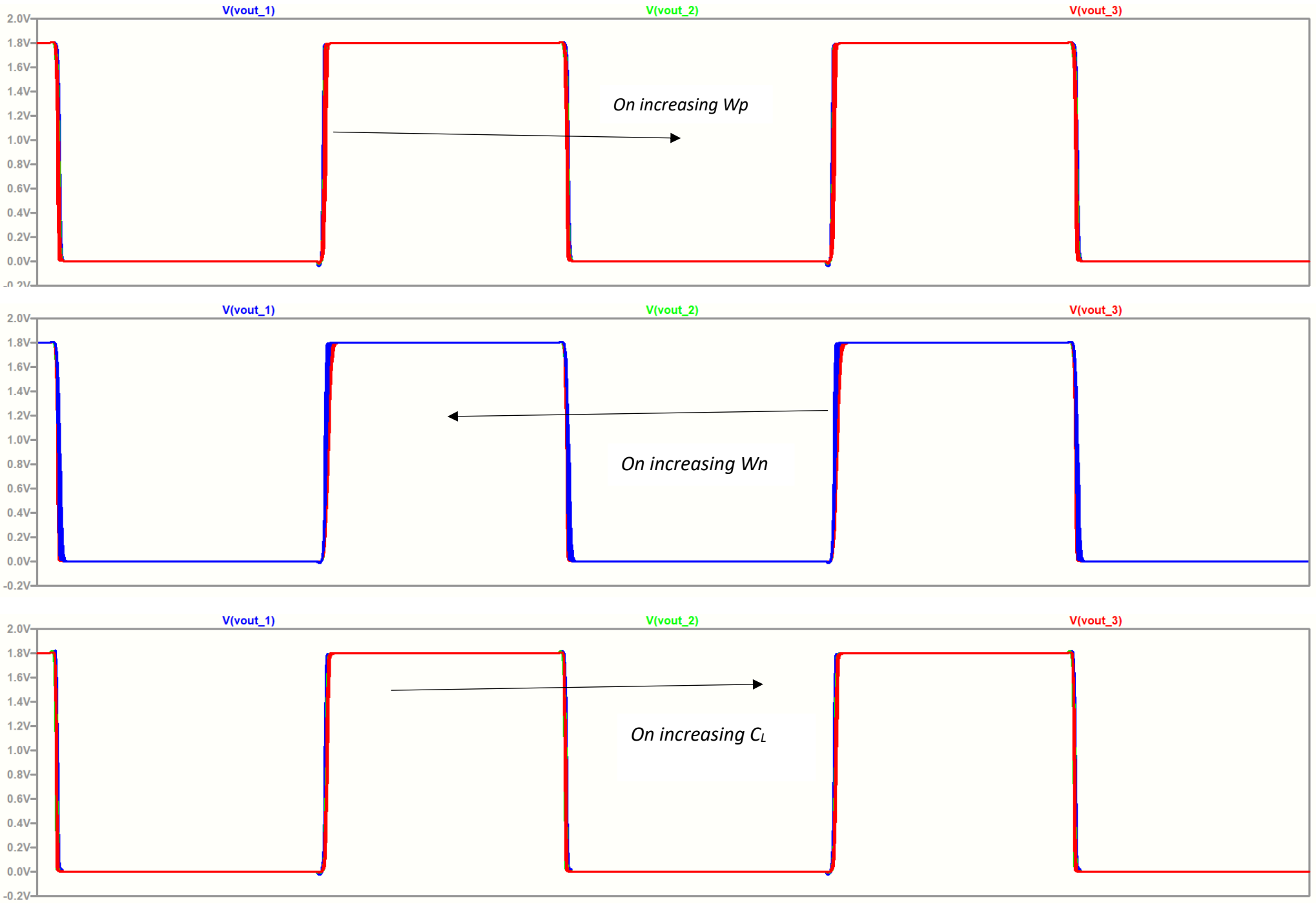
RESULT

1. FOR 180nm TECHNOLOGY

Sr.No.	TEST VECTOR	DELAY (ps)	POWER (mW)
1.	A = B = 0→1	151	1.18
2.	A = 0→1, B=1	86	1.23
3.	A=1, B = 0→1	75	1.01
4.	A = B = 1→0	101	0.789
5.	A = 1→0, B = 1	204	0.062
6.	A = 1, B = 1→0	225	0.058

2. GIVEN FOR 250nm TECHNOLOGY

Input Data Pattern	Delay (psec)
A=B=0→1	69
A=1, B=0→1	62
A= 0→1, B=1	50
A=B=1→0	35
A=1, B=1→0	76
A= 1→0, B=1	57


V(vout_1)
V(vout_2)
V(vout_3)
2.0V
1.8V
1.6V
1.4V
1.2V
1.0V
0.8V
0.6V
0.4V
0.2V
0.0V
-0.2V
On increasing Wp
V(vout_1)
V(vout_2)
V(vout_3)
2.0V
1.8V
1.6V
1.4V
1.2V
1.0V
0.8V
0.6V
0.4V
0.2V
0.0V
-0.2V
On increasing Wn
V(vout_1)
V(vout_2)
V(vout_3)
2.0V
1.8V
1.6V
1.4V
1.2V
1.0V
0.8V
0.6V
0.4V
0.2V
0.0V
-0.2V
On increasing C_L

1.EFFECT OF INCREASING W_P ON DELAY

Wp (µm)	A = B = 0->1	A = 0->1, B = 1	A = 1, B = 0->1	A = B = 1->0	A = 1->0, B = 1	A = 1, B = 1->0
10	1.5106e-10	0.85931e-10	0.754651e-10	1.10465e-10	2.04098e-10	2.25677e-10
20	1.85155e-10	1.21768e-10	1.04279e-10	0.450319e-10	1.30698e-10	1.48377e-10
30	2.0749e-10	1.47807e-10	1.28653e-10	0.137255e-10	0.930851e-10	1.09259e-10
40	2.25146e-10	1.68332e-10	1.47921e-10	-0.0539929e-10	0.692111e-10	0.829001e-10
50	2.39812e-10	1.84452e-10	1.62992e-10	-0.182882e-10	0.515649e-10	0.637658e-10

2. EFFECT OF INCREASING W_N ON DELAY

Wn (µm)	A = B = 0->1	A = 0->1, B = 1	A = 1, B = 0->1	A = B = 1->0	A = 1->0, B = 1	A = 1, B = 1->0
10	1.5106e-10	0.85931e-10	0.754651e-10	1.10465e-10	2.04309e-10	2.25677e-10
20	1.33419e-10	0.207703e-10	0.205597e-10	1.29796e-10	2.34063e-10	2.70811e-10
30	1.32278e-10	-0.107362e-10	-0.0359612e-10	1.43221e-10	2.5283e-10	3.03444e-10
40	1.35692e-10	-0.298984e-10	-0.172759e-10	1.5433e-10	2.67213e-10	3.31397e-10
50	1.40295e-10	-0.429228e-10	-0.26167e-10	1.6431e-10	2.79358e-10	3.55863e-10

3. EFFECT OF INCREASING C_L ON DELAY

C_L (fF)	A = B = 0->1	A = 0->1, B = 1	A = 1, B = 0->1	A = B = 1->0	A = 1->0, B = 1	A = 1, B = 1->0
100	1.5106e-10	0.85931e-10	0.754651e-10	1.10465e-10	2.04309e-10	2.25677e-10
200	2.06643e-10	1.45113e-10	1.27619e-10	1.61177e-10	2.70631e-10	2.87468e-10
300	2.53351e-10	1.94254e-10	1.70563e-10	2.03837e-10	3.26866e-10	3.41181e-10
400	2.93883e-10	2.36462e-10	2.08844e-10	2.40799e-10	3.76309e-10	3.88868e-10
500	3.31367e-10	2.75124e-10	2.43254e-10	2.73834e-10	4.207e-10	4.32015e-10

CONCLUSION

1.Effect of Increasing Wp on Delay:

- *As Wp increases, delays generally decrease for transitions A = B = 0->1, A = 0->1, B = 1, and A = 1, B = 0->1.*
- *For transitions involving falling edges (A = B = 1->0, A = 1->0, B = 1, A = 1, B = 1->0), delays show a decreasing trend initially but become negative at higher Wp, indicating an overshoot or instability.*

2. Effect of Increasing Wn on Delay:

- *Increasing Wn reduces delay for transitions A = B = 0->1.*
- *For other transitions, delays become negative at higher Wn, indicating potential issues like incorrect rise/fall timing due to excessive pull-down strength.*

3.Effect of Increasing CL on Delay:

- *Increasing CL (load capacitance) significantly increases delay across all transitions.*
- *This is expected as higher capacitance leads to slower charging and discharging times.*