EXPERIMENT -07

VLSI DESIGN - LAB (EEM 614)

NAME – SURAJ

ROLL NO. -2201769

1.Schmitt trigger with one PMOS and three NMOS transistors

1a. Circuit and Schematic

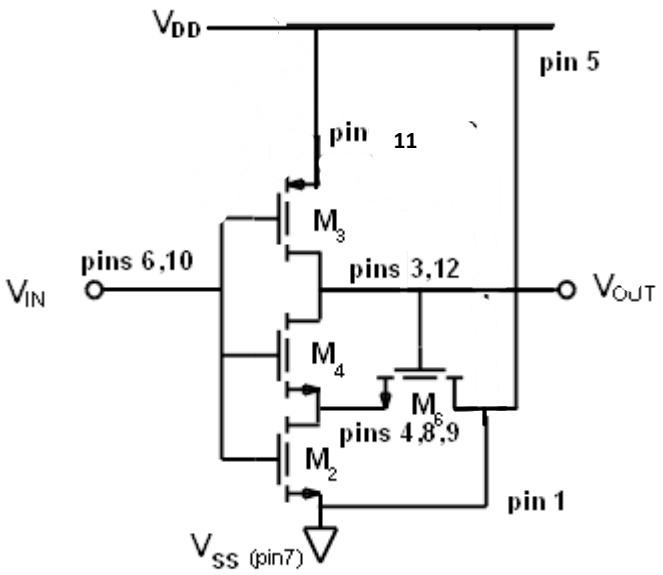


Figure1: Circuit diagram of Schmitt trigger using CD4007 IC

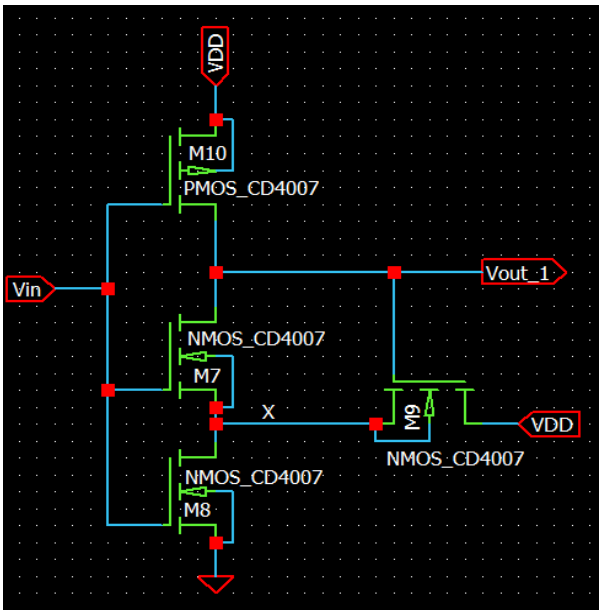


Figure 2: Schematic diagram of Schmitt trigger

1b. Output for different Inputs

INPUTS

OUTPUTS

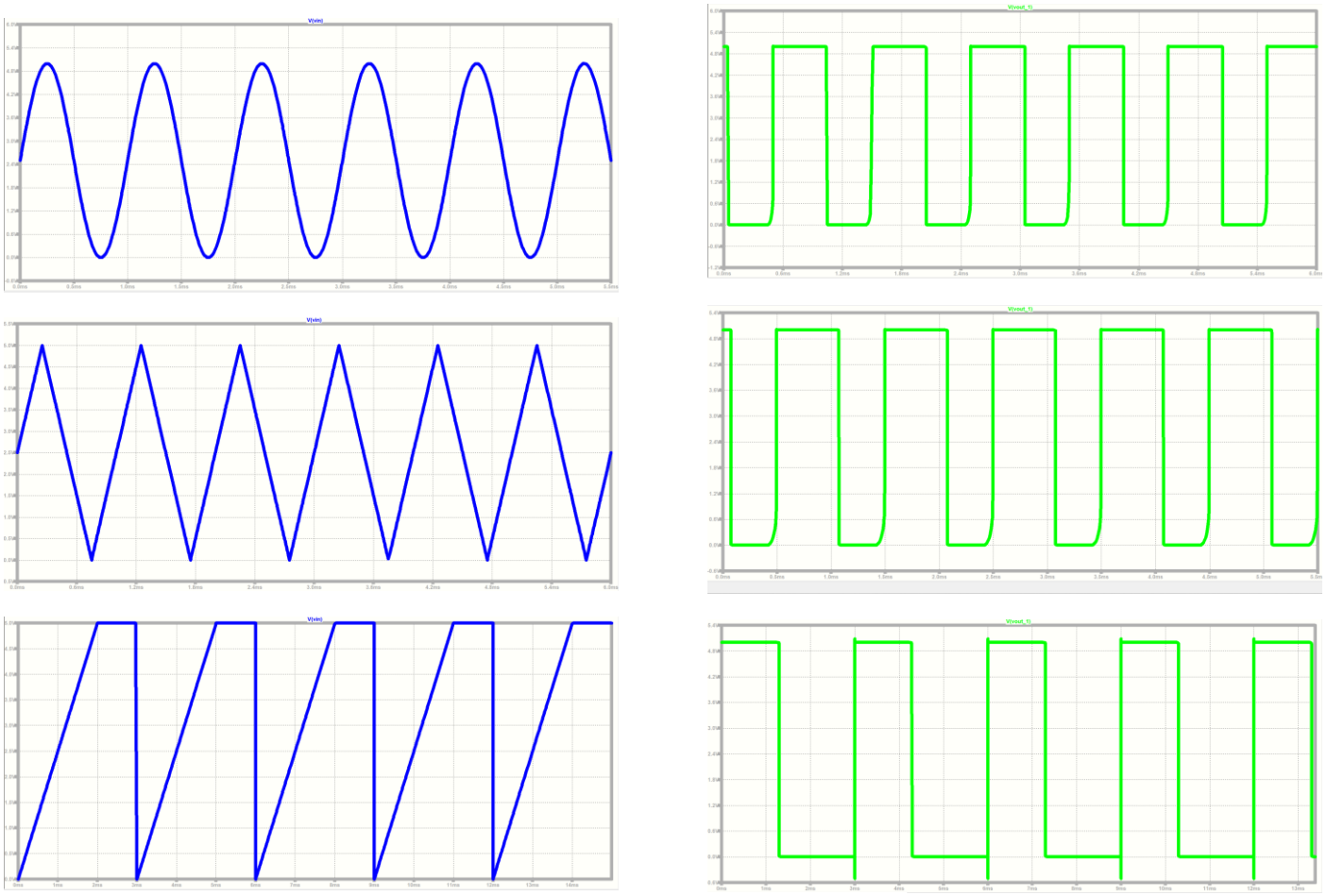
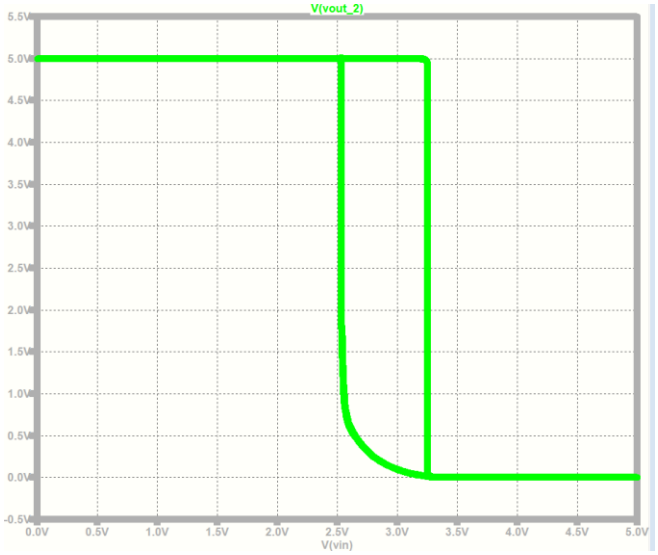


Figure 4: Input Output Waveforms

1c. Characteristics of circui.

A). Output Voltage V/S Input Voltage



B). Vx (VDD -Vtn) V/S Vin

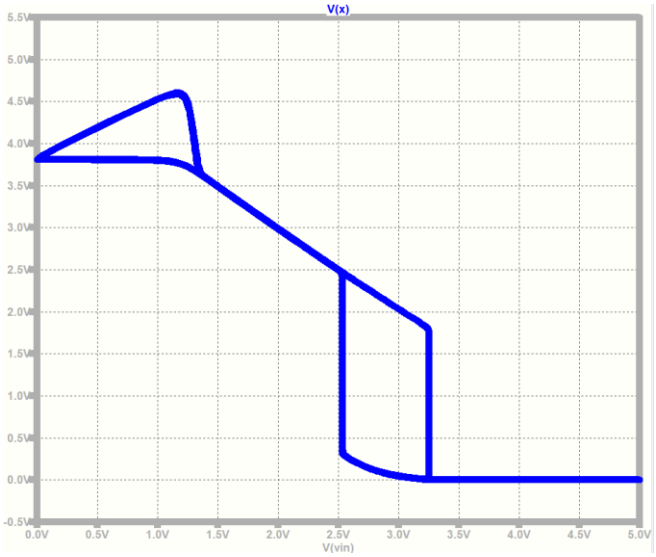
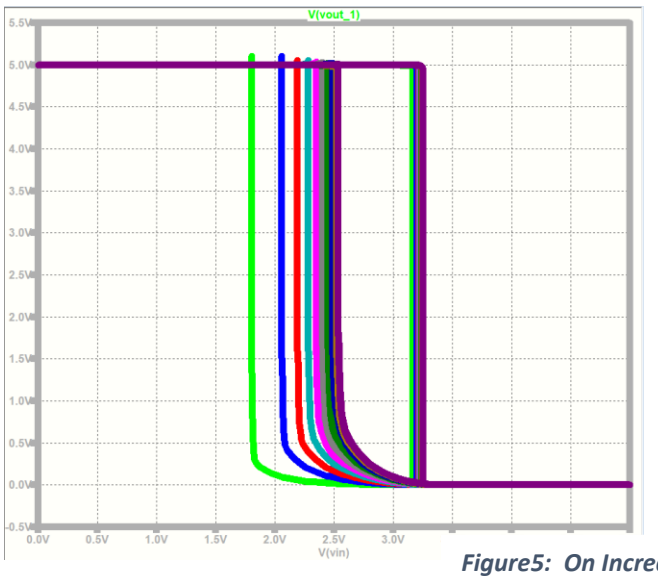


Figure 4: Wn =170u and Wp =360u



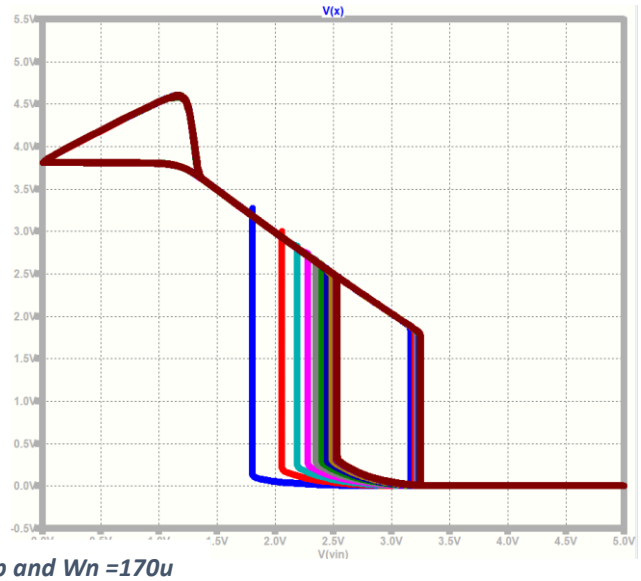
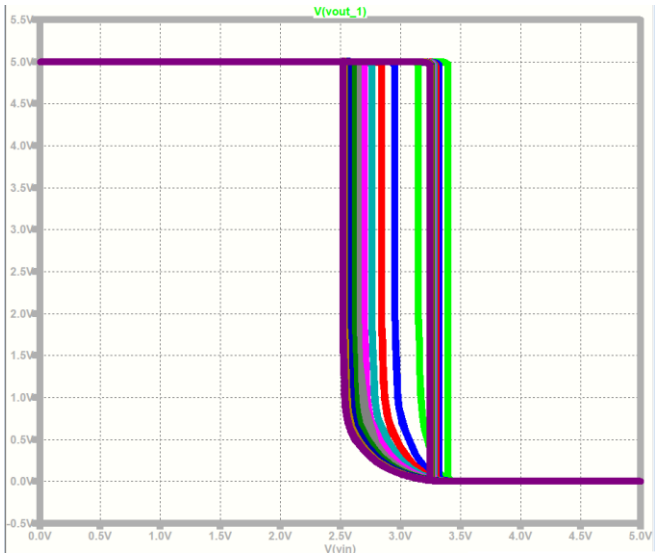


Figure5: On Increasing Wp and Wn =170u



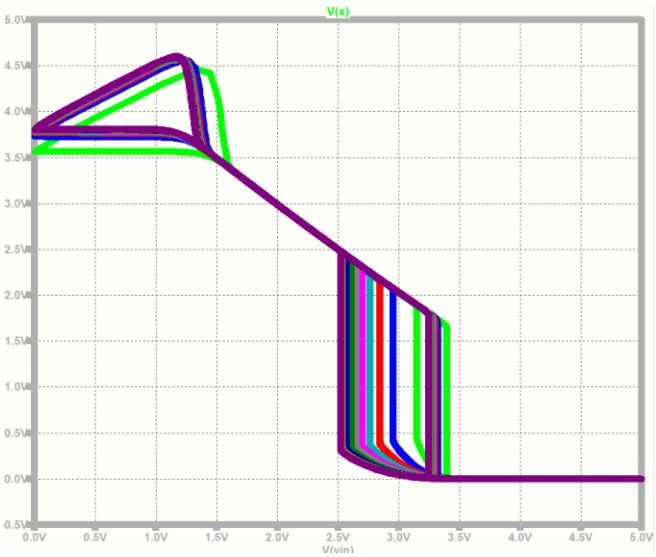
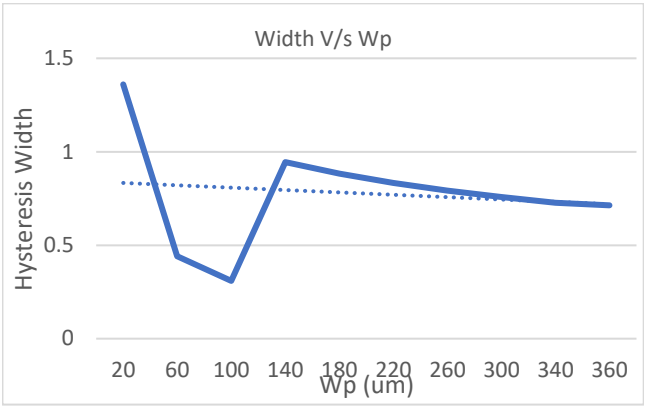


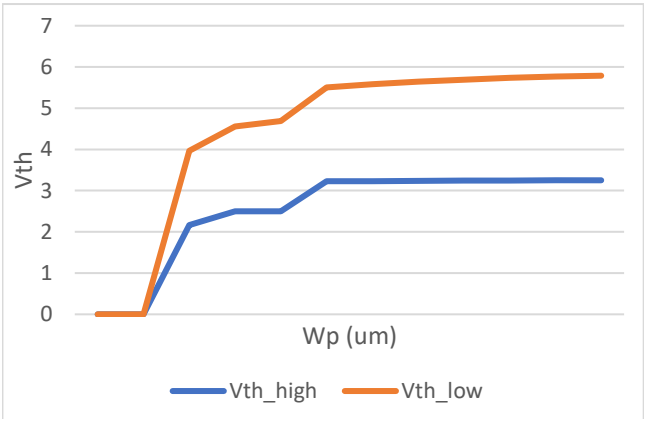
Figure 6: On Increasing Wn and Wp =360u

1d. Results

A) On Increasing Wp and Wn =170u

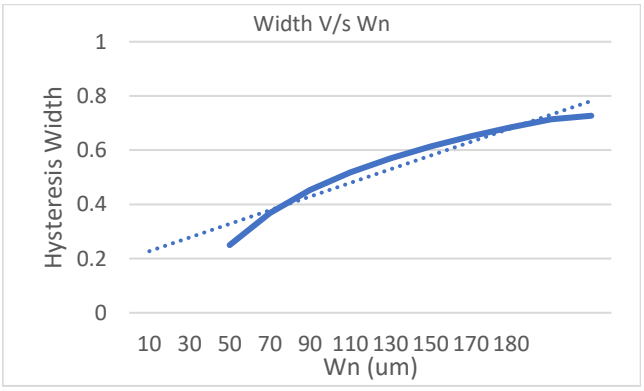
Sr.No.	*Wp (μm)*	*Higher Threshold Voltage (V^+)*	*Lower Threshold Voltage (V^-)*	*Hysteresis Width ($V^+ - V^-$)*
1	20	2.16493	1.80459	1.36034
2	60μ	2.50014	2.05834	0.441799
3	100	2.5	2.19077	0.309232
4	140	3.22584	2.28116	0.944682
5	180	3.23221	2.34951	0.882704
6	220	3.23745	2.40419	0.833262
7	260	3.24186	2.44962	0.79224
8	300	3.24558	2.48825	0.757332
9	340	3.24899	2.52182	0.727173
10	360	3.25053	2.537	0.713528

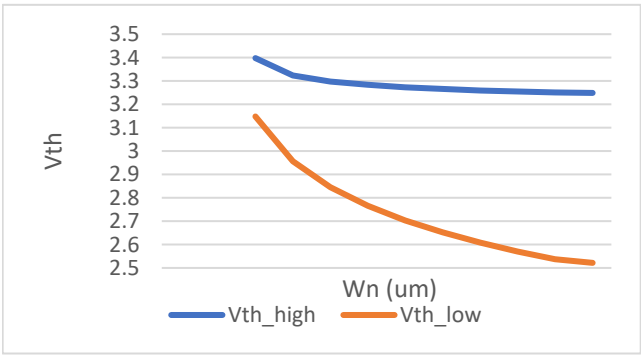




B) On Increasing Wn and Wp =360u

Sr.No.	*Wp (μm)*	*Higher Threshold Voltage (V^+)*	*Lower Threshold Voltage (V^-)*	*Hysteresis Width ($V^+ - V^-$)*
1	10	3.39767	3.14786	0.249812
2	30	3.32364	2.9557	0.367942
3	50	3.2979	2.84491	0.452985
4	70	3.28305	2.76541	0.517642
5	90	3.27295	2.7031	0.569845
6	110	3.26538	2.65179	0.613587
7	130	3.25944	2.60823	0.651212
8	150	3.25452	2.57041	0.684111
9	170	3.25053	2.537	0.713528
10	180	3.2487	2.52168	0.727027





2.Schmitt trigger with one NMOS and three NMOS transistors

2a. Circuit and Schematic

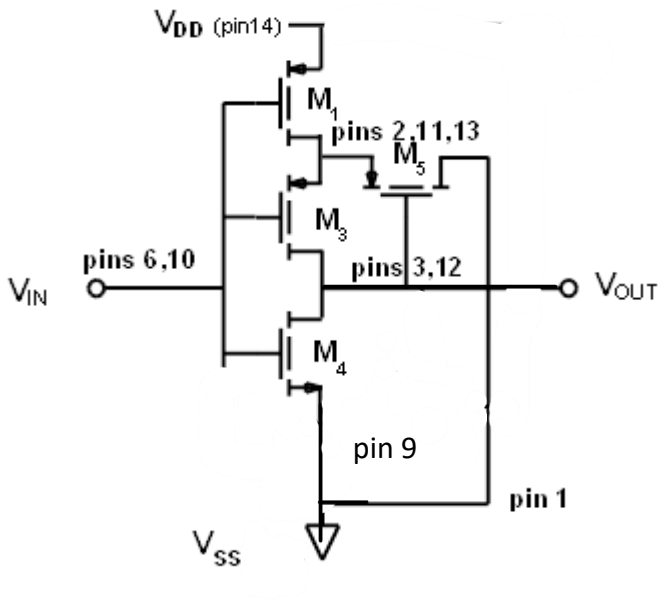


Figure7: Circuit diagram of Schmitt trigger using CD4007 IC

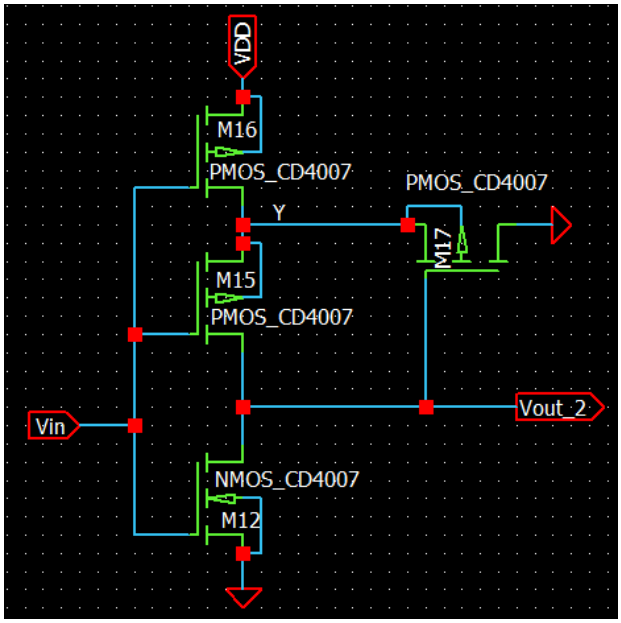
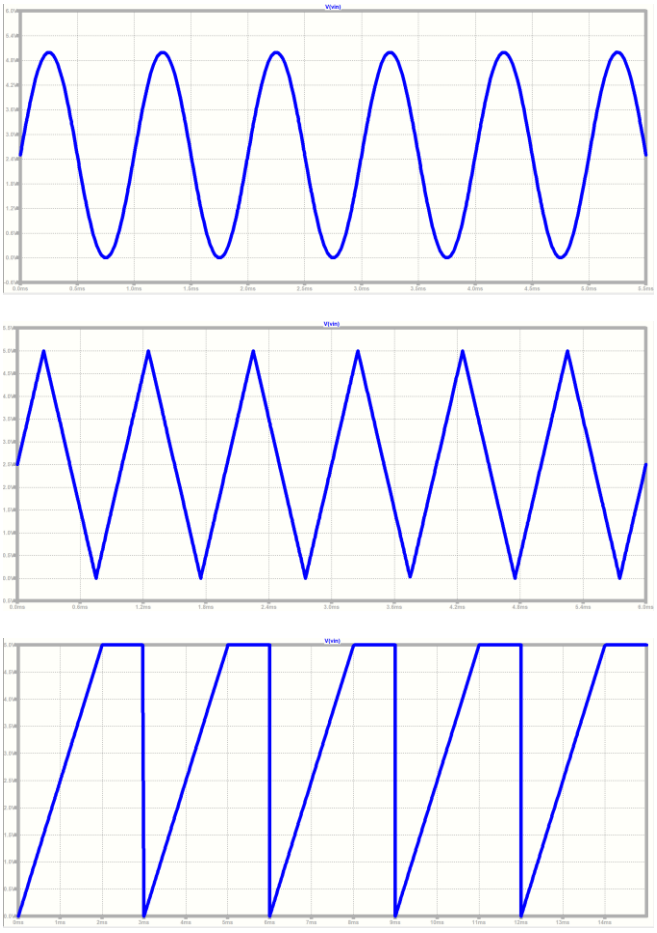


Figure 8: Schematic diagram of Schmitt trigger

1b. Output for different Input

INPUT



OUTPUT

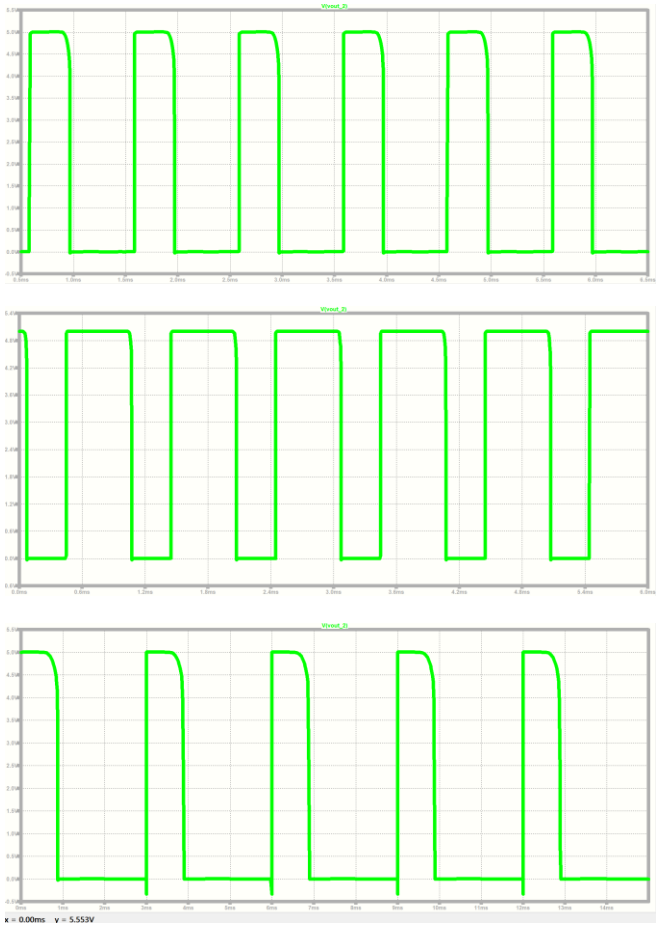
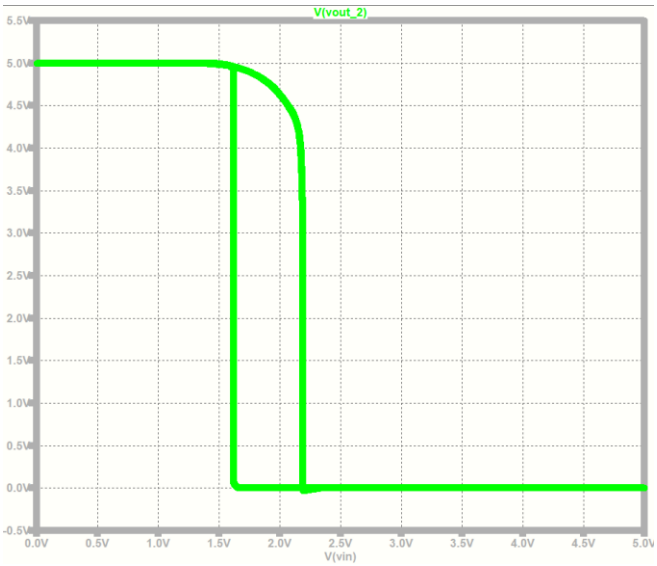


Figure 9: Input Output Waveforms

2c. Characteristics of circuit

A). Output Voltage V/S Input Voltage



B). Vx (VDD -Vtn) V/S Vin

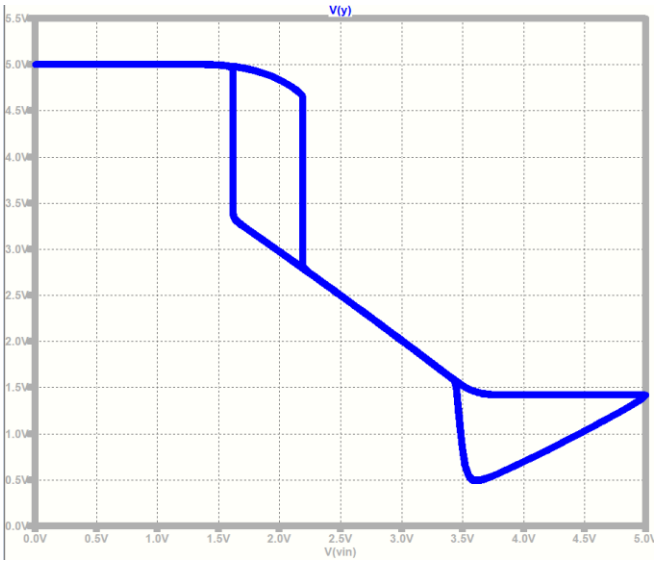


Figure 10: Wn =170u and Wp =360u

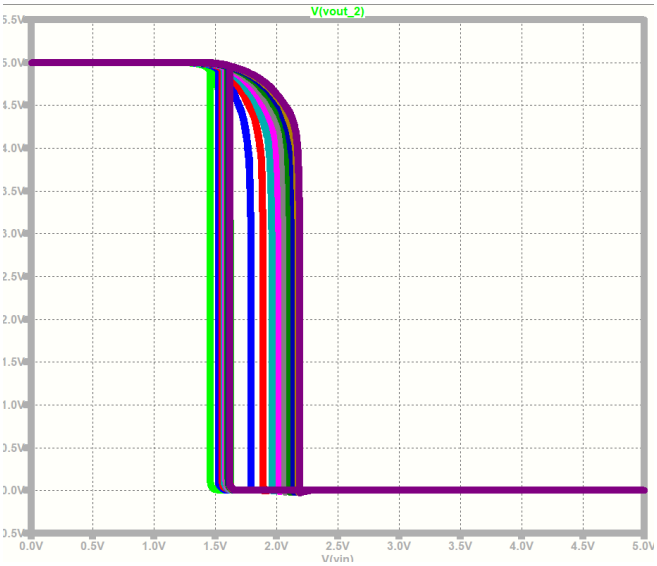
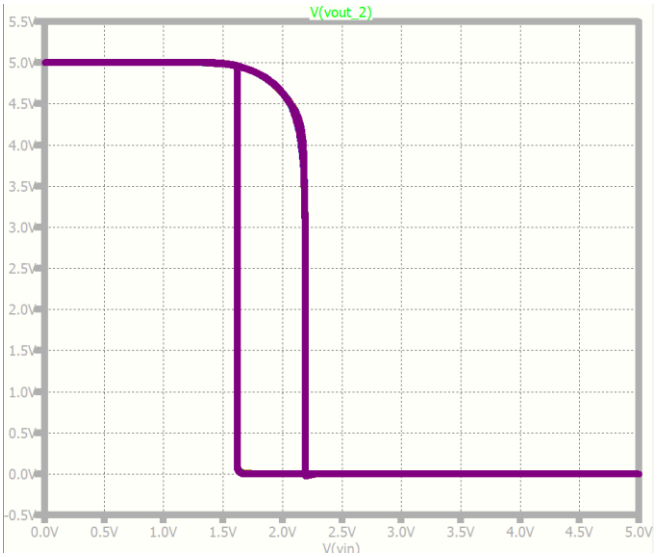


Figure 11: On Increasing Wp and Wn =170u



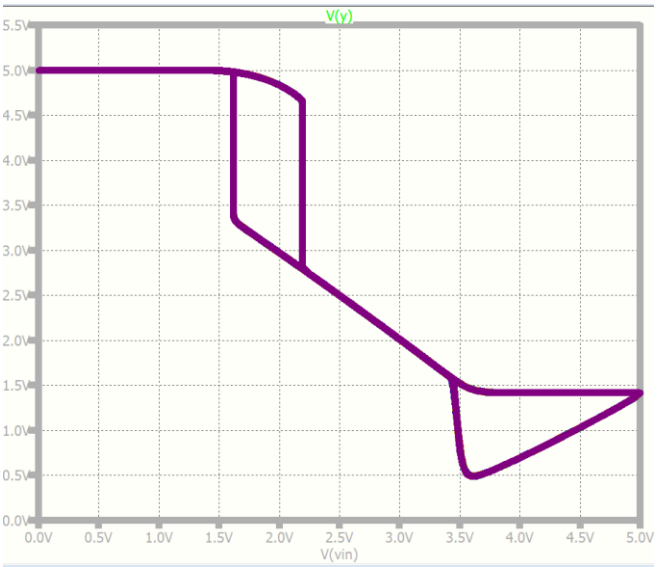
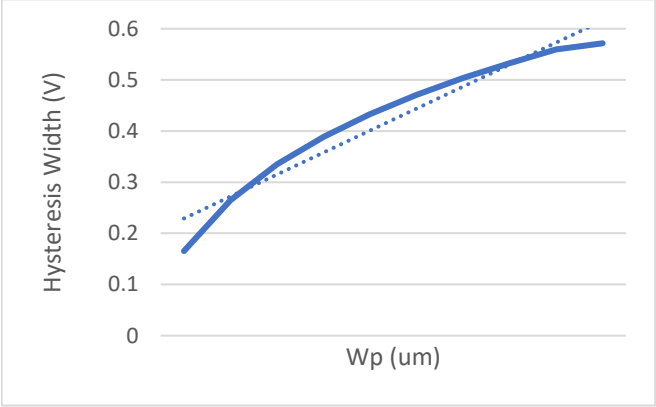


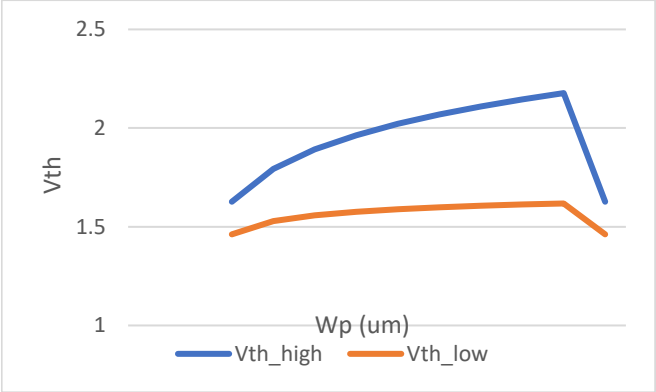
Figure 12: On Increasing Wn and Wp =360u

2d. RESULTS

A) On Increasing Wp and Wn =170u

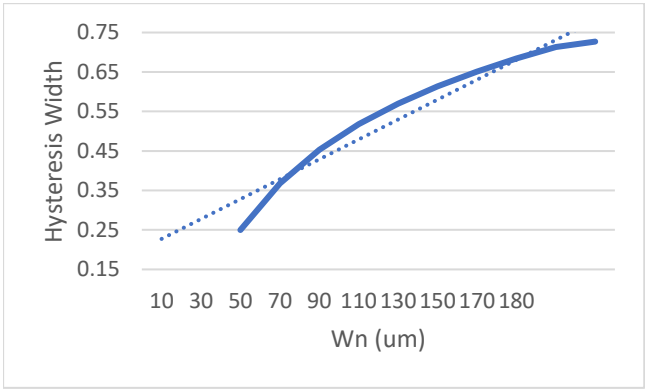
Sr.No.	*Wp (μm)*	*Higher Threshold Voltage (V^+)*	*Lower Threshold Voltage (V^-)*	*Hysteresis Width ($V^+ - V^-$)*
1	20	1.6269	1.46155	0.165351
2	60μ	1.79395	1.52895	0.265002
3	100	1.89218	1.55759	0.334588
4	140	1.9641	1.57564	0.388455
5	180	2.02131	1.58853	0.432784
6	220	2.06894	1.59833	0.470605
7	260	2.1098	1.60623	0.503577
8	300	2.14558	1.6127	0.532878
9	340	2.1774	1.61806	0.55934
10	360	1.6269	1.46155	0.571503

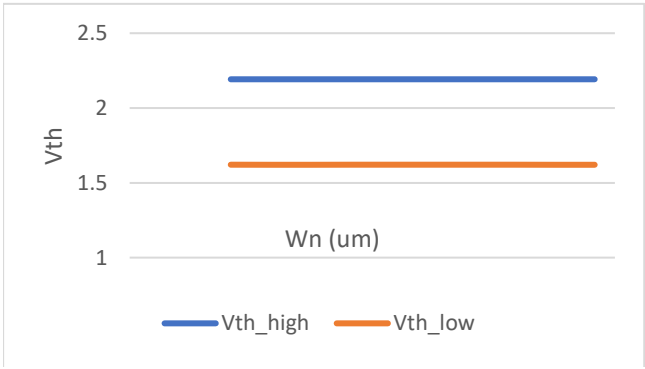




B) On Increasing Wn and Wp =360u

Sr.No.	*Wp (μm)*	*Higher Threshold Voltage (V^+)*	*Lower Threshold Voltage (V^-)*	*Hysteresis Width ($V^+ - V^-$)*
1	10	2.19207	1.62049	0.249812
2	30	2.19207	1.62047	0.367942
3	50	2.19205	1.62047	0.452985
4	70	2.19207	1.62054	0.517642
5	90	2.19207	1.62048	0.569845
6	110	2.19207	1.62048	0.613587
7	130	2.19207	1.62048	0.651212
8	150	2.19207	1.62048	0.684111
9	170	2.19207	1.62057	0.713528
10	180	2.19207	1.62047	0.727027





3.Circuit with three pairs of CMOS transistors

2a. Circuit and Schematic

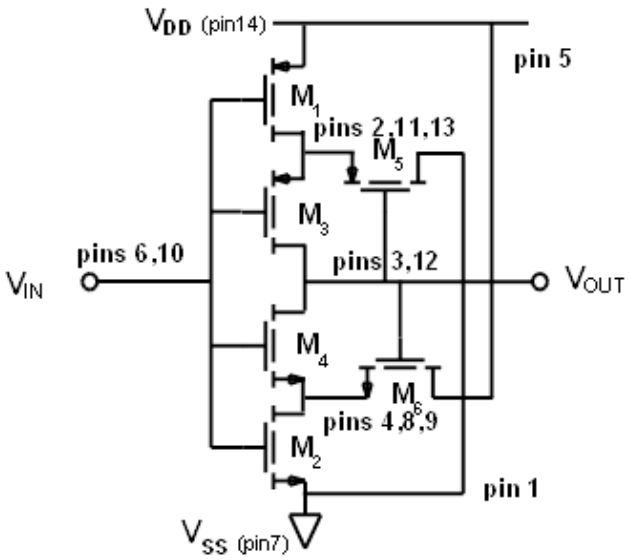


Figure 13: Circuit diagram of Schmitt trigger using CD4007 IC

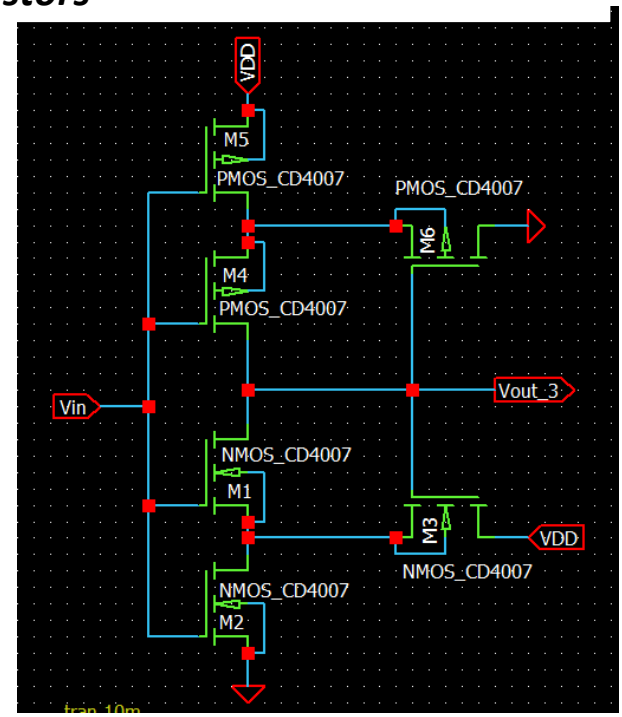


Figure 14: Schematic diagram of Schmitt trigger

1b. Output for different Inputs

INPUTS

OUTPUT

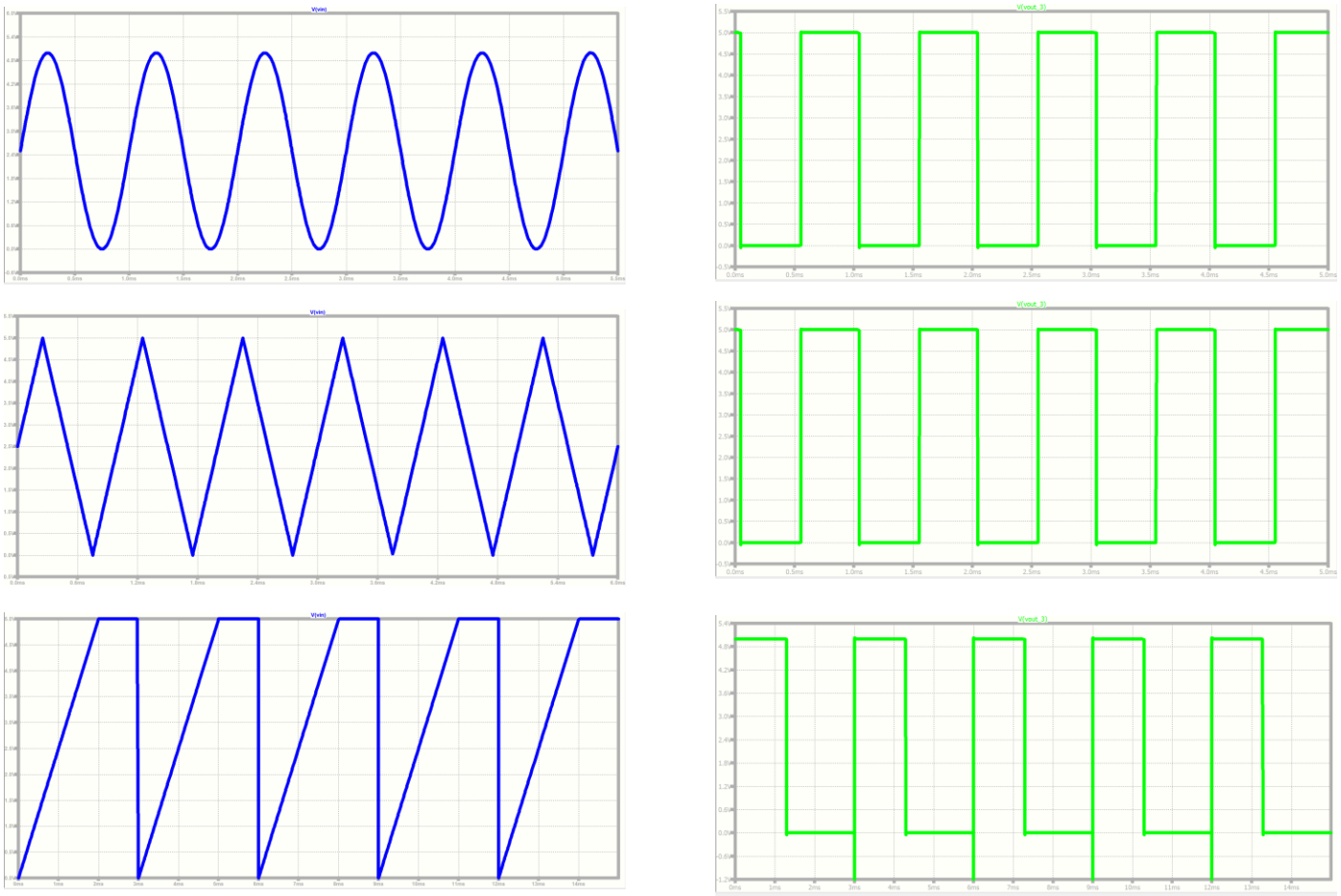
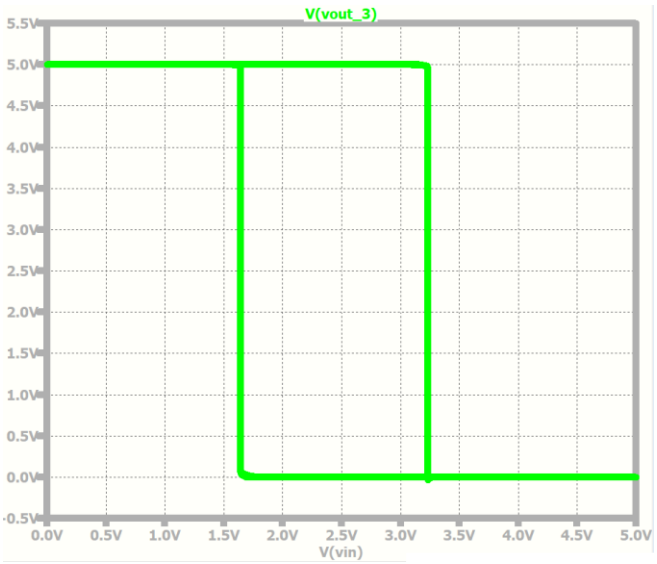


Figure 15: Input Output Waveforms

3c. Characteristics of circuit

A). Output Voltage V/S Input Voltage



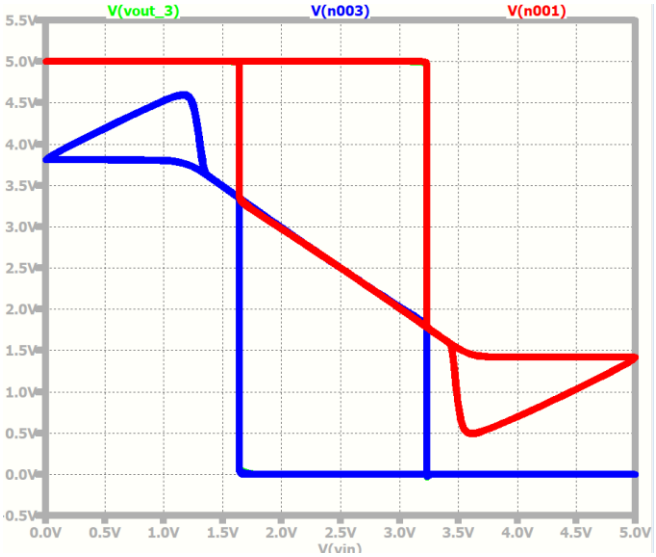
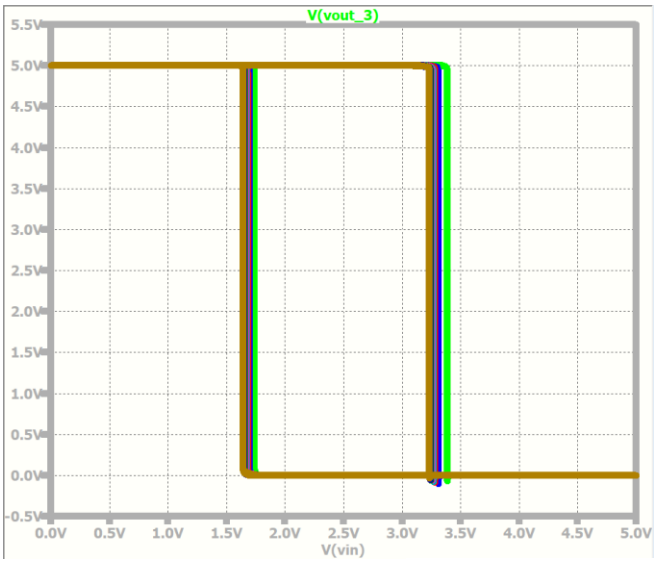


Figure 16: Wn =170u and Wp =360u



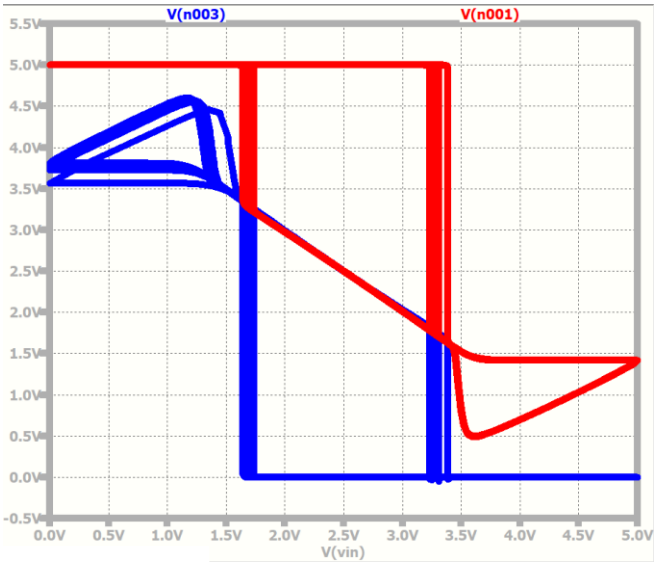
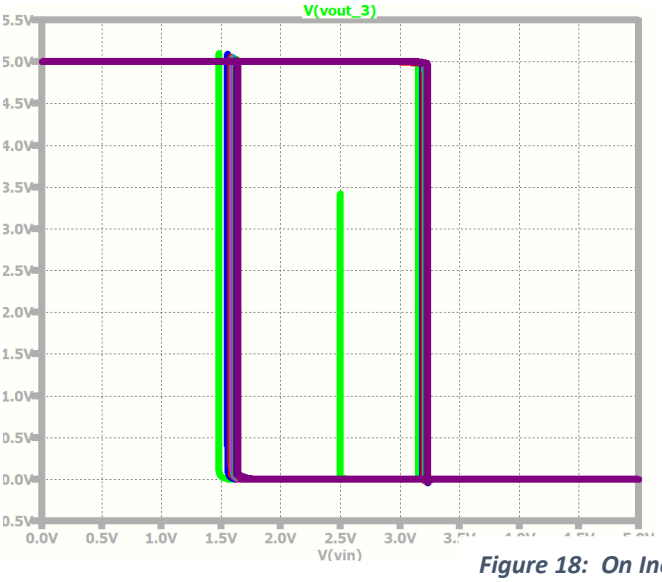


Figure 17: On Increasing Wp and Wn =170u



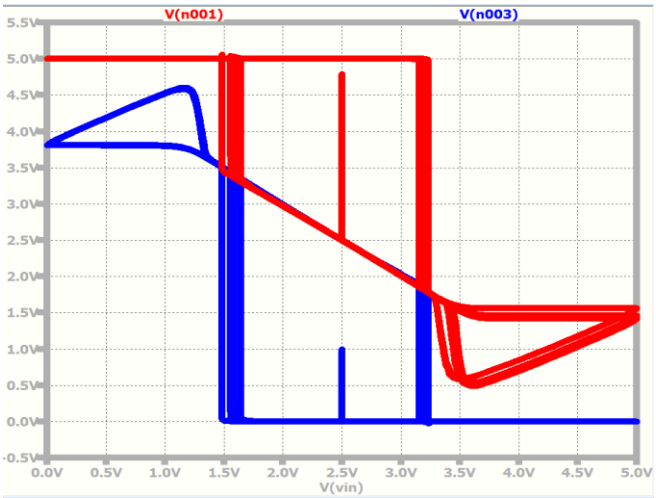
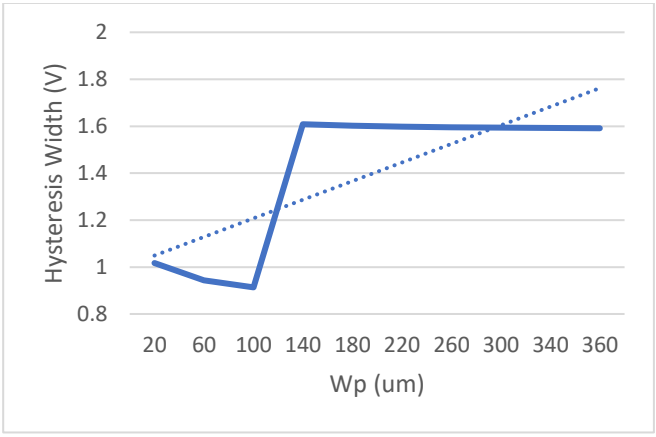


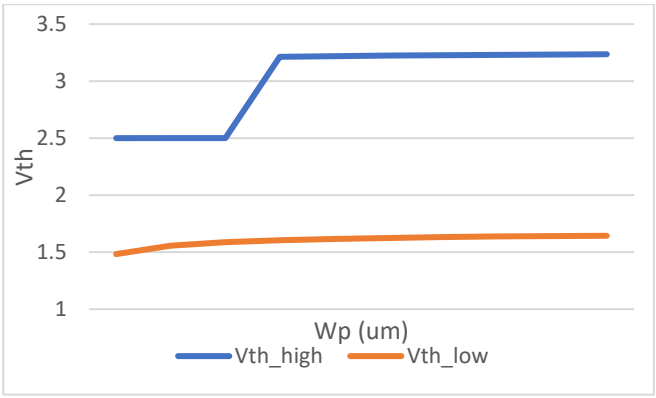
Figure 18: On Increasing Wn and Wp =360u

3d. RESULTS

A) On Increasing Wp and Wn =170u

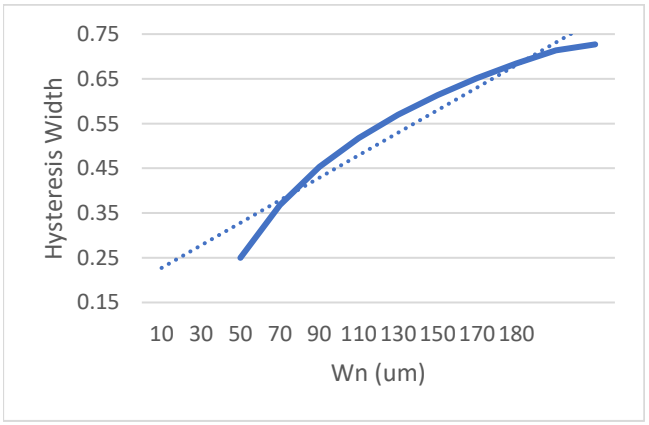
Sr.No.	*Wp (µm)*	*Higher Threshold Voltage (V^+)*	*Lower Threshold Voltage (V^-)*	*Hysteresis Width ($V^+ - V^-$)*
1	20	2.50026	1.4831	1.01715
2	60µ	2.5	1.55721	0.942786
3	100	2.5	1.58652	0.913483
4	140	3.21232	1.60394	1.60837
5	180	3.21843	1.6158	1.60263
6	220	3.22314	1.6246	1.59855
7	260	3.22727	1.63147	1.5958
8	300	3.23063	1.63698	1.59366
9	340	3.23376	1.64166	1.5921
10	360	3.23527	1.64369	1.59158

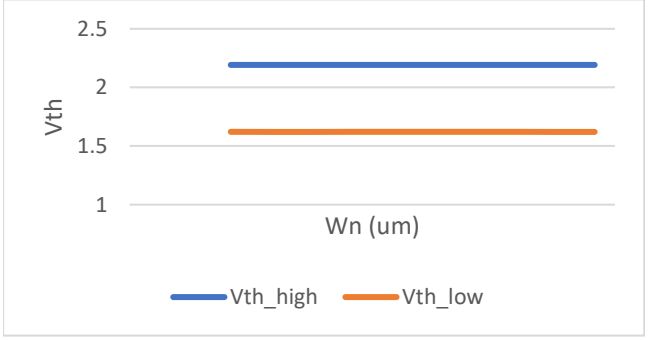




B) On Increasing Wn and Wp =360u

Sr.No.	*Wp (µm)*	*Higher Threshold Voltage (V^+)*	*Lower Threshold Voltage (V^-)*	*Hysteresis Width ($V^+ - V^-$)*
1	10	3.38903	1.73874	1.65029
2	30	3.30819	1.69648	1.61171
3	50	3.28168	1.68148	1.6002
4	70	3.26689	1.67167	1.59522
5	90	3.25685	1.66413	1.59272
6	110	3.24938	1.65791	1.59146
7	130	3.24368	1.65273	1.59095
8	150	3.23912	1.64794	1.59118
9	170	3.23527	1.64369	1.59158
10	180	3.23347	1.64164	1.59183





CONCLUSION

The three Schmitt trigger designs were analysed based on the following configurations:

1. Schmitt Trigger with One PMOS and Three NMOS Transistors
2. Schmitt Trigger with One NMOS and Three PMOS Transistors
3. Schmitt Trigger with Three Pairs of CMOS Transistors

Observations:
Hysteresis Width:

- *The hysteresis width increased as the transistor width (Wp and Wn) increased in all three designs.*
- *Design 3 (Three pairs of CMOS transistors) exhibited the highest hysteresis width, making it the most stable in noise suppression applications.*
- *Design 2 (One NMOS and Three PMOS) consistently showed the lowest hysteresis width, indicating higher sensitivity to noise**.***

Threshold Voltage:

- *The higher threshold voltage (V+) and lower threshold voltage (V-) were highest in Design 3, followed by Design 1 and Design 2.*
- *This indicates that Design 3 required a higher input voltage range to toggle between high and low states, making it more suitable for robust applications**.***

Effect of Width Variation:

- *Increasing Wp and Wn led to a gradual increase in hysteresis width in all three designs.*
- *Design 3 demonstrated more linear and consistent behavior with increasing width, which is desirable in practical applications.*

Conclusion:

Design 3 (Three pairs of CMOS transistors) is the most reliable and noise-tolerant among the three, making it suitable for applications requiring high stability and noise immunity.

Design 1 (One PMOS and Three NMOS) provides a balanced trade-off between noise immunity and sensitivity.

Design 2 (One NMOS and Three PMOS) is the most sensitive but also the least noise-tolerant, making it ideal for low-power applications where noise is minimal.

For applications where stability and noise immunity are critical, Design 3 is recommended.